PHOTONIC INTEGRATION OF HYBRID SILICON

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Abstract

The hybrid silicon platform is a fast growing and increasingly complex integrated circuits with thousands of integrated components including on-chip lasers. It holds great potential in medium-scale and large-scale photonic integrated circuits. Integration of silicon with other materials like III-V (for laser) and Ge or Si-Ge (for detector) requires fully on-chip photonic integration. Thus it become hybrid integration. Lasers, modulators, amplifiers and photodetectors has been tested with these type of integration on its individual components and have shown better and imporved optical functionality. This approch show a unique way to build photonic active devices on silicon and allow application of these silicon photonic integrated hybrids in optical communication.

Contents

Chapter 1

Introduction

Recent research in silicon photonics has been driven by the motivation to realize silicon optoelectronic integrated devices using large scale, low-cost, and highly accurate CMOS technology. Silicon is transparent at the 1.5m and 1.3m telecommunication wavelengths and has demonstrated low loss waveguide with losses in the range of 0.2 dB/cm 1 dB/cm. The large index contrast of silicon waveguides with the silicon dioxide cladding results in highly confined optical modes and the reduction of waveguide bend radii leading to dense photonic integration.

It was only recently that silicon has been demonstrated as a high-speed modulator. Light detection is another major research topic in silicon photonics. An alternative to fabricating the gain element in silicon is to take prefabricated lasers and couple them to silicon waveguides. Recently, we have demonstrated a hybrid integration platform utilizing III-V epitaxial layers transferred to silicon to realize many types of photonic active devices through a single wafer bonding step. The wafer-bonded structure forms a hybrid waveguide, where its optical mode lies both in silicon and III-V layers. This structure enables the use of III-V layers for active light manipulation such as gain, absorption,and electro-optical effect for the amplifiers, lasers, detectors, and modulators.

Chapter 2

Fabrication

2.1 Plasma assisted low-temperature wafer bonding

The transfer of the indium phosphide (InP)-based epitaxial layer structure to the silicon-on-insulator (SOI) substrate is a key step in the fabrication of this hybrid platform and has direct impact on the device performance, yield, and reliability. Due to the mismatch between the thermal expansion coefficient of silicon and indium phosphide, high-temperature not desirable. In order to resolve this issue, low-temperature annealing is used with an oxygen plasma surface treatment to enable strong bonding. After rigorous sample cleaning and close microscopic inspection with 200x magnification, the native oxide on SOI and InP are removed in standard buffer HF solution (1HF : $7H_2O$) and NH_4OH,respectively, resulting in clean, hydrophobic surfaces. The samples then undergo an oxygen plasma surface treatment to grow an ultrathin layer of oxide(¡5nm) which leads to very smooth hydrophilic surfaces, which is less sensitive to the microroughness as compared to the hydrophobic bonding. The following deionized water dip further terminates the oxide surface by polar hydroxyl groops OH^-, forming bridging bonds between the mating surfaces to result in spontaneous bonding at room temperature. To strengthen the bond, the bonded sample is placed in a conventional wafer bonding machine, where the samples are held together for 12 hours. After annealing and cooling, the InP substrate is selectively removed in a 3HCl :$1H_2O$ solution at room temperature.

2.2 Silicon waveguide and III-V back-end processing

The general procedure of silicon waveguide formation on an SOI wafer and III-V back-end processing after wafer bonding process is as follows. The silicon waveguide is formed on the (100) surface of an undoped silicon-on-insulator (SOI) substrate using Cl_2/Ar/HBr-based plasma reactive ion etching. The III-V epitaxial layer is then transferred to the patterned silicon wafer through low-temperature oxygen plasma-assisted wafer bonding. After removal of the InP substrate, mesa structures on III-V layers are formed by dry-etching the p-type layers using a CH_4/H/Ar-based plasma reactive ion etch. For lasers and amplifiers, protons (H^+) are implanted on the two sides of the p-type mesa to create a 4m wide current channel and to prevent lateral current spreading, ensuring a large overlap between the carriers and the optical mode. Ti/Au probe pads are then deposited on the top of the mesa. Then, if necessary, the sample is diced into bars and each bar is polished.

Chapter 3

Optical Amplifier

An optical amplifier is a device that amplifies an optical signal directly, without the need to first convert it to an electrical signal. Optical amplifiers are important in optical communication and laser physics. There are several different physical mechanisms that can be used to amplify a light signal, which correspond to the major types of optical amplifiers. In semiconductor optical amplifiers (SOAs), electron-hole recombination occurs.

Semiconductor optical amplifiers (SOAs) are amplifiers which use a semiconductor to provide the gain medium. Semiconductor optical amplifiers are typically made from group III-V compound semiconductors such as GaAs/AlGaAs, InP/InGaAs, InP/InGaAsP and InP/InAlGaAs.

Chapter 4

Hybrid Silicon Laser

A hybrid silicon laser is a semiconductor laser fabricated from both silicon and group III-V semiconductor materials. The hybrid silicon laser was developed to address the lack of a silicon laser to enable fabrication of low-cost, mass-producible silicon optical devices. The hybrid approach takes advantage of the light-emitting properties of III-V semiconductor materials combined with the process maturity of silicon to fabricate electrically driven lasers on a silicon wafer that can be integrated with other silicon photonic devices.

The hybrid silicon laser is fabricated by a technique called plasma assisted wafer bonding. Silicon waveguides are first fabricated on a silicon on insulator (SOI) wafer. This SOI wafer and the un-patterned III-V wafer are then exposed to an oxygen plasma before being pressed together at a low (for semiconductor manufacturing) temperature of 300C for 12hours. This process fuses the two wafers together. The III-V wafer is then etched into mesas to expose electrical layers in the epitaxial structure. Metal contacts are fabricated on these contact layers allowing electric current to flow to the active region.

Chapter 5

Conclusion

The recent progress of photonic integrated silicon devices with examples like optical amplifiers and hybrid silicon laser is discussed here. This shows the active functionality on silicon photonics platform. The hybrid silicon evanescent device platform provides a unique way to build photonic active devices on silicon, and those studies will expedite the applications of silicon photonic integrated circuits in optical telecommunication and optical interconnects.

Chapter 6

Reference

http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.687.4671&rep=rep1&type=pdf
https://www.ece.ucsb.edu/uoeg/publications/papers/ParkAOT08.pdf
https://en.wikipedia.org/wiki/Hybrid_silicon_laser
https://en.wikipedia.org/wiki/Optical_amplifier