A PROJECT REPORT ON

Silicon Nano wire MOSFET

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CERTICICATE OF ORIGINALITY

I hereby certify that the work which is being presented in the Project entitled" SILICON NANO WIRE" by DALJIT SINGH in partial fulfillment of ELEC421/6221 submitted to Department of Electrical & Computer Engineering at Concordia University is my own. The matter presented in this report has not been submitted by me in any other University. It meets all the expectations of originality.

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ABSTRACT

The Bipolar Power Transistor (BPT), as a switching device for power applications, had a few disadvantages. This led to the development of the power MOSFET (Metal Oxide Semiconductor Field Effect Transistor). The power MOSFET is used in many applications such as SMPS (Switched Mode Power Supplies), computer peripherals, automotive, and motor control. Continuous research and improvement have provided it with ideal characteristics for replacing the BJT (Bipolar Junction Transistor). This application note is a general description of Nano wire MOSFETs and a detailed presentation of its features.

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1 METALOXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

1.1 STRUCTURE OF MOSFET:

MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor. The structure is also known as MOS capacitor. We consider only silicon dioxide system while designing it. MOSFET is mainly use for the amplification of signals. It have four terminals source(S), gate(G), drain(d) and body(B). it is useful in both digital and analog circuits

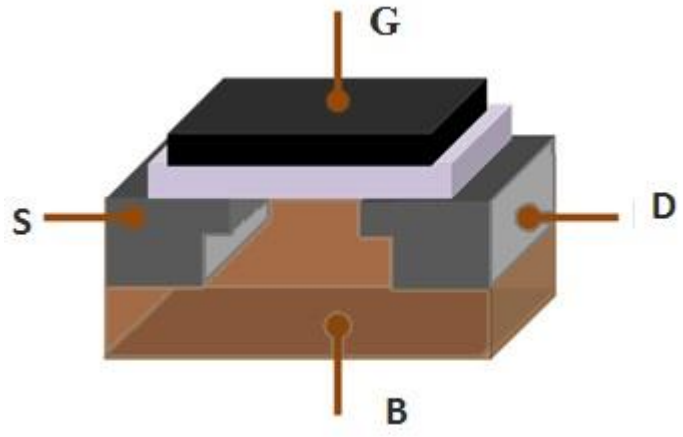

FIGURE 1: STRUCTURE OF MOSFET

Different technologies are been used in designing model such as submicron and deep submicron. such technologies are being used for drain current and parasitic capacitance of the device. With reducing the gate length, we can be achieved sub-micron structure. Based on different CMOS technology submicron can be designed more accurately.

Different CMOS Technologies

- Submicron Technology.
- Deep Sub micro technology.
- Ultra submicron technology.

Feature size:

-Submicron Technology :- $L_{min} \geq$ 0.35 microns.

-Deep Submicron Technology: - 0.1 micron $\leq L_{min} \geq$ 0.35 microns

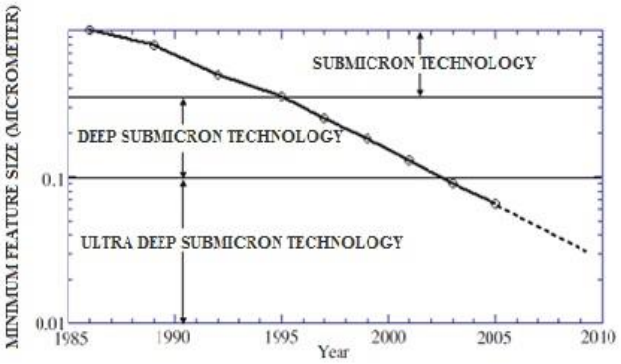

Figure 2 'Graph of CMOS Technology

-Ultra Deep Submicron Technology: -$L_{min} \leq$ 0.35 microns.

Features	Submicron-MOSFET
Cutt-Off	50 GHZ
Noise	More
DC Range	Smaller
Transconductance	Smaller
Output Resistance	Good
Switch Implementation	More
Capacitance	Low
Power Ratio	Fast

Fig. Table based on Specification

1.2 PRINCIPLE OF OPERATION:

Inversion layer in semiconductor acts as a channel. The inversion charges consist of electrons between source and drain contacts. Moreover device fabrication also been carried out between source and drain.

For mos capacitor inversion charge induced in the channel by applying voltage at both the terminals . in terms of strong inversion threshold voltage applied at the gate electrode with respect to the other terminals.

in case of induced inversion channel mosfet gate structure should either overlap with alignments. Which reduces gate- source and gate- drain capacitance.

When V_{ds} is applied to n- channel MOSFET, electrons' move in the channel inversion layer from source to drain. For $V_{gs} > V_t$ there will be increase in voltage steadly from source to drain along the channel, which causes reduction in gate channel bias, which will be equal to V_{gd}.

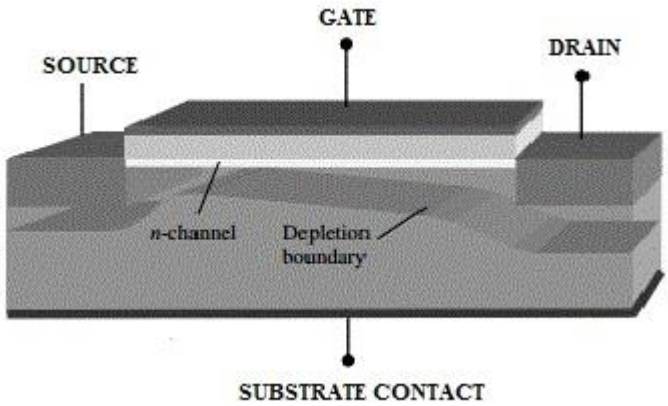

Fig.3 'Submicron Structure

When $V_{ds}=V_t$, the channel reaches threshold at the drain and inversion point gets vanish , such a condition is known as pinch-off, which causes drain current saturate. On the other side $V_{ds}=V_{sat}$ is known as saturation voltage as $V_{gd} = V_{gs}-V_{ds}$.

When $V_{ds} > V_{sat}$ the pinch-off region near drain expands slightly, on the other hand drain current remains constant with some amount of voltage drop. The voltage aroung pinch-off region creates good impact

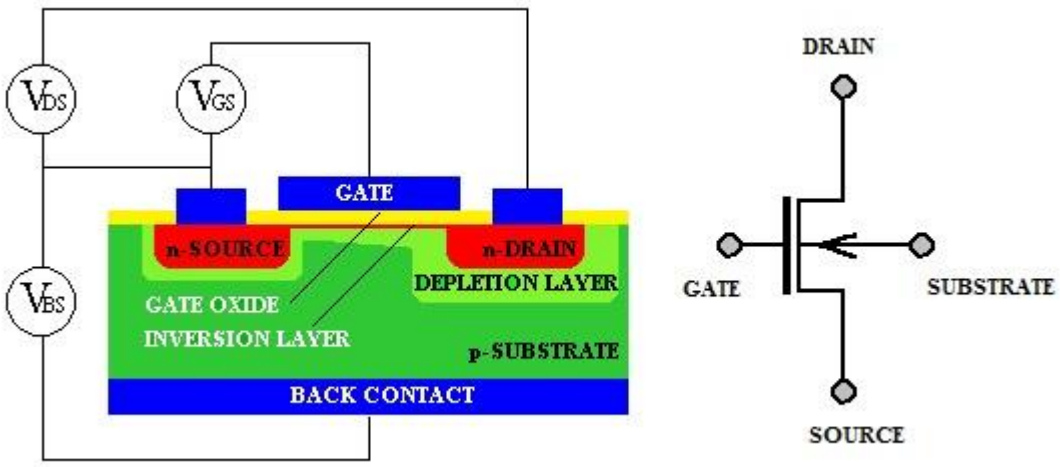

Fig.4 'Working Structure

1.3 Current Voltage Characteristics :

Voltage transfer characteristic gives in response of the circuit. The gate source voltage V_{gs} of the n channel MOSFET is equal to the V_{in} , for p channel it can be considered as $V_{gb}= V_{in} -V_{dd}$.

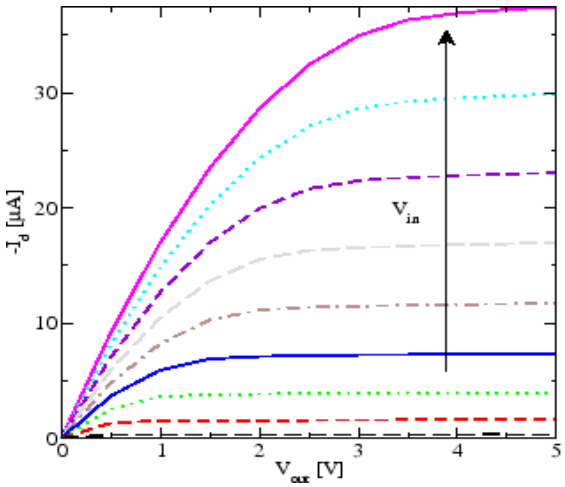

Fig.5 'V_I Characteristics Graph'

MOSFET gate, velocity comes in range near to drain and a lower V_{ds} which causes pinch off. These creates saturation characteristics as shown in below figure.

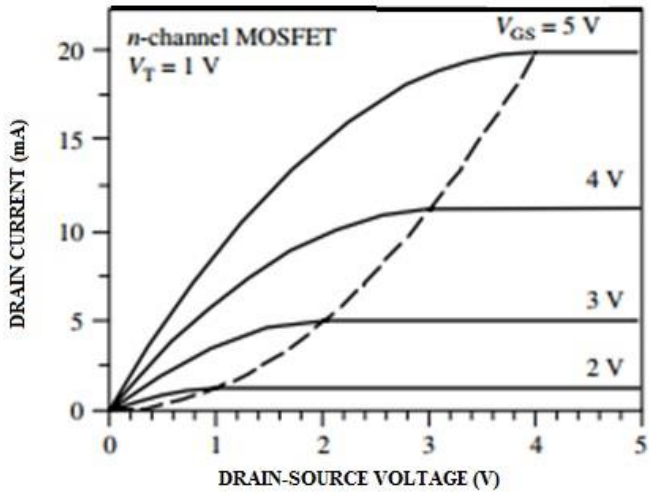

Figure 6 V-I CHARACTERISTICS

1.4 Advantage and Disadvantage of Submicron MOSFET:

Advantages:

- Mosfet are smaller in size
- They are easy to fabricate, also it does not require any space savings on IC's
- Reverse Saturation Current**:** it does not exist as it is a unipolar device.
- Operational Frequency: it is very high, therefore useful at higher frequency
- Infinite Current Gain**:** infinite impedance causes a DC input current is zero. Such case occurs as he offset drives circuits to high input capacitance.
- High Switching Speed: Charge stored in the high voltage transistor. Due to which their causes switching time of 0.5us in compare with few Nano seconds.
- Safe Operating Area: output current of a transistor has a positive temperature coefficient. On increase in current results in a temperature increases. Due to positive temperature coefficient, transistor will take up in an account of highest temperature with maximum current. Due to excessive current transistor will burn out. Moreover, in order to reduce current hogging, transistor should be connected parallel which also increases driving capacity.
- MOSFET have input impedance at low frequencies.

Disadvantages:

- Higher Onstage Voltage Drop: because no injection of minorities because of thick high-voltage devices.

- Higher Production Costs: width of the emitter of a bipolar high voltage transistor between 50um to 100um. therefore, fine lithography need to be used.
- Handling is tough.
- Mosfet is very sensitive to electrostatic charge so it may be destroy pins of a misfit devices.
- trans conductance is lower than BJT.

2 NANO WIRE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

2.1 FABRICATION

The SNAP TECHNIQUE

The key enabling technology for high-performance nanowire logic is the super lattice nanowire pattern transfer (SNAP) technique developed by Melosh. In this technique, Si NWs are formed from silicon-on-insulator (SOI) substrates using a template-mediated, top-down fabrication process. In this section, the process for generating SNAP NWs is qualitatively described. First, superlattices (SLs) consisting of alternating GaAs and AlxGa(1-x) As layers are grown via molecular-beam epitaxy (MBE). The SL wafer is carefully cleaved to form an atomically flat edge. The SLs are then diced into small pieces called “masters” (Figure 7A). As layers, leaving behind GaAs ridges. Metal is then anisotropically deposited onto the cleaved edge of the master, forming metal NWs along the GaAs ridges (Figure 7C). The SL containing the metal NWs are transferred onto the SOI substrate and adhered via an epoxy layer (Figure 7D). The SL is removed using a chemical etch process, leaving behind the metal NWs on the substrate (Figure 7E). The metal NWs act as a physical etch mask and the pattern is transferred into the Si epilayer using a reaction-ion-etching process (Figure 7F). Lastly, the metal NWs are removed by dissolving them in acid

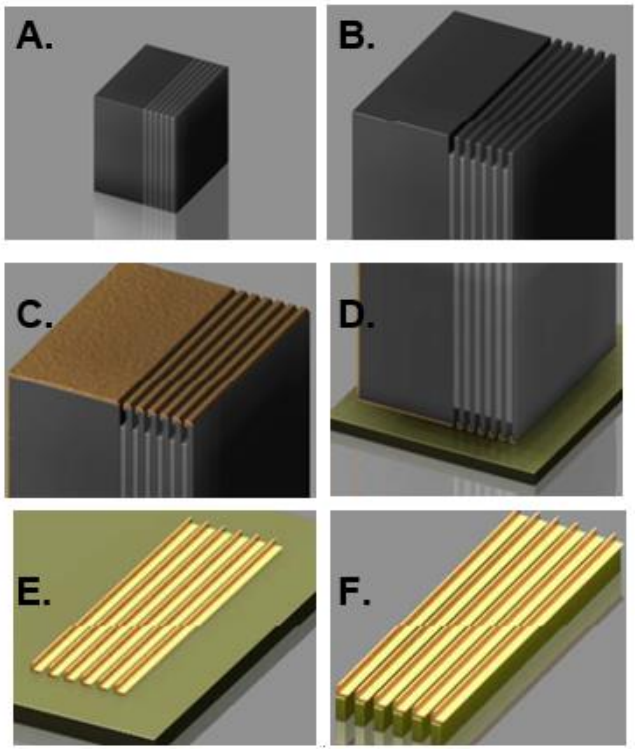

Figure7 . The SNAP process. A. First, the MBE-grown super lattice (SL) is cleaved, exposing the alternating GaAs/AlxGa(1-x)As layers. B. Next, AlxGa(1-x)As layers are selectively etched, leaving behind GaAs ridges. C. Metal is then anisotropically deposit onto the surface of the SL, forming metal NWs on the GaAs ridges. D. The metallized surface of the SL is then put in contact with an SOI substrate. E. The metal NWs are transferred using a wet-etch process. F. The NW pattern is transferred into the underlying Si epilayer using a reactive-ion etch and the metal NWs are removed

For the diffusion doping, spin-on dopants (SODs) were used as the dopant source, which consists of a high concentration of dopant ions within a silica matrix. The SODs are diluted in a solvent and are spin-coated onto the surface.

Eight inch SIMOX SOI wafers of a 32 nm epilayer of intrinsic Si in the <100> orientation and a 150 nm buried oxide layer on a ~ 0.5 mm thick Si substrate. The best method for cleaning the substrate prior to diffusion doping is the RCA cleaning method, which consists of immersing the substrates in three solutions: 5:1:1 H_2O: H_2O_2: NH_4OH at 80°C for 10 minutes;

The development of RTP recipes, the 1-D diffusion model was used to calculate the dopant profile in Si, *C(d,t,T)*

$$C(d,t,T) = C_S erfc\left(\frac{d}{2\sqrt{D(T)t}}\right).$$

Here, *erfc* is the complementary error function, C_S is the concentration of dopant atoms on the silicon surface, *D(T)* is the diffusivity coefficient, and *t* is the anneal time. *D(T)* is empirically determined for each type of dopant atom. *C(d,t,T)* varies more as a function of *T* than anneal time, and thus the RTA recipes were developed more as a function of anneal temperature than anneal time. The final step in the diffusion doping process is removing the SOD post-anneal. The best method for removing the SOD and any organic contaminants without damaging the Si epilayer was the following sequence: 30 seconds BOE immersion, brief DI H2O immersion, vigorous H2O and another vigorous H2O rinse. By repeating this sequence, most SODs will be removed.

The impurity concentration of doped substrates was calculated from a four-point resistivity measurement. A constant current is passed between the two outer probes and the voltage is measured between the two inner probes. This setup effectively counteracts any probe contact resistance and for thin wafers (where the length and width of the substrate is much larger than the thickness), the sheet resistance, R_S, can be calculated as:

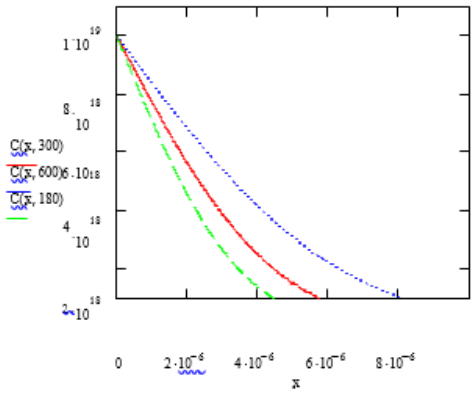

Figure 8 DOPING CONCENTRATION

$$R_S = \frac{V}{I} CF .$$

CF is the correction factor and can be approximated as 4.54 for wafers much larger than the spacing between the probe tips.

To obtain the resistivity, ρ, of the wafer, the sheet resistance is multiplied by the thickness of the Si epilayer:

$$\rho = RSW .$$

The resistivity can be used to determine the impurity concentration in the substrate by applying an empirical formula that relates to the two parameters or by a look-up table

2.2 Device structure and underlying principles

The basic FET structure fabricated from single semiconducting NWs is illustrated in Fig. below. The FET is supported on an oxidized silicon substrate with the underlying conducting silicon used as a global back gate electrode to vary the electrostatic potential of the NW. In a typical NW-FET device, two metal contacts, which correspond to source and drain electrodes, are defined by electron beam lithography followed by evaporation of suitable metal contacts. Current (I) vs. source-drain voltage (Vsd) and I vs. gate voltage (Vg) is then recorded for a NW-FET to characterize its electrical properties.

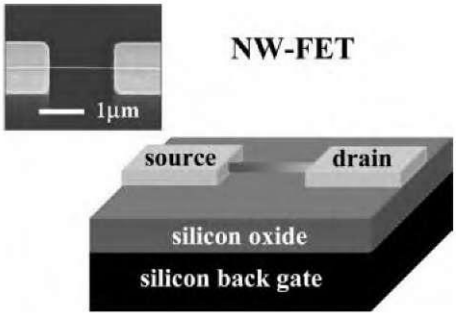

Figure 9 Schematic of a NW-FET. Inset: SEM image of a NW-FET; two metal electrodes

Variation of Vg during characterization of the NW-FET enables important qualitative and quantitative properties to be elucidated. For example, changes in Vg produce variations in the electrostatic potential of the NW, and hence change the carrier concentration and conductance of the NW. As shown in Fig. 4, p-and n-type semiconductor NWs, which are contacted at both ends to metal electrodes, respond in opposite ways to the applied gate. When a positive Vg is applied, the bands are lowered, which depletes the holes and suppresses conductivity in p-NWs, but leads to an accumulation of electrons and an enhancement in conductivity in n-NWs. Conversely, a negative Vg will increase the conductivity of p-type NWs and decrease the conductivity of the n-type NWs

. When a positive voltage is applied, the bands are lowered, which depletes the holes in p-NWs and suppresses conductivity, but leads to an accumulation of electrons **i**n n-NWs and enhances the conductivity. Conversely, a negative gate voltage will raise the bands and increase the

conductivity of p-type NWs and decrease the conductivity of the n-type NWs

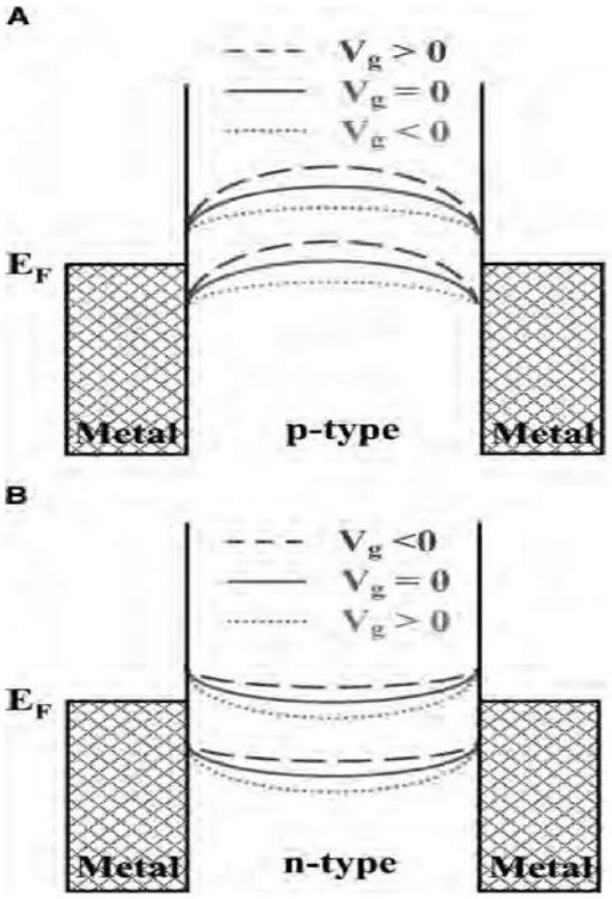

Figure 10 (A,B) Band diagrams illustrating the underlying principle for p- and n-channel NW-FETs

2.3 VOLTAGE CURRENT CHARACTERISTICS:

I vs. Vsd data obtained from a single boron-doped Si NW-FET at different Vgs are shown in Fig. The two-terminal I-Vsd curves are linear, which indicates that the metal electrodes make ohmic contacts to the NW, and moreover, the gate response demonstrates that the NW is p-type; that is, the conductance of the p-Si NW decreases (increases) with increasingly positive (negative) Vg. The transfer characteristics, I-Vg, of p-Si NW devices (Fig. 5, inset) exhibit behavior typical of p-channel metal-oxide-semiconductor FETs (MOSFETs). Significantly, the conductance modulation of the p-Si NW-FET exceeds 103, where the Vg required for switching (-10 to 10 V) could be reduced significantly by reducing the thick (600 nm) oxide dielectric layer in these back-gated devices (see below).

Gate-dependent measurements have also been used to estimate the hole concentration in p-channel NW-FETs. The total NW charge can be expressed as Q = C • Vth, where C is the NW capacitance and Vth the threshold gate voltage required to deplete completely the NW. The capacitance is given by C ffi 2pee0L/ln(2h/r), where e is the effective gate oxide dielectric constant, h is the thickness of the SiO2 layer on the substrate, L is the NW length, and r is the NW radius. The hole density, nh = Q/(e • pr2L), is estimated to be — 1018/cm3 for the device shown. In addition, it is possible to estimate the carrier mobility of the NW-FETs from the transconductance dI/dVg = m(C/L2) Vsd, where m is the carrier mobility. Plots of dI/dVg vs. Vsd are linear for Si NWs, as expected for this model, yield hole mobilities in the range of 50-800 cm2/V sec. Significantly, the p-Si NW-FET mobilities are comparable to or larger than the best p-Si planar devices, 100-300 cm2/V sec, at comparable hole densities (p – 1017-1018/cm3)

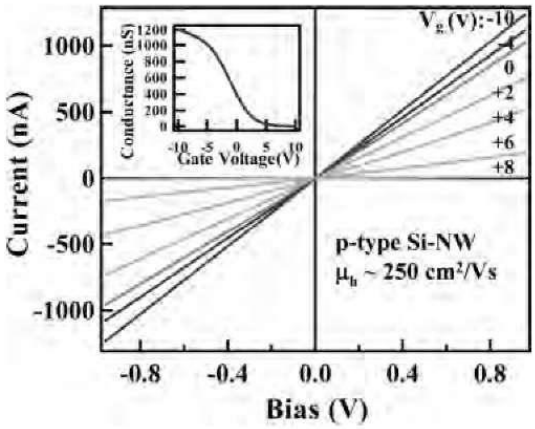

Figure11 Current vs. voltage for a p-type Si NW-FET. The numbers inside the plot indicate the corresponding gate voltages (Vg). The inset shows current vs. Vg for Vsd of 1 V

3 COMPARISON OF NANOWIRE AND MICROWIRE PERFORMANCE

3.1 DIMENSIONAL

Initial attempts to produce NW n-FETs with performance metrics comparable to the NW p-FETs were not successful. The n-FETs were fabricated exactly like the p- FETs but using substrates that were doped n-type at a concentration of ~ 10^{18} cm^{-3}. Typical performance metrics included on/off ratios of ~ 5000 and much larger **S** values than their p-type counterparts.

Low dimensional semiconductor materials are characterized by high surface-area- to-volume ratios. Recent studies have shown that the electronic properties of extremely thin (~ 10 nm) SOI films can be dominated by surface states. Similar results have also been demonstrated on Ge NWs as well. In the semiconductor industry, n-type Si devices have been more challenging to develop due to their enhanced sensitivity to surface states over p-type devices. In the NW community, few literature reports exist of NW n-FETs with high performance metrics. To understand how the high characteristic surface area impacts the performance of Si NW FETs, Si NW FETs and Si microwire (µW) FETs were prepared side-by-side on the same SOI substrate using the SNAP method for the NW FETs and more traditional lithographic patterning for the µW FETs. The device structures are schematically depicted in fig.

A SOI substrate was first doped using either p- or n-type spin-on-dopants (SODs). The SNAP process was then carried out to place a Pt NW array onto the SOI surface. Afterwards, a stripe of ~ 10 µm wide and 10 nm thick Pt thin film was patterned adjacent to the SNAP Pt NWs by e-beam lithography (EBL) and metal deposition. The Pt NWs or microstructures served as masks for a reactive ion etching (RIE) process to transfer the Pt NWs and stripes patterns to form analogous Si NWs and stripes. The resulting structure consisted of an array of Si NWs adjacent to a thin film of Si, both on a SiO_2 dielectric (Figure 12C). Ti/Pt (20 nm/50 nm) S/D contacts were patterned by EBL to be 150 nm wide and separated 2 µm apart. Al_2O_3 (10 nm) was then deposited as a gate dielectric, and a Ti top gate electrode was deposited to conclude the fabrication process, as shown in. Figure 12C

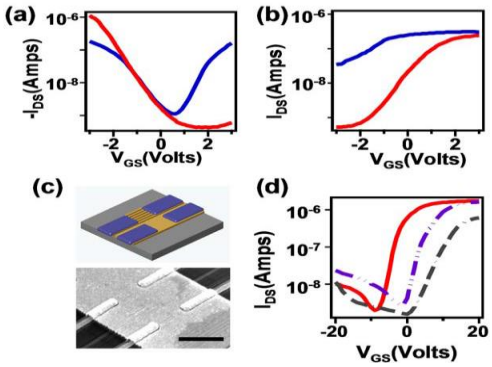

Figure 12. Comparison of NW and µW FET performance. I_{DS}-V_{GS} curves of **A.** P-type and **B.** n-type NW FETs (red) and µW FETs (blue). **C.** Device structure with µW NW FETs side by side. Scale bar: 2µm. **D.** I_{DS}-V_{GS} curves of NW n-FETs after different treatments. Solid red trace: as-fabricated; purple broken line: after O_2 plasma; gray broken line: after H_2 plasma. For all devices, V_{DS}=1.5 V for n-type and -1.5 V for p-type.

3.2 VOLTAGE CURRENT COMPARISON:

Devices were characterized and compared, namely NW p- and n-FETs,. The as-fabricated NW p-FETs exhibited similar characteristics as those described in the previous section,[28] i.e., high on- current at high negative gate potentials and low off-current at high positive gate potentials. The µW p-FETs, however, were typified as ambipolar: a high on-current was observed at both positive and negative gate potentials and a low off- current was only seen at low gate potentials (Figure 12A). This suggests that for µW p- FETs, both hole

(at negative gate potentials) and electron carriers (at positive gate potentials) are important for the conductance, whereas in NW p-FETs only hole carriers

are significant. Given that the NW and μW FETs are fabricated side by side on the same

substrate and have undergone the same processing sequences, the doping levels, crystal orientations and electrical contacts should be identical. The only difference should be the increased surface-area-to-volume ratio for the NWs. It is therefore reasonable to suspect that the difference in device characteristics is mainly a result of the surface effects. Similar differences were also observed on n-FETs: NW n-FETs could be turned off easily while neighboring μW n-FETs that have identical parameters exhibited a noticeably weaker gate response (Figure 12B). It appears that the μW n-FETs have a higher electron carrier concentration than the analogous NW devices.

Considering that all of the measurements were conducted in ambient air, it is suspected that the surfaces of NWs tend to p-dope the channel, hence the hole carriers are enhanced and electrons are suppressed. Similar effects have been widely reported for CNT and organic-material devices. To better understand this, systematic surface treatments on all devices were performed and the corresponding changes of transport characteristics were compared. Taking NW n-FETs as an example, the as-fabricated devices were measured with a bottom gate (i.e., using the underlying Si wafer of the SOI substrate as a gate electrode). These devices were then subjected to gentle O_2 and H_2 plasma treatments (Figure 12D). Such treatments constitute standard cleaning processes that are often employed during FET fabrication. After the O_2 plasma treatment, the clear trend was that the p-channel was enhanced and n-channel suppressed (purple curve in Figure 12D). This may arise because surface-adsorbed O_2 p-dopes the NW channels. By contrast, both the p- and n-channels were suppressed by the H_2 plasma treatment (gray curve in Figure 12D). This universal effect likely arises from surface damage that results from the reaction of H_2 or H-atoms with the Si native oxide, and thus introduces surface states that can trap both holes and electrons. Similar experiments were also carried out on NW p-FETs and μW FETs. And for all devices, O_2 treatments enhanced p-channel and suppressed n-channel while H_2 suppressed both p- and n- channels. Importantly, the effects were always more pronounced for the NW FETs. NW FET performance metrics were clearly more dependent upon the surface treatments that were employed

4 CONCLUSION:

MOSFETs fabricated from small groups of these NWs exhibited extremely good performance characteristics, including high on-current, high on/off ratios and low subthreshold swings. In particular, the unprecedented S ~ 80 mV/decade for p- type Si NWs MOSFETs reveals that the SNAP process can produce high-quality Si NWs with negligible numbers of defects. These results were valid for statistical numbers of devices, and provide a compelling argument for the reproducibility of this process.

In addition, it was demonstrated that Si NW MOSFETs are sensitive to the surface properties, and that information was used as feedback to improve the nanofabrication techniques to achieve consistent performance from n-type Si NW MOSFETs. These results opened up the opportunity to produce complementary logic circuits within ultra-high- density NW arrays.

5 APPENDICES:

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