University of Asia Pacific

Department of Computer Science and Engineering

Mid-Semester Examination Spring-2021

Program: B.Sc. in CSE

Course Title: Design and Testing of VLSI Course No. 457 Credit: 3.00

Time: 1.00 Hour. Full Mark: 60

There are Four Questions. Answer three questions including Q-1 and Q-2.

1. a. Sketch a transistor-level schematic for a compound CMOS logic gate for the following function: **10**

$F = \overline{(A+B).(C+D)}$

b. Briefly explain how to choose an appropriate model for Yield in a chip from defect density information. **10**

2. Consider a wafer with Defect density 2 defects/cm^2, clustering parameter 0.75, chip width 6mm, chip length 7mm. Each wafer has 100 chips. The cost of processing a wafer is $365. **20**

i. Calculate the processing cost of 20 chips.
ii. Calculate the processing cost per chip if the chip area is increased by 20%

3. a. Silicon is doped so that its Fermi level has gone close to 2 eV of Valence Band. **10**

i. Determine the doping level.
ii. Determine the doping level if Fermi level had gone close to 2 eV of Conduction Band.

b. What type of semiconductor does it become after doping in i & ii respectively? Briefly explain why in your own words? **10**

OR

4. a. Consider an nMOS transistor with W/L = 10. In this process, the gate oxide thickness is 100 Å and the mobility of electrons is 350 $cm^2/V\cdot s$. The threshold voltage is 1 V. Plot I_{ds} vs. V_{ds} for V_{gs} = 5 V. **10**

b. Explain how did you get the point where saturation begins? **10**