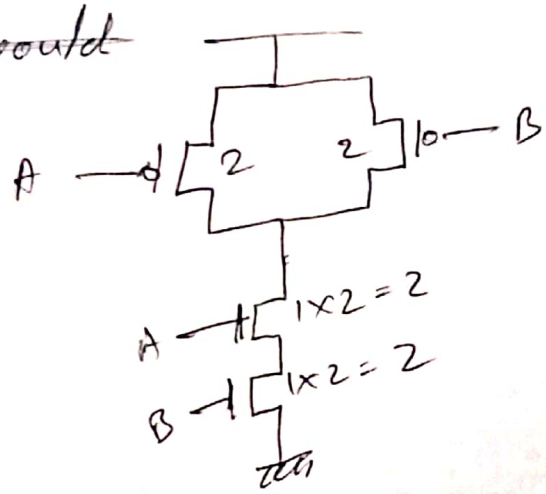
Answer to the Q. No. 1

For 2 input ~~Nand~~ NAND:

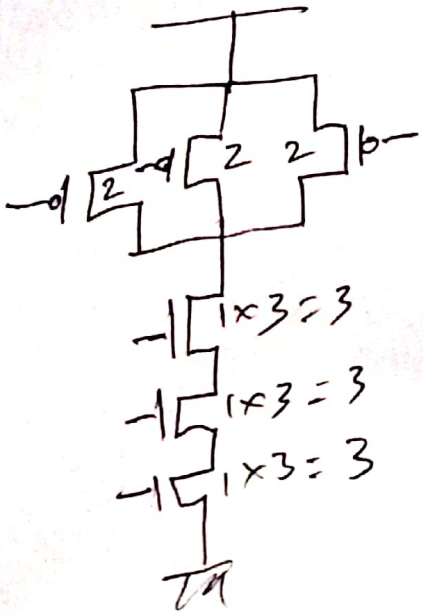
~~There would~~



$\therefore C_{in} = 2+2 = 4$

$\therefore g = \frac{4}{2+1} = \frac{4}{3}$

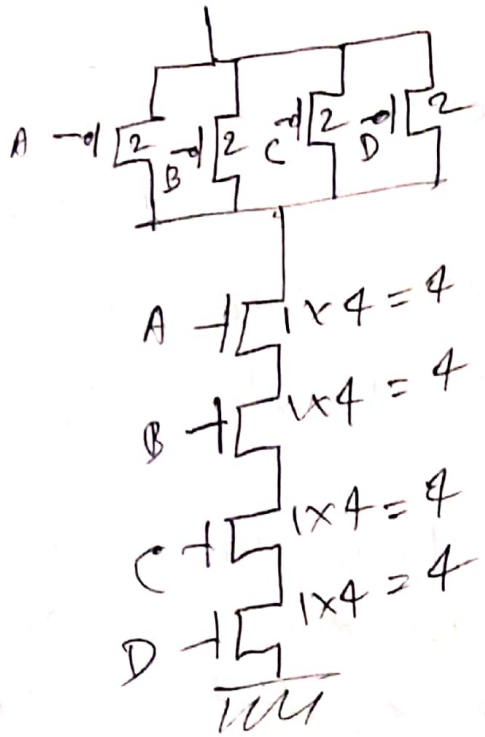
For 3 input NAND



$C_{in} = 2+2+3 = 5$

$g = \frac{5}{3}$

for 4 input NAND:



$$C_{in} = \frac{2+4}{3} = \frac{6}{3} \quad 2+4 = 6$$

$$g = \frac{6}{3}$$

From these three scenarious we can formulate a equation for calculating effort for n input NAND.

$$\text{Effort, } g = \frac{n+2}{3}$$

Ans.

Answer to the Q.No. 2

The logical effort of the inverter is $g=1$, electrical effort of the inverter is $h=1$, The parasistic delay of the inverter is $p=1$. So the delay of each stage is, $d = gh + p = 1+1 = 2$

The N stage ring oscillator has a period of 2N stage delay because of. Therefore total delay of the N stage oscillator would be

$2 \times 2N = 4N$.

Here,

$N = 012$

$\therefore$ delay $= 4 \times 12 = 48$