University of Asia Pacific

Department of CSE

Name: Rashik Rahman

Reg ID: 17201012

Year: 4th

Semester: 2nd

Course Code: CSE 457

Course Title: Design and testing of VLSI

Date: 15.09.2021

"During Examination and upload time I will not take any help from anyone. I will give my exam all by myself."

University of Asia Pacific

Admit Card

Mid-Term Examination of Spring, 2021

Financial Clearance	PAID

Registration No : 17201012

Student Name : Rashik Rahman

Program : Bachelor of Science in Computer Science and Engineering

Sl.NO.	COURSE CODE	COURSE TITLE	CR.HR.	EXAM. SCHEDULE
1	CSE 425	Computer Graphics	3.00	
2	CSE 426	Computer Graphics Lab	1.50	
3	CSE 429	Compiler Design	3.00	
4	CSE 430	Compiler Design Lab	1.50	
5	BUS 401	Business and Entrepreneurship	3.00	
6	BUS 402	Business and Entrepreneurship Lab	0.75	
7	CSE 457	Design and Testing of VLSI	3.00	
8	CSE 458	Design and Testing of VLSI Lab	0.75	
9	CSE 400	Project / Thesis	3.00	

Total Credit: 19.50

1. Examinees are not allowed to enter the examination hall after 30 minutes of commencement of examination for mid semester examinations and 60 minutes for semester final examinations.

2. No examinees shall be allowed to submit their answer scripts before 50% of the allocated time of examination has elapsed.

3. No examinees would be allowed to go to washroom within the first 60 minutes of final examinations.

4. No student will be allowed to carry any books, bags, extra paper or cellular phone or objectionable items/incriminating paper in the examination hall.
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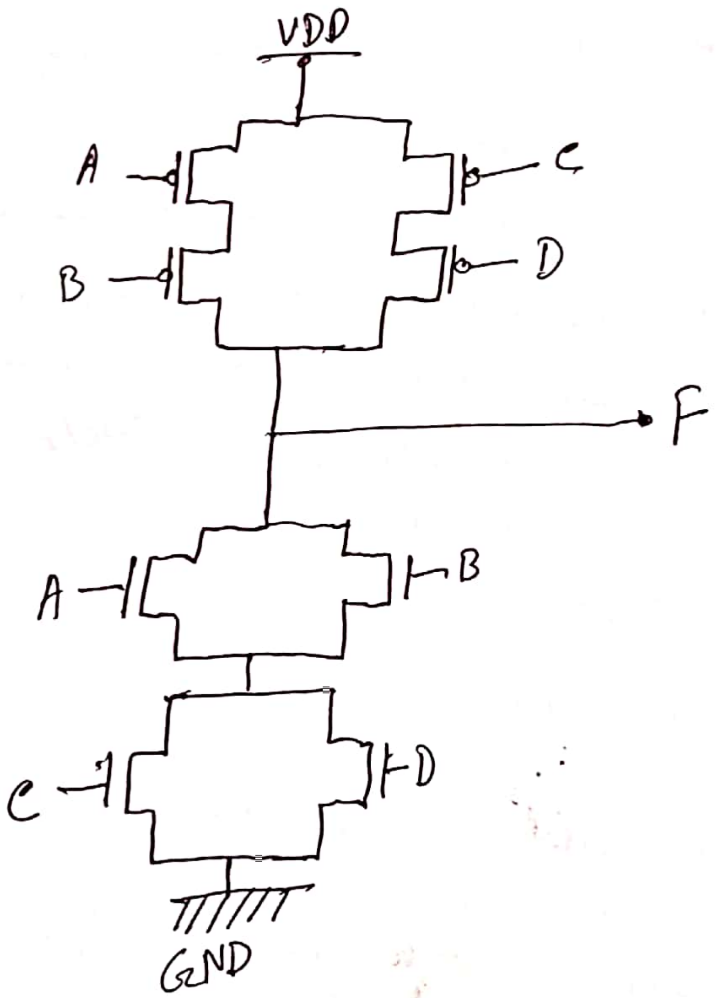
Answer to the Q. No. 1(a)

Output, $F = \overline{(A+B)\cdot(C+D)}$

We know in NAND CMOS, NMOS is ~~sere~~ in series and PMOS in parallel. And in NOR CMOS, NMOS is in parallel and PMOS in series.



Answer to the Q-NO. 1(b)

There are 4 models of Yield depending on the defect density information. These are the followings

i) The Poisson Model:

In this model defect density is constant across each wafer and from wafer to wafer. For this model yield equation is, $Y = e^{-AD}$ where A is chip area and D is defect density.

ii) The Murph Model:

In this model defect density ~~tends to~~ increases towards the edge of the wafer and defect density varies ~~each~~ across the wafer and from wafer to wafer. For this model yield equation is, $Y = \left\{\frac{1-e^{-AD}}{AD}\right\}^2$.

iii) The seed model:

In this model the defects tends to clusters and many clusters are formed. Here defect density varies across the wafer and from wafer to wafer. Here, $Y = \frac{1}{1+AD}$

iv) The Moore Model:

In this model defects tends to cluster at the edge of the wafer. For this reason we may see higher defect density cluster neare the edges. Here, $Y = e^{-\sqrt{AD}}$

Except these four rules we may have to use another rule when a certain parameter alpha (α) is given. Alpha is a clustering parameter. Then yield equation would be,

$$Y = \left(1 + \frac{Ad}{\alpha}\right)^{-\alpha}.$$

Answer to the Q.No.2 (a)

Here,

Defect density, $d = 2$ defect/cm^2

Clustering parameter, $\alpha = 0.75$

Chip area, $A = 6 \times 7\ mm^2$
$= 42\ mm^2$
$= 0.42\ cm^2$

Each wafer has 100 chips and processing cost of wafer is 365 \$.

(i) Now,

$$\text{Yield, } Y = \left(1 + \frac{Ad}{\alpha}\right)^{-\alpha}$$

$$= \left(1 + \frac{0.42 \times 2}{0.75}\right)^{-0.75}$$

$$= \cancel{1+0.9185}\ (2.12)^{-0.75}$$

$$= \cancel{1.919}\ \cancel{0.599}\ 0.569$$

$$\text{Processin cost pen chip} = \cancel{\frac{365}{100 \times 1.919}}\ \$ \quad \frac{365}{100 \times 0.569}\ \$$$

$$= \cancel{1.9\ \$}\ 6.414\ \$$$

$$\therefore \text{ " " of 20 chips} = 6.414 \times 20\ \$$$

$$= \cancel{38\ \$}\ 128.295\ \$$$

(ii)

If the chip size is increase by 20% then yield would be, $\cancel{Y = \left(\frac{0.42 \times 1.2 \times 2}{0.75}\right)^{-0.75} + 1}$

$$Y = \left(\frac{0.42 \times 1.2 \times 2}{0.75} + 1\right)^{-0.75}$$

$$= (2.344)^{-0.75}$$

$$= 0.528$$

N.B
here we increase area by 120%. thus multiply area with $\frac{120}{100}$
$= 1.2$

after ~~size~~ chip area ~~size~~ increased then the wafer contains $100/1.2 = 83$ chips.

$\therefore$ Cost per chip $= \frac{365}{83 \times 0.528}$

$= 8.33\ \$$

Answer to the Q. No. 4(a)

Given,

$W/L = 10$

$t_{ox} = 100\,\text{Å} = 100 \times 10^{-8}\ cm$

$\mu = 350\ cm^2/V.s$

$V_t = 1V$

$V_{gs} = 5V$

We know,

permitivity of free space, $\epsilon_0 = 8.85 \times 10^{-14}\ F/cm$

permitivity of SiO_2, $K_{ox} = 3.9$

$C_{ox} = K_{ox} \frac{\epsilon_0}{t_{ox}} = 3.9 \times \frac{8.85 \times 10^{-14}\ F/cm}{100 \times 10^{-8}\ cm}$

$= 3.451 \times 10^{-7}\ F/cm^2$

C_{ox} is the capacitance per unit area of the gate oxide.

We know,

$$\beta = \mu C_{ox} \frac{W}{L}$$

$$= 350 \times 3.451 \times 10^{-7} \times 10 \ \frac{cm^2}{V.s} \times \frac{F}{cm^2}$$

$$= 1.21 \times 10^{-3} \ \frac{A}{V^2}$$

$$\boxed{F = \frac{A.s}{V}}$$

Now,

Saturation point, $V_{GT} = V_{gs} - V_t$

$$= (5-1)\,v$$

$$= 4\,v$$

We know,

$$I_{ds} = \begin{cases} 0 & ; V_{gt} < V_t \\ \beta\left(V_{GT} - \frac{V_{ds}}{2}\right) V_{ds} & ; V_{ds} < V_{dsat} \\ \frac{\beta}{2} V_{GT}^2 & ; V_{ds} > V_{dsat}. \end{cases}$$

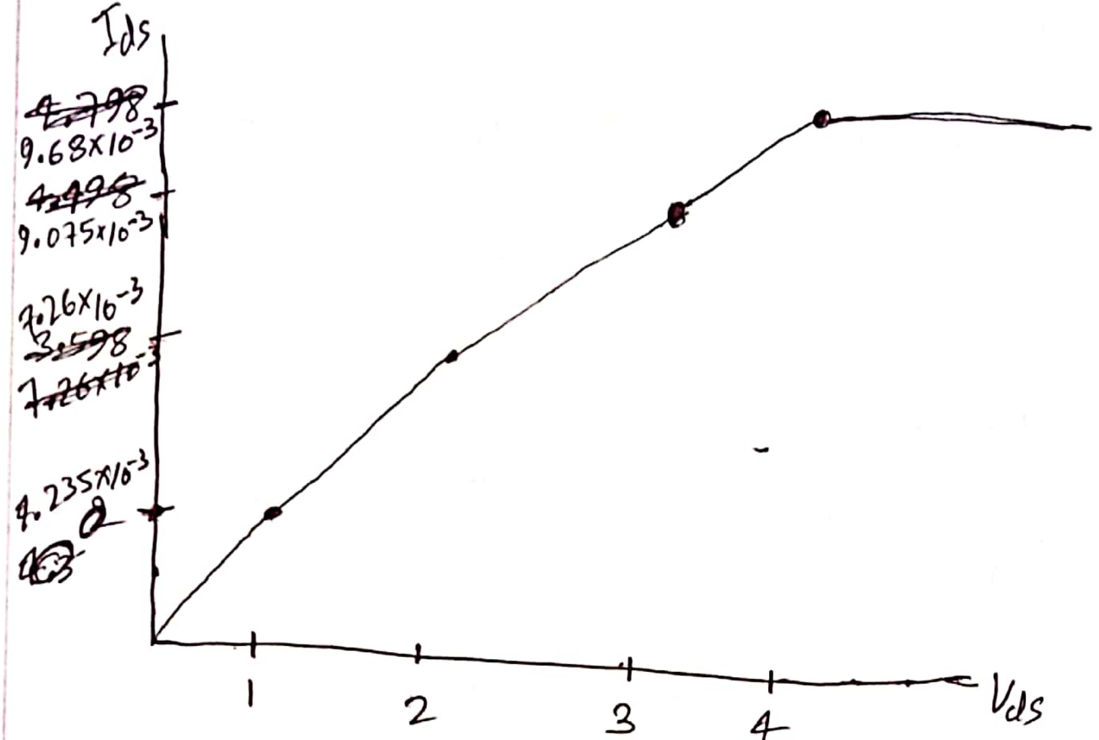


Fig: Ids vs. Vds.

At $V_{ds} = 4$ we his saturation point where $V_{GT} = V_{ds}$

for,

$V_{ds} = 1$,

$$I_{ds} = \beta\left(V_{GT} - \frac{V_{ds}}{2}\right) V_{ds}$$

$$= 1.21\times10^{-3}\left(4 - \frac{1}{2}\right)\times1 = 4.235\times10^{-3}$$

for, $V_{ds} = 2$

$$I_{ds} = \beta\left(V_{GT} - V_{ds}/2\right) V_{ds} = 1.21\times10^{-3}\left(4 - \frac{2}{2}\right)\times2$$

$$= 7.26\times10^{-3}$$

for $V_{ds} = 3$,

$$I_{ds} = \beta\left(V_{GT} - \frac{V_{ds}}{2}\right)V_{ds} = 1.21\times10^{-3}\left(4 - \frac{3}{2}\right)\times 3$$
$$= 9.075\times10^{-3}$$

for, $V_{ds} = 4$,

$$I_{ds} = \frac{\beta}{2} V_{GT}^2 = \frac{1.21\times10^{-3}}{2} \times 4^2$$
$$= 9.68\times10^{-3}$$

Answer to the Q. No. 4 (b)

Where $V_{ds} = V_{GT}$ happens at that point saturation starts. We know $V_{ds} = V_{gs} - V_t$

So to get the ~~poi~~ ~~satio~~ saturation point V_{GT} we can use the following equation,

$$V_{Gt} = V_{gs} - V_t \quad \text{—(i)}$$

Where,

V_{GT} = saturation point

V_{gs} = voltage difference between gate and source

V_t = threshold voltage

Vd

V_{ds} = voltage difference between drain and source.

~~So we can say that when~~

— 0 —