DANG Nam Khanh

PERSONAL INFORMATION

Adaptive System Laboratory
University of Aizu, Aizu-Wakamatsu,
Fukushima, JAPAN

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RESEARCH INTERESTS

ASIC/FPGA design, digital signal processing, video compression, on-chip communication, hardware-software co-design.

EDUCATION

University of Aizu
Department of Computer Engineering

PhD Program **Oct 2014 - Now**

- PhD Theme: "Reliable Many-core 3D-NoC Processor Targeted for Real-Time Vision Applications"
- Advisor: Prof. Ben Abdallah, Abderazek
- Advisor: Assoc. Prof. Xuan-Tu Tran

University of Paris XI

M.Sc. Information, Systems and Technology **Dec 2011 - Mar 2013**

- Grade: 14.0/20
- Graduation Thesis: "An Efficient VLSI design of H.264/AVC Inter-Prediction"
- Advisor: Asoc. Prof. Xuan-Tu Tran
- Description: Thesis proposes an efficient architecture of Main Profile H.264/AVC Inter-Prediction as a part of VENGME Project. This architecture supports variable block-size, bi-predictive and full-fractional motion estimation. Proposed design applies three main key ideas: full-search algorithm, bandwidth efficiency technique and pipeline coding flow. Proposal is designed in VHDL, verified and implemented in 180 *nm* CMOS technology.

University of Engineering and Technology, Vietnam National University, Hanoi, Vietnam

B.Sc., Electronics and Telecommunication **Sep 2007 - Jun 2011**

- Grade: 2.96/4.0
- Graduation Thesis: "Design and implementation of a Re-configurable Router for On-chip Networks"
- Advisor: Asoc. Prof. Xuan-Tu Tran
- Description: Thesis aim to propose re-configurable router for NoC with two steps. First step, the normal router is built for wormhole 2D-Mesh topology Network-on-Chip model. Second step, a by-pass method for router is proposed to avoid router errors. Both of normal and reconfigurable router are designed in VHDL, verified and implemented in FPGA. The normal router model is presented in ICDV 2011.

ACADEMIC EXPERIENCE

The University of Aizu, Aizu-Wakamatsu, Fukushima, Japan

Research Assistantship **Oct. 2014 - present**
Join Adaptive System Laboratory to research PhD theme.

University of Engineering and Technology, Vietnam National University, Hanoi, Vietnam

R&D Engineer **Jul. 2011 - Sep. 2014**
Joins VENGME QGDA.10.02 Project which develop an H264/AVC video encoder in ASIC. Proposes an architecture for inter-prediction. The design is simulated, verified and implemented in CMOS technology. This model is also integrated in H264 encoder and run system simulation.

Research Student **Dec. 2009 - Jun. 2011**

Joins Smart Integrated System Key Laboratory as researching student. Learning VHDL and some EDA tool. Focus on design reconfigurable NoC Router as bachelor thesis.

Publications

Nam-Khanh Dang, Xuan-Tu Tran, Alain Merigot. Apr, 2014, **An Efficient Hardware Architecture for Inter-Prediction in H.264/AVC Encoders**. In Proceedings of the 17th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems (IEEE DDECS 2014), pp. 294-297, Warsaw, Poland.

Nam-Khanh Dang, Xuan-Tu Tran, Thanh-Vu Le-Van. 2011. **FPGA Implementation of a Low Latency and High Throughput Network-on-Chip Router Architecture**. The 2011 International Conference on Integrated Circuits, Design, and Verification.

Nam-Khanh Dang, Xuan-Tu Tran. Nov, 2013. **A VLSI Implementation for Inter-Prediction Module in H.264/AVC Encoders**. The 2013 International Conference on Integrated Circuits, Design, and Verification.

Professional Experience

Dolphin Technology Vietnam Center, Ltd, Hanoi, Vietnam

RTL Designer **Dec 2010 - Apr 2011**

Design multi-input multi-output arbiter with first come first serve priority using matrix base for multi-bank memory controller.

Skills

- Hardware Design: VHDL, verilog/systemverilog.
- Design Tools: Modelsim, Xilinx ISE, Design Compiler.
- Languages: Matlab, C++, Perl, some use of Unix shell scripts.
- Applications: Matlab, Vim, LaTeX, common Windows office, spreadsheet, and presentation software.
- Operating Systems: Unix/Linux, Windows.

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