Audio Generator

Product Guide v1.03

January 6th, 2015

Draft Release

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
October 21st, 2014	1.00	Initial release
October 22nd, 2014	1.01	Changed mapping of channel status bits
December 10th, 2014	1.02	Added audio input
January 6th, 2014	1.03	Updated audio generation with continuous sine pattern Fixed channel status generation

Table of Contents

1. Overview

The audio generator can generate a test audio signal on up to eight audio channels. The audio generator has two AXI interfaces. The audio AXI stream supplies multiple channels uncompressed audio data in AES3 format. A processor, for example the MicroBlaze, controls the audio generator block through the AXI Lite interface.

2. Signals

The audio generator signals are listed in table 1. The audio generator has only been tested with the AXI streaming clock and the Audio clock connected to the same clock.

Table 1 Audio generator signals

Name	Direction	Width	Description
Audio Interface			
axis_aresetn	input	1	Reset (active low)
axis_clk	input	1	Clock
Audio output interface			
axis_aud_pattern_tdata_out	output	32	Audio data
axis_aud_pattern_tid_out	output	3	Audio stream number
axis_aud_pattern_tvalid_out	output	1	Valid
axis_aud_pattern_tready_in	input	1	Ready
Audio input interface			
axis_aud_pattern_tdata_in	input	32	Audio data
axis_aud_pattern_tid_in	input	3	Audio stream number
axis_aud_pattern_tvalid_in	input	1	Valid
axis_aud_pattern_tready_out	output	1	Ready
Audio Clock			
aud_clk	input	1	Audio clock (512*fs)
CPU Interface			
axi_aresetn	input	1	Reset (active low)
axi_aclk	input	1	Clock
axi_awaddr	input	32	Write address
axi_awprot	input	3	Write address protection
axi_awvalid	input	1	Write address valid
axi_awready	output	1	Write address ready
axi_wdata	input	32	Write data
axi_wstrb	input	4	Write data strobe
axi_wvalid	input	1	Write data valid
axi_wready	output	1	Write data ready
axi_bresp	output	2	Write response
axi_bvalid	output	1	Write response valid
axi_bready	input	1	Write response ready
axi_araddr	input	32	Read address
axi_arprot	input	3	Read address protection
axi_arvalid	input	1	Read address valid
axi_arready	output	1	Read address ready
axi_rdata	output	32	Read data
axi_rresp	output	2	Read response
axi_rvalid	output	1	Read data valid
axi_rready	input	1	Read data ready

3. Register map

The CPU interface controls the operation of the audio generator. All registers are 32-bits wide, but can be written per byte. Table 2 shows the register space.

Table 2 Register map

Byte offset (hex)	Register	Access	Description
00	AUD_CTRL	R/W	Audio Control
04	AUD_CFG	R/W	Audio Configuration
10	CH1_CTRL	R/W	Channel 1 Control
20	CH2_CTRL	R/W	Channel 2 Control
30	CH3_CTRL	R/W	Channel 3 Control
40	CH4_CTRL	R/W	Channel 4 Control
50	CH5_CTRL	R/W	Channel 5 Control
60	CH6_CTRL	R/W	Channel 6 Control
70	CH7_CTRL	R/W	Channel 7 Control
80	CH8_CTRL	R/W	Channel 8 Control
A0	CHANSTAT0	R/W	Channel Status 0
A4	CHANSTAT1	R/W	Channel Status 1
A8	CHANSTAT2	R/W	Channel Status 2
AC	CHANSTAT3	R/W	Channel Status 3
B0	CHANSTAT4	R/W	Channel Status 4
B4	CHANSTAT5	R/W	Channel Status 5

3.1. Audio Control register

The Audio Control register is used to reset and enable the audio generator. The reset bit will automatically return to 0 after being set to 1. The AUD_START bit must be set to 1 before writing to the Audio Configuration registers. When the AUD_START bit is set to 0, the audio on the Audio Input Interface will be looped through to the Audio Output Interface.

Table 3 Audio Control register

Bits	Name	Description
0	AUD_RESET	Audio generator reset. Will be cleared automatically.
1	AUD_START	Start audio generator. Must be set to 1 before setting other registers.
2	AUD_UPD_CFG	Updates the audio generator configuration.
3	AUD_DROP	Drop input audio. When set the audio generator always is ready to accept data from the audio input and drops the contents.
31:3	RSVD	Reserved

3.2. Audio Configuration register

The Audio Configuration register sets the audio sample rate and the number of enabled audio channels. The audio sample rate setting is used to calculate the number of audio samples in 250 ms for use in the Ping audio pattern (see 3.3). The audio channels are enabled starting from channel 1. When set to 4, audio channels 1 to 4 are enabled while channels 5 to 8 are disabled.

Table 4 Audio Configuration register

Bits	Name	Description
3:0	SAMPRATE	Sample rate of the audio data (see table 5).
7:4	reserved	Reserved
11:8	NUMCHANS	Number of active audio channels (0-8). Should be set to an even number.
31:12	RSVD	Reserved

Table 5 Sample rate encoding

SAMPRATE	Audio sample rate (kHz)
0	32
1	44.1
2	48
3	88.2
4	96
5	176.4
6	192
7	32
15-8	Reserved

3.3. Channel Control registers

The eight Channel Control registers each control one of the channels. The layout for each registers is the same (see table 6). The audio data pattern can be set to three different patterns. After reset the pattern will be set to Silence. The Ping pattern consists of a sine wave during 250 ms followed by silence for another 250 ms, then back to the sine wave. The audio pattern will only be sent out when the number of channels set in the NUMCHANS field of the Audio Configuration register is set to the channel number or higher.

Table 6 Channel *n* Control register

Bits	Name	Description
1:0	PATTERN	Audio data pattern to generate (see table 7).
7:2	RSVD	Reserved
11:8	PERIOD	Reserved, write as zero.
31:12	RSVD	Reserved

Table 7 Audio pattern encoding

PATTERN	Audio pattern
00	Silence
01	Sine wave
10	Ping
11	Ramp

3.4. Channel Status registers

The Channel Status registers are used to set the channel status bits for insertion in the audio stream. The channel status consists of 192 bits total, one bit per audio sample. The first 42 bits of the status can be set in these registers. The other 150 bits are set to 0. The channel status is sent with CHANSTAT[0] in the first audio sample of the audio frame.

Table 8 Channel Status 0 register

Bits	Name	Description
31:0	CHANSTAT[0:31]	Channel status bits for audio samples 0 to 31.

Table 9 Channel Status 1 register

Bits	Name	Description
31:22	CHANSTAT[32:41]	Channel status bits for audio samples 32 to 41.
21:0	CHANSTAT[42:63]	Reserved for channel status bits for audio sample 42 to 63

Table 10 Channel Status 2 register

Bits	Name	Description
31:0	CHANSTAT[64:95]	Reserved for channel status bits for audio sample 64 to 95

Table 11 Channel Status 3 register

Bits	Name	Description
31:0	CHANSTAT[96:127]	Reserved for channel status bits for audio sample 96 to 127

Table 12 Channel Status 4 register

Bits	Name	Description
31:0	CHANSTAT[127:159]	Reserved for channel status bits for audio sample 127 to 159

Table 13 Channel Status 5 register

Bits	Name	Description
31:0	CHANSTAT[160:191]	Reserved for channel status bits for audio sample 160 to 191