

Figure 1: State machine(s) (a) at position 1, (b) at position 2, (c) at position 3.

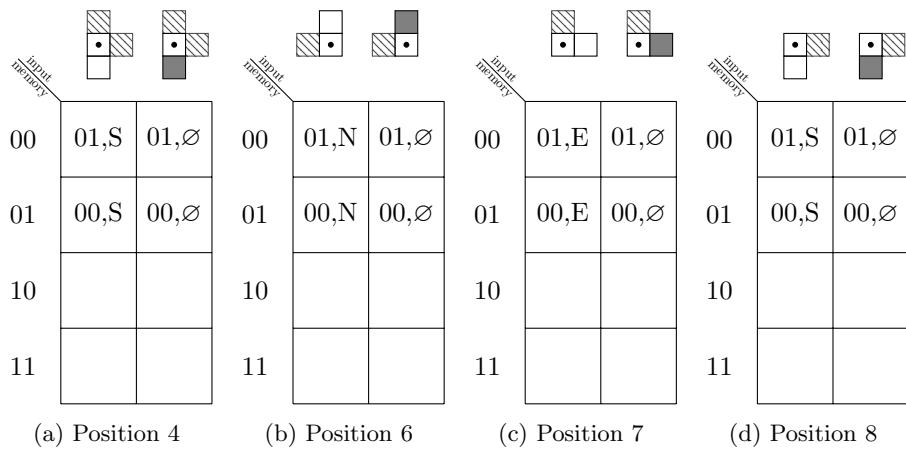


Figure 2: State machine(s) (a) at position 4, (b) at position 6, (c) at position 7, (d) at position 8.

Diagram illustrating two state machines at position 5. The top row shows the initial state for each of the 8 grids. The bottom part shows a 4x8 grid where rows represent memory inputs (00, 01, 10, 11) and columns represent memory addresses (00, 01, 02, 03, 04, 05, 06, 07). Each cell contains a pair: (state, action).

00	11,∅	01,∅	01,∅	11,∅	01,∅	01,∅	11,∅	01,∅
01	00,W	00,N	00,N	10,∅	00,N	00,N	00,∅	00,∅
10	11,∅	11,∅	11,∅	11,∅	11,∅	11,∅	11,∅	01,∅
11	00,W	00,W	00,W	00,W	00,W	00,W	10,∅	00,∅

00	01,∅	01,∅	01,∅	01,∅	11,∅	11,∅	11,∅	11,∅
01	00,N	00,N	00,N	00,N	00,W	00,W	10,∅	10,∅
10	11,∅	11,∅	01,∅	01,∅	11,∅	11,∅	11,∅	11,∅
11	10,∅	10,∅	10,∅	00,∅	00,W	00,W	10,∅	10,∅

(a) Position 5

Figure 3: State machine(s) (a) at position 5.

<i>input memory</i>								
00	01,∅	01,∅	11,∅	01,∅	11,∅	01,∅	11,∅	01,∅
01	00,∅	00,N	10,∅	00,N	10,∅	00,N	10,∅	00,N
10	11,∅	01,∅	11,∅	01,∅	11,S	11,S	11,S	11,S
11	10,∅	10,∅	10,∅	10,∅	10,∅	10,∅	10,∅	10,∅

<i>input memory</i>								
00	11,∅	01,∅	11,∅	01,∅	11,∅	01,∅	11,∅	01,∅
01	10,∅	00,N	10,∅	00,N	10,∅	00,N	10,∅	00,N
10	11,S							
11	10,∅	10,∅	10,∅	10,∅	10,∅	10,∅	10,∅	10,∅

(a) Position 9

Figure 4: State machine(s) (a) at position 9.