

Figure 1: State machine(s) (a) at position 1, (b) at position 2, (c) at position 3.

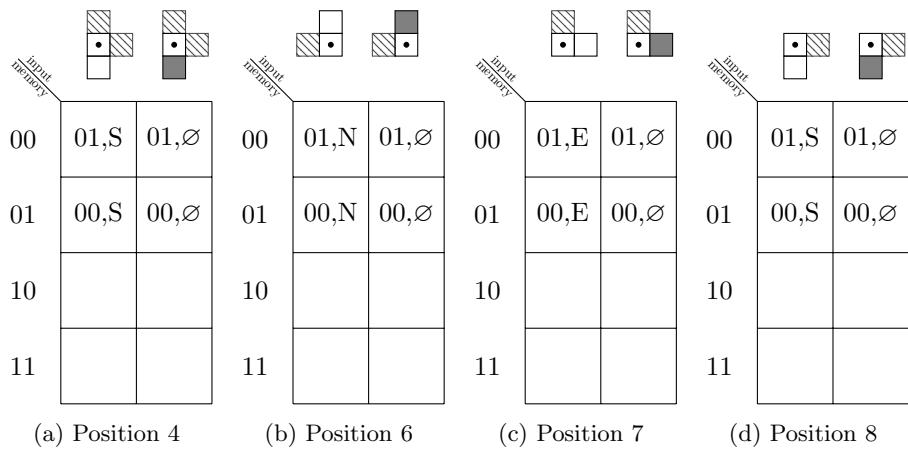


Figure 2: State machine(s) (a) at position 4, (b) at position 6, (c) at position 7, (d) at position 8.

The diagram illustrates two state machines at position 5. Each machine consists of 8 states, represented by 3x3 grids. The top row shows the initial state for each column. The bottom part is a state transition table.

| | 01, \emptyset | 11, \emptyset |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 00 | 01, \emptyset | 11, \emptyset |
| 01 | 10, W | 00, \emptyset | 10, \emptyset |
| 10 | 01, \emptyset | 11, \emptyset | 11, \emptyset | 01, \emptyset | 11, \emptyset | 11, \emptyset | 01, \emptyset | 11, \emptyset |
| 11 | 10, W | 10, N | 10, N | 00, \emptyset | 10, N | 10, N | 10, \emptyset | 10, \emptyset |

| | 01, \emptyset | 01, \emptyset | 11, \emptyset | 11, \emptyset | 01, \emptyset | 01, \emptyset | 01, \emptyset | 01, \emptyset |
|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 00 | 01, \emptyset | 01, \emptyset | 11, \emptyset | 11, \emptyset | 01, \emptyset | 01, \emptyset | 01, \emptyset | 01, \emptyset |
| 01 | 00, \emptyset | 00, \emptyset | 00, \emptyset | 10, \emptyset | 10, W | 10, W | 00, \emptyset | 00, \emptyset |
| 10 | 11, \emptyset | 11, \emptyset | 11, \emptyset | 11, \emptyset | 01, \emptyset | 01, \emptyset | 01, \emptyset | 01, \emptyset |
| 11 | 10, N | 10, N | 10, N | 10, N | 10, W | 10, W | 00, \emptyset | 00, \emptyset |

(a) Position 5

Figure 3: State machine(s) (a) at position 5.

| <i>input memory</i> | | | | | | | | |
|---------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 00 | 01, \emptyset | 11, \emptyset | 01, \emptyset | 11, \emptyset | 01,S | 01,S | 01,S | 01,S |
| 01 | 00, \emptyset |
| 10 | 11, \emptyset | 11, \emptyset | 01, \emptyset | 11, \emptyset | 01, \emptyset | 11, \emptyset | 01, \emptyset | 11, \emptyset |
| 11 | 10, \emptyset | 10,N | 00, \emptyset | 10,N | 00, \emptyset | 10,N | 00, \emptyset | 10,N |

| <i>input memory</i> | | | | | | | | |
|---------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 00 | 01,S |
| 01 | 00, \emptyset |
| 10 | 01, \emptyset | 11, \emptyset |
| 11 | 00, \emptyset | 10,N |

(a) Position 9

Figure 4: State machine(s) (a) at position 9.