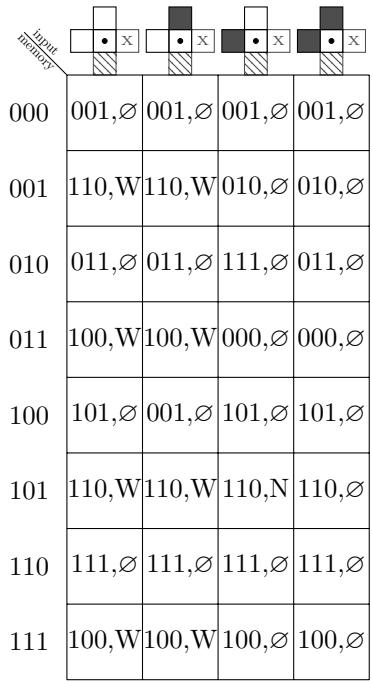


(a) Position 1



(b) Position 5

Figure 1: State machine(s) (a) at position 1, (b) at position 5.

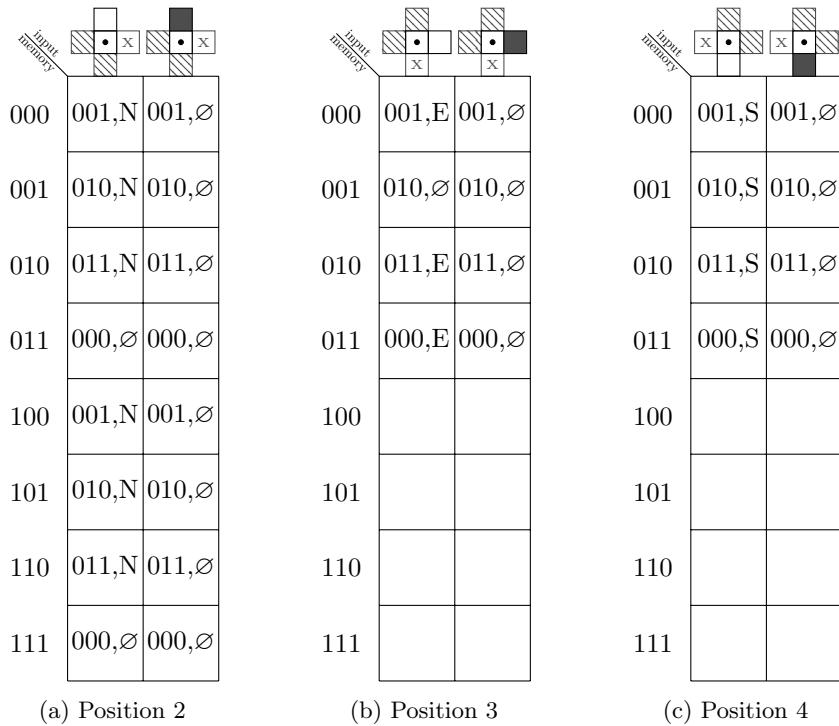


Figure 2: State machine(s) (a) at position 2, (b) at position 3, (c) at position 4.

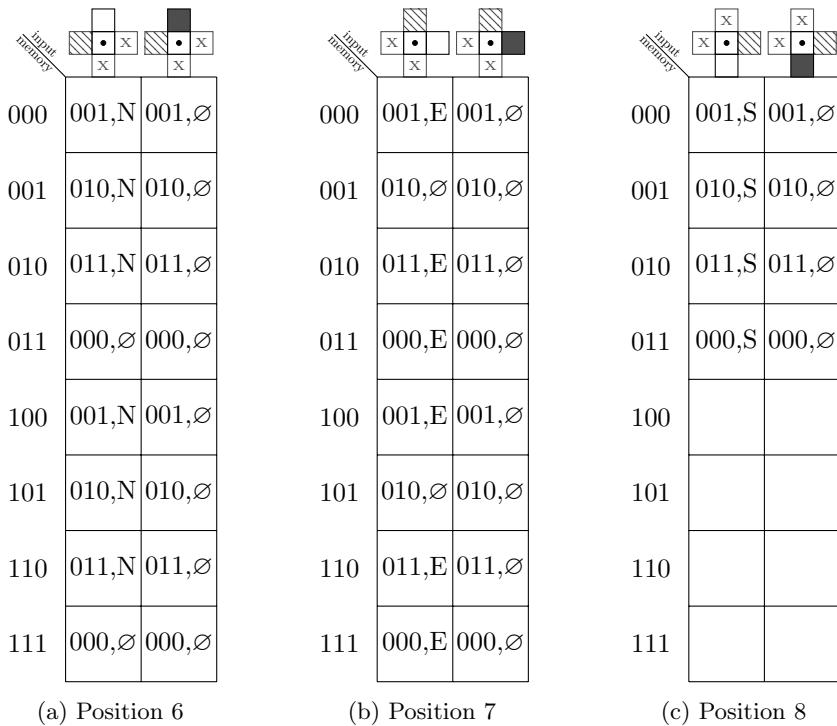


Figure 3: State machine(s) (a) at position 6, (b) at position 7, (c) at position 8.

input memory

000	001,∅ 001,∅ 001,∅ 001,∅ 001,∅ 001,∅ 001,∅ 001,∅ 001,∅
001	010,∅ 010,∅ 010,∅ 010,∅ 010,∅ 010,∅ 010,∅ 010,∅ 010,∅
010	011,∅ 011,S 111,∅ 111,∅ 011,∅ 011,S 011,∅ 011,∅ 011,∅
011	100,W 000,∅ 100,W 000,∅ 100,W 000,∅ 100,W 000,∅
100	101,∅ 101,∅ 101,∅ 101,∅ 101,∅ 101,∅ 101,∅ 101,∅ 101,∅
101	110,∅ 110,N 110,∅ 110,N 010,∅ 010,∅ 110,∅ 110,∅ 110,∅
110	111,∅ 111,∅ 111,∅ 111,∅ 111,∅ 111,∅ 111,∅ 111,∅ 111,∅
111	100,W 100,∅ 100,W 100,∅ 100,W 100,∅ 100,W 100,∅ 100,∅

(a) Position 9

Figure 4: State machine(s) (a) at position 9.