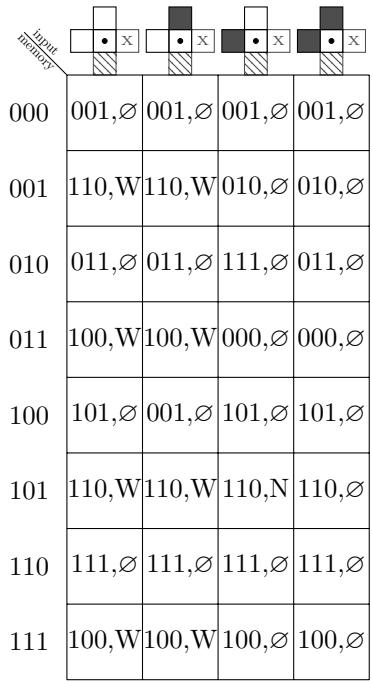


(a) Position 1



(b) Position 5

Figure 1: State machine(s) (a) at position 1, (b) at position 5.

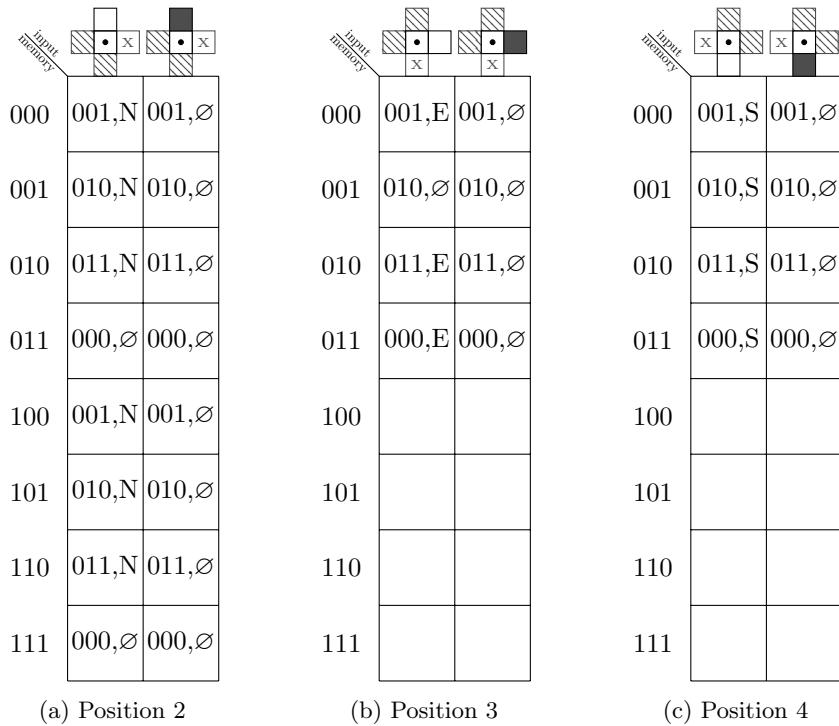


Figure 2: State machine(s) (a) at position 2, (b) at position 3, (c) at position 4.

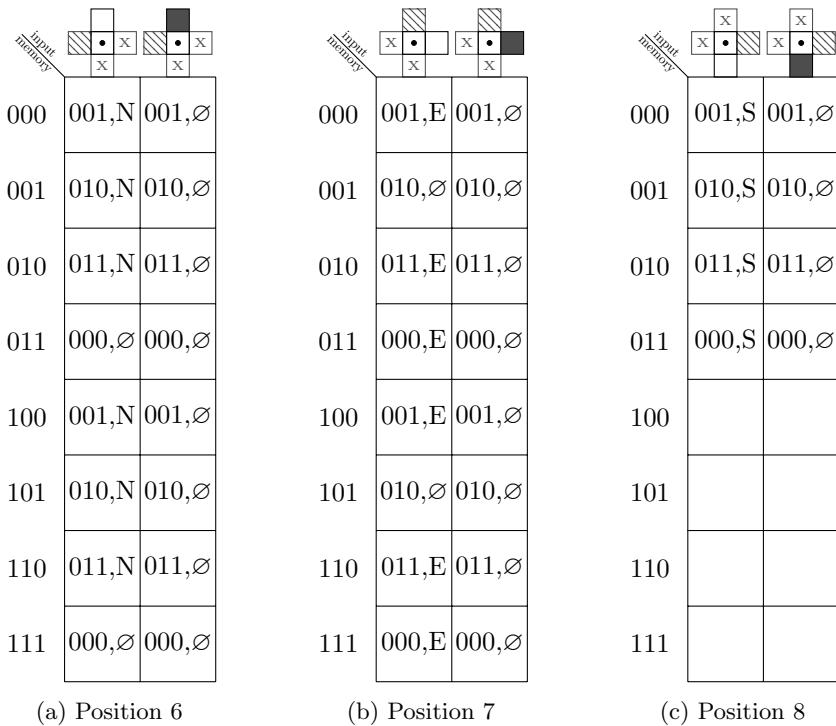


Figure 3: State machine(s) (a) at position 6, (b) at position 7, (c) at position 8.

	input memory							
	• X	• X	• X	• X	• X	• X	• X	• X
000	001, \emptyset							
001	010, \emptyset							
010	011, \emptyset	011, S	111, \emptyset	111, \emptyset	011, \emptyset	011, S	011, \emptyset	011, \emptyset
011	100, W	000, \emptyset						
100	101, \emptyset							
101	110, \emptyset	110, N	110, \emptyset	110, N	010, \emptyset	010, \emptyset	110, \emptyset	110, \emptyset
110	111, \emptyset							
111	100, W	100, \emptyset						

(a) Position 9

Figure 4: State machine(s) (a) at position 9.