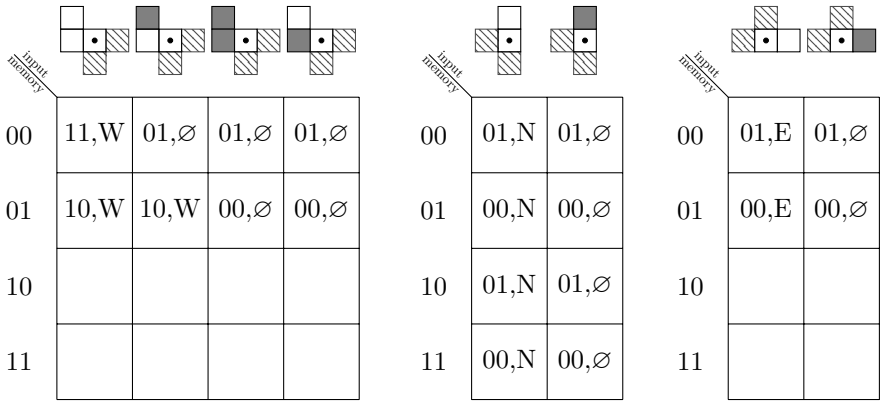
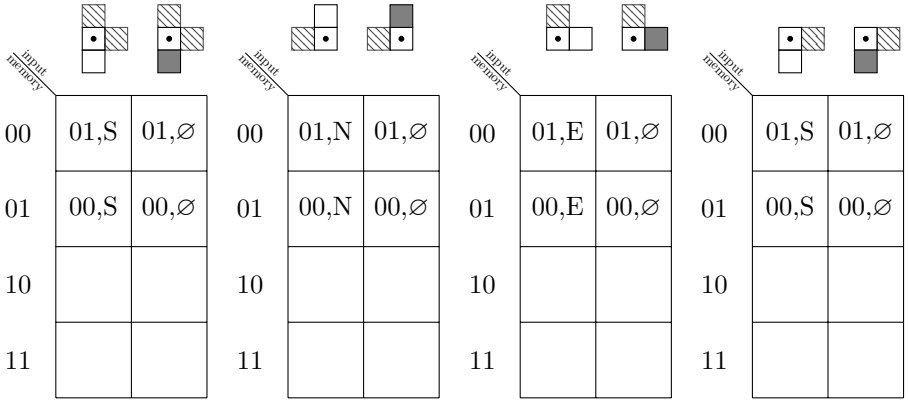


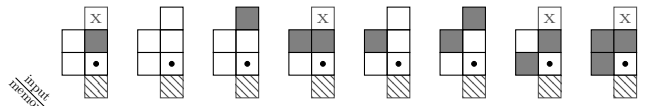
(a) Position 1 (b) Position 2 (c) Position 3

Figure 1: State machine(s) (a) at position 1, (b) at position 2, (c) at position 3.

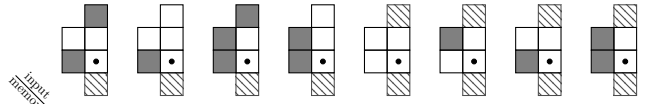


(a) Position 4 (b) Position 6 (c) Position 7 (d) Position 8

Figure 2: State machine(s) (a) at position 4, (b) at position 6, (c) at position 7, (d) at position 8.



input \ memory	00	01	10	11
00	11,W	11,W	11,W	01,∅
01	10,W	10,W	10,W	10,W
10	11,W	11,N	11,∅	01,∅
11	10,W	10,N	10,N	00,∅



input \ memory	00	01	10	11
00	01,∅	01,∅	11,∅	11,∅
01	00,∅	00,∅	00,∅	10,∅
10	11,∅	11,N	11,∅	11,N
11	10,N	10,N	10,N	10,N

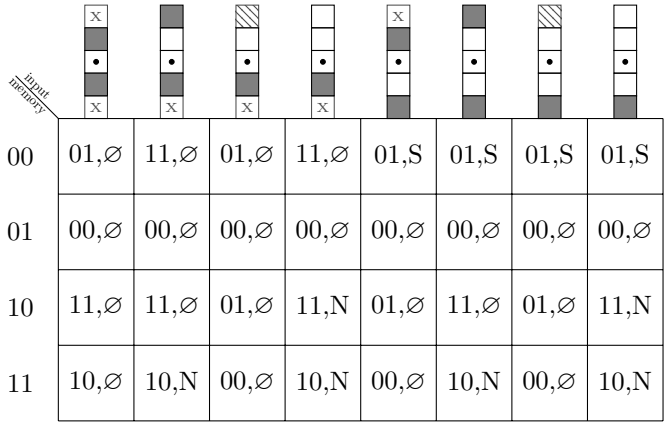
input \ memory	00	01	10	11
00	11,W	11,W	01,∅	01,∅
01	10,W	10,W	10,W	10,W
10	11,W	11,N	11,N	11,∅
11	10,W	10,N	10,N	10,∅

input \ memory	00	01	10	11
00	01,∅	01,∅	11,W	11,W
01	00,∅	00,∅	10,W	10,W
10	11,∅	11,N	11,W	11,W
11	10,N	10,N	10,W	10,W

input \ memory	00	01	10	11
00	01,∅	01,∅	01,∅	11,∅
01	00,∅	00,∅	10,W	10,W
10	11,∅	11,N	01,∅	01,∅
11	10,N	10,N	10,W	10,W

(a) Position 5

Figure 3: State machine(s) (a) at position 5.



(a) Position 9

Figure 4: State machine(s) (a) at position 9.