EE4012 VLSI System Design—Homework 2

1. Fig. 1(a) shows the symbol of a 32K×8-bit SRAM. IOs of the SRAM inclue A[14:0] (Adress), WE (Write Enable), CE (Chip Enabe), D[7:0] (Data Input), and Q[7:0] (Data Output). Design a 256K×8-bit SRAM with multiple 32K×8-bit blocks using Verilog. The symbol of the 256K×8-bit SRAM is as shown in Fig. 1(b). (10 points)

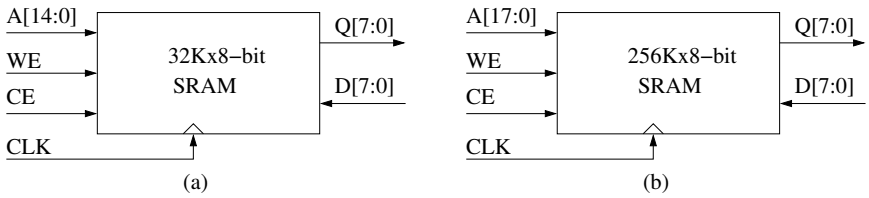

Figure 1: (a) Symbol of a 32K×8-bit SRAM. (b) Symbol of a 256K×8-bit SRAM