Single-Port Synchronous SRAM
16384 Words X 8 Bits, Mux 32 Instance
TSMC CLN90G 90nm Process

Overview

The single-port synchronous SRAM is optimized for speed and density. The memory is designed to take full advantage of TSMC's 90nm CLN90G CMOS process.

The storage array is composed of six-transistor bit cells with fully static circuitry. The SRAM operates at a voltage of 0.9V to 1.1V and a junction temperature range of -40°C to 125°C.

Instance Settings

Parameter	Setting
Instance Name	SRAM
Process	CLN90G
Words	16384
Bits	8
Mux	32
Write Mask	off
Extra Margin Adjustment	on
Redundancy	off
Soft Error Repair	none
BIST Muxes	off
Output Drive	6
Power Routing Type	rings
Ring Width	2µm
Horizontal Ring Layer	MET3
Vertical Ring Layer	MET4
Top Metal	MET5-9
Frequency	100.0 MHz

Description

The single-port synchronous RAM is a fully static memory with write enable (WEN), chip enable (CEN), address (A), data in (D) and data out (Q) pins. The RAM is self-timed and consumes the minimum amount of power for read or write operations.

All synchronous inputs are latched on the rising-edge of the clock signal. When CEN is low and WEN is high the memory will read. When CEN and WEN are both low the word on the D will be written to the memory and it will appear at the outputs (write-through).

When CEN is high the memory is deselected and forced into a low-power standby mode. Stored data is fully retained but memory access is disabled for data read or data write, the existing data outputs continue to drive their previous values.

The Extra Margin Adjustment allows you to adjust the width of the self timing pulse.

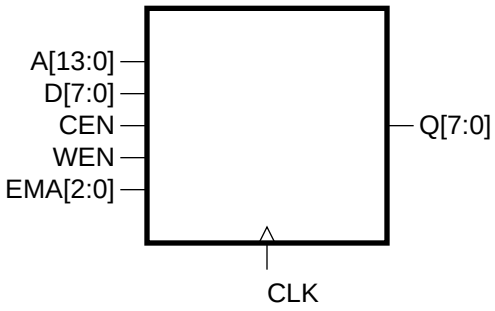
Refer to the users manual for a more detailed description of memory operation.

Physical Dimensions (units = µm)

Parameter	Size
Core Width	440.3
Core Height	420.3
Footprint Width	458.1
Footprint Height	438.1

The footprint area includes the core area and user defined power routing and pin spacing.

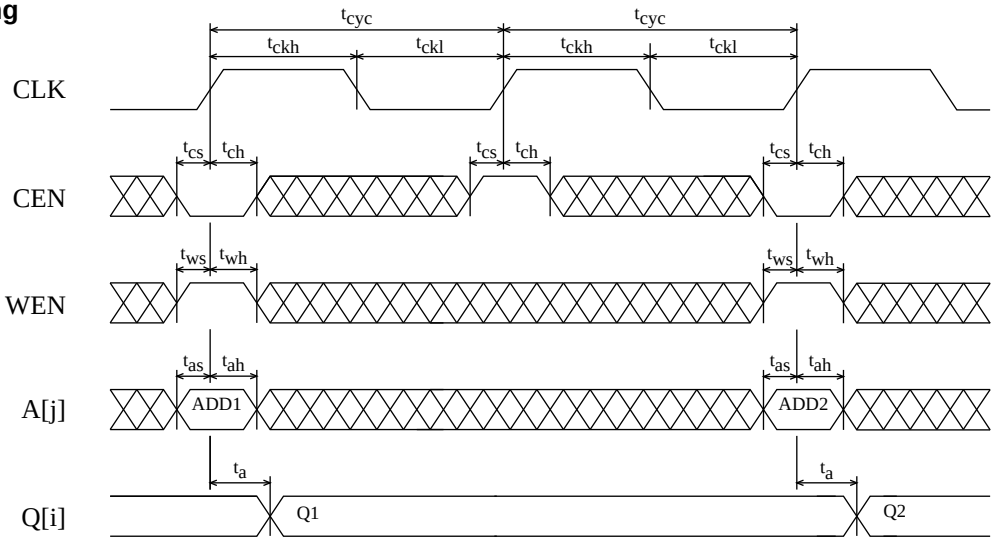
Symbol



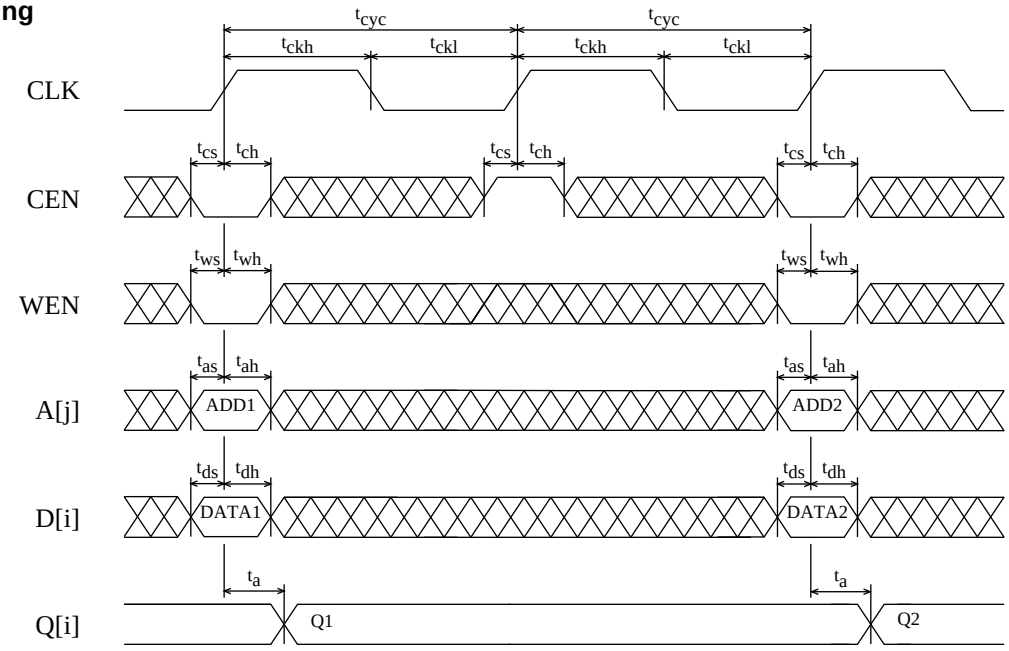
Pin Description

Pin	Description
A[13:0]	Addresses (A[0] = LSB)
D[7:0]	Data Inputs (D[0] = LSB)
CLK	Clock
CEN	Chip Enable (active low)
WEN	Write Enable (active low)
Q[7:0]	Data Outputs (Q[0] = LSB)
EMA[2:0]	Extra Margin Adjustment (EMA[0] = LSB)

Read Cycle Timing



Write Cycle Timing



Timing (units = ns)

The timing tables show values measured from the output threshold to the input threshold. The input pins are driven by standard slews. The slews and thresholds vary depending upon the process corner.

Pin	Symbol	Fast Process 1.1V, -40°C		Fast Process 1.1V, 0°C		Typical Process 1.0V, 25°C		Slow Process 0.9V, 125°C	
		Min	Max	Min	Max	Min	Max	Min	Max
Cycle time	t_{cyc0}	0.595		0.636		0.902		1.493	
Access time[1,2]	t_{a0}	0.562		0.590			0.958		1.612
Address setup	t_{as}	0.233		0.245		0.347		0.597	
Address hold	t_{ah}	0.001		0.001		0.011		0.014	
Data setup	t_{ds}	0.078		0.078		0.124		0.208	
Data hold	t_{dh}	0.021		0.024		0.027		0.023	
Chip enable setup	t_{cs}	0.243		0.256		0.365		0.611	
Chip enable hold	t_{ch}	0.000		0.000		0.000		0.000	
Write enable setup	t_{ws}	0.250		0.268		0.351		0.549	
Write enable hold	t_{wh}	0.000		0.000		0.000		0.000	
Clock high	t_{ckh}	0.062		0.065		0.094		0.144	
Clock low	t_{ckl}	0.246		0.259		0.394		0.675	
Clock rise slew	t_{ckr}		1.000		1.000		1.000		1.000
Output load factor[3]	K_{load}		0.473		0.510		0.868		1.207

[1] Output delays and a load dependency (Kload) which is used to calculate: *TotalDelay = FixedDelay + (Kload x Cload).*

[2] Access time is defined as the longest possible delay to valid output for the typical and slow corners, and the shortest possible delay for the fast corners.

[3] The output load factor units are ns/pF.

Cycle and Access Timing for Different Values of Extra Margin Adjustment (units = ns)

Pin	Symbol	Fast Process 1.1V, -40°C		Fast Process 1.1V, 0°C		Typical Process 1.0V, 25°C		Slow Process 0.9V, 125°C	
		Min	Max	Min	Max	Min	Max	Min	Max
Cycle time EMA=0	t_{cyc0}	0.595		0.636		0.902		1.493	
Cycle time EMA=1	t_{cyc1}	0.695		0.744		1.062		1.773	
Cycle time EMA=2	t_{cyc2}	0.804		0.859		1.236		2.079	
Cycle time EMA=3	t_{cyc3}	0.875		0.935		1.353		2.277	
Cycle time EMA=4	t_{cyc4}	**		**		**		**	
Cycle time EMA=5	t_{cyc5}	**		**		**		**	
Cycle time EMA=6	t_{cyc6}	**		**		**		**	
Cycle time EMA=7	t_{cyc7}	**		**		**		**	
Access time EMA=0	t_{a0}	0.562		0.590			0.958		1.612
Access time EMA=1	t_{a1}	0.662		0.698			1.119		1.892
Access time EMA=2	t_{a2}	0.771		0.814			1.293		2.198
Access time EMA=3	t_{a3}	0.842		0.889			1.409		2.396
Access time EMA=4	t_{a4}	**		**			**		**
Access time EMA=5	t_{a5}	**		**			**		**
Access time EMA=6	t_{a6}	**		**			**		**
Access time EMA=7	t_{a7}	**		**			**		**
EMA setup	t_{emas}	0.595		0.636		0.902		1.493	
EMA hold	t_{emah}	0.595		0.636		0.902		1.493	

**Illegal setting of EMA for this corner.

Pin Capacitance (units = fF)

Pin	Fast Process 1.1V, -40°C	Fast Process 1.1V, 0°C	Typical Process 1.0V, 25°C	Slow Process 0.9V, 125°C
A	32.830	32.700	31.950	30.920
D	15.100	14.990	14.990	14.770
CLK	72.640	72.780	70.610	68.470
CEN	17.680	17.560	17.570	17.320
WEN	21.860	21.730	21.580	21.160
EMA	23.410	23.280	23.150	22.700

Power (current units = mA)

Pin	Fast Process 1.1V, -40°C	Fast Process 1.1V, 0°C	Typical Process 1.0V, 25°C	Slow Process 0.9V, 125°C
AC Current (EMA=0)[1,4]	2.79	2.89	2.43	2.17
AC Current (EMA=1)[1,4]	2.86	2.96	2.48	2.20
AC Current (EMA=2)[1,4]	2.92	3.04	2.52	2.23
AC Current (EMA=3)[1,4]	2.96	3.08	2.55	2.26
AC Current (EMA=4)[1,4]	3.05	3.20	2.63	2.31
AC Current (EMA=5)[1,4]	3.08	3.22	2.64	2.32
AC Current (EMA=6)[1,4]	3.14	3.27	2.67	2.35
AC Current (EMA=7)[1,4]	3.17	3.31	2.71	2.37
Read AC Current (EMA=0)[4]	2.78	2.89	2.42	2.17
Read AC Current (EMA=1)[4]	2.85	2.96	2.48	2.20
Read AC Current (EMA=2)[4]	2.92	3.03	2.52	2.23
Read AC Current (EMA=3)[4]	2.96	3.08	2.54	2.26
Read AC Current (EMA=4)[4]	3.05	3.19	2.62	2.31
Read AC Current (EMA=5)[4]	3.08	3.22	2.63	2.31
Read AC Current (EMA=6)[4]	3.13	3.26	2.67	2.34
Read AC Current (EMA=7)[4]	3.17	3.31	2.71	2.36
Write AC Current (EMA=0)[4]	2.79	2.89	2.43	2.17
Write AC Current (EMA=1)[4]	2.86	2.96	2.48	2.21
Write AC Current (EMA=2)[4]	2.93	3.04	2.52	2.24
Write AC Current (EMA=3)[4]	2.96	3.09	2.55	2.26
Write AC Current (EMA=4)[4]	3.06	3.20	2.63	2.31
Write AC Current (EMA=5)[4]	3.09	3.22	2.64	2.32
Write AC Current (EMA=6)[4]	3.14	3.27	2.68	2.35
Write AC Current (EMA=7)[4]	3.18	3.31	2.71	2.37
Peak Current	35.54	34.04	22.92	14.03
Deselected Current[2,4]	6.45E-1	6.70E-1	5.73E-1	5.15E-1
Standby Current[3]	5.85E-1	1.41	2.60E-1	5.78E-1

** Illegal setting of EMA for this corner.

1 The AC current value assumes 50% read and write operations, where all addresses and 50% of input and output pins switch at the user defined frequency of 100.0MHz. It is assumed that EMA pins do not switch.

2 The deselected current assumes the memory is deselected, all addresses switch, and 50% of input pins switch at the user defined frequency of 100.0MHz. The logic switching component of deselected power becomes negligibly small if the input pins are held stable by externally controlling these signals with chip select. It is assumed that EMA pins do not switch.

3 The standby current value is independent of frequency and assumes all inputs and outputs are stable.

4 The standby current component is not included in this value.

Clock Noise Limit

Symbol	Fast Process 1.1V, -40°C		Fast Process 1.1V, 0°C		Typical Process 1.0V, 25°C		Slow Process 0.9V, 125°C	
	Pulse Width	Voltage	Pulse Width	Voltage	Pulse Width	Voltage	Pulse Width	Voltage
CLK	10.0ns	0.3V	10.0ns	0.3V	10.0ns	0.3V	10.0ns	0.3V

The clock noise limit is the maximum voltage allowed (for the indicated pulse width) that does not cause an unintentional memory cycle or other memory failure.

Supply Noise Limit (units = V)

Pin	Fast Process 1.1V, -40°C	Fast Process 1.1V, 0°C	Typical Process 1.0V, 25°C	Slow Process 0.9V, 125°C
Power	0.11	0.11	0.10	0.09
Ground	0.11	0.11	0.10	0.09

The power and ground noise limit is the maximum supply voltage transition that is allowed without causing a memory failure.