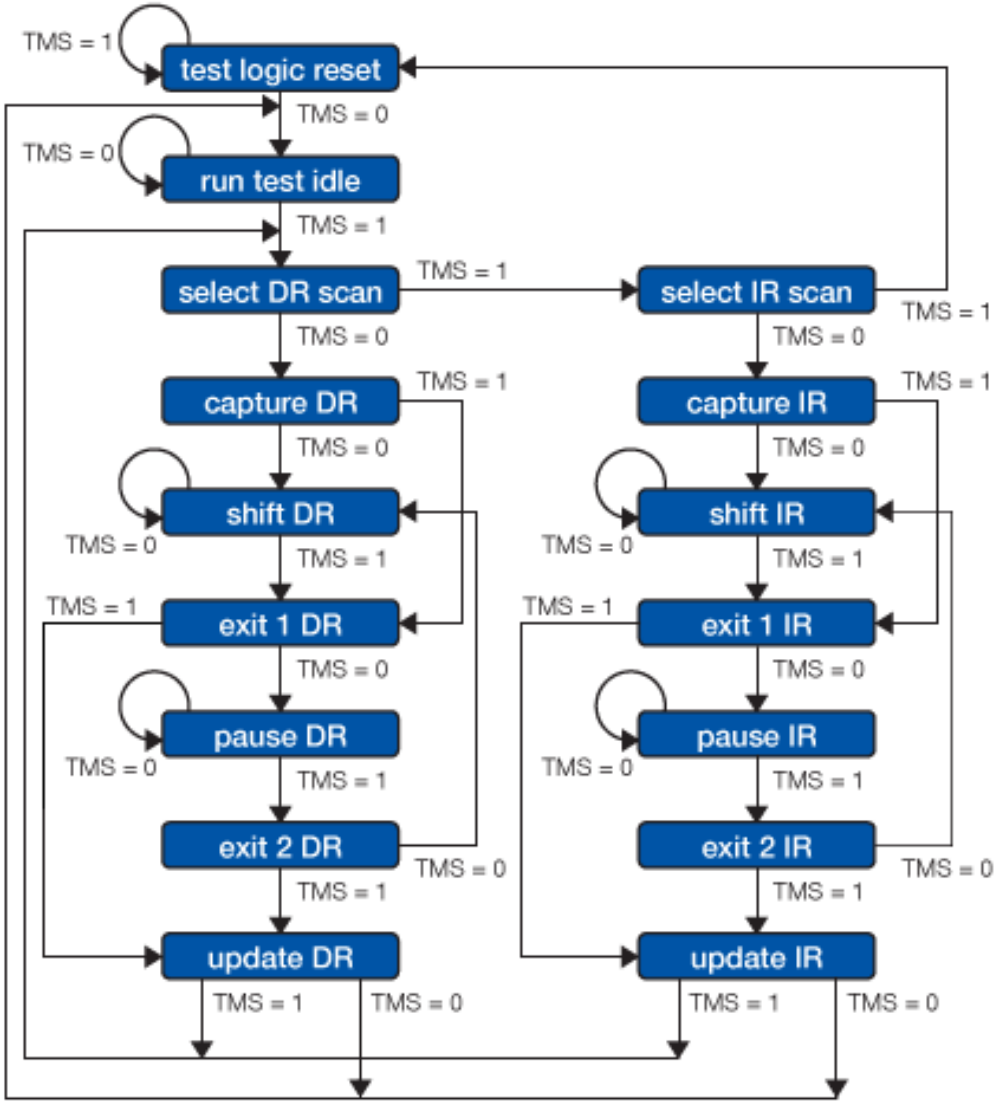
JTAG Study

Tony Xia


test logic reset
run test idle
select DR scan
capture DR
shift DR
exit 1 DR
pause DR
exit 2 DR
update DR
select IR scan
capture IR
shift IR
exit 1 IR
pause IR
exit 2 IR
update IR
TMS = 1
TMS = 0

State

RESET ... stable (with TMS high); acts as if TRST were pulsed
RUN/IDLE ... stable; don’t assume this always means IDLE
DRSELECT
DRCAPTURE
DRSHIFT ... stable; TDI/TDO shifting through the data register
DREXIT1
DRPAUSE ... stable; data register ready for update or more shifting
DREXIT2
DRUPDATE
IRSELECT
IRCAPTURE
IRSHIFT ... stable; TDI/TDO shifting through the instruction register
IREXIT1
IRPAUSE ... stable; instruction register ready for update or more shifting
IREXIT2
IRUPDATE

State

Note that only **six** of those states are fully “stable” in the face of TMS fixed (low except for RESET) and a free-running JTAG clock. For all the others, the next TCK transition changes to a new state.

From DRSHIFT and IRSHIFT, clock transitions will produce side effects by changing register contents. The values to be latched in upcoming DRUPDATE or IRUPDATE states may not be as expected.

RUN/IDLE, DRPAUSE, and IRPAUSE are reasonable choices after drscan or irscan commands, since they are free of JTAG side effects.

RUN/IDLE may have side effects that appear at non-JTAG levels, such as advancing the ARM9E-S instruction pipeline. Consult the documentation for the TAP(s) you are working with. instruction register ready for update or more shifting

State

* Test-Logic-Reset

All test logic is disabled in this controller state enabling the normal operation of the IC. The TAP controller state machine is designed so that, no matter what the initial state of the controller is, the Test-Logic-Reset state can be entered by holding TMS at high and pulsing TCK five times. This is why the Test Reset (TRST) pin is optional.

* Run-Test-Idle

In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it is executed when the controller enters this state. The test logic in the IC is idle otherwise.

* Select-DR-Scan

This controller state controls whether to enter the Data Path or the Select-IR-Scan state.

State

* Select-IR-Scan
This controller state controls whether or not to enter the Instruction Path. The Controller can return to the Test-Logic-Reset state otherwise.

* Capture-IR
In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits must always be "01".

* Shift-IR
In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register.

* Exit1-IR
This controller state controls whether to enter the Pause-IR state or Update-IR state.

State

* Pause-IR

This state allows the shifting of the instruction register to be temporarily halted.

* Exit2-IR

This controller state controls whether to enter either the Shift-IR state or Update-IR state.

* Update-IR

In this controller state, the instruction in the instruction register is latched to the latch bank of the Instruction Register on every falling edge of TCK. This instruction becomes the current instruction once it is latched.

* Capture-DR

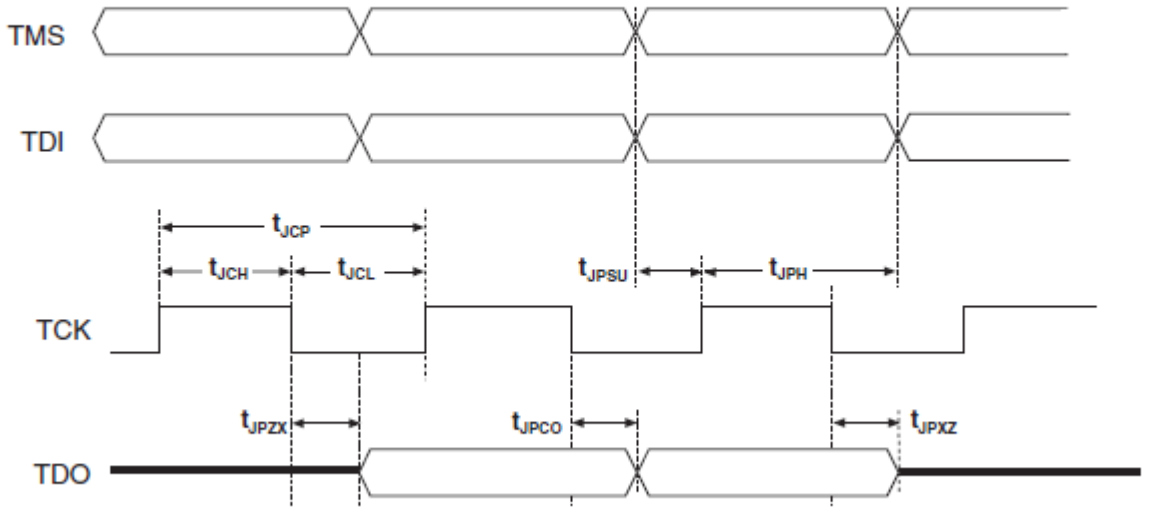
In this controller state, the data is parallel-loaded into the data registers selected by the current instruction on the rising edge of TCK.

* Shift-Dr, Exit1-DR, Pause-DR, Exit2-DR and Update-DR

These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR and Update-IR states in the Instruction path.

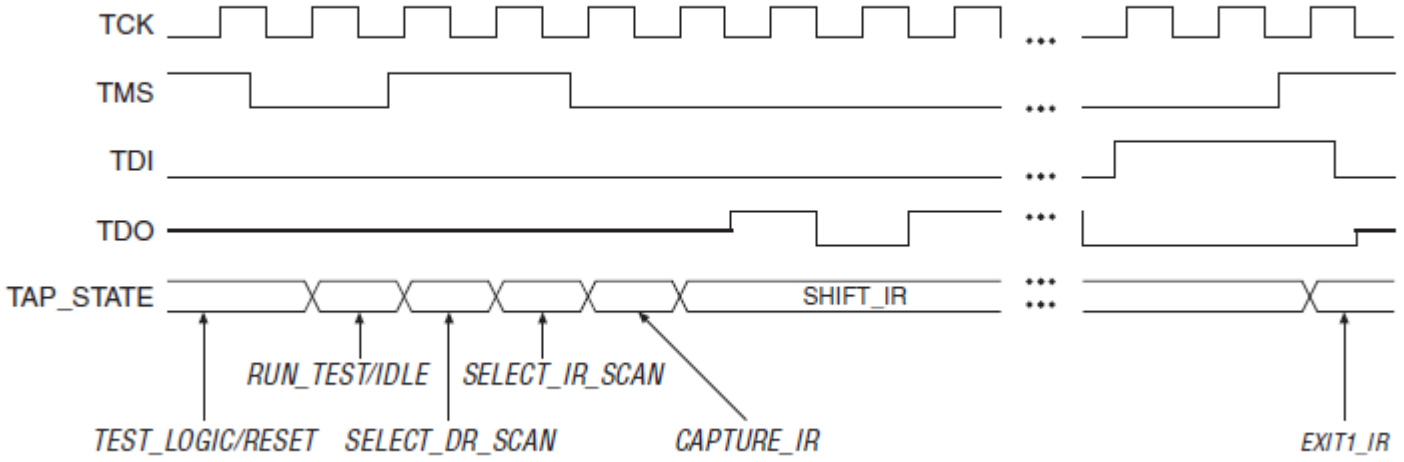
Timing Waveforms

Figure 13–6. IEEE Std. 1149.1 Timing Waveforms



Selecting the instruction Mode

Figure 13–7. Selecting the Instruction Mode

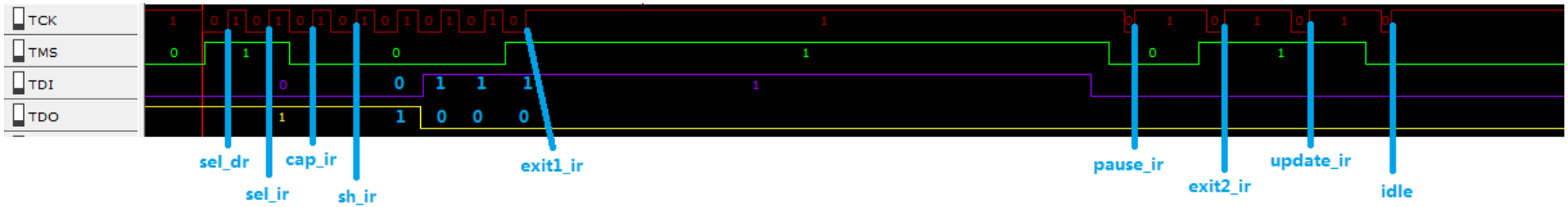


The TDO pin is tri-stated in all states except in the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

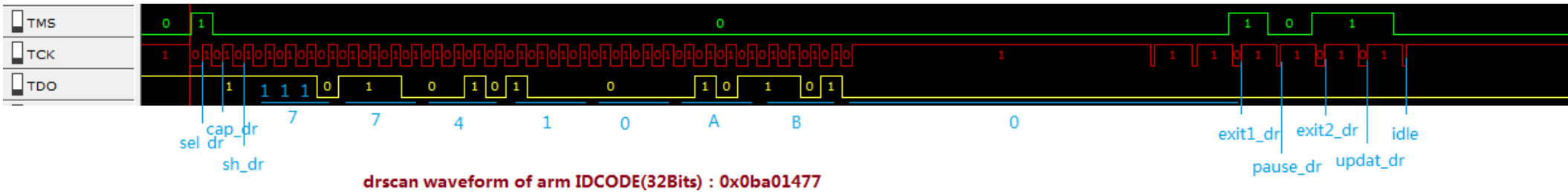
When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the instruction code is clocked at the same time that the next state, EXIT1_IR, is activated. Set TMS high to activate the EXIT1_IR state. After the EXIT1_IR state is activated, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to serially shift test data in one of three modes.

Lesson Learn

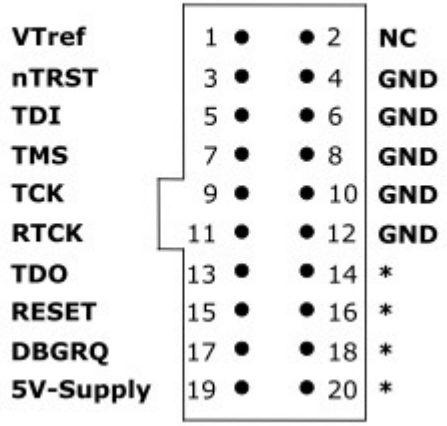


irscan waveform of arm instr of IDCODE(4bits): 'b1110

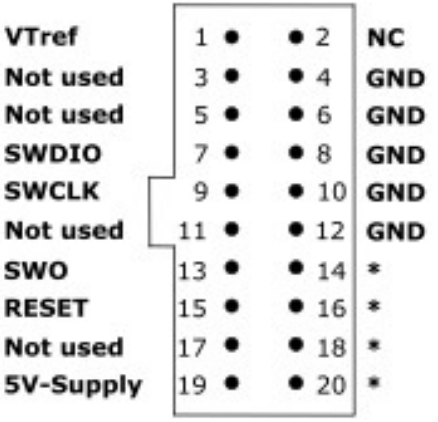


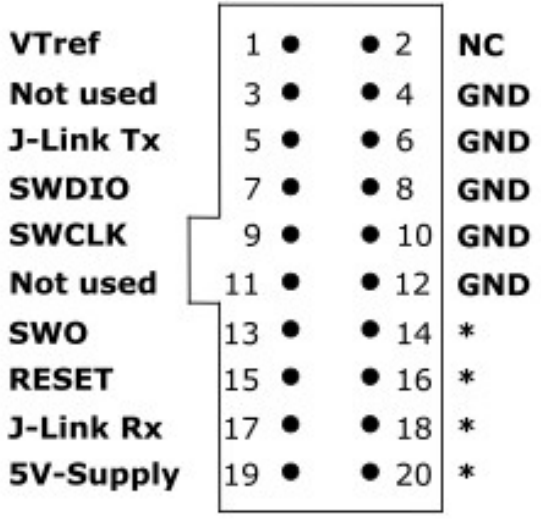
drscan waveform of arm IDCODE(32Bits) : 0x0ba01477

18.1.1 Pinout for JTAG



18.1.2 Pinout for SWD





18.1.4 Pinout for SPI