Basics of Bus Switches

Outline:

This document describes the series and operation of the bus switches and the associated functions (level shift and tolerance).
It also describes the lineup of the Toshiba's bus switch series and its applications, examples of signal switching, on/off level shift, and calculation methods for rise and fall time.

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1. Overview of bus switches

This section briefly describes bus switches, including where they are used and what types of bus switches are available.

1.1. Where bus switches are used

There are various types of switches for electronic circuit applications. Load switches are used along power supply lines whereas analog switches and bus switches are used along signal lines. Analog switches are specifically optimized for the switching of analog signals whereas bus switches are designed for digital signals. As the speed of digital signals increases, each semiconductor device manufacturer is expanding its lineup of high-speed bus switches.

Figure 1.1 shows an application of a bus switch. There are signal lines that interconnect between the CPU and the following IC. A bus switch is used along these signal lines.

Since bus switches are not designed to pass large current, they cannot be used along power supply lines. For power supply lines, use load switches (MOSFETs or load switch ICs) that match your application requirements.

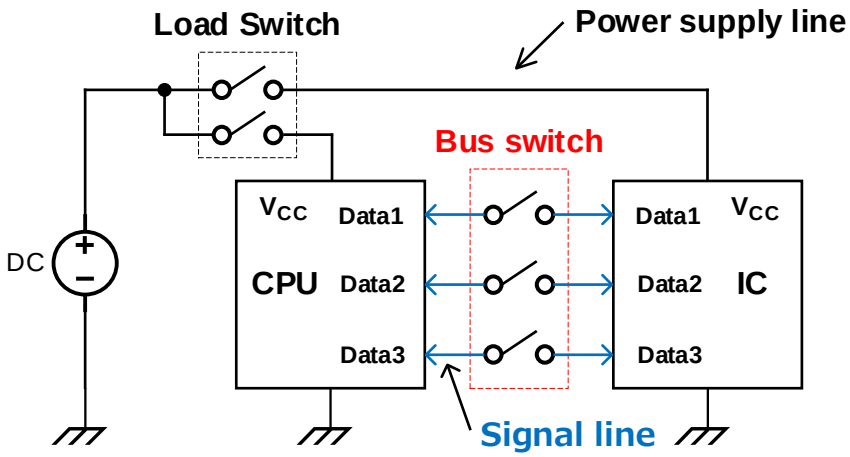


Figure 1.1 Application of a bus switch

1.2. What is a bus switch?

As described above, bus switches are used along signal lines. They are optimized for the switching of digital signals. A bus switch is composed of MOSFETs that make and break electrical connections just like a mechanical switch (Figure 1.2). A bus switch can be used for both unidirectional and bidirectional signals.
Whereas mechanical switches simply pass a signal from input to output, some bus switches provide level shifting, i.e., a function to step up or down the input voltage to obtain a desired output voltage.

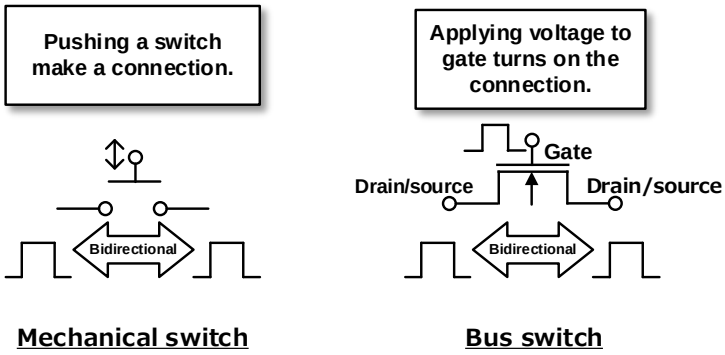


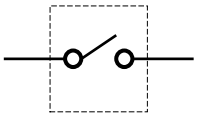
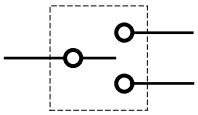
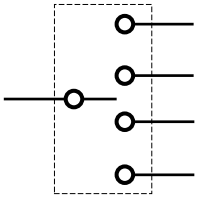
Figure 1.2 Mechanical switch vs. bus switch

As is the case with mechanical switches, several types of bus switches are available, including simple signal on-off switches and changeover switches, as shown in Figure 1.3.

Figure 1.3 Signal on-off and changeover switches

There are terms for these types of bus switches as shown in Figure 1.3.
Since abbreviations are generally used to indicate the types of bus switches, you should remember these abbreviations, what they stand for, and how each type of bus switch functions (Table 1.1).

Table 1.1 Contact terminology

Abbreviation	Expansion of Abbreviation	Symbol
SPST	Single-Pole Single-Throw	
SPDT	Single-Pole Double-Throw	
SP4T	Single-Pole quadruple-Throw	

1.3. Differences between bus switches and standard logic ICs in terms of how they supply current to a load

In the case of a bus switch, current travels between the drain and the source of a MOSFET. Therefore, its load is supplied with current from an input signal source.

In contrast, a standard logic IC is composed of a collection of the minimum building blocks shown in Figure 1.4. In a standard logic IC, n- and p-channel MOSFETs are connected in series. When an input signal is applied to their gate, each MOSFET turns on or off. This causes the on-state MOSFET to supply current to the load.

As an example, the following paragraphs refer to a bidirectional standard logic buffer in order to describe how the characteristics and functions of the bus switch differ from those of the standard logic IC.

Bus switches, which use a MOSFET to pass a signal from input to output, cause little signal delay, making it possible to transfer a signal bidirectionally at high speed. Buffers cause a longer signal delay than bus switches. However, since buffers have a higher drive capability, their input signal sources are not affected even when a heavy load is connected to the output.

Table 1.2 and Figure 1.5 compare a bus switch and a standard logic IC (bidirectional bus buffer).

Bus switches and bidirectional bus buffers have distinct characteristics. Choose whichever best suit your requirements.

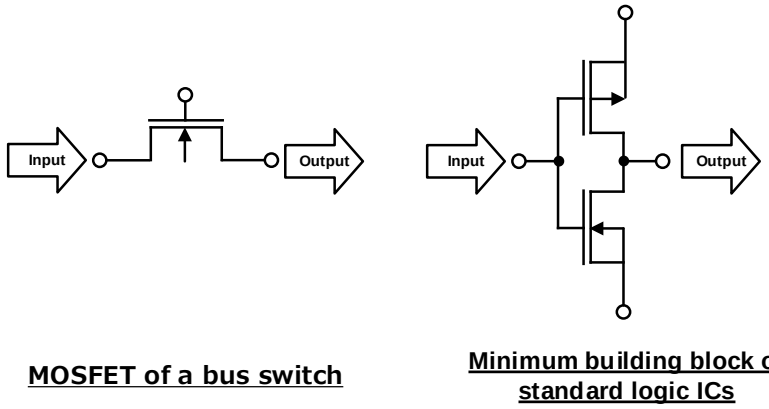


Figure 1.4 Configurations of a bus switch and a standard logic IC

Table 1.2 Comparison of a bus switch and a standard logic IC (bidirectional bus buffer)

	Bus switch (TC7MBL3245C)	Standard logic IC (TC74VHC245)
Propagation delay time	≤ 1 ns	A few nanoseconds
Signal amplification	N/A	±4mA typical (at V_{CC}=3 V)
Signal direction control via the DIR pin	Not required	Required

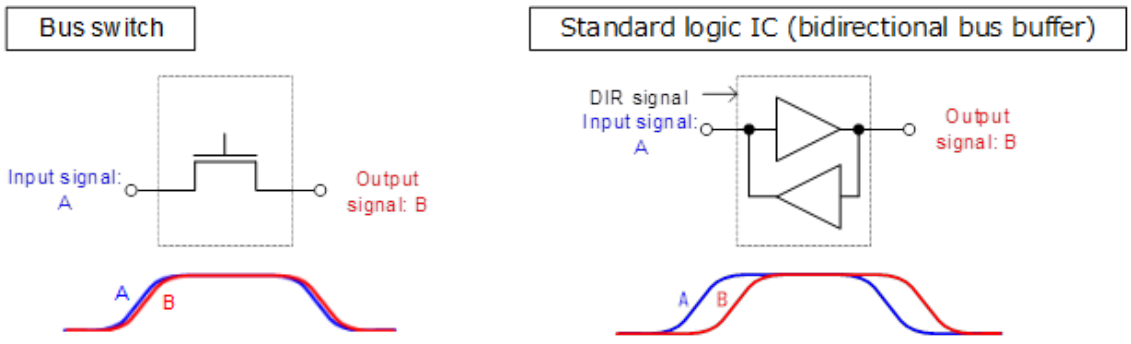


Figure 1.5 Comparison of the circuits and waveforms of a bus switch and a standard logic IC (bidirectional bus buffer)

2. Types of bus switches and their operations

There are three types of bus switches as shown in Table 2.1: n-channel MOSFET (Nch MOSFET) bus switches, bus switches that consist of parallel n- and p-channel MOSFETs, and bus switches using a charge pump. These bus switches differ in terms of the configuration of an internal switch and require a different power supply circuit.

The following subsections describe the basic operation of the MOSFET as well as the characteristics and operations of each type of bus switch.

Table 2.1 Types of bus switches

Type	Level-Shifting Function	Full-Swing Switching (Input and output voltages)	High-Speed Switching
Nch MOSFET bus switches	✓	-	-
Parallel Nch/Pch MOSFET bus switches	-	✓	-
Bus switches using a charge pump	-	✓	✓

2.1. Basic operation of the MOSFET

The “back gate” of the n-channel MOSFET used as a switch is connected to GND as shown in Figure 2.1.

When voltage is applied across the gate and the back gate, the p region in the vicinity of the insulating oxide layer is converted into an n-type channel.

The n-type channel stretches from drain to source, allowing bidirectional signal conduction.

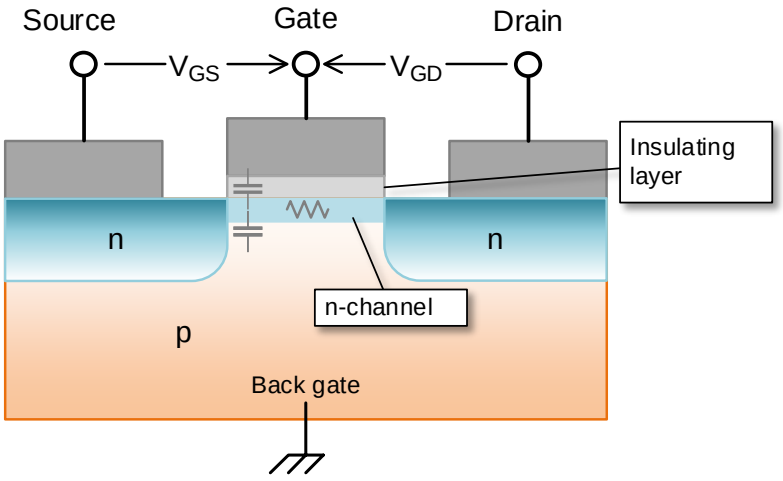


Figure 2.1 Cross-sectional view of the n-channel MOSFET

2.2. Nch MOSFET bus switches

In the case of an Nch MOSFET bus switch, supply voltage (V_{CC}) is applied to the gate of the MOSFET in the "on" state. Therefore, the input signal voltage is applied to either the drain or the source.

When the signal voltage changes, the on-resistance of the bus switch changes as follows (Figure 2.2):

- When the signal voltage is decreased:
  → The gate-drain voltage (V_{GD}) and gate-source voltage (V_{GS}) of the MOSFET increase.
  → The electric charge in the channel increases, causing its on-resistance to decrease.
- When the signal voltage is increased:
  → The gate-drain voltage (V_{GD}) and gate-source voltage (V_{GS}) of the MOSFET decrease.
  → The electric charge in the channel decreases, causing its on-resistance to increase.

When a difference between the supply voltage and the input signal voltage is lower than a given value (typically the threshold voltage, V_{th}), a channel is not formed in the MOSFET. Therefore, there is no electrical conduction between the drain and the source.

In such a state, the upper limit of the input signal voltage is equal to the supply voltage (V_{CC}) minus the given value (typically the threshold voltage, V_{th}).

However, a pull-up resistor is added to the input and/or output switch pins to pull the signal voltage to the supply voltage in each domain. For how to do this, see Section 3.1 or 5.3.

A level-shifting function is available with some of the Nch MOSFET bus switches. See Section 3 for level shifting.

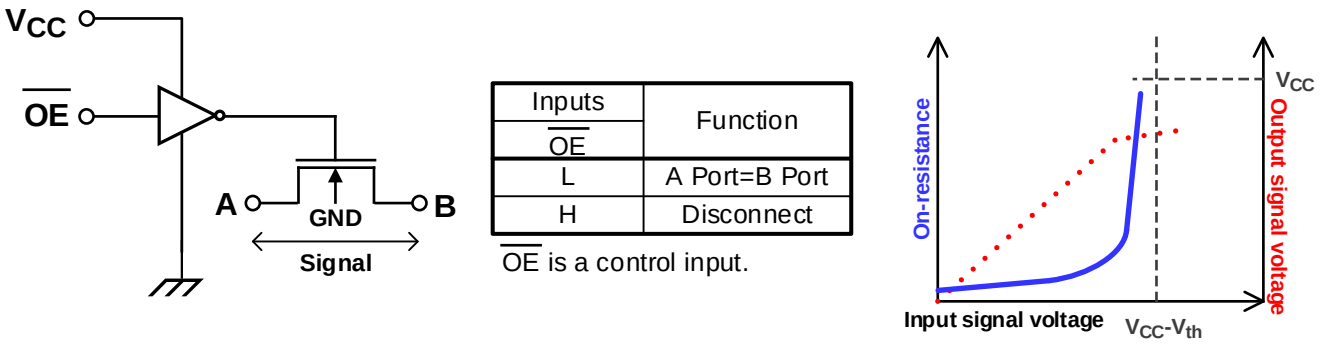


Figure 2.2 Block diagram and characteristics curve of an Nch MOSFET bus switch

2.3. Parallel Nch/Pch MOSFET bus switches

The on-resistance of an n-channel MOSFET increases considerably as the input signal voltage approaches the gate voltage. Therefore, the output signal voltage is restricted between 0 V and (gate voltage – threshold voltage).

In contrast, parallel Nch/Pch MOSFET bus switches are designed to provide an output voltage between V_{CC} and GND.

In these bus switches, an n-channel MOSFET and a p-channel MOSFET are connected in parallel as shown in Figure 2.3. In this configuration, the switch section exhibits a fairly flat on-resistance curve across the entire input voltage range from 0 V to V_{CC} because the on-resistance curves of the n- and p-channel MOSFETs are combined.

As a result, parallel Nch/Pch MOSFET bus switches provide an output with a full swing from 0 V to V_{CC}.

Parallel Nch/Pch MOSFET bus switches can also be used for analog applications since they have the same configuration as analog switches. In this case, however, they should be fully evaluated since they are optimized for digital applications.

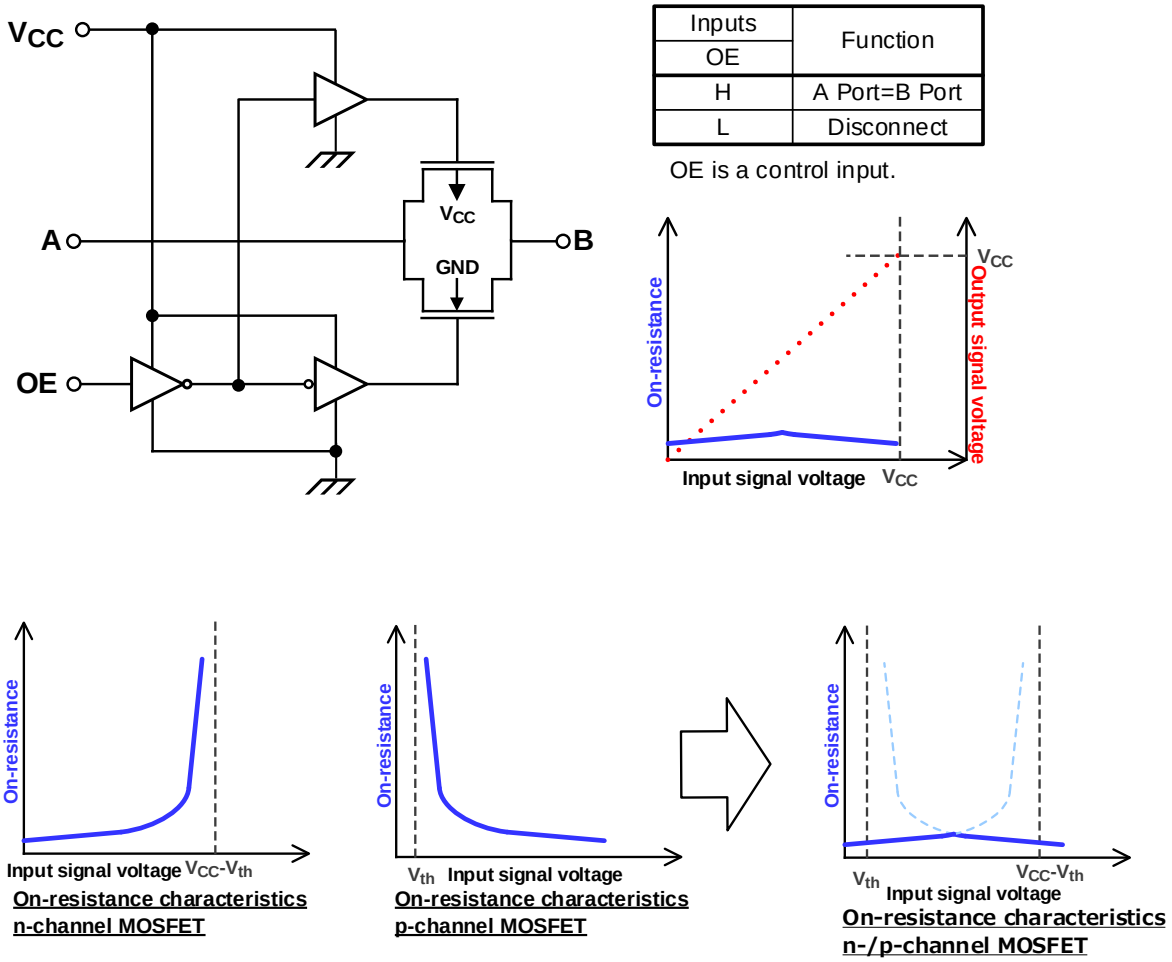


Figure 2.3 Block diagram and characteristics curve of a parallel Nch/Pch MOSFET bus switch

2.4. Bus switches using a charge pump

A bus switch using a charge pump employs an n-channel MOSFET. As is the case with parallel Nch/Pch MOSFET bus switches, bus switches using a charge pump provide an output with a full swing from 0 V to V_{CC}.
This type of bus switch uses a charge pump* to raise the supply voltage to maintain the gate voltage of the n-channel MOSFET and thereby keep its on-resistance low over the entire input voltage range. As a result, the bus switch exhibits an almost flat on-resistance-vs-input voltage curve.
This makes it possible for the input and output voltages to swing from 0 V to V_{CC}.
In addition, since a bus switch using a charge pump contains only one MOSFET, the parasitic capacitance of the switch section is lower than that of the parallel Nch/Pch MOSFET bus switch.
For the above reasons, bus switches using a charge pump are suitable for the conduction of a high-speed signal. However, a drawback is that bus switches using a charge pump consume more power than the other types of bus switches because of the charge pump.

* A charge pump is a circuit composed of multiple capacitors and switching devices to raise voltage.

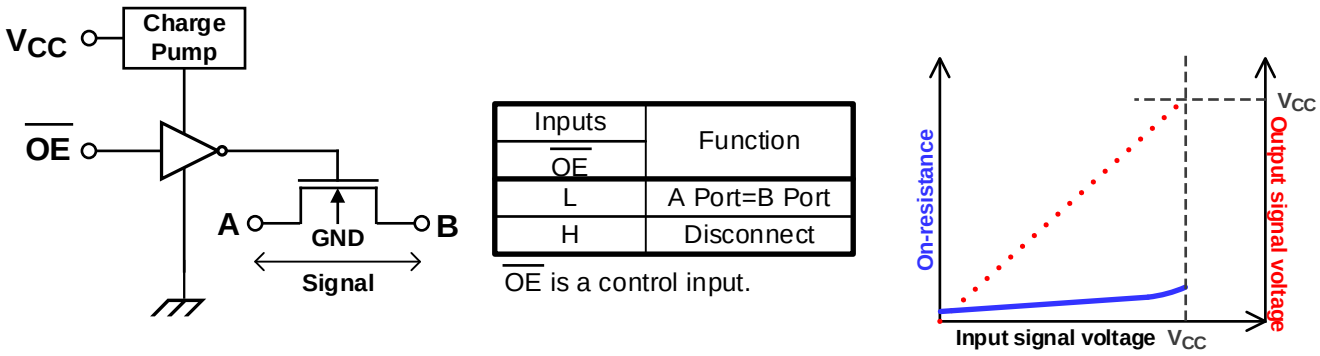


Figure 2.4 Block diagram and characteristics curve of a bus switch using a charge pump

3. Additional functions available with bus switches

As described in Section 1, a bus switch is used to pass or block a digital signal.
Some bus switches are available with level-shifting and tolerant functions. (Level-shifting bus switches can pass a signal between two different voltage domains.)

3.1. Level-shifting function

An ability to pass a signal across two different voltage domains is available with bus switches using an n-channel MOSFET. A pull-up resistor is added to the input and/or output switch pins to pull the signal voltage to the supply voltage in each domain. When a bus switch is used to pass a signal bidirectionally, the switch pins can be either an input or an output. In this case, pull-up resistors must be added to both the switch pins, as shown in Figure 3.1. In contrast, when a bus switch is used to pass a signal unidirectionally, it is unnecessary to add a pull-up resistor to the input switch pin.

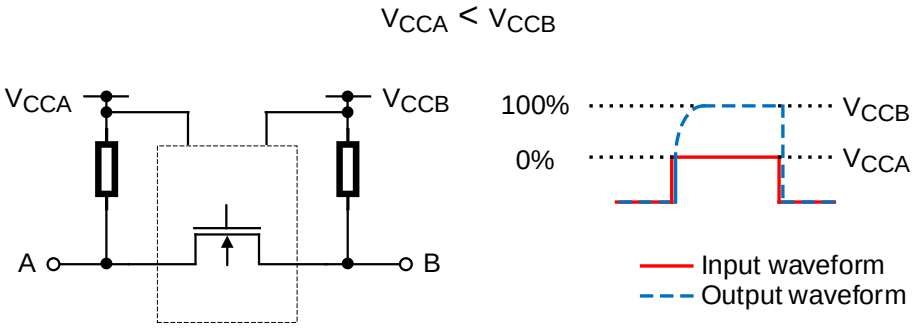


Figure 3.1 Equivalent circuit of a dual-supply bus switch and its input and output waveforms

This bus switch allows on/off control via a control input (referenced to V_{CCA}).
In cases where a bus switch is controlled to be turned on via the control input, it turns off when the input voltage exceeds the reference voltage, which is determined by V_{CCA}. Suppose that the reference voltage is V_{CCA} and that a bus switch passes a signal from pin A to pin B. Then, the bus switch turns off when the input voltage rises to V_{CCA}, and the output signal is pulled up to V_{CCB} by a pull-up resistor on the V_{CCB} side. Likewise, suppose that the bus switch passes a signal from pin B to pin A. Then, the bus switch turns off when the input voltage rises to V_{CCA}, and the output voltage is maintained by the pull-up resistor on the V_{CCA} side.
Since a dual-supply bus switch uses pull-up resistors for level shifting, its output rise time is longer than the output fall time. The maximum operating frequency of a bus switch can be calculated based on its rise waveform. Since voltage is determined by the charging and discharging of a capacitor through a resistor, let's use a time constant (that represents a time required for a signal to rise to 63% of the supply voltage) to calculate the maximum operating frequency:
Maximum operating frequency ≈ 1/(τ), where τ is a time constant:

$1/(\tau) = 1/(C \times R)$

For example, suppose that the TC7SPB9306 is used under the following conditions. Then, the time constant τ is calculated as τ = (14 pF+30 pF)×1 kΩ. Therefore, the maximum operating frequency of this bus switch is calculated to be roughly 20 MHz. Bus switches should be sufficiently evaluated to ensure that they work properly under the actual operating conditions because their propagation delay times change with the board capacitance and other conditions.

Switch input/output capacitance, $C_{I/O}$: 14 pF
Load capacitance, C_L: 30 pF
Pull-up resistor, R_{pu}: 1 kΩ

Difference in level shifting available with a bus switch and a standard logic buffer:
As shown in Section 1.3, a standard logic buffer is composed of CMOS devices. A digital signal is applied to a gate to drive internal MOSFETs. Therefore, it has an inherent drive capability and provides a digital output. In addition, the output is delayed relative to the input, as shown in Figure 3.2.

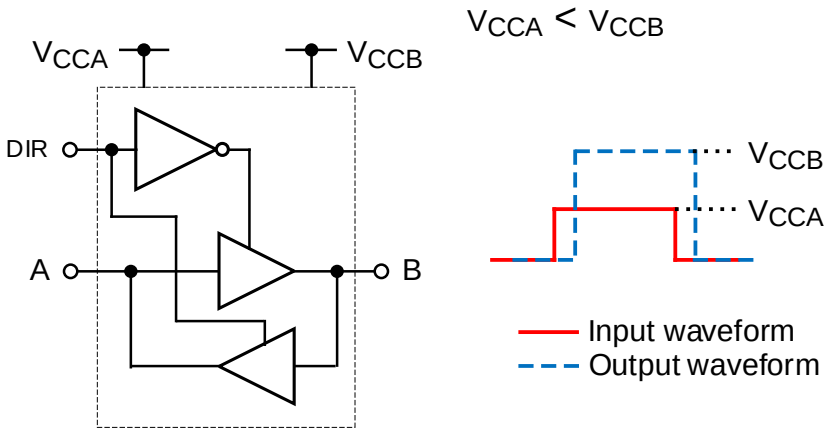


Figure 3.2 Equivalent circuit of a standard logic buffer and its input and output waveforms

3.2. Input- and output-tolerant functions

The control and switch pins of a bus switch provide tolerant functions. The input-tolerant function of the control pin is designed to prevent current from flowing from an input to the power supply when the input voltage is set higher than the supply voltage (V_{CC}) or when V_{CC} = 0 V. The input voltage specification is shown in the Operating Ranges table of the technical datasheet.

For example, when the input voltage range is specified as 0 to V_{CC}, voltage higher than V_{CC} must not be applied because the bus switch has a clamp diode between the input and V_{CC} pins (i.e., no input-tolerant function). In contrast, when the input voltage range is specified as 2.0 to 5.5 V, the input pin can accept voltage of up to 5.5 V regardless of the supply voltage (V_{CC} ≤ 5.5 V).

The tolerant function of the switch pin is designed to prevent current from flowing from the switch pin to V_{CC} when V_{CC} = 0 V and during a switch-off operation.

See individual technical datasheets for the availability of tolerant functions.

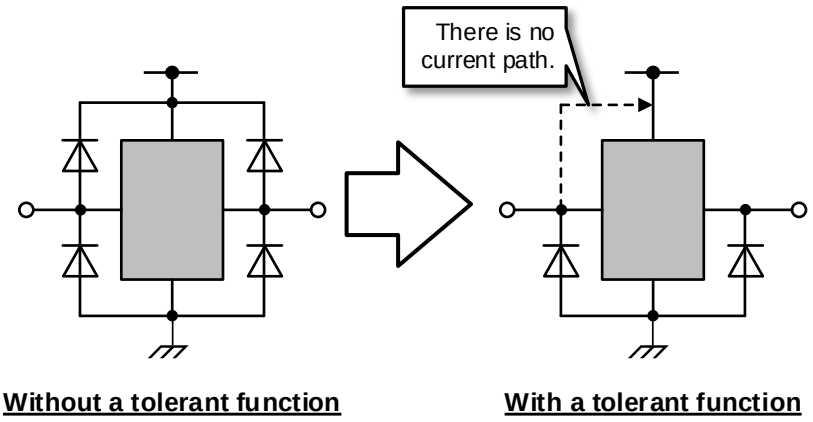


Figure 3.3 Bus switches with and without tolerant functions

Table 3.1 Characteristics related to the tolerant functions

Operating conditions

Characteristic	Symbol	Without a tolerant function	With a tolerant function
Supply voltage	V_{CC}	2.0 to 5.5 V	2.0 to 5.5 V
Control input voltage	V_{IN}	0 to V_{CC}	0 to 5.5 V*
Switch I/O voltage	V_S	0 to V_{CC}	0 to 5.5 V*

* Up to the maximum operating supply voltage

4. Bus switch lineup

Toshiba provides general-purpose and high-bandwidth bus switches.
Table 4.1 shows the categories of Toshiba's bus switches with different data rates.

Table 4.1 Categories of bus switches

Major Category	Sub-category	Data Rate	Bus Standard Example	Product Series Example
General-purpose bus switches	Low voltage	200 Mbps	-	TC7SBL series TC7WBL series TC7MBL series
	5 V			TC7SB series TC7WB series
	Dual-supply level shifting	200 Mbps (Depends on usage environment)	I^2C	TC7SPB series TC7WPB series TC7QPB series TC7MPB series
High-bandwidth bus switches	USB 2.0	480 Mbps	USB 2.0	TC7USB series
		2.5 Gbps	PCIe Gen. 1.1	
		3 Gbps	SATA 2.0	
		3 Gbps	SAS 1.0	
		3.4 Gbps	HDMI 1.4	
	USB 3.0	5 Gbps	USB 3.0	TC7USB3 series
		5 Gbps	PCIe Gen. 2.0	
		5.4 Gbps	Displayport 1.2	
		6 Gbps	SATA 3.0	
		6 Gbps	SAS 2.0	
	PCIe Gen. 3.0	8 Gbps	PCIe Gen. 3.0	TC7PCI series
		10 Gbps	USB 3.1	

4.1. General-purpose bus switches

Toshiba provides three types of general-purpose bus switches: low-voltage, 5-V, and dual-supply level-shifting bus switches. Table 4.2 summarizes the available switch configurations, supply voltages, types, and tolerant functions.

General-purpose bus switches are suitable for use along signal lines with a data rate lower than 200 Mbps.

Table 4.2 Lineup of general-purpose bus switches

Category	Switch Configuration	V_{CC} (V)		Type	Product Series	Tolerant Function	
						Control Pin	Switch Pin
Low voltage	SPST	1.65 to 3.6		Parallel n-, p-channel MOSFETs	TC7SBL series TC7WBL series TC7MBL series	✓	✓ * Unavailable with SBL66C
	SPDT				TC7MBL series	✓	✓
	SP4T				TC7MBL series	✓	✓
5 V	SPST	1.65 to 5.5			TC7SB series TC7WB series	✓	-
	SPDT				TC7SB series	✓	-
Dual-supply level shifting	SPST	V_{CCA} 1.65 to 5.0	V_{CCB} 2.3 to 5.5	n-channel MOSFET	TC7SPB series TC7WPB series TC7QPB series TC7MPB series	✓	✓
	SPDT				TC7MPB series	✓	✓

4.2. High-bandwidth bus switches

High-bandwidth bus switches are used along USB 2.0, USB 3.0, and PCIe 3.0 serial links (with a data rate of 480 Mbps to 10 Gbps).

Toshiba's high-bandwidth bus switches have lower input and output capacitances than general-purpose bus switches, making it possible to handle faster signals.

Table 4.3 summarizes the available switch configurations, supply voltages, types, and tolerant functions.

Table 4.3 Lineup of high-bandwidth bus switches

Category	Switch Configuration	V_{CC} (V)	Type	Product Series	Tolerant Function	
					Control Pin	Switch Pin
USB 2.0 (480 Mbps)	SPDT	2.3 to 4.3	Parallel n-, p-channel MOSFETs	TC7USB series	✓	✓
USB 3.0 (5 Gbps)	SPDT	1.65 to 1.95	Charge pump	TC7USB series	✓	✓
PCIe 3.0 (8 Gbps)	SPDT	3.0 to 3.6		T7PCI series	✓	-

Technical datasheets for high-bandwidth bus switches show their frequency response characteristics. Figure 4.1 shows the frequency response characteristics of different categories of bus switches.

High-bandwidth bus switches and other devices for high-speed signal links are evaluated using an eye pattern like the one shown in Figure 4.2.

It shows the eye pattern of a PCIe 3.0 switch when USB 3.1 (10-Gbps) signals are applied. An open eye pattern indicates minimal signal distortion.

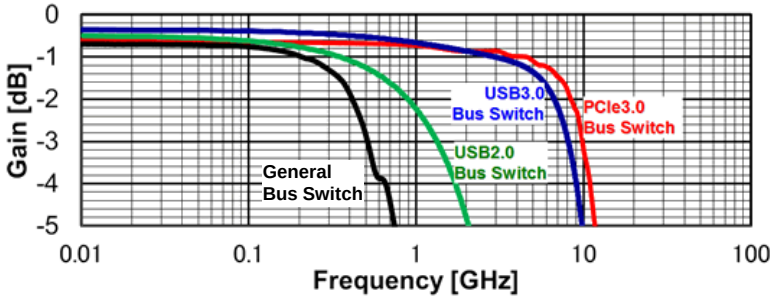


Figure 4.1 Frequency response characteristics of different categories of high-bandwidth bus switches

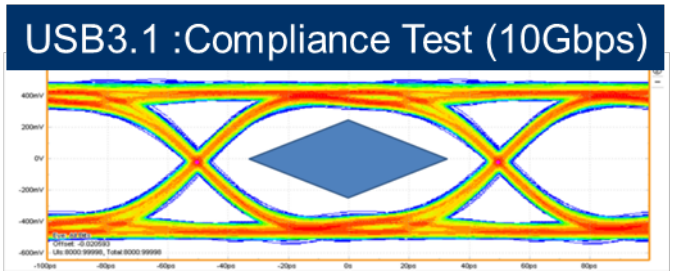


Figure 4.2 Eye pattern evaluation

5. Examples of bus switch applications

Bus switches are used to simply turn on/off the connection to a signal line or to switch the connection from one path to another. A level-shifting function is available with some bus switches.
The following subsections show several examples of bus switch applications.

5.1. Switching the signal connection from one path to another

An SPDT bus switch is used to select the destination of a CPU output signal from two ICs (IC1 and IC2).
A bus switch can pass a signal bidirectionally. Therefore, the bus switch can also pass the output signals of IC1 and IC2 to the CPU.
The bus switch causes a voltage decay that is equal to its on-resistance multiplied by current. However, the signal voltage hardly decays since little current generally flows in the case of a digital signal.
The output rise and fall delays are affected by the switch I/O capacitance ($C_{I/O}$) and on-resistance (R_{ON}) of the bus switch as well as external capacitance and resistance. Typically, bus switches can operate at a frequency higher than several tens of megahertz. See Section 6 for how to calculate the maximum possible operating frequency.

5.2. Turning on/off the connection to a signal line (for load reduction and IC protection)

The circuit shown in Figure 5.1 passes an output signal of a CPU to IC1 and IC2.
When there is an operating mode in which it is unnecessary to pass the CPU output signal to IC1, an SPST bus switch is used between the CPU and IC1.
The bus switch makes it possible to pass the CPU output signal to IC1 when necessary and blocks it when unnecessary, reducing the load on the CPU.

In Figure 5.1, the devices that might be placed under partial power-down conditions are highlighted by a red box. Suppose that partial power-down might cause the supply voltage of these devices to become zero.
If this occurs, the bus switch might be destroyed. IC1 might also be destroyed if the CPU output signal flows to IC1, causing current to flow to the power supply via the parasitic diode of IC1.
To protect IC1 from the CPU output signal, use a bus switch with switch pins having a tolerant function. Connect the power supply pin of the bus switch to the same power supply as for IC1. If the power supply for the devices under partial power-down conditions (i.e., the power supply for IC1 and the bus switch) becomes 0 V, the bus switch breaks the connection between the CPU and IC1 because its switch pins have a tolerant function. Consequently, IC1 is protected.

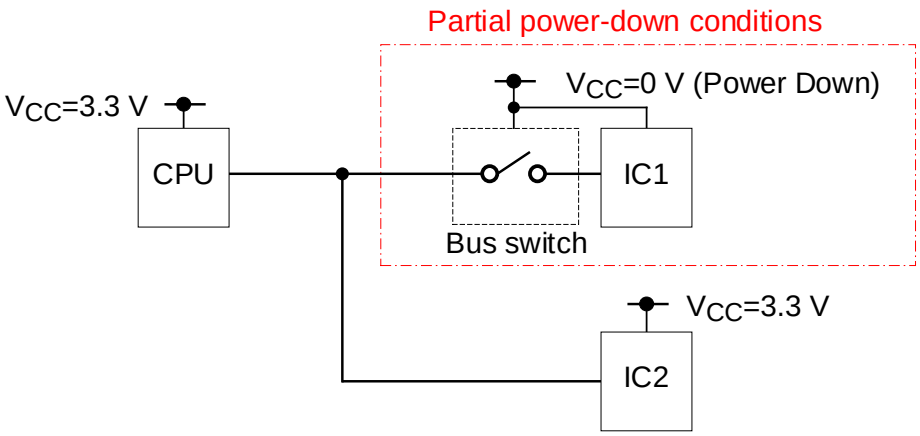


Figure 5.1 Example of a basic circuit that turns on/off the connection to a signal line

5.3. Signal level shifting

In Figure 5.2, the CPU and the IC operate at different supply voltages. Therefore, signal level shifting is necessary to enable communication between these two devices.

In this case, you can use a dual-supply level-shifting SPST bus switch between the CPU and the IC. Add pull-up resistors (R_{PU}) to pull the input and output of the bus switch to the power supplies for the CPU and the IC, respectively. This enables the two devices in different voltage domains (e.g., 3.3-V and 5.0-V domains) to communicate with each other.

Dual-supply level-shifting bus switches allow V_{CCA} to be 1.65 to 5.0 V and V_{CCB} to be 2.3 to 5.5 V. However, V_{CCA} must be lower than V_{CCB}. Toshiba's product portfolio contains 1-, 2-, 4-, and 8-bit dual-supply level-shifting bus switches.

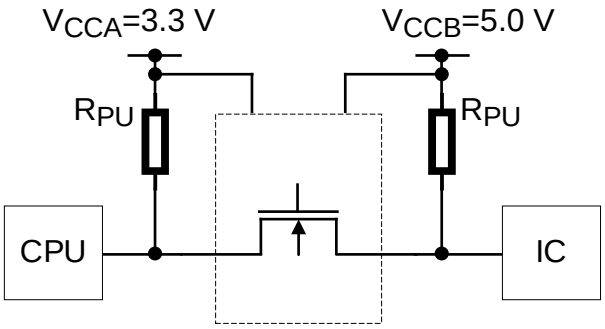


Figure 5.2 Example of a basic circuit with a level-shifting bus switch

6. Calculating output rise and fall times (t_r and t_f)

The output rise and fall times ($t_{r(out)}$ and $t_{f(out)}$) of a bus switch are affected by the RC time constant, where R is on-resistance (R_{ON}) and C is switch I/O capacitance ($C_{I/O}$). In practice, the output rise and fall times are also affected by external capacitance and resistance.

Example of calculating the output rise and fall times:
Let's use the TC7SB66CFU as an example.
The output rise and fall times can be approximated as follows. (See Figure 6.1 for a circuit.)
Approximate equation:

$$t_{r(out)} \ / \ t_{f(out)} = -(C_{I/O} + C_L) \times (R_{DRIVE} + R_{ON}) \times \ln \frac{((V_{OH} - V_{OL}) - V_M)}{(V_{OH} - V_{OL})}$$

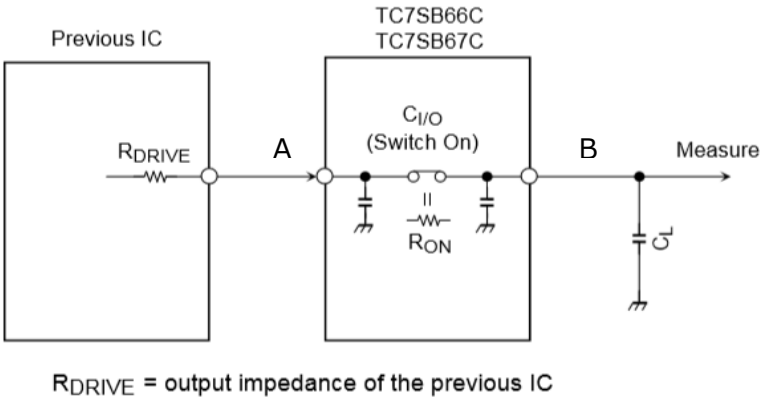
where, R_{DRIVE} is the output impedance of the preceding IC.

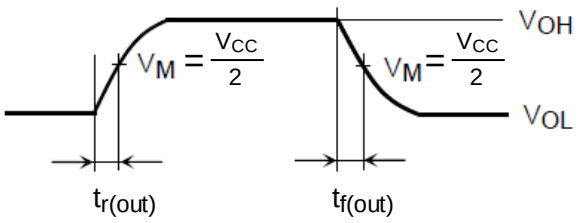
Calculation example:

$$t_{r(out)} \ / \ t_{f(out)} = -(10 + 15)E^{-12} \times (120 + 4) \times \ln \frac{((4.5 - 0) - 2.25)}{(4.5 - 0)} \approx 2.1 \quad ns$$

Calculation conditions:

V_{CC} = 4.5 V, C_L = 15 pF, R_{DRIVE} = 120 Ω (output impedance of the preceding IC),
V_M = 2.25 V ($= \frac{V_{CC}}{2}$)
Output voltage of the preceding IC: Digital signal (high-level output voltage = V_{CC}, low-level output voltage = GND)





Parameter	V_{CC}			
	5.0 ± 0.5 V	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 ± 0.15 V
V_M	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2

Figure 6.1 Equivalent circuit for the calculation of output rise and fall times and output waveform

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