AN5426

Hardware Design Guidelines for S32K1xx Microcontrollers

Rev. 5 — March 2021

Application Note

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1 Introduction

The S32K series further extends the highly scalable portfolio of ARM® Cortex® MCUs in the automotive industry. It builds on the legacy of the KEA series, whilst introducing higher memory options alongside a richer peripheral set extending capability into a variety of automotive applications.

With a 2.70–5.5 V supply and focus on automotive environment robustness, the S32K series devices are well suited to a wide range of applications in electrical harsh environments. These devices are optimized for cost-sensitive applications offering low pin-count options.

The S32K series offers a broad range of memory, peripherals, and package options. They share common peripherals and pin counts allowing developers to migrate easily within the MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the S32K series for their end product platforms, maximizing hardware and software reuse and reducing time to market.

Following are the general features of the S32K series MCUs:

- 32-bit ARM Cortex-M4 core with IEEE-754 compliant FPU, executing up to 112 MHz.
- Scalable memory footprints up to 2 MB flash and up to 256 KB SRAM.
- Precision mixed-signal capability with on chip analog comparators and multiple 12-bit ADCs.
- Powerful timers for a broad range of applications including motor control, lighting control and body applications.
- Serial communication interfaces such as LPUART, LPSPI, LPI2C, FlexCAN, CAN-FD and FlexIO.
- SHE specification compliant security module.
- Single power supply (2.70–5.5 V) with full functional flash program/erase/read operations.
- Functional safety compliance with ISO26262, with internal watchdog, voltage monitors, clock monitors, memory protection and ECC.
- Ambient operation temperature range:
  - –40°C to +105°C
  - –40°C to +125°C
  - –40°C to +150°C
- Software enablement: S32 Software Development Kit (SDK), S32 Design Studio (S32DS).

2 Power system

Subsequent sections describe the different options for power supply configurations, as well as considerations to have for a proper connection of supply and ground pins.

Table 1. S32K1xx - Power supply pins and domains

MCU Pin Name	Description	Normal Operating Voltage	S32K1xx MCU Package - Pin Number						
			176 LQFP	144 LQFP	100 BGA	100 LQFP	64 LQFP	48 LQFP	32QFN
VDD	Supply Voltage	+3.3V or +5.0V	18	11	E5	10	7	5	3
			39	32	E6	38	41	31	21
			59	51	F5	61	-	-	-
			77	67	F6	87	-	-	-
			110	91	-	-	-	-	-
			129	124	-	-	-	-	-
			152	-	-	-	-	-	-
			172	-	-	-	-	-	-
VDDA[1]	Analogue supply voltage	VDD	20	13	E4	11	8	6	-
VREFH[2]	ADC Reference Supply high	≤VDDA	21	14	E3	12	9	-	-
VREFL	ADC Reference Supply low	VSS/GND	22	15	E2	13	-	-	-
VSS[3]	Supply Ground	VSS/GND	19	12	D4	14	10	30	4
			23	16	D7	37	40	7	20
			38	31	G4	60	-	-	-
			58	50	G7	86	-	-	-
			76	66	-	-	-	-	-
			109	90	-	-	-	-	-
			130	123	-	-	-	-	-
			151	-	-	-	-	-	-
			171	-	-	-	-	-	-

1. All VDD and VDDA pins must be shorted and connected externally together to a common reference on the PCB. A decoupling capacitor must be used per each supply pin and a local Bulk/bypass capacitor just for the VDD and VDDA domains.
2. VREFH must be equal or less than VDD and VDDA.
3. VSS and VREFL must be shorted to GND at package level.

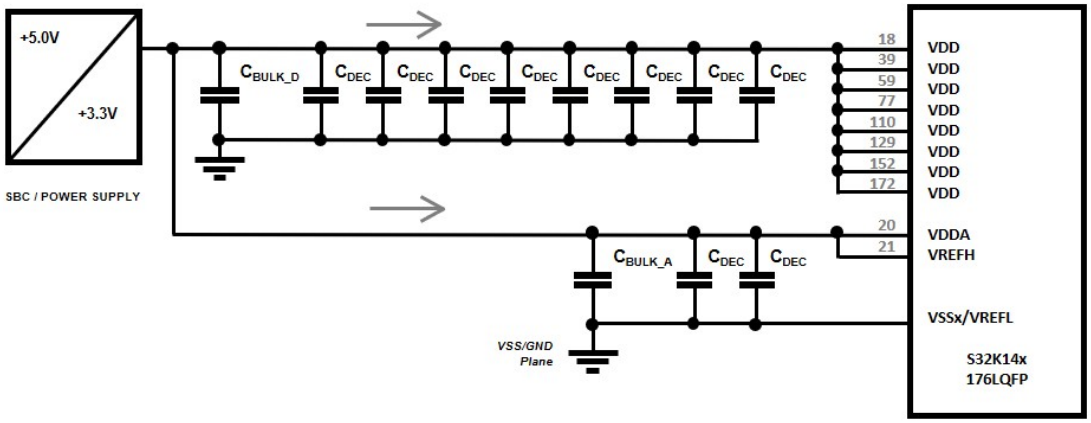


Figure 1. Power supply pins and domains for the S32K14x – 176LQFP package

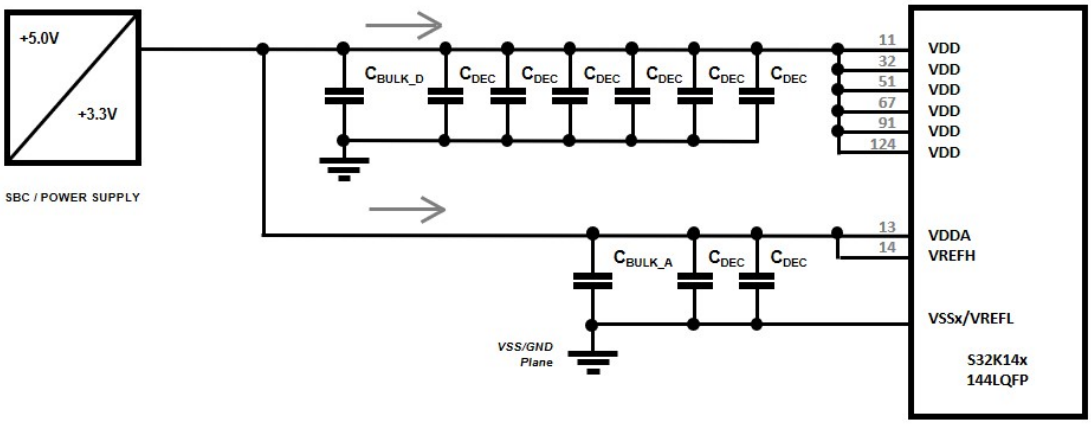


Figure 2. Power supply pins and domains for the S32K14x – 144LQFP package

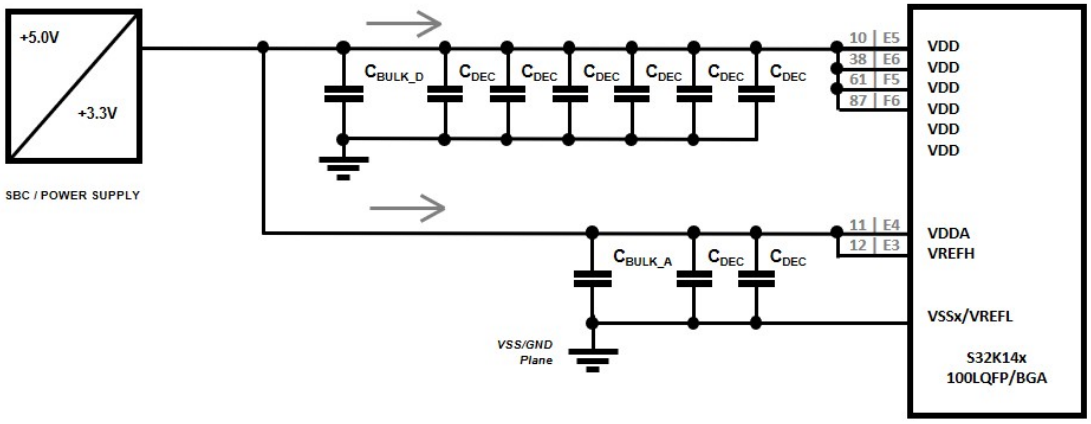


Figure 3. Power supply pins and domains for the S32K14x – 100LQFP and 100BGA package

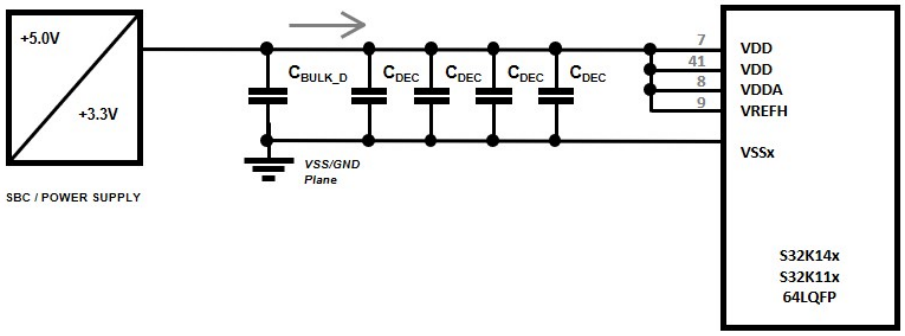


Figure 4. Power supply pins and domains for the S32K14x and the S32K11x – 64LQFP package

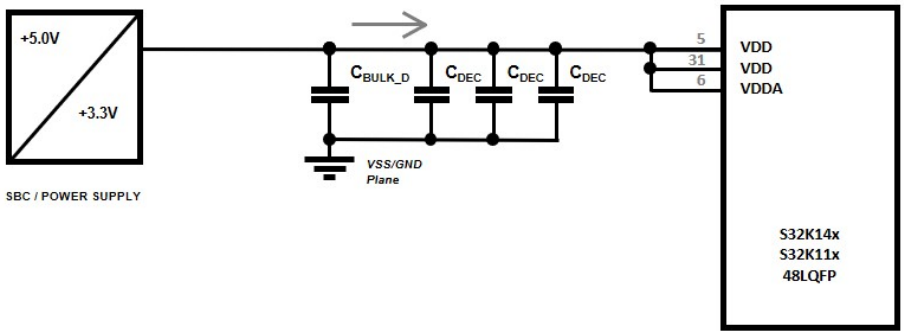


Figure 5. Power supply pins and domains for the S32K14x and the S32K11x – 48LQFP package

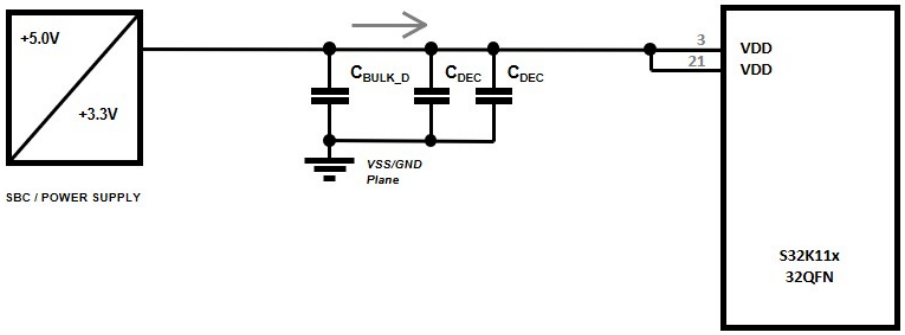


Figure 6. Power supply pins and domains for the S32K11x – 32QFN package

Table 2. S32K1xx – Bulk/Bypass and decoupling capacitors

Symbol	Characteristic	Value	Description
C_{BULK_D}	X7R Ceramic	10uF	Local Bulk/Bypass Capacitor for domain.
C_{BULK_A}	X7R Ceramic	10uF	Local Bulk/Bypass Capacitor for domain.[1,2]
C_{DEC}	X7R Ceramic	100nF	Decoupling Capacitor per power pin.[1,2]

1. All VDD and VDDA pins must be shorted and connected externally together to a common and same reference on PCB.
2. X7R Ceramic.

2.1 Bulk and decoupling capacitors

The effectiveness of the bulk/bypass and the de-coupling capacitors depends on the optimum placement and connection type. The bulk capacitor acts as a local power supply to the power pin, near the decoupling capacitors and close as possible to the assigned reference voltage pin. Decoupling capacitors make the current loop between supply, MCU, and ground reference as short as possible for high frequency transients and noise. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pin; the ground side of the decoupling capacitor should have a via to the pad which goes directly down to the internal ground plane. The capacitor should not route to the power plane through a long trace.

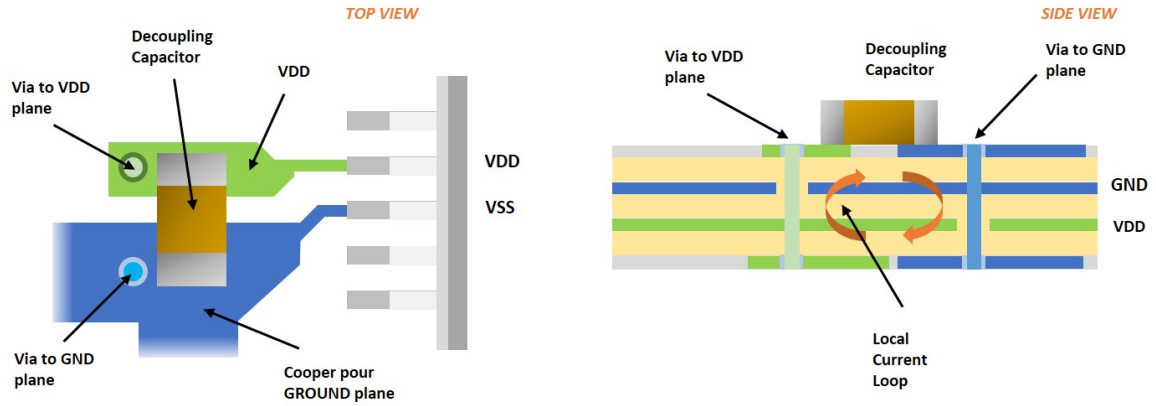


Figure 7. Bulk and decoupling capacitor connection

2.2 MCU power supply ramp rate

In the S32K1xx datasheet, there is a parameter called "MCU supply ramp rate" with a maximum and a minimum limit. During the power-on of MCU, the power supply must assure a ramp-rate within this range from VDDOFF to the voltage operating level VDD. The outcome of violating the specification causes unexpected behavior, stuck operation or damage in the MCU.

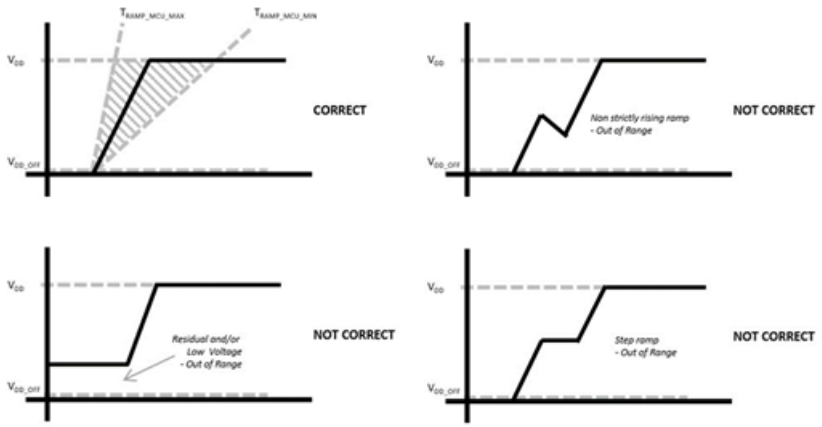


Figure 8. MCU power supply ramp rate

3 Clock circuitry

The S32K1xx has the following clock sources:

- Fast internal reference clock (FIRC): 48 MHz.
- Slow internal reference clock (SIRC): 8 MHz.
- PLL: External oscillator as input source.
- External square wave input clock: up to 50 MHz.
- External oscillator clock (OSC): 4–40 MHz.

FIRC, SIRC are internal and does not have to be considered from the hardware design perspective. The external oscillator works with a range from 4–40 MHz. It provides an output clock that can be provided to the PLL or used as clock source for some peripherals. When using the external oscillator as input source for the PLL, the frequency range of the external oscillator should be 8–40 MHz.

3.1 EXTAL and XTAL pins

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. The pierce oscillator provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. S32K1xx supports crystals or resonators from 4 MHz to 40 MHz. The Input Capacitance of the EXTAL, XTAL pins is 7 pF.

Table 3. S32K1xx - EXTAL and XTAL pins

MCU Pin Name	Function	Signal Description	S32K1xx - MCU Pin Number						
			176 LQFP	144 LQFP	100 LQFP	100 BGA	64 LQFP	48 LQFP	32 QFN
PTB6	XTAL	External Crystal Output	25	18	16	F1	12	9	6
PTB7	EXTAL	External Crystal Input	24	17	15	E1	11	8	5

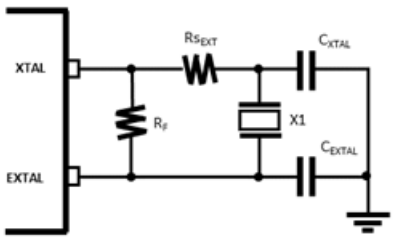


Figure 9. Reference oscillator circuit

Table 4. Components of the oscillator circuit

Symbol	Description
Rs_{EXT}[1]	Series resistor for current limitation
R_F	Feedback Resistor

Table continues on the next page...

Table 4. Components of the oscillator circuit (continued)

Symbol	Description
	• When Low-gain is selected, internal $R_F$will be selected, and external R_F is not required. • When High-gain is selected, external R_F(1M Ohm) need to be connected for proper operation of crystal. For external resistor, up to 5% tolerance is allowed.
X_1	Quartz Crystal / Ceramic Resonator
C_{XTAL}	External load capacitor on XTAL pin.
C_{EXTAL}	External load capacitor on E_{XTAL} pin.

1. The Rs_{EXT} and load capacitors values are dependent on the specifications of the crystal and on the board capacitance. It is recommended the customer develops evaluation and characterization of the crystal on their PCB with the part manufacturer.

3.2 Suggestions for the PCB layout of oscillator circuit

The crystal oscillator is an analog circuit and must be designed carefully and according to the analog-board layout rules:

- The crystal oscillator is an analog circuit and must be designed carefully and according to the analog-board layout rules:
- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum regarding , and capacitors. The data sheet includes recommendations for the tank capacitors and . These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point.
- Signal traces between the XTAL/EXTAL pins, the crystal and the external capacitors must be as short as possible, these traces pins should only be connected to required oscillator components and must not be connected to any other devices or components. The connection between the MCU and the external oscillator should not have more than a single via with its the ground-via. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI.
- Keep other digital signal lines, especially clock lines, analog and frequently switching signal lines, as far away from the crystal connections as possible. Crosstalk from the digital activities may affect the small-amplitude of the oscillator signal.
- A ground area should be placed under the crystal oscillator area. This ground plane must be clean ground connected to the VSSx reference of the S32K1XX. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to to to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitor’s ground connections should always be as close together as possible.

The following figure, shows the recommended placement and routing for the oscillator layout.

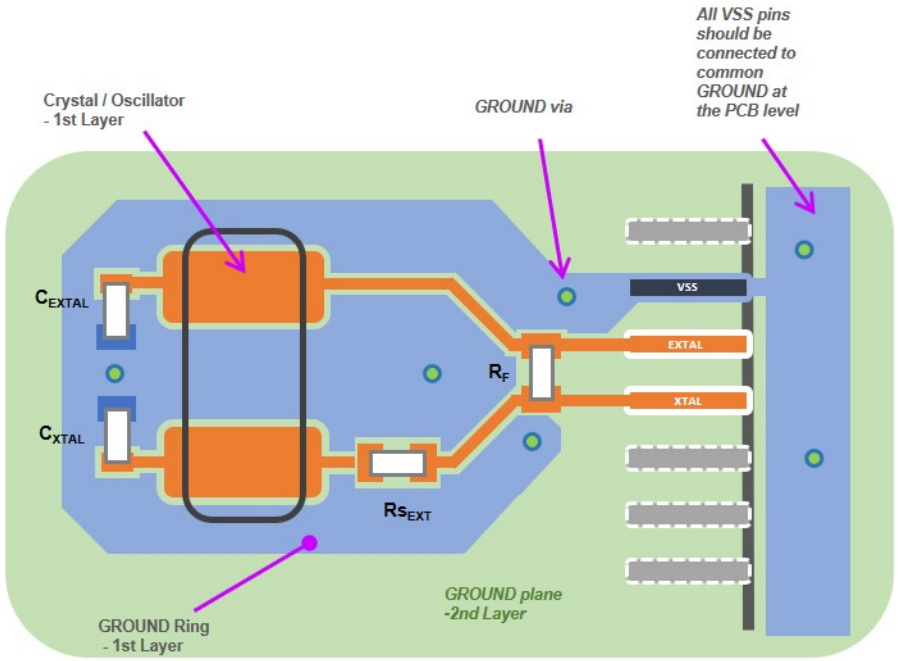


Figure 10. Suggested crystal oscillator layout

Crystal oscillator circuit provides a very-safe stable oscillation when the $g_{mXOSC} > 5 \times g_{merit}$. The g_{merit} is defined as:

$$g_{merit} = 4 \times (ESR_{OSC} + Rs_{EXT}) \times (2\Pi \times F_{OSC})^2 \times (C_{O\_OSC} + C_{LOAD})^2$$

where:

Table 5. Transconductance Equation - Parameters

Parameter	Description
g_{mXOSC}	Transconductance of the internal oscillator circuit
F_{OSC}	Frequency of the external crystal oscillation.
ESR_{OSC}	Equivalent series resistance of the external crystal
C_{O_OSC}	Shunt capacitance of the external crystal
C_{LOAD}	Total load capacitance on the external crystal $C_{LOAD} = C_S([C_{XTAL} + C_{EXTAL}]/[C_{XTAL} \times C_{EXTAL}])$ For the frequency to be accurate, the oscillator circuit has to show the same load capacitance to the crystal as the one the crystal was adjusted for. Frequency stability mainly requires that the load capacitance be constant. The external capacitors and are used to tune the desired value of to reach the value specified by the crystal manufacturer.

Table continues on the next page...

Table 5. Transconductance Equation - Parameters (continued)

Parameter	Description
C_S	Stray or parasitic capacitance on the pin due to any PCB traces, 5pF~7pF.
C_{EXTAL}	External load capacitor on EXTAL pin.
C_{XTAL}	External load capacitor on XTAL pin.
Rs_{EXT}	External series resistance connected between XTAL pin and external crystal for current limitation, RS should be selected carefully to have appropriate oscillation amplitude for both protecting crystal or resonator device and satisfying proper oscillation startup condition and prevents the oscillator from vibrating at the odd harmonics of the fundamental frequency If the power dissipation in the selected crystal or oscillator is lower than the drive level (uW) specified by the crystal supplier, the insertion of is not recommended and its value is then 0Ω. An approximation for the initial value of can be obtained by considering the voltage divider formed by and . Thus, the value of is equal to the reactance of . Then $Rs_{EXT} = 1/(2\Pi \times F_{OSC} \times C_{XTAL})$

For example, to design the oscillation loop in a S32K1xx microcontroller with a maximum Amplifier Transconductance value gmOSCX=47 mA/V for a frequency range 8MHz-40MHz, and it is selected the crystal AT-16.000MAGE-x - 16MHz /TXC crystal, with the following characteristics:

Table 6. Example – Pierce Oscillator Design

Parameter	Value	Value	Units
F_{OSC}	Frequency of the external crystal oscillation.	32	MHz
ESR_{OSC}	Equivalent series resistance of the external crystal	50	Ω
Rs_{EXT}	Series resistor for current limitation	100	Ω
C_{O_OSC}	Shunt capacitance of the external crystal	10	pF
C_{LOAD}	Total load capacitance on the external crystal	10.5	pF
C_S	Stray or parasitic capacitance on the pin due to any PCB traces	7	pF
C_{EXTAL}	External load capacitor on EXTAL pin.	7	pF
C_{XTAL}	External load capacitor on XTAL pin.	7	pF

g_{merit} = 4 X (60 + 100) X (2Π X [16 X 10^6])^2 X ([12 X 10^{-12}] + [8 X 10^{-12}]^2

g_{merit} = 2.587 $^{mA/V}$

5 x g_{merit} = 12.935 $^{mA/V}$

Due to the Crystal oscillator transconductance (47 $^{mA/V}$) is higher than 5 x g_{merit}, The estimation of the gain margin is sufficient to start the oscillation and the oscillator is expected to reach a stable oscillation after a typical delay specified in the datasheet.

Based on the analysis and characterization of the oscillator manufacturer, the Rs_{EXT} and the values for C_{EXTAL} and C_{XTAL} can be adjusted or redefined in order to assure a safe oscillation margin.

To check and measure the crystal oscillation or any other signal characteristics, a frequency counter equipment is useful. Oscilloscopes and spectrum analyzers are generally not recommended because these types of equipment are usually not able to distinguish main oscillation from spurious), and the other hand, if the probes of the oscilloscope (despite that some probes are of low impedance) are connected directly to the oscillation circuit, it will stop and may affect or attenuate the crystal's oscillations.

4 Debug and programing interface

4.1 RESET system

Resetting the MCU provides a way to start processing from a known set of initial conditions. System reset begins with the on-chip regulator in full regulation and system clocking generation from an internal reference.

4.1.1 External pin RESET

For all reset sources, the RESET_B pin is driven low by the MCU for at least 128 bus clock cycles and until flash memory initialization has completed.

After flash memory initialization has completed, the RESET_B pin is released and the internal chip reset deasserts. Keeping the RESET_B pin asserted externally delays the negation of the internal chip reset.

During a pin reset, the RCM's SRS[PIN] bit is set. Hence, application software can detect an external pin RESET by reading this register.

In case RESET_PIN_CFG within Flash Option Register (FTFC_FOPT) is cleared, RESET_B pin is disabled following a POR and cannot be enabled as reset function. When this option is selected, there could be a short period of contention during a POR ramp where the device drives the pin low prior to establishing the setting of this option and releasing the reset function on the pin. The RESET pin is the same as the standard GPIO. It can operate as a pseudo open-drain output because there is also a PMOS device in the output stage.

This bit is preserved through system resets and low-power modes. When RESET_B pin function is disabled, it cannot be used as a source for low-power mode wake-up.

NOTE

When the reset pin has been disabled and security has been enabled by means of the FSEC register, a mass erase can be performed only by setting both the Mass Erase and System Reset Request fields in the MDM-AP register.

The reset pin, similar to some other GPIO has a weak internal pull-up. If the environment and the customer application is noisy, an external pull up resistor to VDD must be added directly to the reset pin in order to avoid a sporadic or unintended reset occurs. Refer to the device datasheet for the levels of voltage and current allowed in the pin.

Despite a capacitor in the reset line is not directly required for the MCU. In some cases, in order to add a further ESD protection, an external capacitor is added between the RESET pin to ground. The values of the pull up resistor and the capacitor must be selected according to the design requirements of the application. Refer to the device datasheet for the minimum RESET pulse value that can be detected for the MCU.

4.2 JTAG and TRACE interface

A number of commonly used debug connectors are shown here. Most of the ARM development tools uses one of these pin out's. When developing your ARM circuit board, it is recommended to use a standard debug signal arrangement to make connection to debugger easier.

The SWD/SWV pins are overlaid on top of the JTAG pins as follows:

Table 7. S32K1xx - JTAG and SWD signal description

JTAG Function	Signal Description	MCU Port	S32K1xx - MCU Pin Number						
			176 Intro LQFP	144 Intro LQFP	100 LQFP	100 BGA	64 Intro LQFP	48 Intro LQFP	32 QFN
TCLK/ SWD_CLK	Clock into the core	PTC4	169	140	96	D5	62	46	30
TDI	JTAG Test Data Input	PTC5	168	139	95	D6	61	45	29
TDO	JTAG Test Data Output / SWV trace data output (SWO)	PTA10	164	136	92	C5	58	44	28
TMS/ SWD_DIO	JTAG Test Mode Select/ Serial Wire Debug Data I/O	PTA4	173	142	98	C3	64	48	32
RESET	Reset MCU	PTA5	170	141	97	C4	62	47	31

Table 8. S32K1xx - JTAG and SWD interface

JTAG Mode	SWD Mode	Signal Description	MCU Port	Recommendation	R_{PU} and R_{PD} Value	I/O Power Domain
TCK	SWD_CLK	Clock into the core	PTC4	Pull-Down	10k-47k	VDD
TDI	-	JTAG Test Data Input	PTC5	Pull-Up	10k-47k	
TDO	-	JTAG Test Data Output / SWV trace data output (SWO)	PTA10	Pull-Up	10k-47k	

Table continues on the next page...

Table 8. S32K1xx - JTAG and SWD interface (continued)

JTAG Mode	SWD Mode	Signal Description	MCU Port	Recommendation	R_{PU} and R_{PD} Value	I/O Power Domain
TMS	SWD_DIO	JTAG Test Mode Select/Serial Wire Debug Data I/O	PTA4	Pull-Up	10k-47k	
RESET	RESET	Reset MCU	PTA5	Pull-Up	10k	
GND	GND	Ground	VSSx	-		VSS
External pull up/down resistors for the JTAG signals can be added in order to increase debugger connection robustness.						

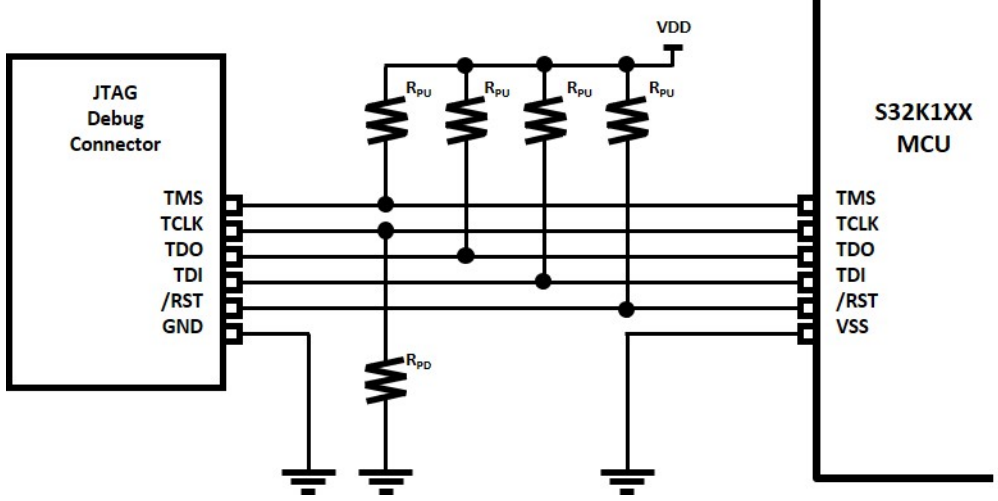


Figure 11. JTAG/SWD signal connections

4.3 Debug connector pinouts

4.3.1 20-pin Cortex Debug D ETM connector

Some newer ARM microcontroller board use a 0.05” 20-pin header (Samtec FTSH-110) for both debug and trace. (The signals greyed out are not available on the Cortex-M3 or Cortex-M4.) The 20-pin Cortex Debug D ETM connector support both JTAG and Serial Wire debug protocols. When the Serial debug protocol is used, the TDO signal can be used for Serial Wire Viewer output for trace capture. The connector also provides a 4-bit wide trace port for capturing of trace that require a higher trace bandwidth (example, when ETM trace is enabled).

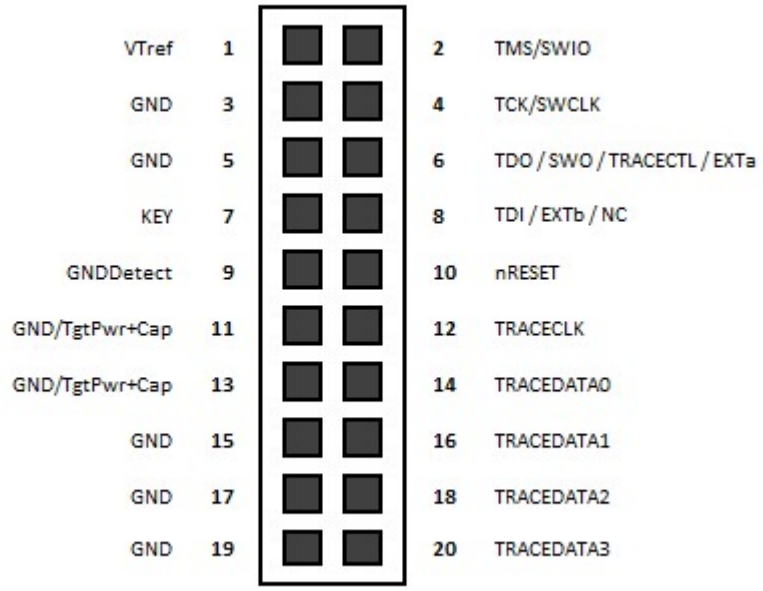


Figure 12. 20-pin Cortex Debug D ETM connector pin layout

4.3.2 10-pin Cortex Debug connector

For device without ETM, you can use an even smaller 0.05” 10-pin connector (Samtec FTSH-105) for debug. Similar to the 20-pin Cortex Debug D ETM connector, both JTAG and Serial-Wire debug protocols are supported in the 10-pin version.

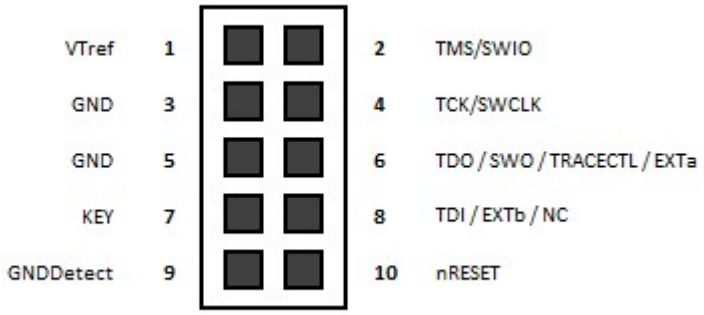


Figure 13. 10-pin Cortex Debug connector pin layout

4.3.3 Legacy 20-pin IDC connector

A common debug connector used in ARM development boards is the 20-pin IDC connector. The 20-pin IDC connector arrange support JTAG debug, Serial Wire debug (SWIO and SWCLK), Serial Wire Output (SWO). The nICEDETECT pin allows the target system to detect if a debugger is connected. When no debugger is attached, this pin is pulled high. A debugger connection connects this pin to ground. This is used in some development boards that support multiple JTAG configurations. The nSRST connection is optional; debugger can reset a Cortex-M system via the System Control Block (SCB) so this connection is often omitted from the top level of microcontroller designs.

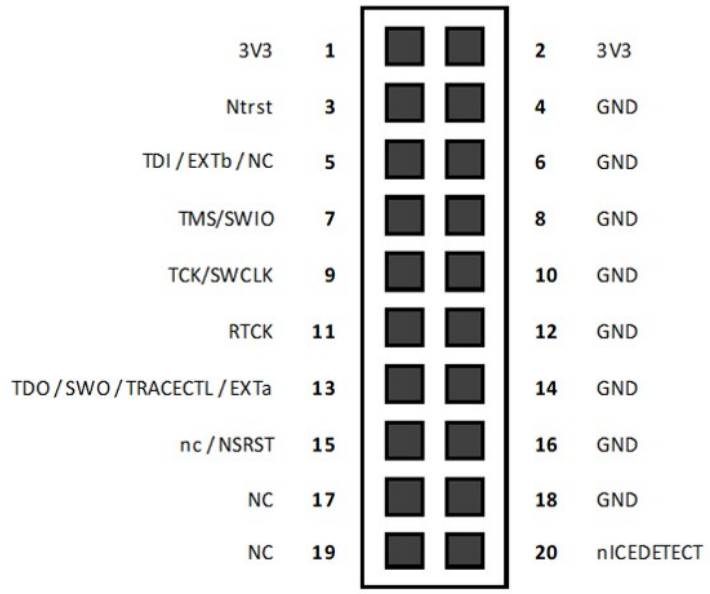


Figure 14. 20-pin IDC connector

5 Analog comparator interface

The comparator (CMP) module provides a circuit for comparing two analog input voltages in the S32K1xx Microcontrollers. The comparator circuit is designed to operate across the full range of the supply voltage, known as rail-to-rail operation. **CMPO** is high when the non-inverting input is greater than the inverting input, and is low when the non-inverting input is less than the inverting input.

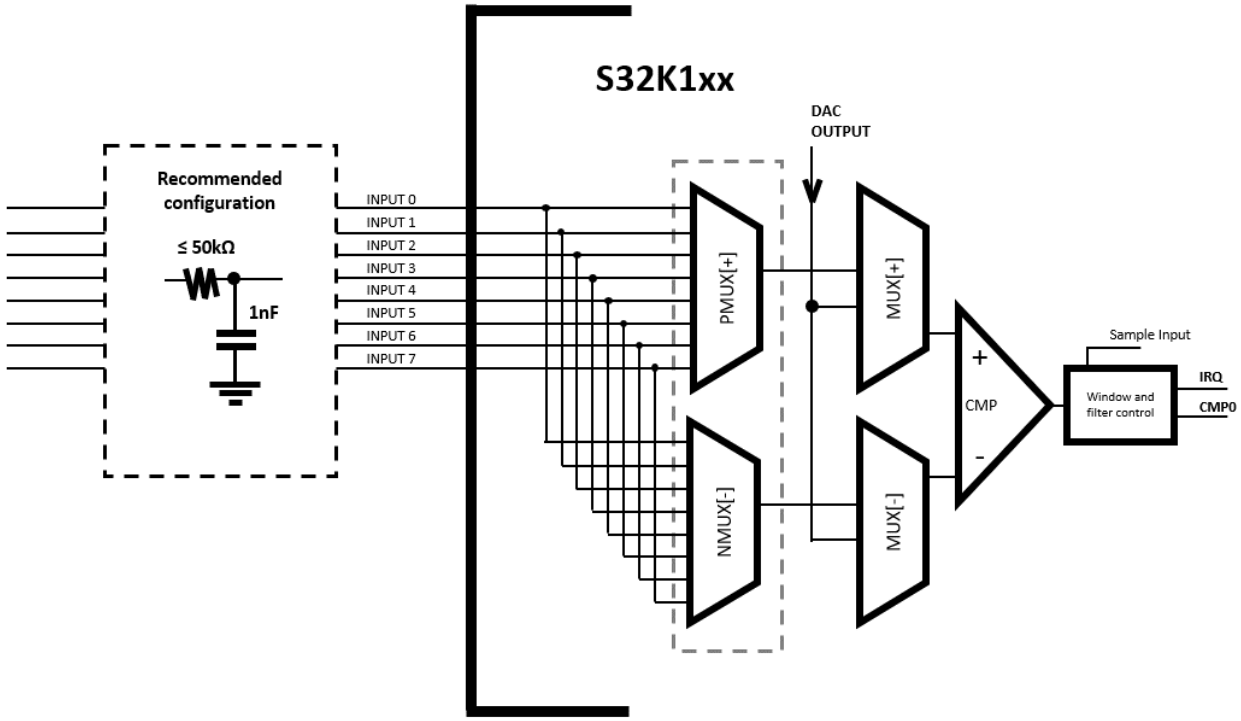


Figure 15. CMP high level diagram

The switching of the high-speed interfaces or any GPIO may introduce some noise to the analog or comparator inputs due to inductance/capacitive coupling between the MCU pins. The cross-talk may be introduced by PCB tracks that run close to each other or that cross each other. In order to avoid and mitigate the high-frequency noise and any coupling. Please ensure that the analog comparator input signal impedance is 50K or less.(see Figure 15)

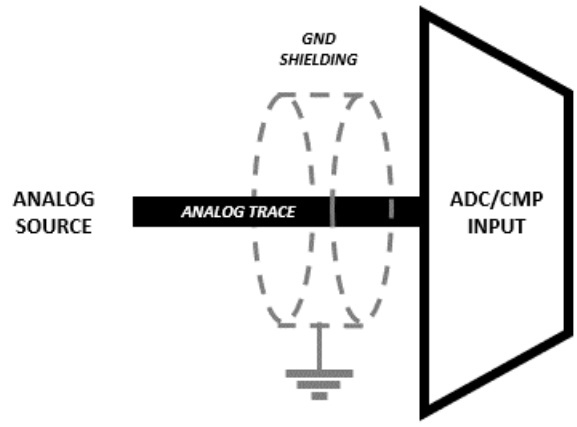


Figure 16. Shielding of analog signals

Placing ground planes and shapes alongside sensitive analog signals provides shielding on the PCB. Care should be taken to minimize the length of the paths of these types of signal on the PCB. This prevents interference and I/O cross-talk affecting the signal. The large amount of metal has the lowest possible resistance and lowest possible inductance because of the large, flattened conductor pattern. The ground plane acts as a low-impedance return path for decoupling high-frequency currents caused by fast digital logic. It also minimizes emissions from electromagnetic interference/radio-frequency interference (EMI/RFI). In other hand, the ground planes also permit high-speed digital or analog signals to be transmitted via transmission-line (microstrip or stripline) techniques, where controlled impedances are required.

6 Communication modules

6.1 LIN interface for LPUART module

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks. As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

Features of the LPUART module supports and include:

- LIN master and slave operation
- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock:
  - Baud rate can be configured independently of the bus clock frequency
  - Supports operation in Stop modes
- Interrupt, DMA or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
  - Receive data match
- Hardware parity generation and checking
- Programmable 7-bit, 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection

- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- Independent FIFO structure for transmit and receive
  - Separate configurable watermark for receive and transmit requests

Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty.

Table 9. LPUART signal description

Signal	Description	I/O
TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
RXD	Receive data.	I
CTS_B	Clear to send.	I
RTS_B	Request to send.	O

The LIN bus topology utilizes a single master and multiple nodes, as shown below. Connecting application modules to the vehicle network makes them accessible for diagnostics and service.

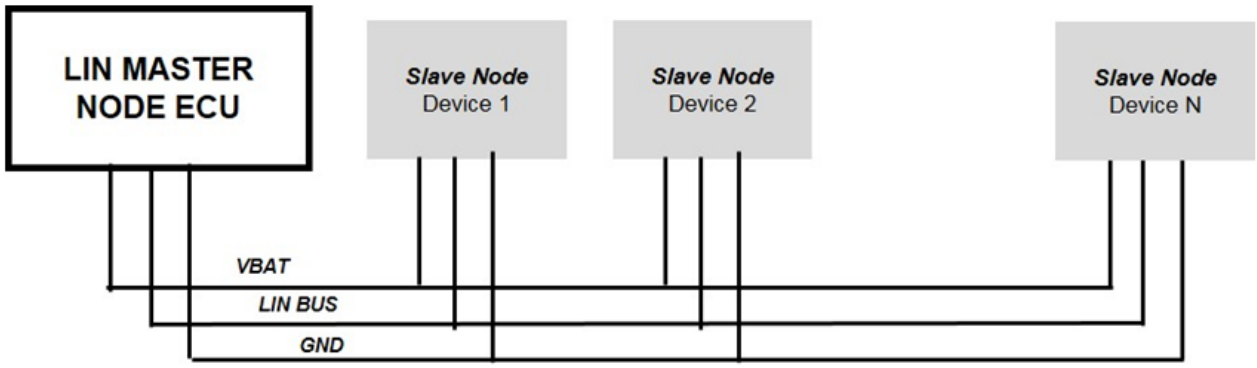


Figure 17. LIN bus topology

The LIN transmitter is a low-side MOSFET with current limitation and overcurrent transmitter shutdown. A selectable internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. To be used as a master node, an external resistor of 1 kΩ in series with a diode must be placed in parallel between VBAT [Battery Voltage] and the LIN Bus line. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions.

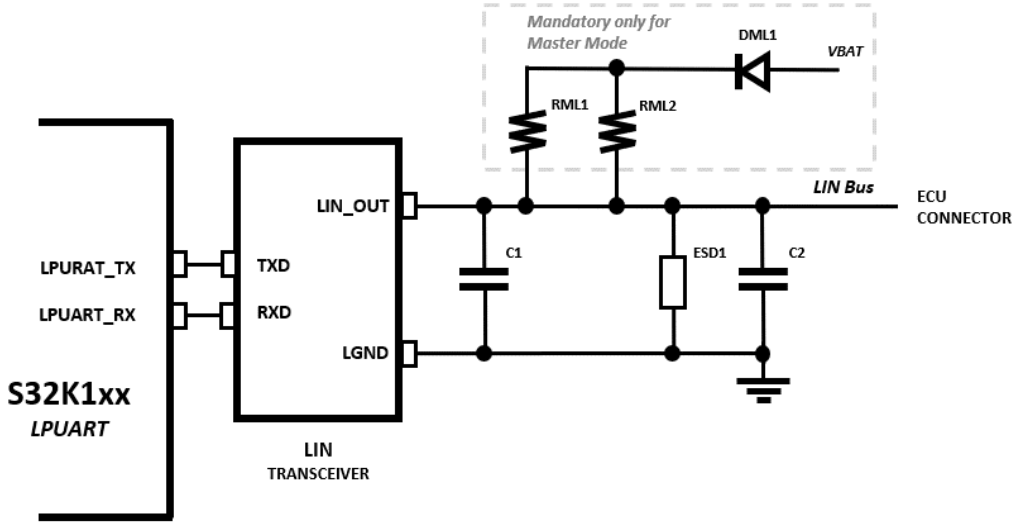


Figure 18. Circuit diagram for LIN interface

6.1.1 LIN components data

Table 10. LIN components

Reference	Part	Mounting	Remark
DMLIN	Diode	Mandatory only for master ECU	Reverse Polarity protection from LIN to VSUP.
RML1 and RML2	Resistor: 2 kΩ Power Loss: 250 mW Tolerance: 1% Package Size: 1206 Requirement: Min Power rating of the complete master termination has to be ≥ 500 mW	Mandatory only for Master ECU	For Master ECU If more than 2 resistors are used in parallel, the values have to be chosen in a way that the overall resistance RM of 1 kΩ and the minimum power loss of the complete master termination has to be fulfilled. For Slave ECU RMLIN1 and RMLIN2 are not needed on the PCB layout
C1	Capacitor: Slave ECU: typically 220 pF Master ECU: from 560 pF up to approximately ten times that value in the slave node	Mandatory	The value of the master node has to be chosen in a way that the LIN specification is fulfilled.

Table continues on the next page...

Table 10. LIN components (continued)

Reference	Part	Mounting	Remark
	[CSLAVE], so that the total line capacitance is less dependent on the number of slave nodes. Tolerance: 10% Package Size: 0805 Voltage: ≥50 V		
C2	Capacitor: Package Size: 0805	Optional	Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.
ESD1	ESD Protection Package Size: 0603-0805	Optional	Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

6.2 CAN interface for FlexCAN module

The physical layer characteristics for CAN are specified in ISO-11898-2. This standard specifies the use of cable comprising parallel wires with an impedance of nominally 120 Ω (95 Ω as minimum and 140 Ω as maximum). The use of shielded twisted pair cables is generally necessary for electromagnetic compatibility (EMC) reasons, although ISO-11898-2 also allows for unshielded cable. A maximum line length of 40 meters is specified for CAN at a data rate of 1 Mb. However, at lower data rates, potentially much longer lines are possible. ISO-11898-2 specifies a line topology, with individual nodes connected using short stubs.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations. A typical CAN system with an S32K1xx microcontroller is shown in Figure 19

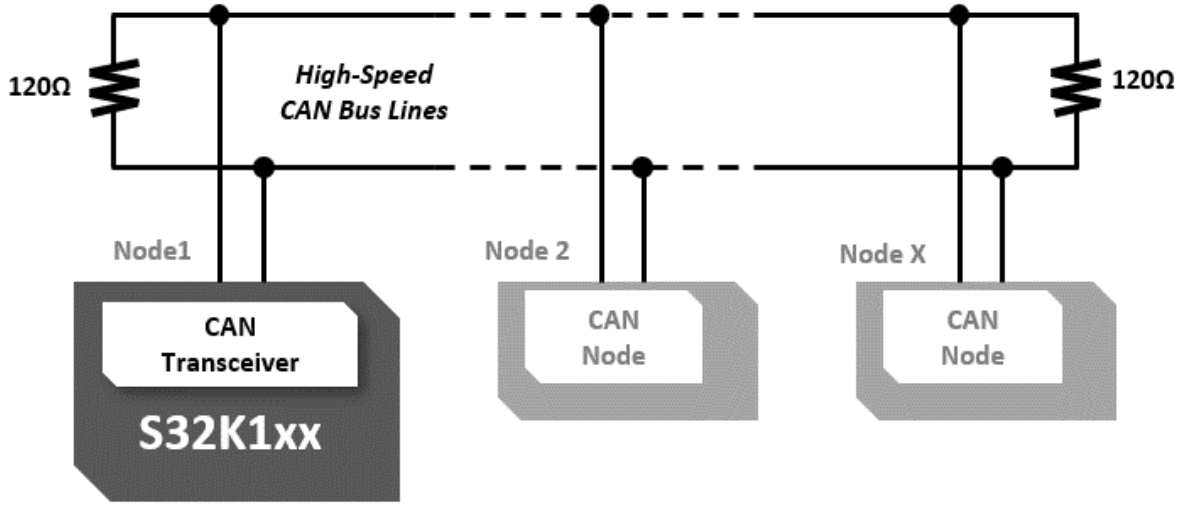


Figure 19. CAN system

The FlexCAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads up to 64 bytes transferred at faster rates up to 8 Mbps. The message buffers are stored in an embedded RAM dedicated to the FlexCAN module. See the chip configuration details in the Reference Manual for the number of message buffers configured in the chip.

Like most others CAN physical transceivers, the CANH, CANL and SPLIT pins are available for the designer to terminate bus depending on the application. The Figure 20 and Figure 21 show examples of the CAN node terminations.

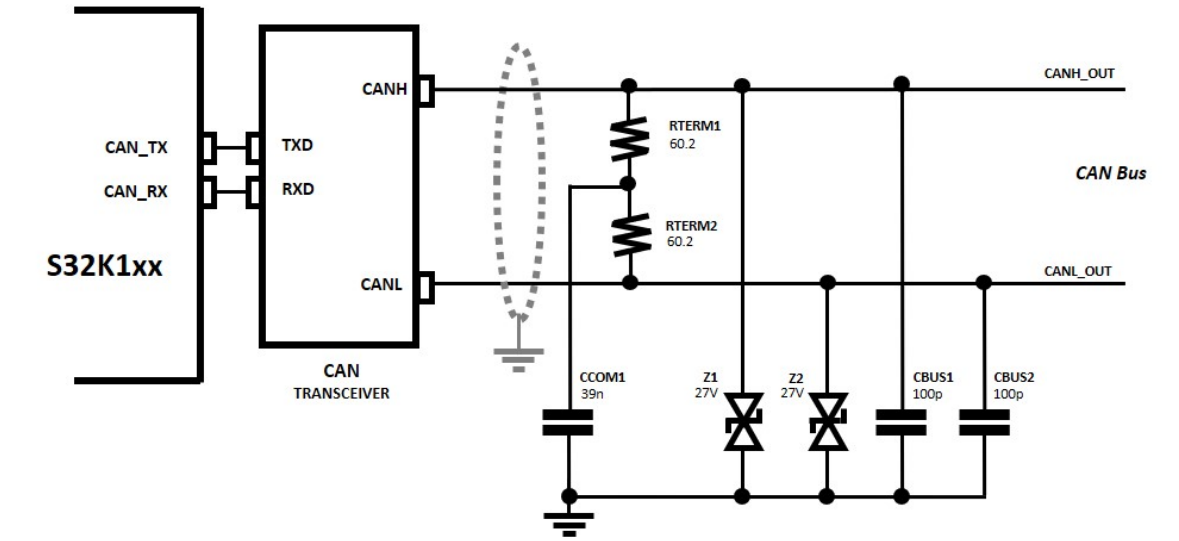


Figure 20. CAN physical transceiver circuit

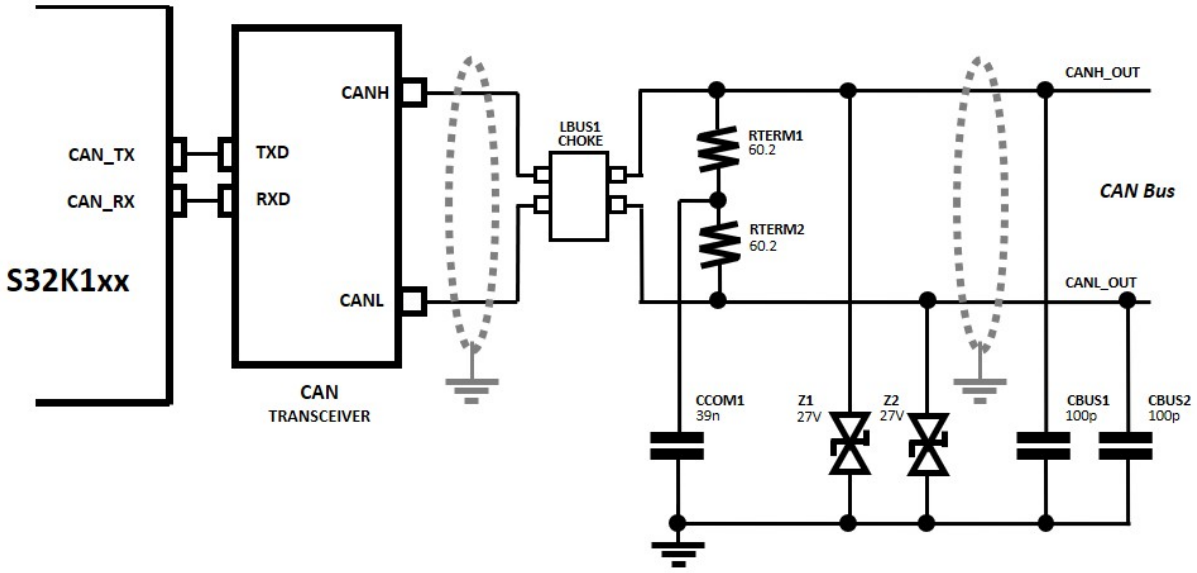


Figure 21. CAN physical transceiver circuit with common mode choke

6.2.1 CAN components data

Table 11. CAN components

Reference	Description
	Denotes a guard track next to a high/medium speed track. Guard tracks are connected such that each end of the track is connected to ground. A guard track should be connected to the ground plane at least every 500 mils. Spacing from any protected conductor and the guard track must not exceed 20 mils.
CBUS1 and CBUS2	The Capacitors CBUS1 and CBUS2 are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300 pF total. If zener stacks are also needed, the parasitic capacitance of the zener stacks must also be included in the total capacitance budget.
Z1 and Z2	The zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.
RTERM1, **RTERM2 and CCOM1**	Depending on the position of the node within the CAN network it might need a specific termination. RTERM1, RTERM2 and CCOM1 must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus

Table continues on the next page...

Table 11. CAN components (continued)

Reference	Description
	do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks. The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.
LBUS1–Common mode choke	A common mode choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins can greatly reduce coupled electromagnetic noise, and high-frequency transients. LBUS1 is not specifically required.

6.2.2 CAN termination

In a transmission line, there are two current paths, one to carry the currents from the driver to the receiver and another to provide the return path back to the driver. In the CAN transmission lines is more complex because there are two signals that are sharing a common termination as well as a ground return path. For reliable CAN communications, it is essential that the reflections in the transmission line be kept as small as possible. This can only be done by proper cable termination. Figure 22 and Figure 23 demonstrates two CAN termination schemes.

Reflections happen very quickly during and just after signal transitions. On a long line, the reflections are more likely to continue long enough to cause the receiver to misread logic levels. On short lines, the reflections occur much sooner and have no effect on the received logic levels.

6.2.2.1 Parallel termination

In CAN applications, both ends of the bus must be terminated because any node on the bus may transmit/receive data. Each end of the link has a termination resistor equal to the characteristic impedance of the cable, although the recommended value for the termination resistors is nominally 120 Ω (100 Ω as minimum and 130 Ω as maximum).

There should be no more than two terminating resistors in the network, regardless of how many nodes are connected, because additional terminations place extra load on the drivers. ISO-11898-2 recommends not integrating a terminating resistor into a node, but rather attaching standalone termination resistors at the furthest ends of the bus. This is to avoid a loss of a termination resistor if a node containing that resistor is disconnected. The concept also applies to avoiding the connection of more than two termination resistors to the bus, or locating termination resistors at other points in the bus rather than at the two ends.

Figure 22. d CAN Bus - parallel termination

6.2.2.2 Parallel termination with common-mode filtering

To further enhance signal quality, split the terminating resistors at each end in two and place a filter capacitor, CSPLIT, between the two resistors. This filters unwanted high frequency noise from the bus lines and reduces common-mode emissions.

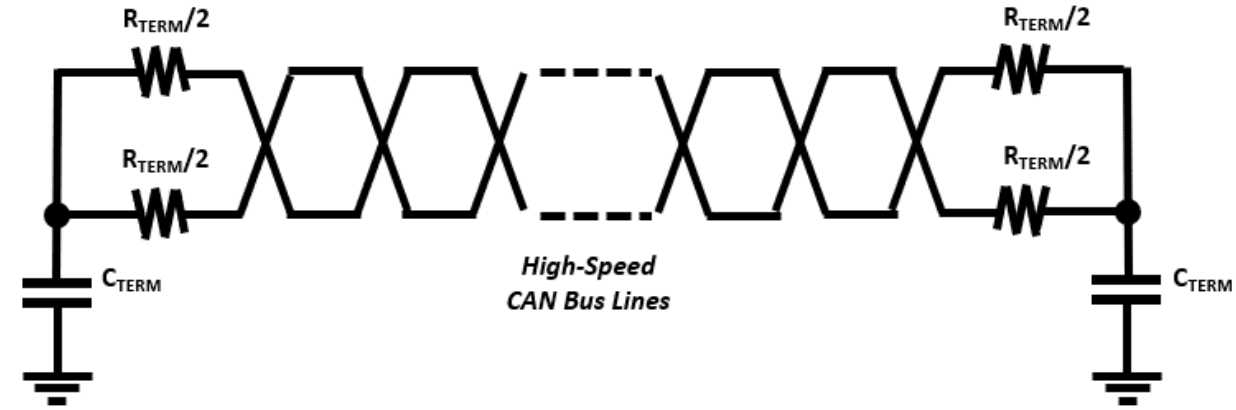


Figure 23. CAN Bus – parallel transmission with common-mode filtering

6.3 Ethernet MAC Interface

MII/RMII Interface signal can be directly routed to the MAC-NET interface, however series termination resistors may be considerate on RXCLK, TXCLK and all RX/TX signals for EMI suppression. MII/RMII series termination should be placed within 100 of the Ethernet Physical Interface and routed to an uninterrupted reference plane. 33-50 Ohms series termination resistors have been to be good recommended value for improving EMI.

Although RMII and MII are synchronous bus architectures, there are a number of factors limiting signal trace lengths. With a longer trace, the signal becomes more attenuated at the destination and thus more susceptible to noise interference. Longer traces also act as antennas, and if run on the surface layer, can increase EMI radiation. If a long trace is running near and adjacent to a noisy signal, the unwanted signals could be coupled in as cross talk. It is recommended to keep the signal trace lengths as short as possible. Ideally, keep the traces under 6 inches. Trace length matching, to within 2.0 inches on the MII or RMII bus is also recommended. Significant differences in the trace lengths can cause data timing issues. Minimize the use of vias throughout the design. Vias add capacitance to signal traces. As with any high-speed data signal, good design practices dictate that impedance should be maintained and stubs should be avoided throughout the entire data path.

MII signaling: Figure 24 shows the PHY-MAC and MAC-MAC connections in an MII interface. Data is exchanged via 4-bit wide data nibbles TXD[3:0] and RXD[3:0]. Data transmission is synchronous with the transmit (TX_CLK) and receive (RX_CLK) clocks. For the PHY-MAC interface, both clock signals are provided by the PHY and are typically derived from an external crystal running at a nominal 25 MHz or from the CLK_OUT signal on the switch. When the Ethernet Switch is configured for MAC-MAC communication, the switch provides the clocks and acts like a PHY.

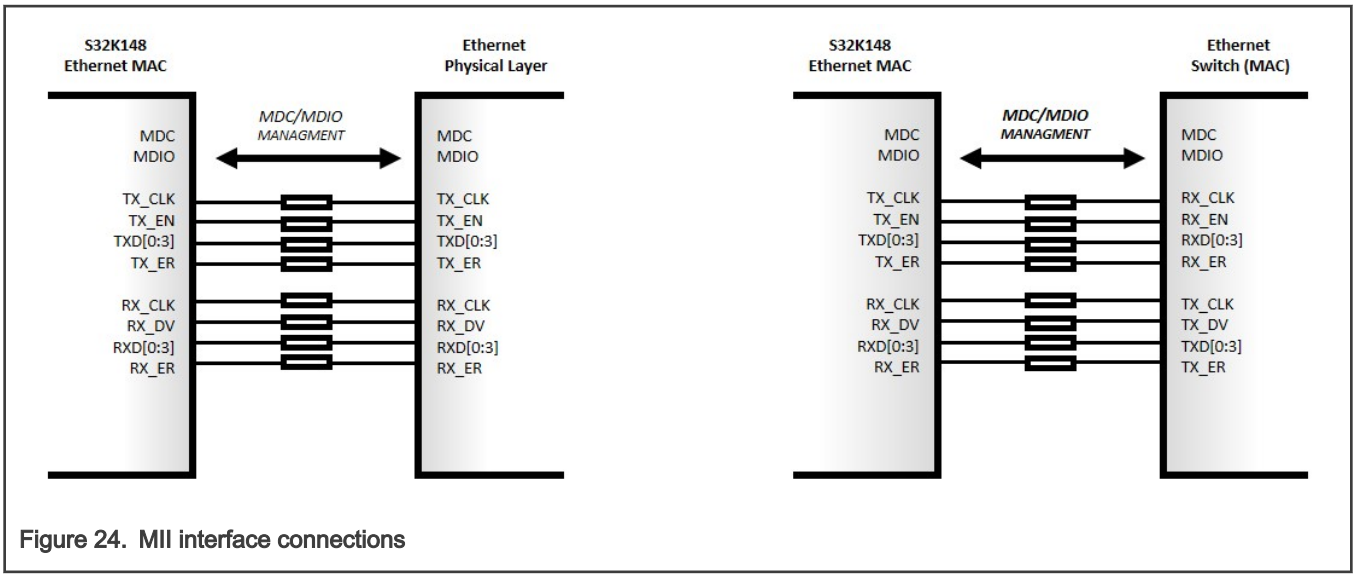


Figure 24. MII interface connections

RMII signaling: RMII data is exchanged via 2-bit data signals TXD[1:0] and RXD[1:0] as shown in Figure 25. Transmit and receive signals are synchronous with the shared reference clock, REF_CLK.

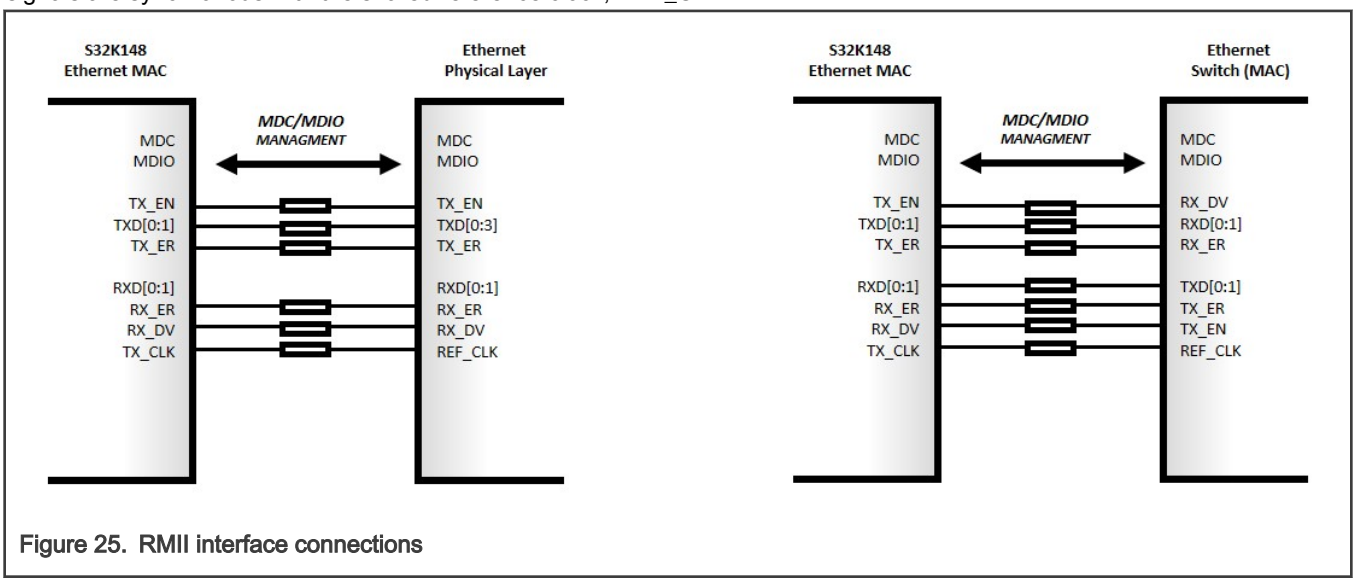


Figure 25. RMII interface connections

7 Quad Serial Peripheral Interface

S32K1xx has one instance of QuadSPI. The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to external serial flash device. It supports SDR and HyperRAM modes upto 4 and 8 bidirectional data lines respectively. The QuadSPI supports an A-side and a B-side. The A-side of the QuadSPI is connected to the fast pads (80 mA) while the B-side connects to the 20 mA pads. See datasheet for operating values.

Only one external memory will be supported in any given application and it will not be permitted to run the A-side and the B-side of the QuadSPI simultaneously. As such the following external memory options can be supported:

- Single Quad Flash on the A-side

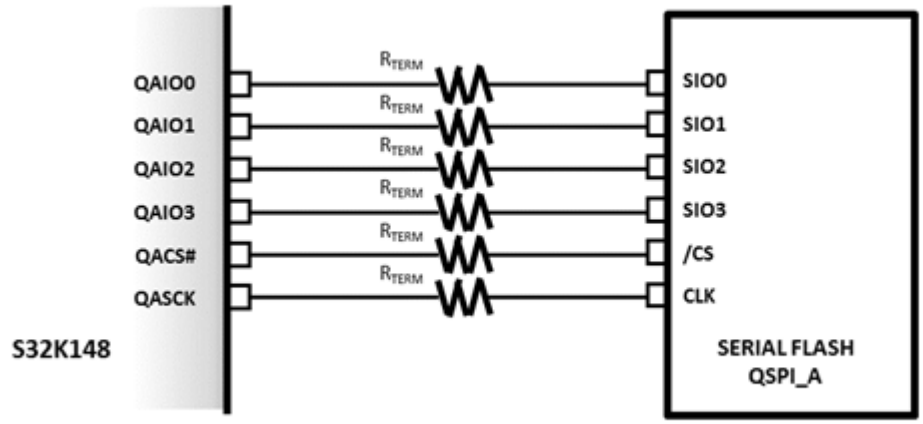


Figure 26. External memory option - Single Quad Flash on the A-side

- Single HyperRAM on the B-side

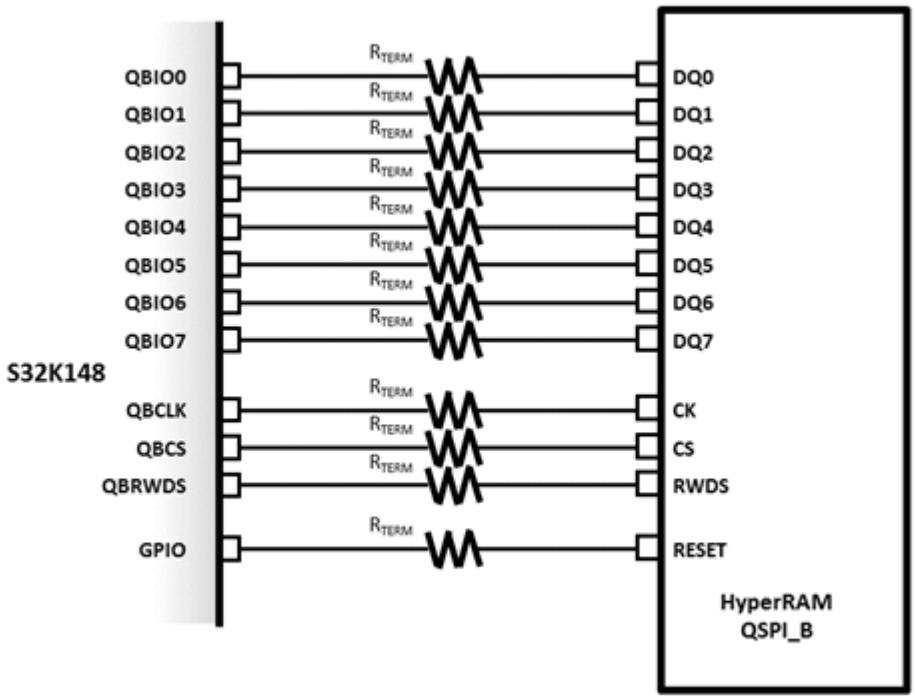


Figure 27. External memory option - Single HyperRAM on the B-side

- Single Quad Flash on the B-side.

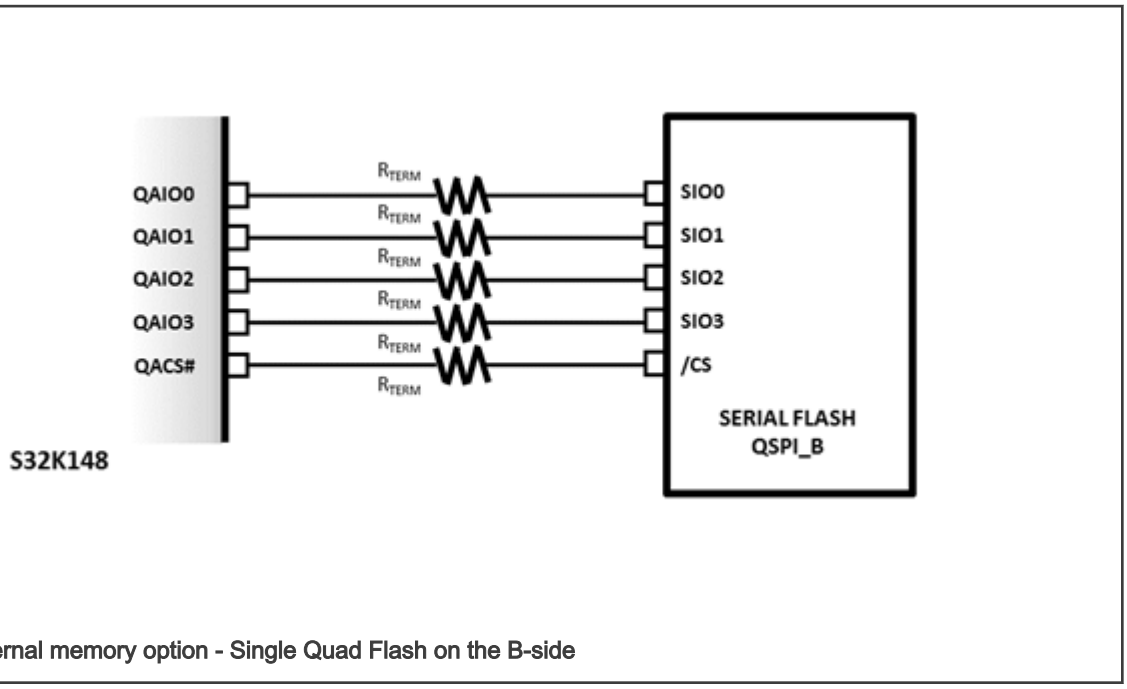


Figure 28. External memory option - Single Quad Flash on the B-side

Data and Clock Signal Termination: Clock generation and distribution becomes more difficult as the speed and performance of microprocessors increase to higher limits. Controlled and precise clocking distribution techniques are needed to maintain a synchronous system. Clock signal quality and skew are the two major problems with distributing clock signals. With higher frequencies, and the associated fast edge rates, long traces behave like transmission lines. Ring back, overshoot, and undershoot occur as a result of poor termination of transmission lines. They contribute to bad signal quality, false switching, and they can cause damage in extreme cases.

Given the effective output driver strength of 25-33 Ohms and the transmission line characteristic impedance of 50 Ohms, one should add the termination resistor close to the output driver, to minimize the reflection as shown below.

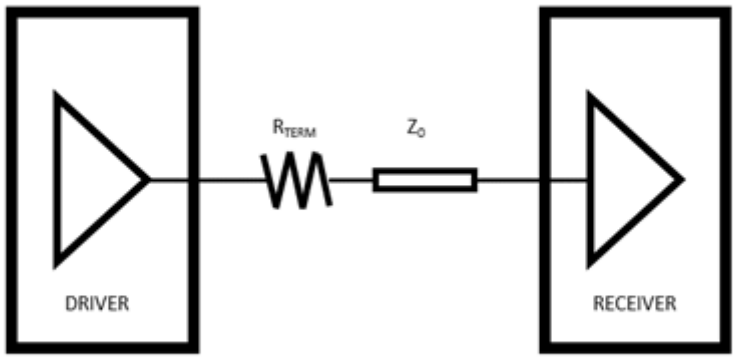


Figure 29. Point-To-Point transmission line

Data Signal Routing: In order to keep the correct timing for the data transfer from the Microcontroller to the IC Memory, the PCB data traces should be the same length and time delay as the clock trace from Microcontroller to the IC Memory. Data signals should be routed with controlled impedance traces to reduce signal reflections. Avoid routing traces with 90 ° angle corners. The recommendation is to cut the corner and smooth the trace when a trace route needs to change direction. To further improve the

signal integrity, avoid using multiple signal layers for data signal routing. All signal traces should have a continuous and solid reference plane, either GND or VDD.

Clock Signal Routing: In high speed synchronous data transfer, good signal integrity in a PCB design is of critical importance, especially for the clock signals, SCLK and DQS. When routing the clock signal, special cares should be taken. The following practices are recommended.

- Run the clock signal at least -w3w of the trace width away from all other signal traces. This helps keep the clock signal clean from crosstalk noise.
- Use as few via(s) as possible for the whole clock signal path. Vias cause impedance change and signal reflection.
- All signal traces should go with a solid reference plane, either GND or VCC.
- Run the clock trace as straight as possible and avoid using serpentine routing.
- Keep a continuous ground in the next layer as reference plane.
- Route the clock trace with controlled impedance.
- Keep the clock signal from disturbance or crosstalk by separating it from other signals by using wider spacing. Data bus should be routed with matching length to the reference of the clock. The matching length is recommended to be within ± 50 mils.

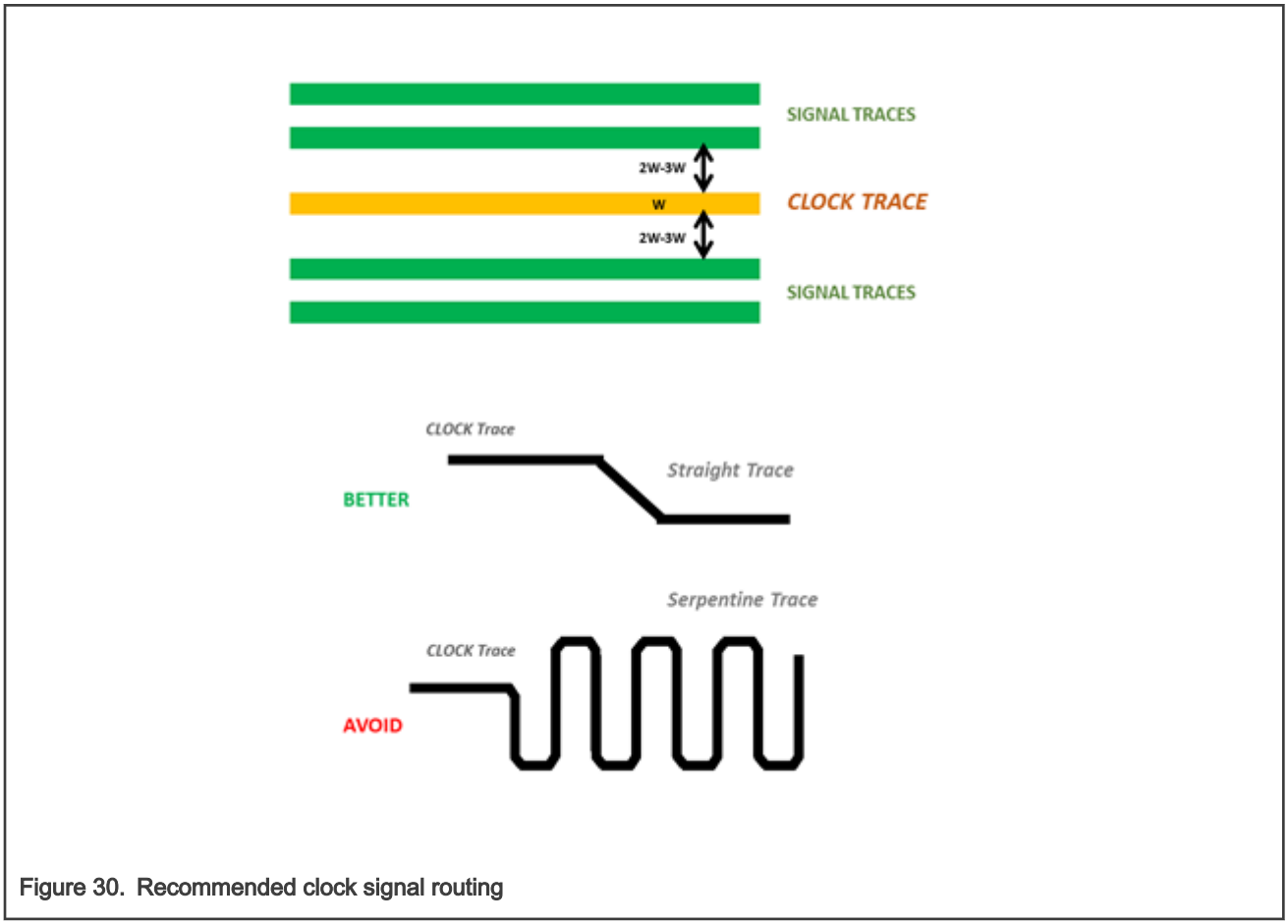


Figure 30. Recommended clock signal routing

8 Unused pins

The following table describes the options and configurations for the unused pins and the considerations for other modules and sections of the MCU.

Table 12. S32K1xx - Used pins configuration

Module	Pin Name	Function	Recommendation
GPIO	PTx[1]	ENETx	The unused pins should be left unconnected, or externally connected to VSS/GND.
		FTMx	
		FlexIOx	
		CANx	
		LPUARTx	
		LPI2Cx	
		ADCx	
		CMPx	
		Others	
	PTB6	XTAL	The pins with the XTAL and EXTAL functions should be left unconnected, or externally connected to VSS/GND.[2,3]
	PTB7	EXTAL	
JTAG	PTA4	JTAG_TMS/SWD_DIO	The pins with the JTAG function should be left unconnected. In order to increase debugger connection robustness, it is recommended to add external pull resistors in parallel to the internal weak pull-ups (TDI, TDO and TMS) or pull-down resistor (TCK). Refer to Debug and programing interface.
	PTA10	JTAG_TDO/SW_DO	
	PTC5	JTAG_TDI	
	PTC4	JTAG_TCK/SWD_CLK	
RESET	PTA5	PTA5/TCLK1/RESET_b	Reset pin should not be left unconnected. Refer to RESET system.
POWER	VDDx	VDD	No Power pin should be left unconnected. VDDx and VDDA/VREFH must be shorted together externally to a common reference on PCB. Appropriate decoupling capacitors to be used to filter noise on the supplies. Refer to Power supplies.

Table continues on the next page...

Table 12. S32K1xx - Used pins configuration (continued)

Module	Pin Name	Function	Recommendation
	VSSx	VSS	No Ground pin should be left unconnected. All VSSx and VREFL must be shorted together externally to a common GND.
• If the unused pin is connected to VSS/GND, and the pin is unintentionally configured to output with a high-logic state, then there could be a path that can increase current drastically and causes major damage in the MCU.			

1. Pins bonded and not bonded out.
2. For unused digital and analog pins, the pin function should be set to DISABLED by setting the corresponding
3. PORTx_PCRn[MUX] field to 0b000. The DISABLED function is default state for all pins not initialized. For pins with ADC functionality software should not trigger ADC channel conversion on the channel which is multiplexed with the unused pin. For pins with CMP functionality software should not enable CMP channel connected to the unused pin.

9 CAD/CAE schematic symbols and PCB footprints

Microcontroller symbols and footprints in a single are available at NXP for download in a vendor neutral BXL format which can then be exported to the leading EDA CAD/CAE design tools using the Ultra Librarian Free Reader.

Table 13. CAD/CAE schematic symbols and PCB footprints

CAD/EDA schematic symbols formats	CAD PCB footprints formats
• Altium PCAD (importable by Altium Designer) • Cadence Allegro DE HDL (Concept) • Cadence Orcad Capture • Eagle • Mentor DxDesigner • Mentor Design Capture • Mentor Design Architect • Mentor PowerLogic • Target 3001 • Zuken Cadstar	• Altium PCAD (importable by Altium Designer) • Cadence Orcad Layout • Cadence Orcad PCB Editor • Cadence Allegro • Eagle • Mentor Boardstation • Mentor PowerPCB (PADS) • Mentor Expedition • Target 3001 • Zuken Cadstar

10 General board layout guidelines

10.1 Traces recommendations

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in Figure 31.

Figure 31. Poor and correct way of bending traces in right angles

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other.

Complex boards need to use vias while routing; you have to be careful when using them. These add additional capacitance and inductance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace.

10.2 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

- Route high-speed signals above a solid and unbroken ground plane.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.
- There should be no floating metal/shape of any kind near any area close to the microcontroller pins. Fill copper in the unused area of signal planes and connect these coppers to the ground plane through vias.

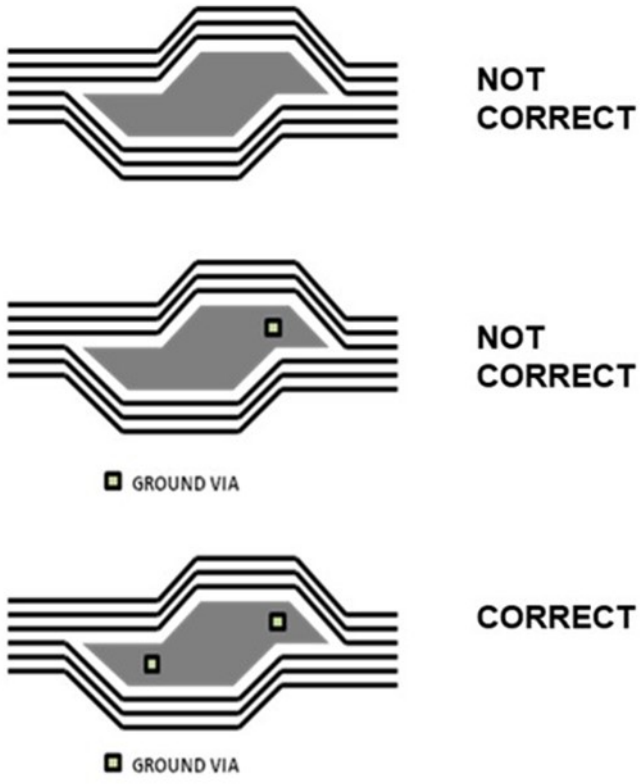
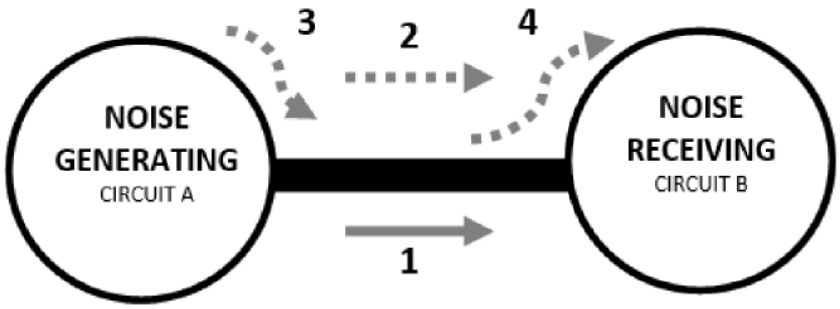


Figure 32. Eliminating floating metal/shape

10.3 EMI/EMC and ESD considerations for layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.

This application note does not go into the electromagnetic theory or explain the whys of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: Conduction and Radiation.



	Propagation path
1	Conductor
2	Air
3	Air to Conductor
4	Conductor to Air

Figure 33. Electromagnetic noise propagation

The design considerations narrow down to:

- The radiated & conducted EMI from the board should be lower than the allowed levels by the standards you are following.
- The ability of the board to operate successfully counteracting the radiated & conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for a system consists of several components such as PCB, connectors, cables and so on. The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses and PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test. This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.

However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

11 PCB layer stacking

To reach signal integrity and performance requirements, at minimum a four-layer PCB is recommended for implementing Ethernet applications and systems. The following layer stack-ups are recommended for four, six, and eight-layer boards, although other options are possible.

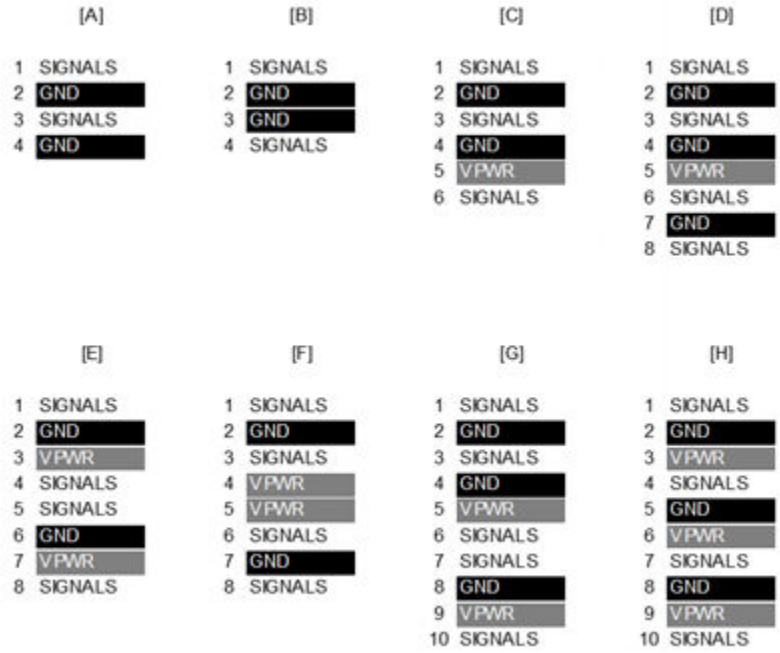


Figure 34. Recommended PCB layer stack-up

12 Injection current

All pins implement protection diodes that protect against electrostatic discharge (ESD). These internal ESD diodes of the microcontroller are designed just for short discharge pulses only, and these do not sustain a constant current over time. Therefore, the maximum continuous voltage that drops over them is specified in the DC electrical parameters and the maximum high input voltage should not be higher than VDDx + 0.3 V, and the current injection also should be limited as defined in the device datasheet. In other words, the voltage and current of an input signal must be within the electrical parameter allowed. The outcome of violating these specifications causes unexpected behavior, stuck operation or damage in the MCU.

When the MCU is in an unpowered state, current injected through the chip pins may bias internal chip structures (for example, ESD diodes) and incorrectly power up these internal structures through inadvertent paths. The presence of such residual voltage may influence different chip-internal blocks in an unpredictable manner and may ultimately result in unpredictable chip behavior (for example, POR flag not set). Once in the illegal state, powering up the chip further and then applying reset will clear the illegal state. Injection current specified for the chip under the aspect of absolute maximum ratings represent the capability of the internal circuitry to withstand such condition without causing physical damage.

For more reference see AN4731.

13 References

- Crystal Oscillator Troubleshooting Guide - NXP Semiconductors
- AN2049 Some Characteristics and Design Notes for Crystal Feedback ...
- AN10853 ESD and EMC sensitivity of IC - NXP Semiconductors

- AN2321: Designing for Board Level Electromagnetic Compatibility - NXP Semiconductors
- AN10897 A guide to designing for ESD and EMC

14 Revision history

Table 14. Sample revision history

Revision number	Date	Substantive changes
0	03/2017	Initial release
1	06/2017	1. In #unique_2/ unique_2_Connect_42_TABLE_YJM_2YD_CZ Footnote is added in the table 2. In Clock circuitry the value of Fast internal reference clock is changed to 48MHz from 48-60MHz and value of External square wave input clock changed to 50 MHz from 60 MHz 3. In #unique_8/ unique_8_Connect_42_TABLE_WGL_5ZD_CZ deleted the line (if not .....by MCU) 4. External pin RESET changed from When the RESET..... drain output to The RESET pin.....output stage 5. In Power system #unique_37 updated. 6. In Clock circuitry When using the external oscillator....the frequency range of the external oscillator should be 4–40 MHz changed to 8–40 MHz 7. New chapter Analog comparator interface added
2	02/2018	1. Updated the table #unique_2/ unique_2_Connect_42_TABLE_YJM_2YD_CZ. 2. Added the following sections Quad Serial Peripheral Interface, Injection current, PCB layer stacking, Ethernet MAC Interface
3	12/2018	1. Updated #unique_2/ unique_2_Connect_42_FIG_O2X_ZXD_CZ 2. In Debug and programing interface removed the text " Usually, MCUs do not include pull-up or pull-down resistors on JTAG/SWD pins". 3. In External pin RESET removed the paragraph "In prototype designs.....330 pF are recommended" and added "The reset line has an .....pull-up resistor value" and "Despite a capacitor in.....detected for the MCU".

Table continues on the next page...

Table 14. Sample revision history (continued)

Revision number	Date	Substantive changes
		4. Removed the column "Required pull-up / pulldown" from #unique_8/ unique_8_Connect_42_TABLE_W1D_VLQ_DGB. 5. In External pin RESET removed the figure "RESET circuit". 6. Updated Unused pins and added a note.
4	09/2019	1. Added text "In the S32K1xx.....or damage in the MCU" in Power system. 2. Updated the Figure 9. 3. Removed the last paragraph in Debug and programing interface. 4. Removed the text "On this device, RESET.....device from any mode" in External pin RESET. 5. Updated the test from "The reset line has.....pull-up resistor value" to "The reset pin.....current allowed int he pin" in External pin RESET. 6. Added a table and removed the text in Unused pins. 7. Added CAD/CAE schematic symbols and PCB footprints. 8. Completely updated Injection current. 9. Updated #unique_27/ unique_27_Connect_42_TABLE_LDW_4L4_2JB. 10. Removed the figure General windowed timing diagram from Analog comparator interface. 11. Updated #unique_8/ unique_8_Connect_42_TABLE_W1D_VLQ_DGB and added JTAG/SWD signal connections. 12. Added two new bullets in Suggestions for the PCB layout of oscillator circuit. 13. Renamed section from "VDD power supply ramp rate" to "MCU Power supply ramp rate" and moved the figure from section "Bulk and decoupling capacitors".

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