variables entrada Clk : 1 bitdatain: 8 bits Inicio enable: 1 bits reset: 1bitcs=1run=0done=0variables salida ${\rm countd}{=}0$ dataout: 8 bits datare[7:0]=0datase[7:0] = datainNO enable=1SIrun=1 cs=0datase[7] = mosiNO $\operatorname{sclk} \downarrow$ SIdatare=miso,datare[7:1] mosi=datase[7] ${\rm datare}{>}1$ countd = countd + 1 ${\rm datase}{<}1$ countd=7 NO SIrun=0done=1datare[7:0] = dataoutSI ${\rm countd}{=}0$ NO reset=1SI