+12V

R1
10k

R2
200k

Adds DC offset of +6V
(virtual ground)

+6V

R3
1M

GND

C1
47n

Source of the noise
by avalanche effect

(400mVpp)

Q2
2N3904

Q1
2N3904

GND

3
+
2
−
1

11

LM324
U1.1

4

+12V

Voltage follower

C2
47n

R4
10k

+6V

R6
1M

12
+
13
−
14

LM324
U1.4

R5
47k

(1.9Vpp)

Summing amplifier
with virtual ground
Gain = 4.7

+6V

10
+
9
−
8

LM324
U1.3

Comparator to generate
a square pulse.

(10.5V)

R7
10k

(5.1V)

R8
10k

GND

D1
BZX85C5V1

GND

Monostable Timer
T = 5.2ms

U2
NE555P

GND

1 GND   VCC 8 +5V
2 TRIG   DISCH 7
3 OUT   THRES 6
4 RESET CONT 5

+5V

RPG

+5V

R11
47k

C5
0.1u

GND

R9
1M

+12V

C3
4.7u

R10
1M

5
+
6
−
7

LM324
U1.2

+6V

C4
0.1u

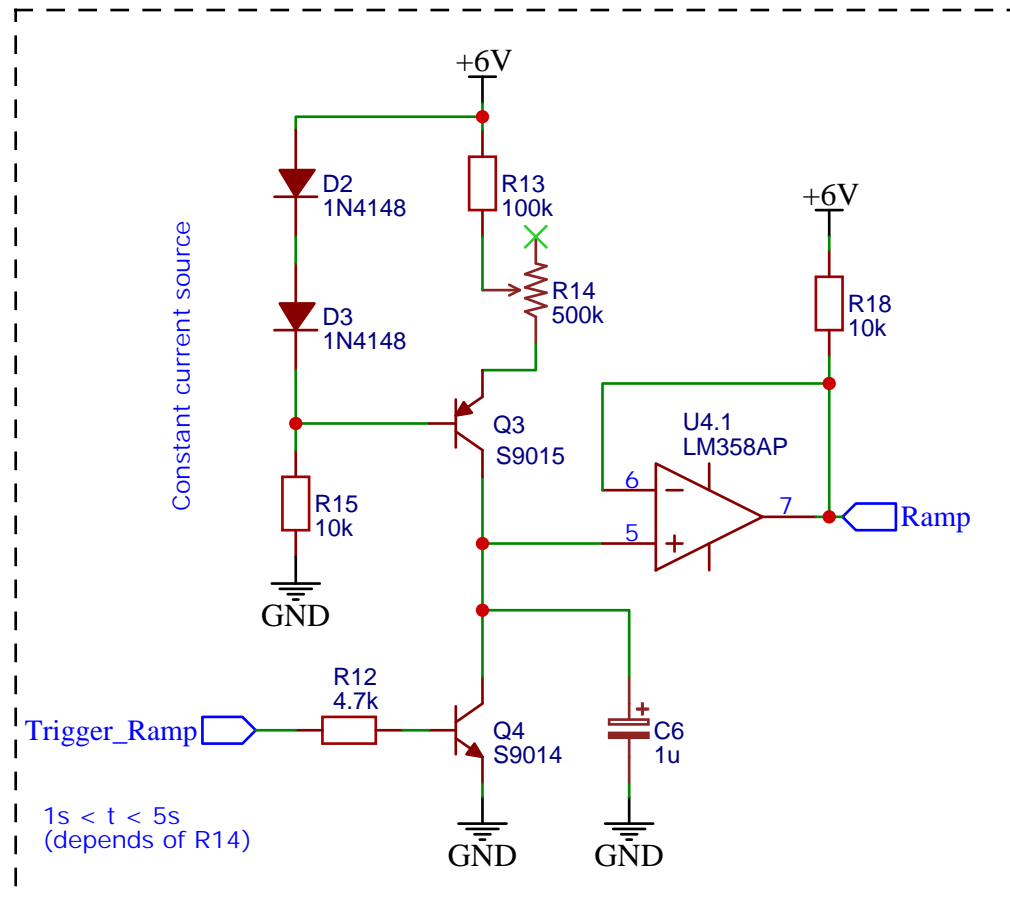Virtual ground

GND   GND   GND

This circuit will generate a random sequence of 5ms square pulses.
The trimmer R2 controls the ammount of random pulses it is generated.
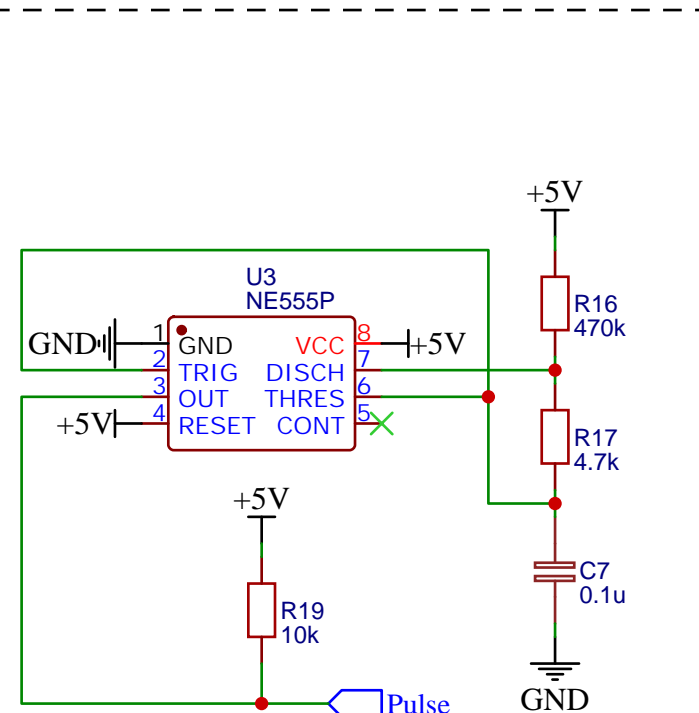
TITLE:
Noise Source (Layer D)

REV: 1.0

EasyEDA   Company: @dabecart   Sheet: 1/1
Date: 2024-09-29   Drawn By: @dabecart

Ramp Generator

Constant current source

+6V

D2
1N4148

D3
1N4148

R13
100k

R14
500k

R15
10k

GND

Q3
S9015

U4.1
LM358AP

6 −
5 +
7 → Ramp

+6V

R18
10k

Trigger_Ramp

R12
4.7k

Q4
S9014

C6
1u

GND   GND

1s < t < 5s
(depends of R14)

Creates a rising ramp on a falling edge.
The rise time is calculated as: t = (R13+R14)*C6*Vcc/0.7
This will be the modulating signal to control the duty cycle
of the output PWM.

Pulse generator

U3
NE555P

GND   1 GND   VCC 8   +5V
2 TRIG   DISCH 7
3 OUT   THRES 6
+5V   4 RESET   CONT 5

+5V

R16
470k

R17
4.7k

C7
0.1u

GND

+5V

R19
10k

Pulse

f = 30.04 Hz
DC = 0.0098
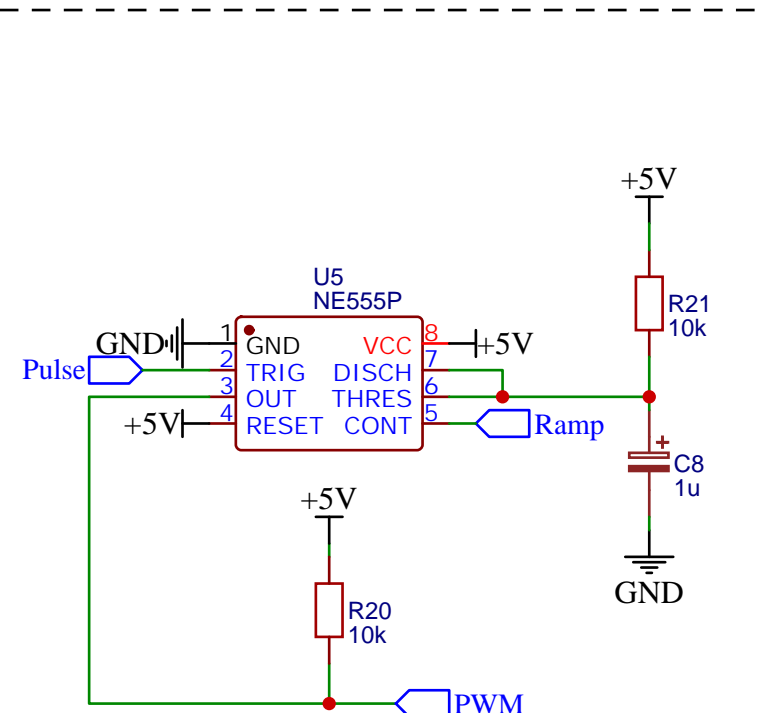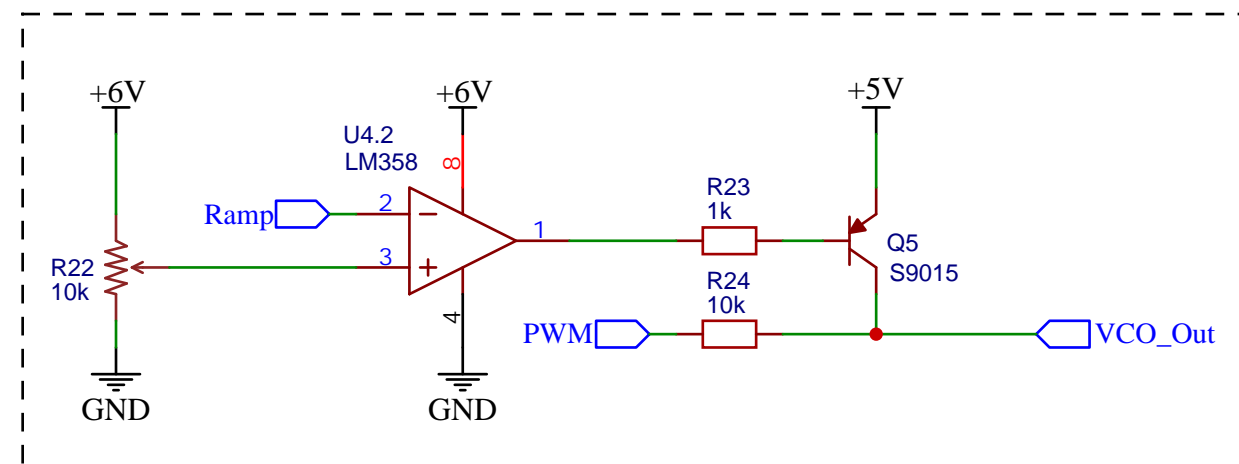
Astable multivibrator with a very low duty cycle.
Gives the frequency of the output PWM.
Frequency: f=1.44/[(R16+2R17)C7]
Duty cycle: DC=Rb/(R16+2R17)

Modulator

U5
NE555P

GND   1 GND   VCC 8   +5V
Pulse   2 TRIG   DISCH 7
3 OUT   THRES 6
+5V   4 RESET   CONT 5 → Ramp

+5V

R21
10k

C8
1u

GND

+5V

R20
10k

PWM

Converts the pulse input into a PWM with its duty cycle
controlled by a modulating signal. In this case, the output
of the ramp generator.
If T is the pulse period, then: R21*C8=T/4
The output DC is directly proportional to the ramp input.

Output saturation

+6V

R22
10k

Ramp

U4.2
LM358

8
2 −
3 +
1
4

+6V

GND

R23
1k

Q5
S9015

R24
10k

PWM

+5V

VCO_Out

GND

The modulator is incapable of fully generating a duty cycle of 0% or 100%, therefore this stage
pulls high the VCO when the ramp is in its idle voltage (HIGH too). R22 will have to be adjusted
so the normal output of this stage is +5V.

These circuits are used to create a PWM signal whose duty cycle will normally be 100%.
When the tilt switch is triggered, it will make the duty cycle of the PWM fall to almost
0% and then raise slowly when no shaking is applied to the dice.
This PWM will be ANDed to the PWM so that the number stop increasing slowly, but still
randomnly until they eventually stop. In other words, when the PWM's DC is 0% (almost) all
random pulses will be passed to the counter. When the DC starts raising, less pulses will
get through simulating a slow down of the dice, similar to a roullete.

TITLE: VCO (Layer D)
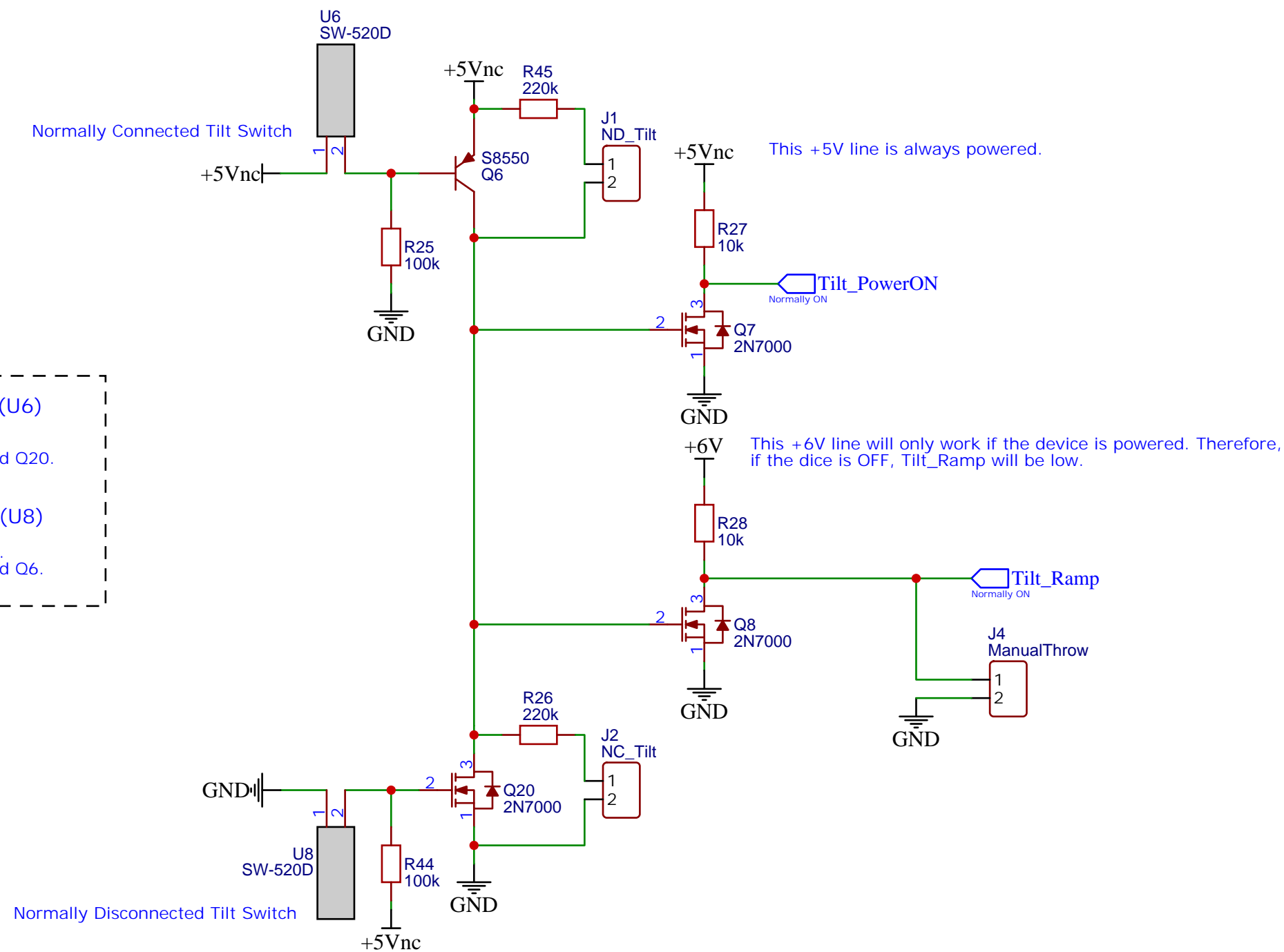
REV: 1.0

Company: @dabecart

Date: 2024-09-29   Drawn By: @dabecart

Sheet: 1/1

EasyEDA

U6
SW-520D

Normally Connected Tilt Switch

+5Vnc

+5Vnc

R45
220k

J1
ND_Tilt

S8550
Q6

R25
100k

GND

+5Vnc

R27
10k

This +5V line is always powered.

Tilt_PowerON
Normally ON

Q7
2N7000

GND

+6V

This +6V line will only work if the device is powered. Therefore, if the dice is OFF, Tilt_Ramp will be low.

R28
10k

Tilt_Ramp
Normally ON

Q8
2N7000
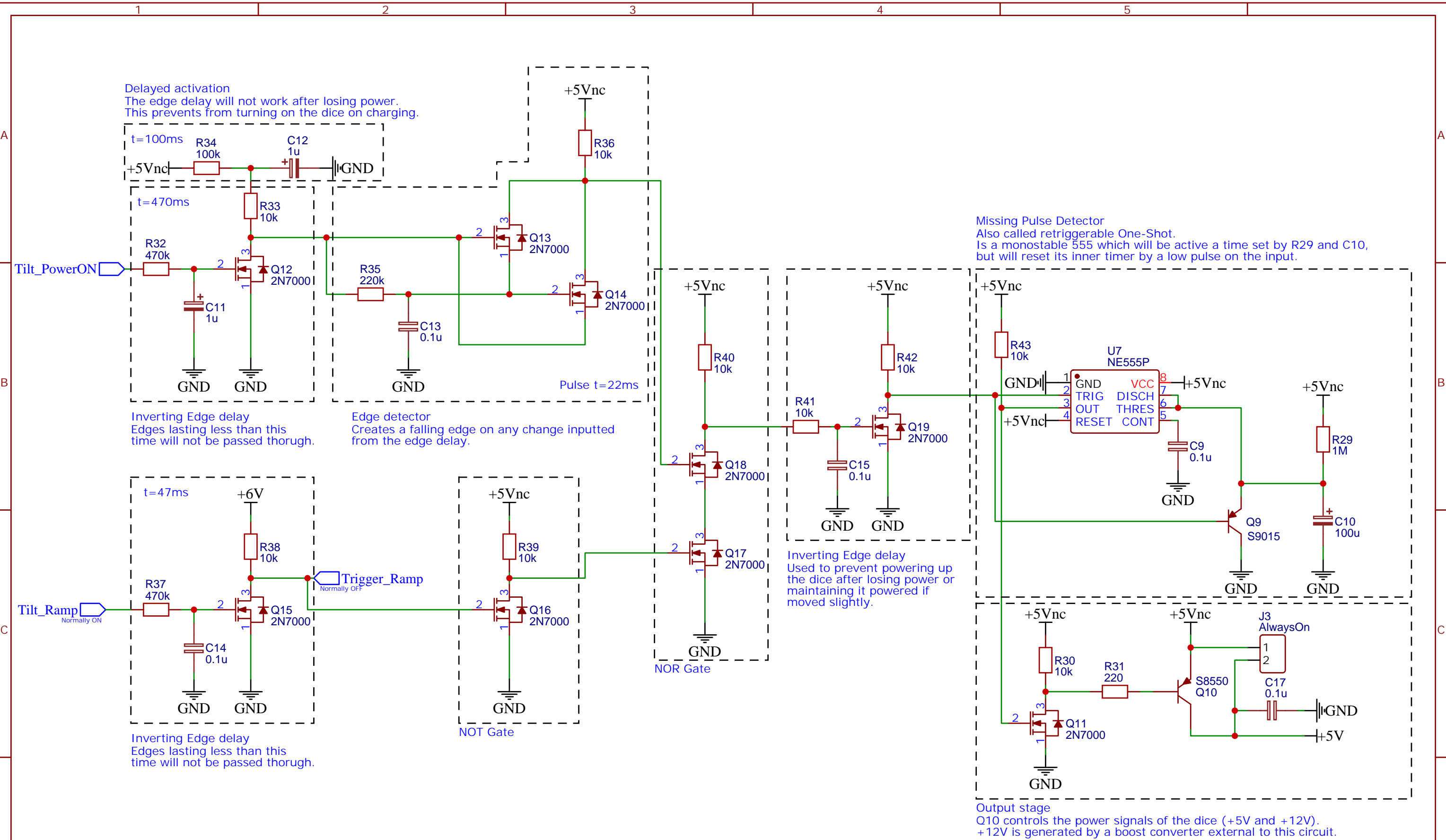
GND

J4
ManualThrow

GND

Using a NC Tilt Switch (U6)
- Shortcircuit J2.
- Put U6, R25, R26 and Q6.
- Don't put U8, R44, R45 and Q20.

Using a ND Tilt Switch (U8)
- Shortcircuit J1.
- Put U8, R44, R45 and Q20.
- Don't put U6, R25, R26 and Q6.

R26
220k

J2
NC_Tilt

GND

Q20
2N7000

GND

U8
SW-520D

R44
100k

Normally Disconnected Tilt Switch

+5Vnc

The tilt switch is a normally closed element. For this circuit we need something that is normally open.
This simple circuit achieves just that.
It generates two triggers (which are normally HIGH): the PowerOn is used to wake up the dice, the tilt
ramp trigger is used to generate the ramp, which basically emulates throwing the dice.
Both these triggers should maintain the dice powered son on "PowerManager" these signals are filtered
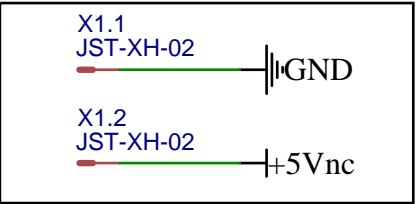and joined.

TITLE:
Tilt Switch (Layer D)

REV: 1.0

Company: @dabecart

Sheet: 1/1

Date: 2024-09-29   Drawn By: @dabecart

EasyEDA

Delayed activation
The edge delay will not work after losing power.
This prevents from turning on the dice on charging.

t=100ms

R34 100k   C12 1u   GND

t=470ms

R33 10k

R32 470k   Tilt_PowerON   Q12 2N7000   C11 1u   GND   GND

Inverting Edge delay
Edges lasting less than this time will not be passed thorough.

R35 220k   Q13 2N7000   C13 0.1u   Q14 2N7000   GND

Edge detector
Creates a falling edge on any change inputted from the edge delay.

+5Vnc   R36 10k

Pulse t=22ms

t=47ms   +6V

R38 10k   Trigger_Ramp (Normally OFF)

R37 470k   Tilt_Ramp (Normally ON)   Q15 2N7000   C14 0.1u   GND   GND

Inverting Edge delay
Edges lasting less than this time will not be passed thorough.

+5Vnc   R39 10k   Q16 2N7000   GND

NOT Gate

+5Vnc   R40 10k   Q18 2N7000   Q17 2N7000   GND

NOR Gate

+5Vnc   R42 10k   R41 10k   Q19 2N7000   C15 0.1u   GND   GND

Inverting Edge delay
Used to prevent powering up the dice after losing power or maintaining it powered if moved slightly.

Missing Pulse Detector
Also called retriggerable One-Shot.
Is a monostable 555 which will be active a time set by R29 and C10, but will reset its inner timer by a low pulse on the input.

+5Vnc   R43 10k

U7 NE555P
1 GND	VCC 8	+5Vnc
2 TRIG	DISCH 7
3 OUT	THRES 6
4 RESET	CONT 5

GND   +5Vnc   C9 0.1u   GND

+5Vnc   R29 1M   Q9 S9015   C10 100u   GND   GND

+5Vnc   R30 10k   R31 220   S8550 Q10   J3 AlwaysOn   1 2   C17 0.1u   GND   +5V

Q11 2N7000   GND

Output stage
Q10 controls the power signals of the dice (+5V and +12V).
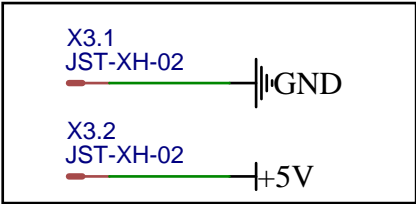+12V is generated by a boost converter external to this circuit.

The inputs to this circuit are the triggers from the tilt sensor. It takes care to filter both triggers so that their timing is consistent and prevents the dice from booting up if it looses power and then gains it, for example, when charging it.
The dice will be turned ON when it's tilted for over a certain threshold time, set by R32 and C11.
The dice will be "thrown" whenever an edge of more than a certain threshold time set by R37 and C14 is detected.
On either case, all triggers that match criteria will keep the dice on for a time set by R29 and C10.
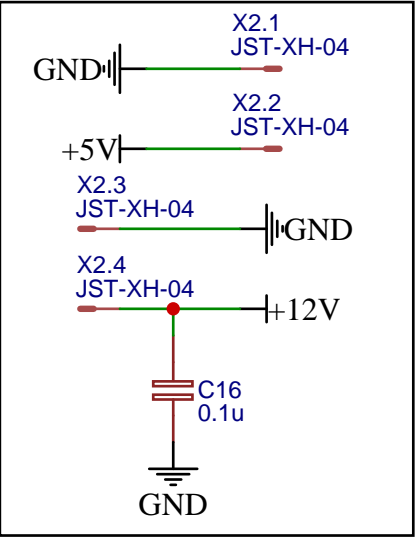
TITLE: **Power Manager (Layer D)**   REV: 1.0

Company: @dabecart   Sheet: 1/1

Date: 2024-09-29   Drawn By: @dabecart
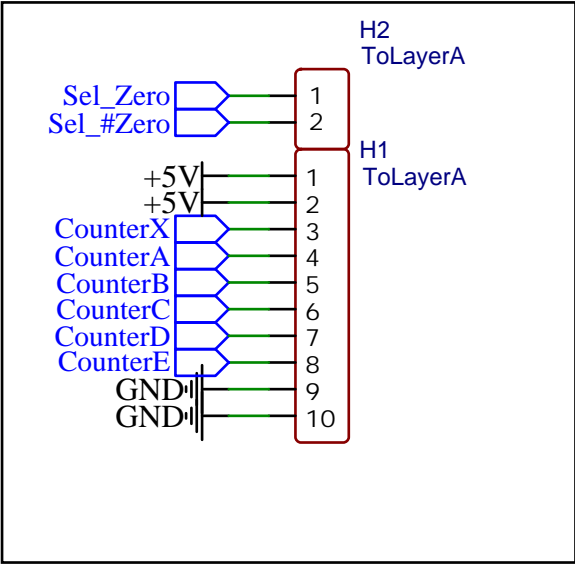
X1.1
JST-XH-02
‖GND

X1.2
JST-XH-02
+5Vnc

+5V Input
From +5V Boost Converter.

X3.1
JST-XH-02
‖GND

X3.2
JST-XH-02
+5V

+5V Output
Spare output.

X2.1
JST-XH-04
GND‖

X2.2
JST-XH-04
+5V

X2.3
JST-XH-04
‖GND

X2.4
JST-XH-04
+12V

C16
0.1u

GND

+12V Boost Converter
Input the controlled +5V to
generate +12 V.

H2
ToLayerA

Sel_Zero   1
Sel_#Zero   2

H1
ToLayerA

+5V   1
+5V   2
CounterX   3
CounterA   4
CounterB   5
CounterC   6
CounterD   7
CounterE   8
GND‖   9
GND‖   10

Binary Comparator
Compares the binary counter
with the number set by the
switches.

U11
TestPad

GND‖   1 | 1

U12
SN74HC02N

RPG — 1 1Y   VCC 14 — +5V
VCO_Out — 2 1A   4Y 13
3 1B   4B 12 — Sel_Zero
+5V — 4 2Y   4A 11 — Sel_#Zero
+5V — 5 2A   3Y 10
6 2B   3B 9
GND — 7 GND 3A 8

NOR

U10
SN74HC393N

1 1CLK VCC 14 — +5V
2 1CLR 2CLK 13
3 1QA   2CLR 12
4 1QB   2QA 11 — CounterX
5 1QC   2QB 10 — CounterA (MSB)
6 1QD   2QC 9 — CounterB
GND — 7 GND 2QD 8 — CounterC
— CounterD
— CounterE (LSB)