Preliminary Program

RTCSA 2014

The 20th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications

Aug.20- Aug. 22, 2014 , Chongqing, China

Wanyou Conifer hotel, Chongqing, China

Aug.20 (WED)	International Convention Hall	Jade Room	Amber Room	Crystal Room
09:00-09:10	RTCSA Open Talk: **Dr. Edwin Sha**			
09:10-10:10	RTCSA Keynote: **Dr. Tei-Wei Kuo**			
10:10-10:40	Coffee Break			
10:40-11:40	NVMSA Keynote: **TBA**			
11:50-13:40	Lunch Break			
13:40-15:20		RTCSA Session 1	RTCSA Session 2	NVMSA Session 1
15:20-15:50	Coffee Break			
15:50-17:30		RTCSA Session 3	RTCSA Session 4	NVMSA Session 2
18:00-	Receiption Dinner			
Aug.21 (THU)	**International Convention Hall**	**Jade Room**	**Amber Room**	**Crystal Room**
09:00-10:00	RTCSA Keynote: Dr. Zane Wei			
10:00:10:30	Coffee Break			
10:30-11:50		RTCSA Session 5	RTCSA Session 6	NVMSA Session 3
11:50-13:40	Lunch Break			
13:40-15:20		RTCSA Session 7	RTCSA Session 8	NVMSA Session 4
15:20-15:50	Coffee Break			
15:50-17:30		RTCSA Session 9	RTCSA Session 10	NVMSA Session 5
18:00-	Banquet			
Aug.22 (FRI)	**International Convention Hall**	**Jade Room**	**Amber Room**	**Crystal Room**
08:30-09:50		RTCSA Session 11	IWMSA Session 1	Tutorial1
09:50-10:20	Coffee Break			
10:20-11:40		RTCSA Session 12	IWMSA Session 2	Tutorial2

SPONSORING SOCIETIES

IEEE Advancing Technology for Humanity

IEEE Taipei Section

TCRTS Technical Committee on Real-Time Systems

IEEE computer society

IEEE Taipei Section

Chongqing University 1929

WENSDAY, AUGUST 20th

09:00-09:10	**RTCSA Open Talk**
09:10-10:10	**RTCSA Keynote Speech:** Non-Volatile Memory Innovation
10:10-11:40	**NVMSA Keynote Speech: TBA**
13:40-15:20	**RTCSA Session 1**: Embedded System Architecture **(Jade Room)**
13:40-14:00	1.1 Non-volatile Registers Aware Instruction Selection and Register Reallocation for Embedded Systems ***Mimi Xie,*** *Chen Pan, Jingtong Hu, Chun Jason Xue and Qingfeng Zhuge*
14:00-14:20	1.2 Dynamic Tail Packing to Optimize Space Utilization of File Systems in Embedded Computing Systems ***Nien-I Hsu,*** *Tseng-Yi Chen, Yuan-Hao Chang, Hsin-Wen Wei and Wei-Kuan Shih*
14:20-14:40	1.3 An Efficient Thermal Estimation Scheme for Microprocessors ***Pei-Shu Huang,*** *Quan-Chung Chen, Chen-Wei Huang and Shiao-Li Tsao*
14:40-15:00	1.4 Multi-objective aware design flow for coarse-grained systems on chip ***Peng Chen,*** *Chao Wang, Xi Li and Xuehai Zhou*
15:00-15:20	1.5 CCM: Low Cost Dynamic data Exchange to Emulate RAM on NAND Flash ***Junhua Zhao,*** *Hejun Wu and Weiwei Liu*
13:40-15:20	**RTCSA Session 2:** Real-Time System Analysis **(Amber Room)**
13:40-14:00	2.1 Direct Handling of Infeasible Paths in the Event Dependency Analysis ***Kilian Kempf*** *and Frank Slomka*
14:00-14:20	2.2 Component-Based Analysis of Hierarchical Scheduling using Linear Hybrid Automata ***Youcheng Sun****, Giuseppe Lipari, Romain Soulat, Laurent Fribourg and Nicolas Markey*
14:20-14:40	2.3 Impact Analysis for Timing Requirements on Real-Time Systems ***Tayfun Gezgin****, Ingo Stierand, Achim Rettberg and Stefan Henkler*
14:40-15:00	2.4 Static WCET Analysis of the H.264/AVC Decoder Exploiting Coding Information ***Chen-Wei Huang****, Timon Kelter, Bjoern Boenninghoff, Jan Kleinsorge, Michael Engel, Peter Marwedel and Shiao-Li Tsao*
15:00-15:20	2.5 A Framework for the Derivation of WCET Analyses for Multi-Core Processors (**WIP**) ***Michael Jacobs***

15:50-17:30	**RTCSA Session 3:** Embedded System Memory **(Jade Room)**
15:50-16:10	3.1 Minimum-cost Data Allocation with Guaranteed Probability on Multiple Types of Memory ***Shouzhen Gu**, Qingfeng Zhuge, Jingtong Hu, Juan Yi and Edwin H.M. Sha*
16:10-16:30	3.2 Memory Power Optimization on Different Memory Address Mapping Schemas ***Zongwei Zhu**, Xi Li, Chao Wang and Xuehai Zhou*
16:30-16:50	3.3 A Mixed Critical Memory Controller Using Bank Privatization and Fixed Priority Scheduling ***Leonardo Ecco**, Sebastian Tobuschat, Selma Saidi and Rolf Ernst*
16:50-17:10	3.4 PUMA: Pseudo Unified Memory Architecture on Single-ISA Heterogeneous Multi-core Systems ***Gangyong Jia**, Liang Shi, Xi Li, Jian Wan and Dong Dai*
17:10-17:30	3.5 Wear-Leveling for PCM Main Memory on Embedded System via Page Management and Process Scheduling ***Chen Pan**, Mimi Xie, Jingtong Hu, Meikang Qiu and Qingfeng Zhuge*
15:50-17:30	**RTCSA Session 4:** Real-Time Task Schedule A **(Amber Room)**
15:50-16:10	4.1 Contention-Aware Task and Communication Co-Scheduling for Network-on-Chip based Multiprocessor System-on-Chip ***Lei Yang**, Weichen Liu, Weiwen Jiang and Edwin Sha*
15:10-16:30	4.2 Optimal Semi-Partitioned Scheduling in Soft Real-Time Systems ***Jim Anderson**, Jeremy Erickson, Umamaheswari Devi and Benjamin Casses*
16:30-16:50	4.3 Minimizing Response Times of Automotive Dataflows on Multicore ***Glenn A. Elliott**, Namhoon Kim, Jeremy P. Erickson, Cong Liu and James H. Anderson*
16:50-17:10	4.4 Improving the Response Time Analysis of Global Fixed-Priority Multiprocessor Scheduling ***Youcheng Sun**, Giuseppe Lipari, Nan Guan and Wang Yi*
16:10-17:30	4.5 Effects of Structured Parallelism by Parallel Design Patterns on Embedded Hard Real-time Systems ***Ralf Jahr**, Mike Gerdes, Theo Ungerer, Haluk Ozaktas, Christine Rochange and Pavel G. Zaykov*
13:40-15:20	**NVMSA Session 1: (Crystal Room)**
	TBA
15:50-17:30	**NVMSA Session 2: (Crystal Room)**
	TBA

THURSDAY, AUGUST 21th

09:00-10:00	**RTCSA Keynote Speech:** High Throughput Computing Data Center
10:30-11:50	**RTCSA Session 5:** Architecture-Aware Schedule **(Jade Room)**
10:30-10:50	5.1 Energy Efficient Real-Time Task Scheduling for Embedded Systems with Hybrid Main Memory ***Zhiyong Zhang**, Zhiping Jia, Lei Ju and Peng Liu*
10:50-11:10	5.2 Current-Aware Scheduling for Flash Storage Devices ***Tzu-Jung Huang**, Chien-Chung Ho, Po-Chun Huang, Yuan-Hao Chang, Che-Wei Chang and Tei-Wei Kuo*
11:10-11:30	5.3 An Adaptive Server-Based Scheduling Framework with Capacity Reclaiming and Borrowing ***Meng Liu**, Moris Behnam, Shinpei Kato and Thomas Nolte*
11:30-11:50	5.4 A Memory Schedule Policy Oriented to Stream Architecture ***Chiyuan Ma** and Xiaoqiang Ni*
10:30-11:50	**RTCSA Session 6:** Real-Time System Architecture **(Amber Room)**
10:30-10:50	6.1 A Dynamic Virtual Memory Management under Real-Time Constraints ***Martin Boehnert** and Christoph Scholl*
10:50-11:10	6.2 A Hardware Architecture to Deploy Complex Multiprocessor Scheduling Algorithms ***Renato Mancuso**, Prakalp Srivastava, Deming Chen and Marco Caccamo*
11:10-11:30	6.3 Optimal and fast composition of resource-sharing components in hierarchical real-time systems ***Martijn M.H.P. Van Den Heuvel**, Moris Behnam, Reinder J. Bril, Johan Lukkien and Thomas Nolte*
11:30-11:50	6.4 A Context Aware Cache Controller to Bridge the Gap Between Theory and Practice in Real-Time Systems ***Yannick Allard**, Geoffrey Nelissen, Joël Goossens and Dragomir Milojevic*
13:40-15:20	**RTCSA Session 7:** Multicore Embedded System **(Jade Room)**
13:40-14:00	7.1 On Self-Timed Ring for Consistent Mapping and Maximum Throughput ***Weiwen Jiang**, Qingfeng Zhuge, Juan Yi, Lei Yang and Edwin Sha*
14:00-14:20	7.2 Energy-Efficient Allocation of Real-Time Applications onto Heterogeneous Processors ***Alexei Colin**, Arvind Kandhalu and Raj Rajkumar*
14:20-14:40	7.3 Adaptive Dynamic Power Management for Hard Real-time Pipelined Multiprocessor Systems

	***Gang Chen**, Kai Huang and Alois Knoll*
14:40-15:00	7.4 Operating System Support to an Online Hardware-Software Co-Design Scheduler for Heterogeneous Multicore Architectures ***Maikon Bueno**, José Holanda, Erinaldo Pereira and Eduardo Marques*
15:00-15:20	7.5 A Task-Level Superscalar Microarchitecture for Large Scale Chip Multiprocessors ***Jianqing Xiao**, Pengwei Lv, Mian Lou, Xunying Zhang and Xubang Shen*
13:40-15:20	**RTCSA Session 8:** Networked System and Analysis **(Amber Room)**
13:40-14:00	8.1 Schedulability Analysis of Ethernet AVB Switches ***Unmesh D. Bordoloi**, Amir Aminifar, Petru Eles and Zebo Peng*
14:00-14:20	8.2 Network-Harmonized Scheduling for Multi-Application Sensor Networks ***Vikram Gupta**, Nuno Pereira, Shashank Gaur, Eduardo Tovar and Ragunathan Rajkumar*
14:20-14:40	8.3 The trajectory approach for AFDX FIFO networks revisited and corrected ***Xiaoting Li**, Olivier Cros and Laurent George*
14:40-15:00	8.4 Reduced Buffering Solution for Multi-Hop HaRTES Switched Ethernet Networks ***Mohammad Ashjaei**, Moris Behnam, Paulo Pedreiras, Reinder J. Bril, Luis Almeida and Thomas Nolte*
15:00-15:20	8.5 Worst-Case Communication Delay Analysis for Many-Cores using a Limited Migrative Model ***Borislav Nikolic**, Patrick Meumeu Yomsi and Stefan M. Petters*
15:50-17:30	**RTCSA Session 9:** Embedded System Software **(Jade Room)**
15:50-16:10	9.1Time square -- marriage of real-time and logical-time in GALS and synchronous languages ***Heejong Park**, Avinash Malik and Zoran Salcic*
16:10-16:30	9.2 An Evaluation of Code Generation of Dataflow Languages on Manycore Architectures ***Suleyman Savas**, Essayas Woldu, Zain Ul-Abdin, Tomas Nordstr 枚 m and Mingkun Yang.*
16:30-16:50	9.3 Light-PREM: Automated Software Refactoring for Predictable Execution on COTS Embedded Systems ***Renato Mancuso**, Roman Dudko and Marco Caccamo*
16:50-17:10	9.4 Hazard Analysis for AADL Model ***Xiaomin Wei**, Yunwei Dong, Mengmeng Yang, Ning Hu and Hong Ye*

17:10-17:30	9.5 A Dynamic Covering Algorithm of Wireless Sensor Network Based on CVT ***Hongxing Wei*** *and Qiang Mao*
15:50-17:30	**RTCSA Session 10:** Real-Time Task Schedule B **(Amber Room)**
15:50-16:10	10.1 Federated Scheduling for Stochastic Parallel Real-time Tasks ***Jing Li****, Kunal Agrawal, Christopher Gill and Chenyang Lu*
16:10-16:30	10.2 Service Guarantee Exploration for Mixed-Criticality Systems ***Hang Su****, Nan Guan and Dakai Zhu*
16:30-16:50	10.3 Power Minimization for Parallel Real-Time Systems with Malleable Jobs and Homogeneous Frequencies ***Antonio Paolillo****, Joël Goossens, Pradeep M. Hettiarachchi and Nathan Fisher*
16:50-17:10	10.4 Partitioned Multiprocessor Scheduling of Mixed-Criticality Parallel Jobs ***Guangdong Liu****, Ying Lu, Shige Wang and Zonghua Gu*
17:10-17:30	10.5 Computation Offloading for Sporadic Real-Time Tasks ***Anas Toma****, Jian-Jia Chen and Wei Liu*
10:30-11:50	**NVMSA Session 3: (Crystal Room)**
	TBA
13:40-15:20	**NVMSA Session 4: (Crystal Room)**
	TBA
15:50-17:30	**NVMSA Session 5: (Crystal Room)**
	TBA

FRIDAY, AUGUST 22th

08:30-09:50	**RTCSA Session 11:** Emerging Applications **(Jade Room)**
08:30-08:50	11.1 Towards Scalable, Fair and Robust Data Dissemination via Cooperative Vehicular Communications ***Kai Liu****, Joseph Ng, Victor Lee and Sang Son*
08:50-09:10	11.2 Deadline-Aware Load Balancing for MapReduce ***Zhao-Rong Lai****, Che-Wei Chang, Xue Liu, Tei-Wei Kuo and Pi-Cheng Hsiu*
09:10-09:30	11.3 Workload Migration Framework for Streaming Applications on Smartphones ***Chi-Sheng Daniel Shih****, Shun-Min Wang and Yu-Hsin Wang*
09:30-09:50	11.4 Development of Gaze Tracking System with iPad ***Jiajin Zhang****, Lichang Chang and Liu Di*
10:20-11:40	**RTCSA Session 12:** System Design Practice **(Jade Room)**
10:20-10:40	12.1 The Acceleration of Pipeline Workloads under the FPGA Area

	and Bandwidth Constraints ***Wei-Ning Huang**, Sheng-Wei Cheng, Che-Wei Chang, Yu-Chen Wu, Tei-Wei Kuo, Yung-Chin Hsu and Wen-Yih Isaac Tseng*
10:40-11:00	12.2 An Energy Efficient OpenCL Implementation of a Fingerprint Verification System on Heterogeneous Mobile Device ***Zhi Qi** and Wen Wen*
11:00-11:20	12.3 A Real-Time Distributed Hash Table ***Tao Qian**, Frank Mueller and Yufeng Xin*
11:20-11:40	12.4 A Management Architecture of Cloud Server Systems ***Hua Nie**, Gongbo Li, Xingkui Liu, Xiaojun Yang and Keping Long*
11:40-12:00	12.5 Design and Implementation of A Multi-Node WIFI Heart Rate Variability Analysis System ***Kai Li**, Xin Wang and Jianhua Shen*
08:30-09:50	**IWMSA Session 1 (Amber Room)**
08:30-08:50	1.1 TACO: A Scalable Framework for Timing Analysis and Code Optimization of Synchronous Programs ***Zhenmin Li**, Avinash Malik and Zoran Salcic*
08:50-09:10	1.2 A Plasmonic Refractive Index Sensor Based on A MIM Waveguide with A Side-coupled Nanodisk Resonator ***Yexiong Huang**, Yiyuan Xie, Weilun Zhao, Hongjun Che, Weihua Xu, Xin Li and Jiachao Li*
09:10-09:30	1.3 An Implementation of Partitioned Scheduling Scheme for Hard Real-Time Tasks in Multicore Linux with Fair Share for Linux Tasks ***N. Saranya** and R. C. Hansdah*
09:30-09:50	1.4 Enhancing Lifetime of NVM-based Main Memory with Bit Shifting and Flipping ***Xianlu Luo**, Duo Liu, Kan Zhong, Dan Zhang, Yi Lin, Jie Dai, Weichen Liu*
10:20-11:40	**IWMSA Session 2 (Amber Room)**
10:20-10:40	2.1 Performance Isolation for Real-time Systems with Xen Hypervisor on Multi-cores ***Wei Jing**, Nan Guan and Wang Yi*
10:40-11:00	2.2 Performance Improvement in Mesh-based Optical Networks-on-Chip ***Weilun Zhao**, Yiyuan Xie, Hongjun Che, Yexiong Huang, Weihua Xu, Xin Li and Jiachao Li*
11:00-11:20	2.3 Energy efficient routing techniques with guaranteed reliability based on multi-level uncertain graph ***Wendi Nie**, Yaoxin Duan, Kaijie Wu, Qingfeng Zhuge and Edwin Sha*

11:20-11:40	2.4 A Hardware-Software Co-design Experiments Platform for NAND Flash Based on Zynq ***Wei Debao**, Deng Libao, Huang Min, Gong Youhua, Qiao Liyan*
11:40-12:00	2.5 Performance Optimization in Torus-based Optical Networks-on-Chip ***Weihua Xu**, Yiyuan Xie, Yantao Wang, Hongjun Che, Weilun Zhao, Yexiong Huang, Xin Li and Jiachao Li*
08:30-09:50	**Tutorial 1:** Automotive Cyber-Physical Systems **(Crystal Room)**
	Samarjit Chakraborty, TU Munich, Germany *Majid Zamani, TU Munich, Germany*
10:20-11:00	**Tutorial 2:** Automotive Cyber-Physical Systems **(Crystal Room)**
	Jason Xue, City University of Hong Kong

KEYNOTE SPEECH 1

Non-Volatile Memory Innovation

Dr. Tei-Wei Kuo

Distinguished Professor, IEEE Fellow, National Taiwan University

Abstract

As flash memory gains its huge momentum in the storage market, people have high expectation on other potential roles that could be played by non-volatile memory. It has been a grand challenge to position selected non-volatile memory technologies in the memory hierarchy. In this talk, I will take flash memory and phased change memory (PCM) as examples to address the challenges and design methodologies for non-volatile memory as a storage medium or to serve as the role of DRAM. The talk will be concluded by moving the discussion forward to the opportunities of non-volatile memory in system designs, such as server cache and data storage in data manipulation.

KEYNOTE SPEECH 2

High Throughput Computing Data Center

Dr. Zhulin Wei

VP, Huawei Technologies Co. and Head of Huawei Shannon Research Lab.

Abstract

Over the last few decades, data center (DC) technology has evolved from DC 1.0 (tightly-coupled silos) to DC 2.0 (computer virtualization) in order to enhance data processing capability. In the era of big data, highly diversified analytics applications stress data centers. The mounting requirements on throughput, resource utilization, manageability and energy efficiency demand seamless integration of heterogeneous system resources to adapt to varied big data applications, for which DC 2.0 does not suffice. By rethinking the challenges of big data applications, Huawei proposes a High Throughput Computing Data Center architecture (HTC-DC) toward the design of DC 3.0. HTC-DC features resource disaggregation via unified interconnection. It offers PB-level data processing capability, intelligent manageability, high scalability and high energy efficiency, hence a promising candidate for DC 3.0.

TUTORIAL

Automotive Cyber-Physical Systems

Samarjit Chakraborty, TU Munich, Germany

Majid Zamani, TU Munich, Germany

Jason Xue, City University of Hong Kong

Abstract

Modern cars have 50-100 electronic control units (ECUs) that are connected by a complex communication network using CAN, FlexRay and Ethernet and several gateways. Such a platform is used to support various control applications ranging over safety-critical, driver assistance and comfort-related functions. In such a setup, traditional control theoretic techniques -- where control engineers are only concerned with high-level plant and controller models and abstract away platform-specific implementation details like numerical precision, computation times and message communication delays -- suffer from a number of problems.

In particular, in such cases model-level semantics and control performance deviates significantly from what is seen after the implementation. In order to close this gap, a considerable effort is spent on integration, testing and debugging which significantly increases the development cost and poses an obstacle towards certification.

The goal of this tutorial is to highlight these problems and present approaches currently being developed in the area of cyber-physical systems towards co-design of control algorithms and their implementation platforms. In particular we will discuss techniques for communication, computation and memory-aware controller design, along with techniques for controller synthesis from formal specifications.

Target audience: This tutorial is targeted towards an audience with a background in real-time and embedded systems. No previous experience in automotive systems or control theory will be assumed.