

# Simulation Topology and Important Parameters

This document provides topological diagram for distribution network simulation, along with the capacity parameters of the connected controllable photovoltaic (PV) converters and energy storage (ES) converters. The topological diagram for distribution network simulation is shown in Fig. 1:

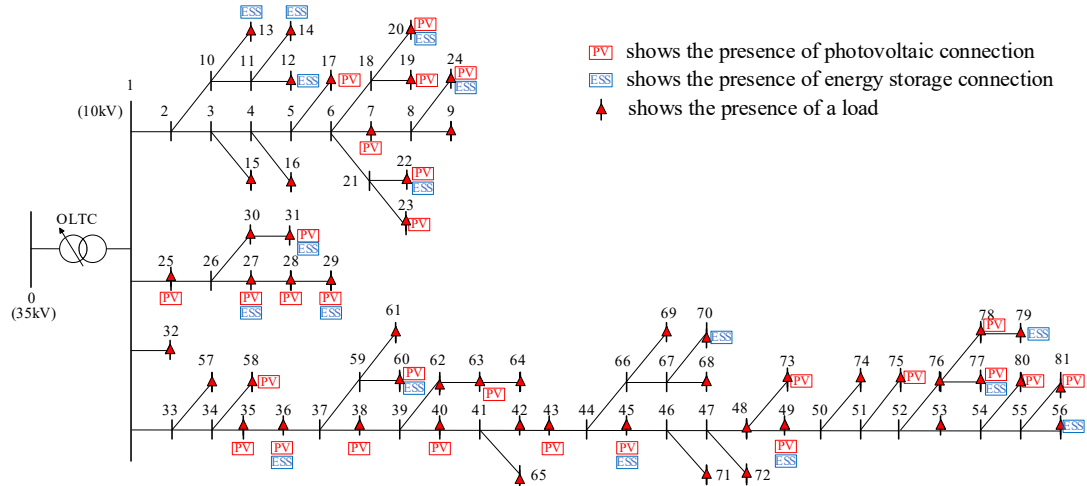


Fig. 1 Topology diagram of 10kV AND.

The capacity parameters of the controllable PV converters and ES converters are shown in Table I:

TABLE I  
PARAMETERS OF CONTROLLABLE PV INVERTERS AND ES INVERTERS

Controllable Resources	Nodes	Controllable Capacity/MVA
Energy Storage Converter	12、13、14、20、22、24、	0.2
	27、29、31、36、45、49、	
	56、60、70、77、79	
Photovoltaic Converter	22、25、27、36、38、58、	0.06
	63、73、77、78	
	23、24、31、43、60、75、81	0.12
	17、20、28、35、45、80	0.24
	7、19、29、40、49	0.36

The technical parameters of energy storage system are shown in Table II:

TABLE II

TECHNICAL PARAMETERS OF ENERGY STORAGE SYSTEM

Controllable Resources	Nodes	Controllable Capacity/MVA	Charge and discharge loss ratio	Maximum/Minimum state of charge	Maximum discharge/charging power/MW
Energy Storage	12、13、14、 20、22、24、 27、29、31、 36、45、49、 56、60、70、 77、79	0.2	5%	0.95/0.05	0.15/0.15

The system and control parameters are shown in Table III:

TABLE III

SYSTEM AND CONTROL PARAMETERS

Parameter Name	Value
Maximum unbalanced power	6000KW
Total droop coefficient for the ADN	3MW/Hz
Total droop coefficient of the generators in the bulk system	11 MW/Hz
Total inertia coefficient of the generators in the bulk system	3000 MW·s/Hz
Optimization period	60s
Optimization time scale	2s
Frequency prediction time scale	1ms
Droop coefficient optimization time interval	60 s
Reactive power optimization time interval	10 s
Dead zone of PFR	0.05 Hz

The topological diagram for IEEE 39-bus test system is shown in Fig. 2:

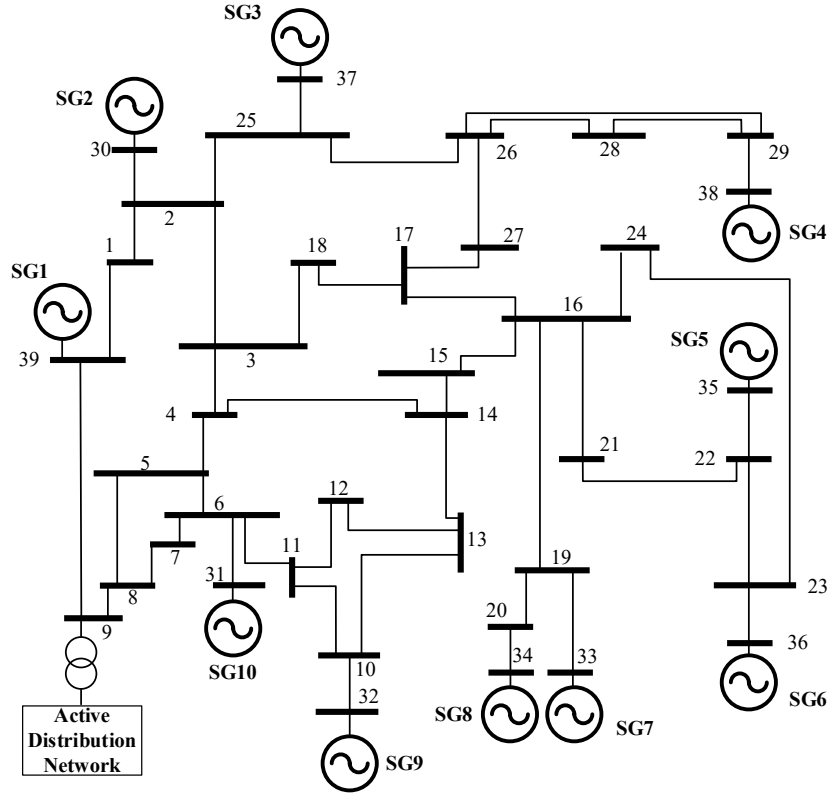


Fig. 2 Active distribution network integrated IEEE 39-bus test system.

The inverter control structure used in this paper is shown in Fig. 3:

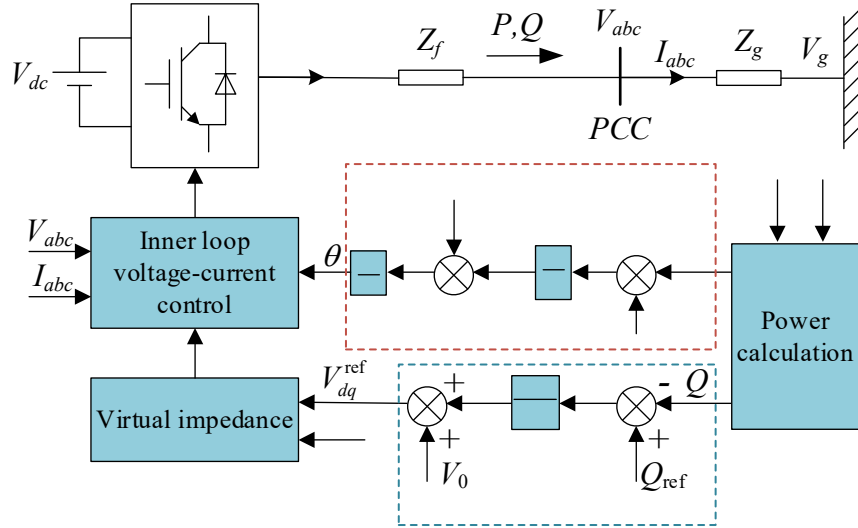


Fig. 3 Converter circuit topology and control structure.