(T)EE2026

Digital Fundamentals

(L7: Logic IC families)

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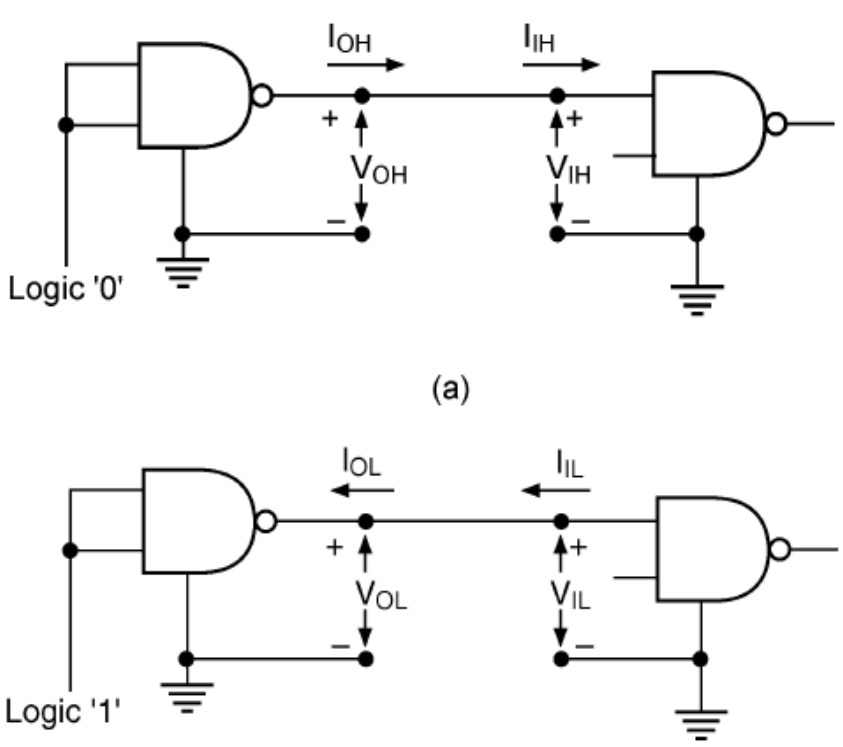
Outline

- Introduction to digital IC technologies
- Logic gate characteristics
- CMOS logic gates
- TTL logic gates
- Commercial logic families
- CMOS-TTL Interfacing

Logic gate characteristics

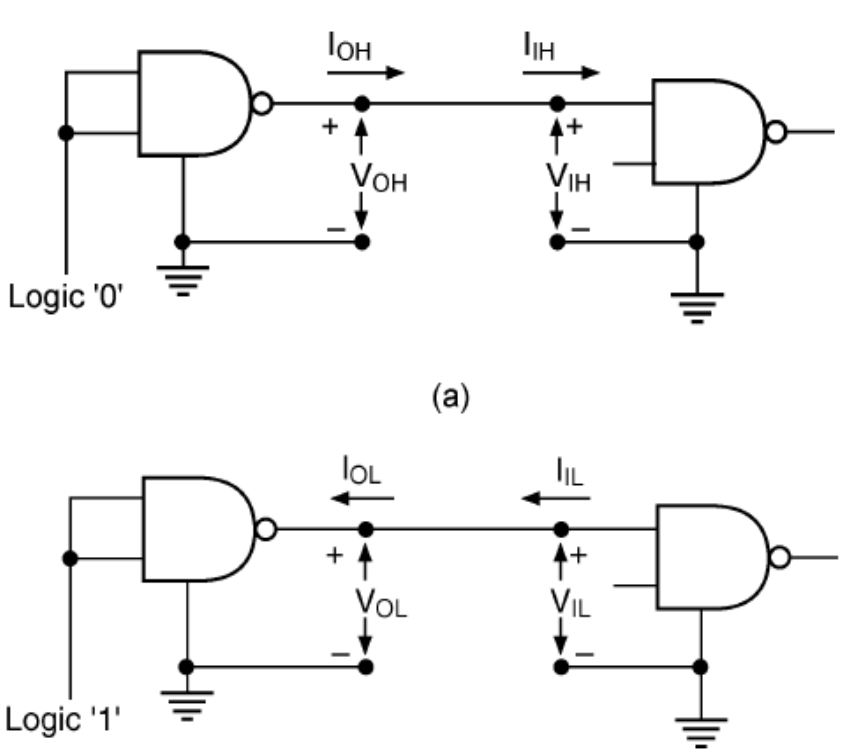
- **Static parameters**
  - V_{OL} → Maximum Logic LOW output voltage
  - V_{OH} → Minimum Logic HIGH output voltage
  - V_{IL} → Maximum Logic LOW input voltage
  - V_{IH} → Minimum Logic HIGH input voltage
  - NM_H → Noise margin high
  - NM_L → Noise margin low
  - I_{OL}/I_{OH} → Logic LOW/HIGH output currents
  - I_{IL}/I_{IH} → Logic LOW/HIGH input currents (for TTL only)
  - Power dissipation
- **Dynamic parameters**
  - Propagation delay
  - Fan-out

V_{OH}, V_{OL}, V_{IH}, V_{IL}



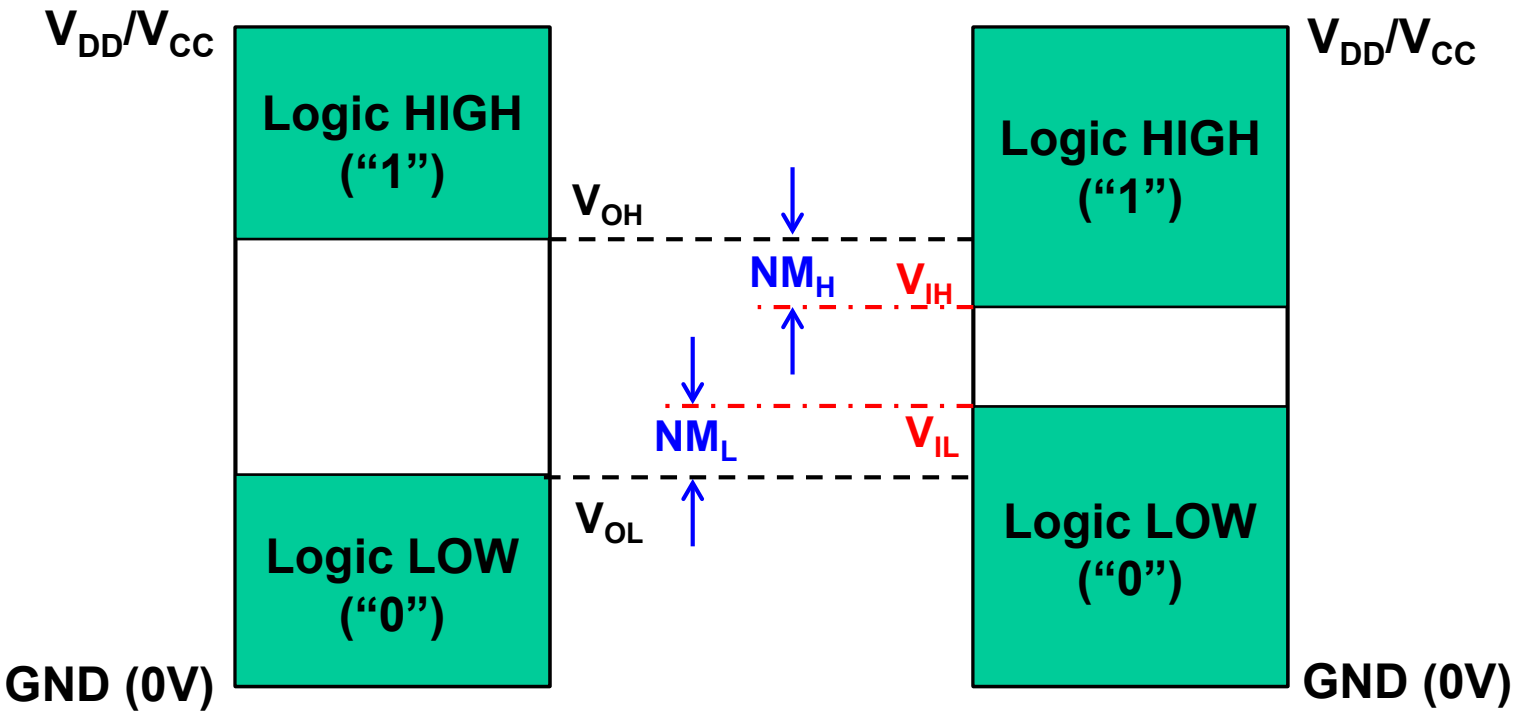
- $\mathbf{V_{OH}}$ is minimum output voltage that establishes valid logic high to the following gate
- $\mathbf{V_{OL}}$ is the maximum output voltage that established valid logic low to the following gate
- $\mathbf{V_{IH}}$ is the minimum valid logic high input voltage
- $\mathbf{V_{IL}}$ is the maximum valid logic low input voltage

I_{OH}, I_{OL}, I_{IH}, I_{IL}



- I_{OH} is maximum current that can flow out of an output when output voltage maintains a valid logic high
- I_{OL} is the maximum current that can flow into an output when output voltage maintains a valid logic low
- I_{IH} is the current flowing into or out of an input when the input voltage is a valid logic high
- I_{IL} is the current flowing into or output an input when the input voltage is a valid logic low

Noise margin (NM_H, NM_L)

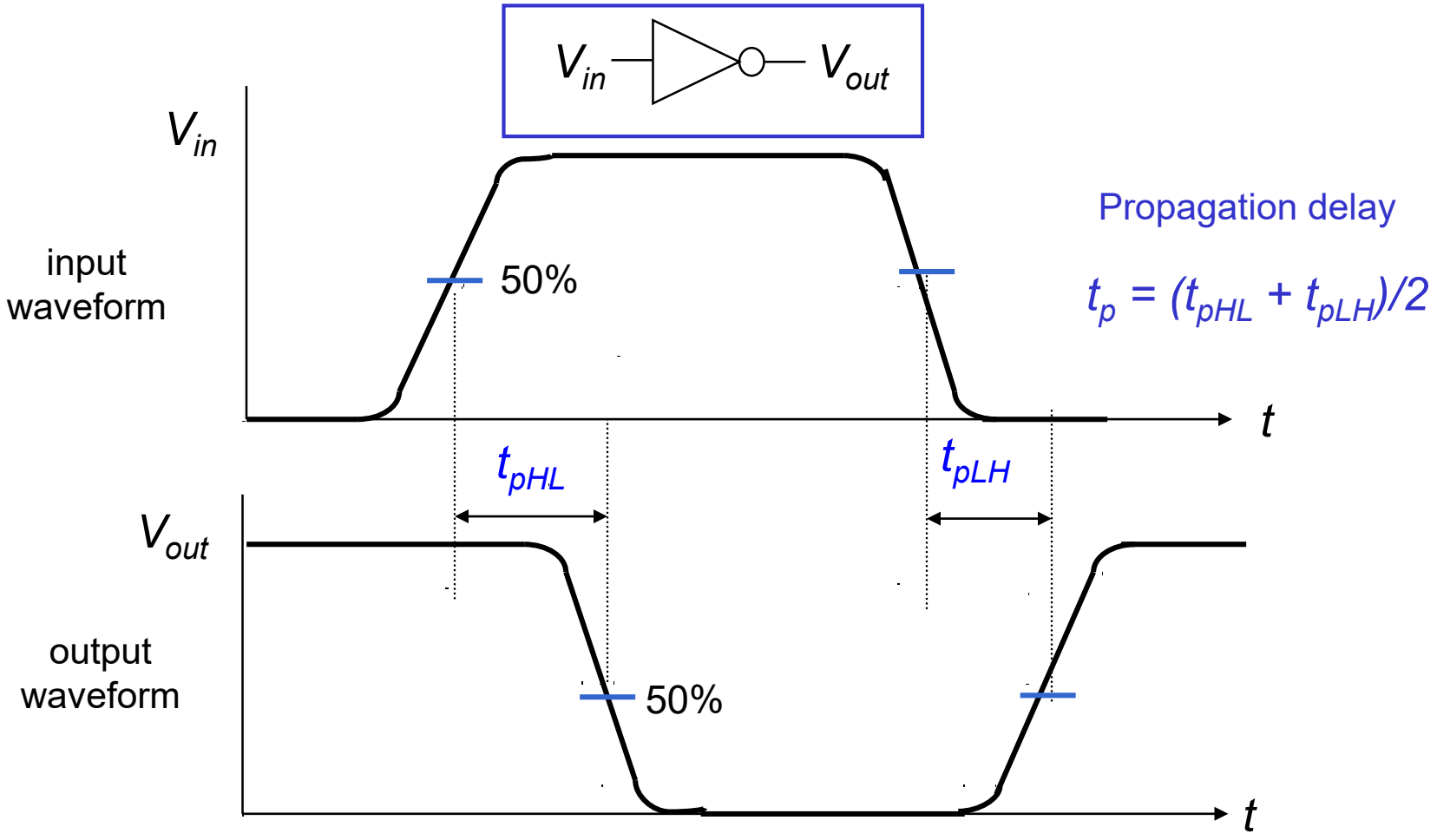


$$NM_H = V_{OH} - V_{IH}$$
$$NM_L = V_{IL} - V_{OL}$$

Power Dissipation

- Represents the amount of power needed by the gate. Often expressed in mW (milliwatts).
- Calculated from the supply voltage V_{CC} and the current I_{CC} that is drawn by the circuit.
- Power dissipation $P_D = V_{CC} * I_{CC}$
- Current drawn depends on the logic state of gate.

Propagation delay

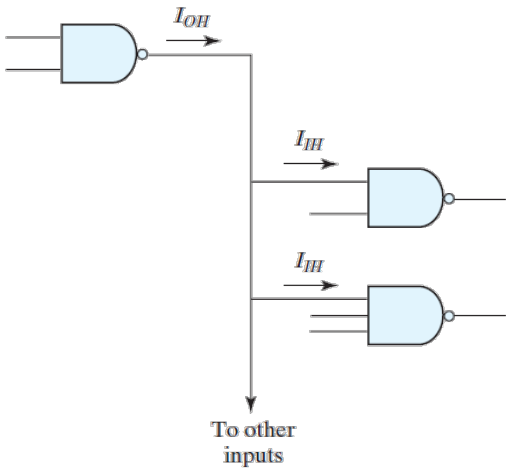


Fan-Out

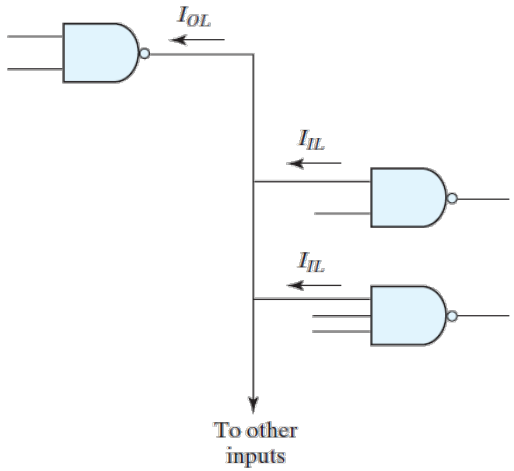
- Determines how many standard loads can be connected to the output of a gate
  - A standard load is defined as the amount of current needed by an input of another gate in the same logic family
  - Loading is also used to indicate fan-out.
- The output of a gate can supply a limited amount of current. Above that it is said to be overloaded.
- Each input of a gate also requires current
- Each additional connection adds to the gate load
- Exceeding the maximum load may cause malfunction

Fan-Out

Output is logic HIGH:



Output is logic LOW:



- Calculated from the amount of current available in the gate-output to that is needed in the input.
- Fan-out = min(I_{OH}/I_{IH}, I_{OL}/I_{IL})
- Example: standard TTL gates

  I_{OH} = 400 μA, I_{IH} = 40 μA, I_{OL} = 16 mA, I_{IL} = 1.6 mA
  - Fan-out = min(400/40, 16/1.6) = 10
  - The maximum number of gates that can be connected (or driven) is 10

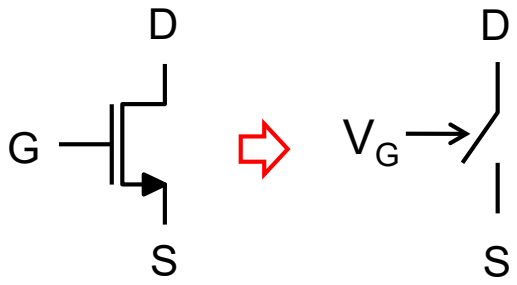
Digital IC technologies

- Digital integrated circuits can be designed in different technologies
- Technology will impact on the performance of ICs
- The two mainstream technologies are
  - CMOS IC technology
  - Bipolar IC technology
- CMOS IC technology is based metal-oxide-semiconductor field-effect transistors (MOSFET)
- Bipolar IC technology is based on bipolar junction transistors (BJT)

Transistor as a switch

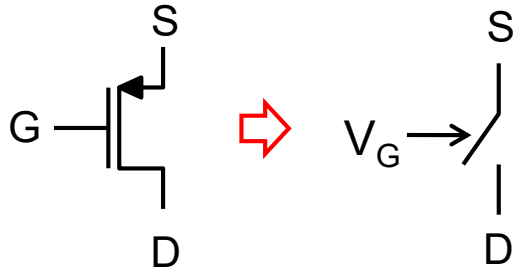
- In this part, we consider an MOS transistor (MOSFET) as a switch
- MOS transistors can be either NMOS or PMOS transistors
- We view a 3-terminal MOSFET as a blackbox whose drain and source terminals are equivalent to the two terminals of an ordinary switch and the gate controls the switch

NMOS transistor:



$V_G = V_{DD}$ (“1”) → NMOS is **on** (switch closed)
$V_G =$ 0V (“0”) → NMOS is **off** (switch open)

PMOS transistor:



V_G = 0V (“0”) → PMOS is **on** (switch closed)
$V_G = V_{DD}$ (“1”) → PMOS is **off** (switch open)

Logic ICs based on BJT IC technology

- **TTL** (Transistor-Transistor Logic)
  - Invented by *TRW Inc.* in US, first commercial TTL logic IC was introduced by Sylvania in 1963 and became popular with *Texas Instrument*'s 5400 and 7400 series
- **ECL** (Emitter-Coupled Logic)
  - Invented by IBM, first commercial integrated-circuit ECL family was introduced by *Motorola* in 1962
  - Suitable for high-speed logic circuits

TTL logic gates

Features of TTL logic gates

- Based on BJTs
- Most widely used logic ICs at gate or MSI level
- Typically operated under 5V supply voltage
- Having different series that optimized for low power, high speed, etc
- Inputs of the gate draw static current

- Due to lack of prerequisite, we will not discuss circuit details of logic gates (look forward to seeing you attending EE4415 module)

CMOS/TTL Comparison (static)

Input/output voltage levels (in volts) with $V_{DD} = V_{CC} = +5$ V.

	CMOS							TTL			
Parameter	4000B	74HC	74HCT	74AC	74ACT	74AHC	74AHCT	74	74LS	74AS	74ALS
V_{IH} (*min*)	3.5	3.5	2.0	3.5	2.0	3.85	2.0	2.0	2.0	2.0	2.0
V_{IL} (*max*)	1.5	1.0	0.8	1.5	0.8	1.65	0.8	0.8	0.8	0.8	0.8
V_{OH} (*min*)	4.95	4.9	4.9	4.9	4.9	4.4	3.15	2.4	2.7	2.7	2.7
V_{OL} (*max*)	0.05	0.1	0.1	0.1	0.1	0.44	0.1	0.4	0.5	0.5	0.4
V_{NH}	1.45	1.4	2.9	1.4	2.9	0.55	1.15	0.4	0.7	0.7	0.7
V_{NL}	1.45	0.9	0.7	1.4	0.7	1.21	0.7	0.4	0.3	0.3	0.4

Noise margin H and L

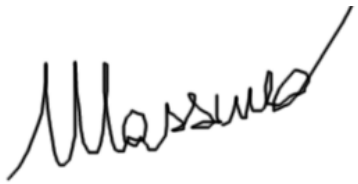
Summary

- Digital IC technology
  - BJT and MOSFET
  - BJT and CMOS technology
- CMOS logic gates
  - Implementation of NOT, NAND, NOR, AND and OR gates
- Commercial logic families
  - TTL and CMOS
- Logic gate characteristics
  - Static parameters (V_{OH}, V_{OL}, V_{IH}, V_{IL}, I_{OH}, I_{OL}, I_{IH}, I_{IL}, NM_H, NM_L and P_D)
  - Dynamic parameters (t_p and fan-out)
  - CMOS/TTL comparison
- Logic family interfacing (TTL driving CMOS, CMOS driving TTL)

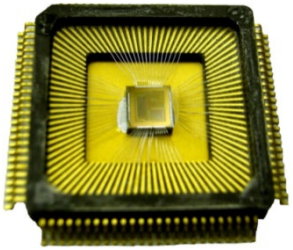
To keep in mind, overall…

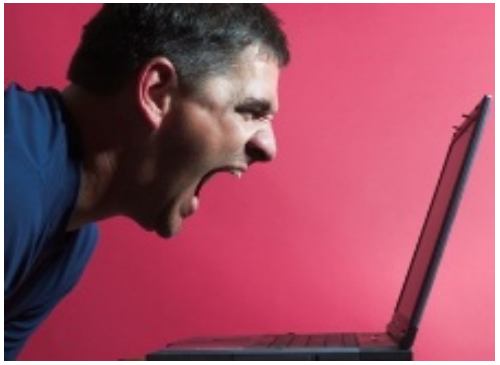
MOTIVATION: WHY ARE WE DOING THIS?

IMPACT: WHAT CAN YOU DO WITH YOUR KNOWLEDGE?



What You Will Be Able to Do in a Few Weeks...





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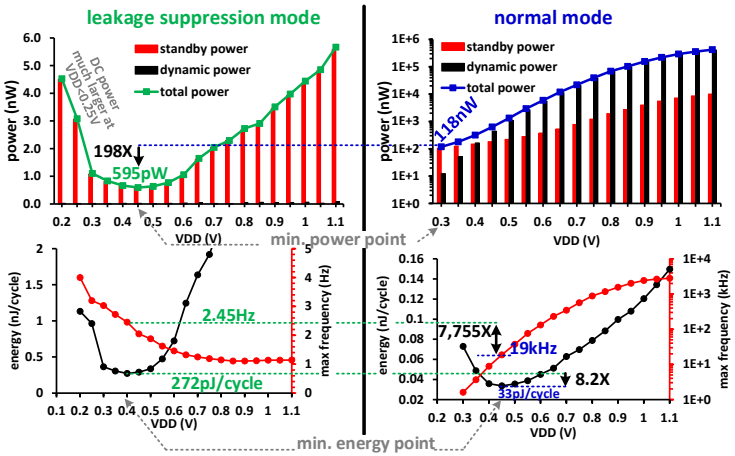

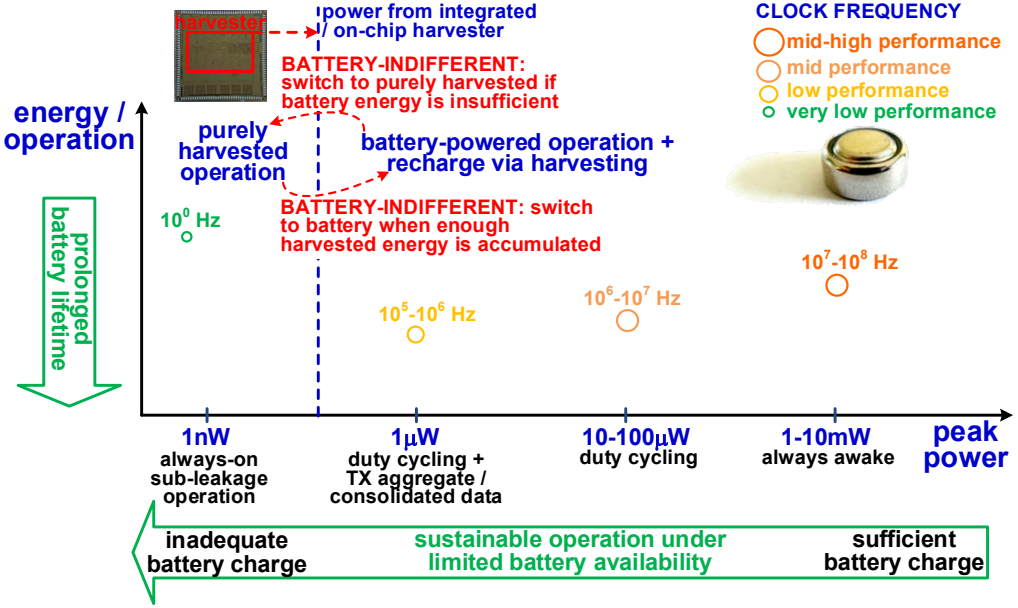

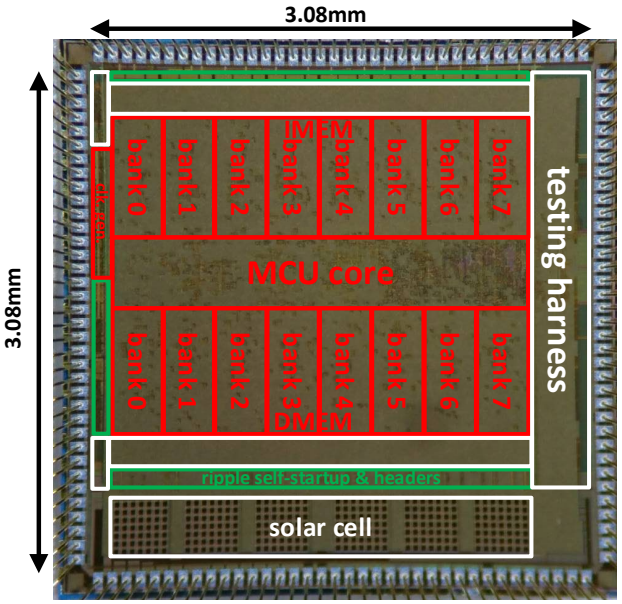

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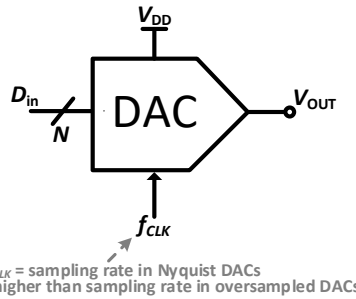
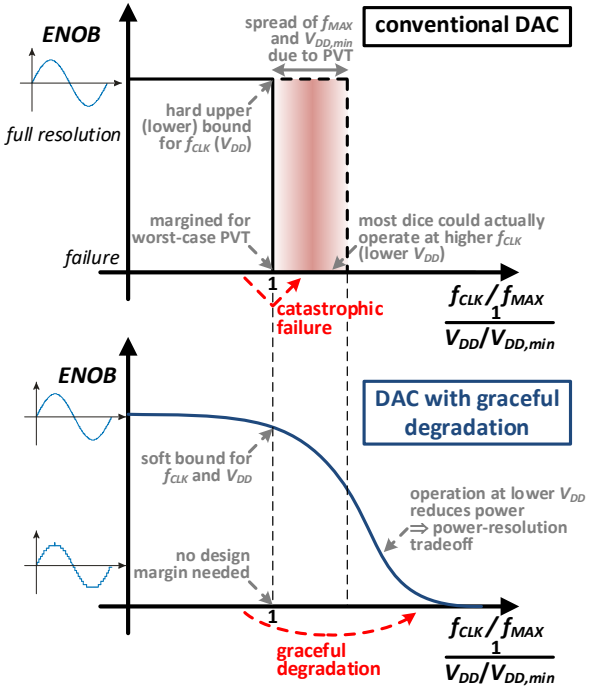
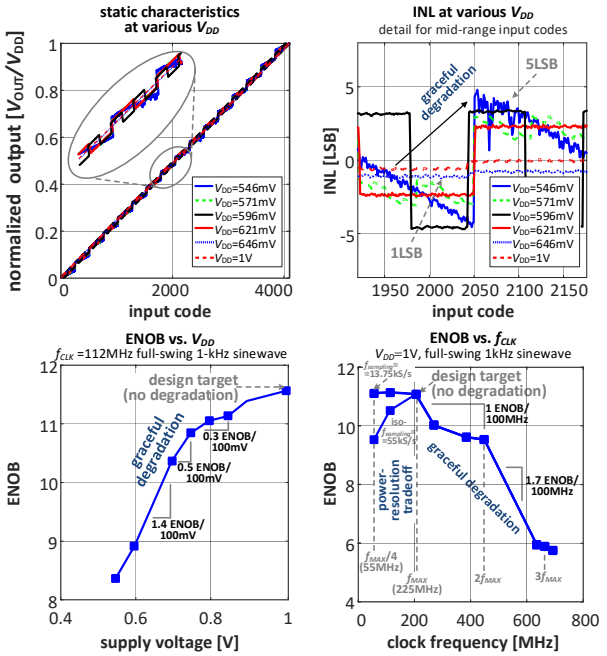
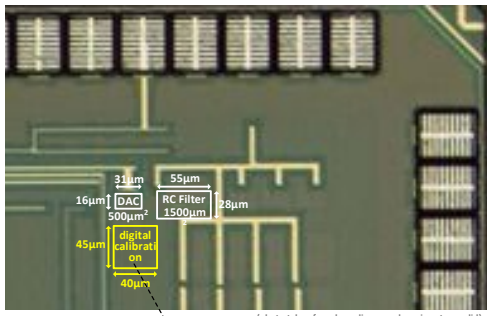


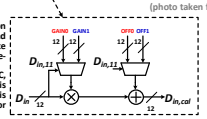


	conventional DAC	DAC with graceful degradation
design margin	worst-case PVT	no margin (design at TT corner)
operation at $V_{DD} < V_{DD,min}$ (design target)	not allowed	allowed (at degraded ENOB)
operation at $f_{CLK} > f_{MAX}$ (design target)	not allowed	allowed (at degraded ENOB)
dynamic energy-resolution tradeoff	NO	YES (at degraded ENOB)





DIGITAL CALIBRATION
offset and gain correction (different for $D_{in}<2^{N-1}$ and $D_{in}>2^{N-1}$) to compensate gain, offset and double-slope errors.
Area not counted in DAC, as calibration circuitry is not needed when DAC is driven by DSP or microprocessor



DAC Core	
technology	40nm CMOS
area	16µm x 31µm
design flow	digital (fully automated)
gate count	181

What You Will Be Able to Do in a Few Years...

Comparison table and summary (best performance in bold)

specification		[3]	[4]	This work
process		90nm	32nm	28nm
area (F^2, with F=min. feature size)		$247 \cdot 10^6$	**$43 \cdot 10^6$** *	$167 \cdot 10^6$
EQ scalable		NO	NO	**YES**
ADC on chip		NO (fully analog)	NO	YES
sampling rate (kS/s)		N.A.	16	8
interval between decisions (ms)		< 100	10	8†
energy (nJ/frame)		600 (10.6X)	500* (8.9X)*	**56.5 - 182.4** (1 - 3.2X)
VAD classification quality	accuracy	87% ‡	97%	85.8% - 87.6%
	F-measure ‡	87.3%	N.A. §	83.4% ‖
SNR in adopted benchmark (dB)		12	N.A. §	10

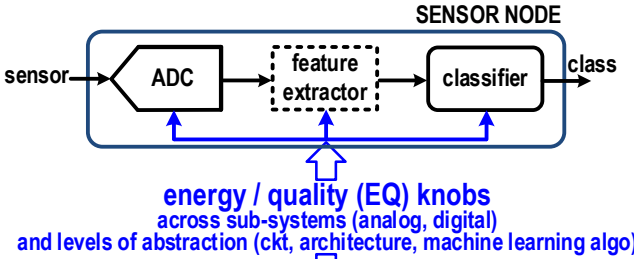
* analog interface is not included

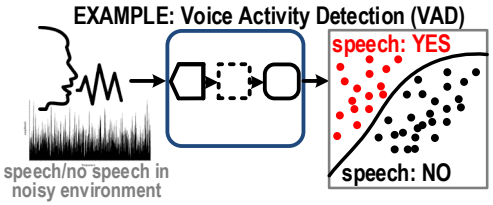
† shorter interval between decisions means finer temporal granularity in classification, increasing the opportunities to save energy in the subsequent blocks (e.g., speech recognition)

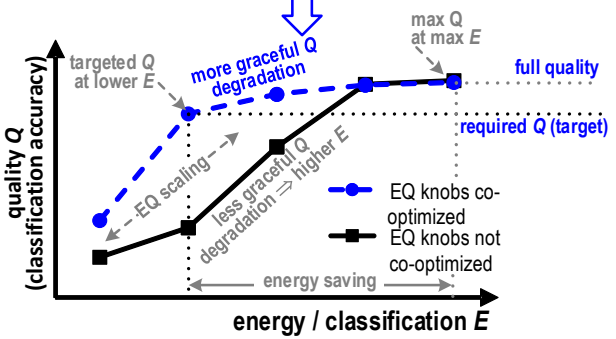
‡ assuming 50% true positives and 50% true negatives

§ no information on benchmark is available

‖ at OSR=512

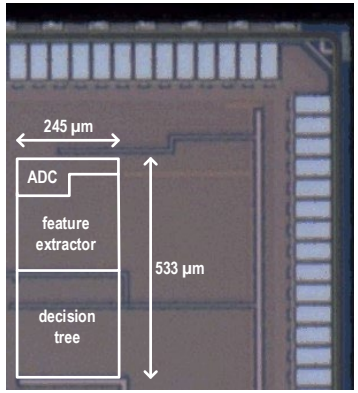






LOWER QUALITY OFTEN ACCEPTABLE

level	example
APPLICATION	automated light control in the presence of speech needs lower accuracy than security
CONTEXT	lower accuracy is enough if uninterrupted speech was detected for a long period
DATASET	highest quality is not useful in noisy environment (max accuracy is degraded anyway)



ADC		voltage	1 V
		frequency	< 4.1 MHz (oversampling clock)
			8 kHz (downsampling clock)
		area	0.015 mm²
		integrator RC time constant	40 µs
FE	FFT	frequency	8 kHz
		architecture	64-pt SDF radix-2
		bit width	23 bits
	PSD	frequency	512 kHz
	overall	voltage	0.5 V
		area	0.046 mm²
DT		voltage	0.5 V
		frequency	8 kHz
		area	0.069 mm²
		memory size	10.5 kb
overall		area	0.13 mm²
		power	7.06 – 22.8 µW

What You Will Be Able to Do in a Few Weeks...

The limit is our imagination and creativity...

Unleash them (please)

Let Us Play a Bit…

o we use 2's complement representation in c systems?

re we interested in minimizing Boolean func

y do we learn about digital systems, and FPG

op

ich interesting applications can we apply wh learned?

l you contribute to our society with the know
are gaining in this module?

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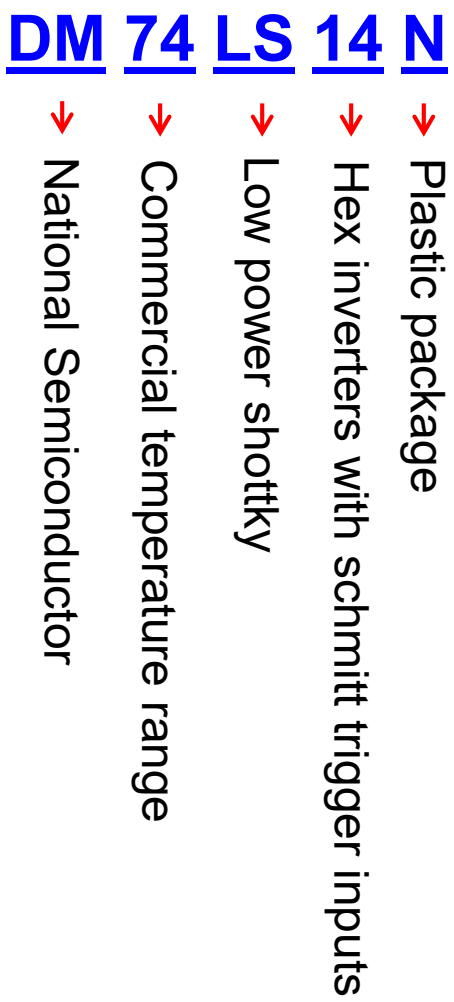
Commercial logic families

- 74xxx Series
  - **TTL** family (**T**ransistor-**T**ransistor **L**ogic)
  - Use Bipolar or CMOS technology
- Name convention
  - 1st field: 2 or 3 letters → Manufacturer (sometimes omitted)
  - 2nd field: 74 → Commercial temperature range (54 → Military)
  - 3rd field: 4 letters → Logic sub-family
  - 4th field: 2 or more digits → Type of device
  - 5th field: Type of package or other information (sometimes omitted)

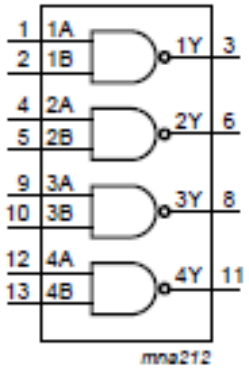


74 series Logic Sub-families (3rd field)

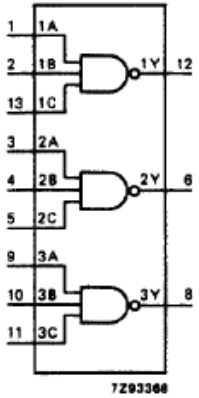
- TTL (Bipolar)
  - 74L → Low power
  - 74H → High speed
  - 74LS → Low power Schotty
  - 74AS → Advanced low power schotty
  - 74ALS → Advanced low power schotty
  - .....
- CMOS (not TTL, but retains some compatibility)
  (same part numbers as bipolar are retained to identify the function)
  - 74C → CMOS 4-15V
  - 74HC → High speed
  - 74AC → Advanced CMOS
  - 74LVC → Low voltage, 1.65 to 3.3V
  - 74LVX → 3.3V with 5V tolerant inputs
  - ……

Some 74 series Logic gates

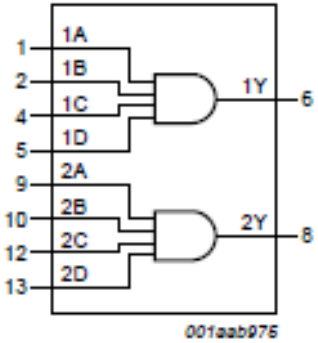
7400 (74HC00)
(Quad 2-input NAND gate)



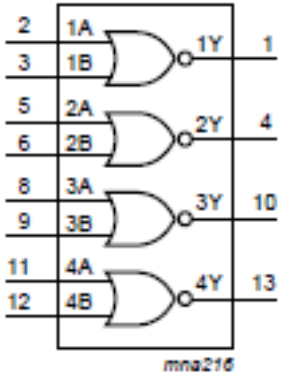
7410(74HC10)
(Dual 3-input AND gate)



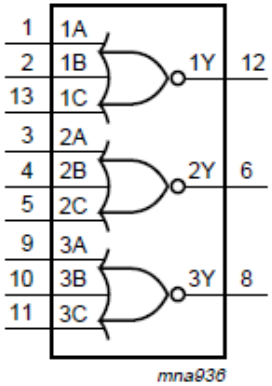
7421(74HC21)
(Dual 4-input AND gate)



7402(74HC02)
(Quad 2-input NOR gate)



7427(74HC27)
(Quad 3-input NOR gate)



7404(74HC04)
(Hex inverters)