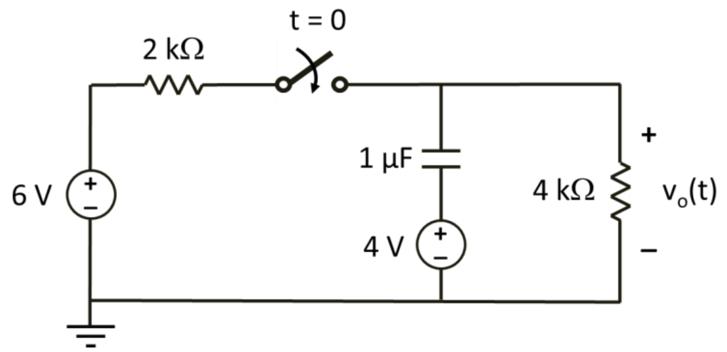
The Hong Kong University of Science and Technology
Department of Electronic and Computer Engineering

ELEC2400 | **ELECTRONIC CIRCUITS** | FALL 2021-22

HOMEWORK 5 SOLUTION

Q1. Assume the switch has been open for a long time. The switch is closed at t = 0. Find the equation of the voltage $v_o(t)$ for t > 0.



In the steady state up to $t = 0^-$, the capacitor behaves like an open circuit. No current goes through the 4-kΩ resistor. Hence, $v_o(0^-) = 0$ V.

At $t = 0^+$, the capacitor voltage is unchanged. Same is true for the 4-V source. Hence, $v_o(0^+) = v_o(0^-) = 0$ V.

In the steady state when $t \to \infty$, the capacitor behaves like an open circuit again.

$$v_o(\infty) = 6\left(\frac{4}{2+4}\right) = 4\text{ V}$$

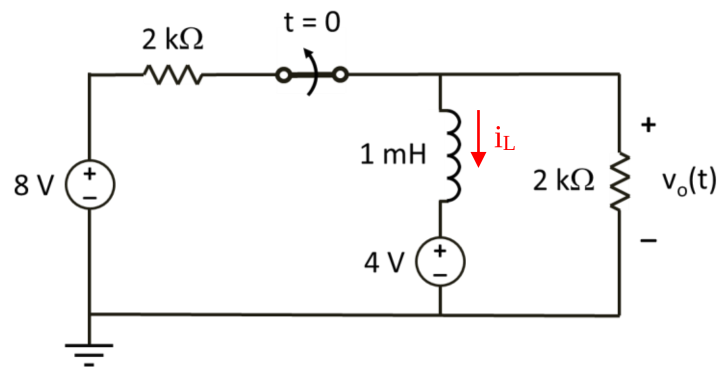
Time constant:

$$\tau = R_{eq}C = (2\text{k}||4\text{k})1\mu = 1.333\text{ ms}$$

Therefore, for t > 0

$$v_o(t) = 0 + (4-0)\left(1 - e^{-\frac{t}{1.333\text{m}}}\right) = 4(1 - e^{-750t})\text{ V}$$

Q2. Assume the switch has been closed for a long time. The switch is opened at t = 0. Find the equation of the voltage $v_o(t)$ for t > 0.



In the steady state up to t = 0^-, the inductor behaves like a short circuit. Hence, $v_o(0^-) = 4$ V. Furthermore, KCL at the node v_o yields $i_L(0^-) = 0$ A.

At t = 0^+, the inductor current is unchanged. Hence, $i_L(0^+) = i_L(0^-) = 0$ A. Moreover, the switch is already opened. There is no current going through the 2-kΩ resistor on the right and $v_o(0^+) = 0$ V.

In the steady state when $t \to \infty$, the inductor behaves like a short circuit again and $v_o(\infty) = 4$ V.

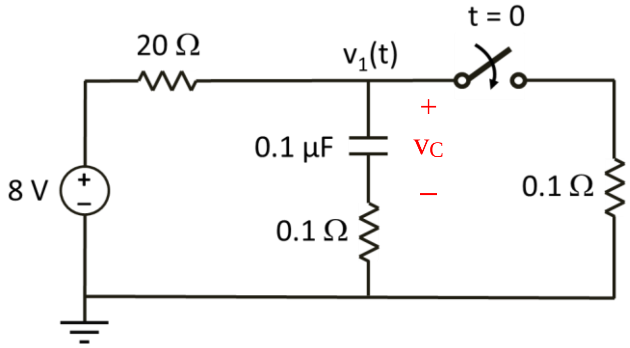
Time constant: only the 2-kΩ resistor on the right takes part in the transient.

$$\tau = L/R_{eq} = 1\text{m}/2\text{k} = 0.5\ \mu\text{s}$$

Therefore, for t > 0

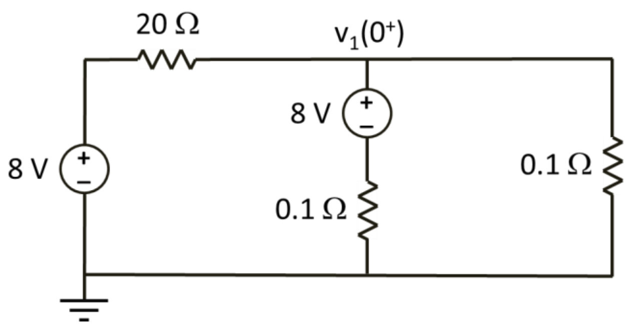
$$v_o(t) = 0 + (4-0)\left(1 - e^{-\frac{t}{0.5\mu}}\right) = 4(1 - e^{-2000000t})\ \text{V}$$

Q3. Assume the switch has been open for a long time. The switch is closed at t = 0.
(a) Find the equation of the voltage $v_1(t)$ for t > 0.
(b) Plot $v_1(t)$ as a function of time starting from t < 0.



In the steady state up to t = 0^-, the capacitor behaves like an open circuit. No current goes through any resistor. Hence, $v_1(0^-) = v_C(0^-) = 8$ V.

At t = 0^+, the capacitor voltage is unchanged. Hence, $v_C(0^+) = v_C(0^-) = 8$ V. The capacitor behaves momentarily as an 8-V battery and the following circuit diagram applies



Apply KCL to the node v_1,

$$\frac{v_1 - 8}{20} + \frac{v_1 - 8}{0.1} + \frac{v_1}{0.1} = 0$$

$$v_1 - 8 + 200v_1 - 1600 + 200v_1 = 0$$

$$401v_1 = 1608$$

$$v_1(0^+) = 4.0100 \text{ V}$$

In the steady state when $t \to \infty$, the capacitor behaves like an open circuit again.

$$v_1(\infty) = 8\left(\frac{0.1}{20 + 0.1}\right) = 0.0398 \text{ V}$$

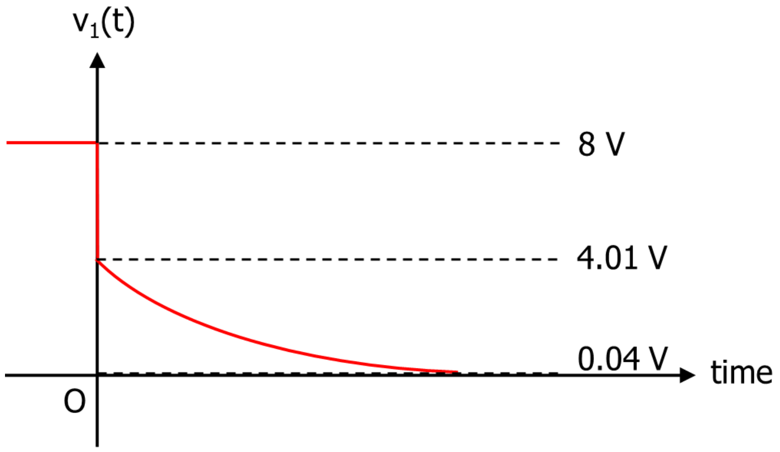
Time constant:

$$\tau = R_{eq}C = (0.1 + 20||0.1)0.1\mu = 0.01995 \text{ µs}$$

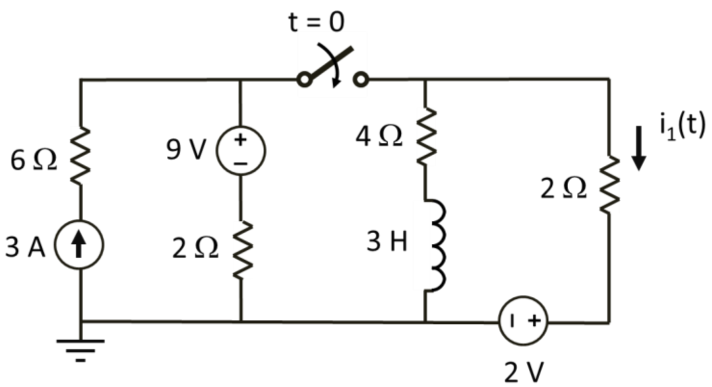
Therefore, for $t > 0$

$$v_1(t) = 0.0398 + (4.0100 - 0.0398)e^{-\frac{t}{0.01995\mu}} = 0.04 + 3.97e^{-50100000t} \text{ V}$$

Following is a plot of $v_1(t)$ starting from $t < 0$.

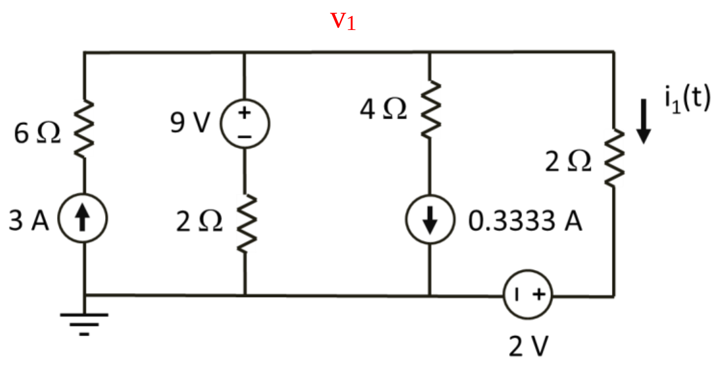


Q4. Assume the switch has been open for a long time. The switch is closed at t = 0.
(a) Find the equation of the current $i_1(t)$ for $t > 0$.
(b) Plot $i_1(t)$ as a function of time starting from $t < 0$.



In the steady state up to $t = 0^-$, the inductor behaves like a short circuit. Hence, $i_1(0^-) = -2/6 = -0.3333$ A.

At t = 0^+, the inductor current is unchanged. The inductor behaves momentarily as a 0.3333-A current source and the following circuit diagram applies



Apply KCL to the node v_1, noting that $v_1 = 2i_1 + 2$,

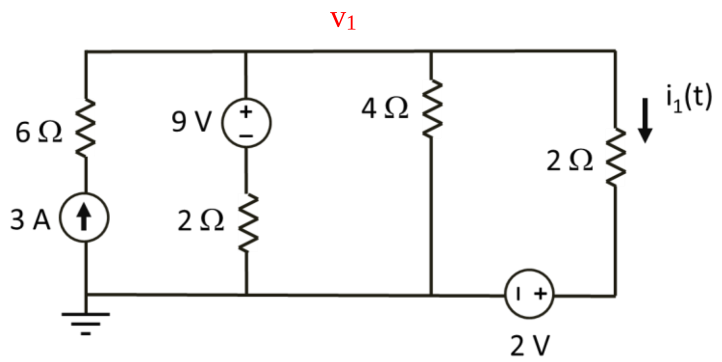
$$-3 + \frac{(2i_1 + 2) - 9}{2} + 0.3333 + i_1 = 0$$

$$-6 + 2i_1 + 2 - 9 + 0.6667 + 2i_1 = 0$$

$$4i = 12.3333$$

$$i_1(0^+) = 3.083\ \text{A}$$

In the steady state when t → ∞, the inductor behaves like a short circuit again and the following circuit diagram applies



Apply KCL to the node v_1, noting that $v_1 = 2i_1 + 2$,

$$-3 + \frac{(2i_1 + 2) - 9}{2} + \frac{2i_1 + 2}{4} + i_1 = 0$$

$$-12 + 4i_1 + 4 - 18 + 2i_1 + 2 + 4i_1 = 0$$

$$10i_1 = 24$$

$$i_1(\infty) = 2.4\ \text{A}$$

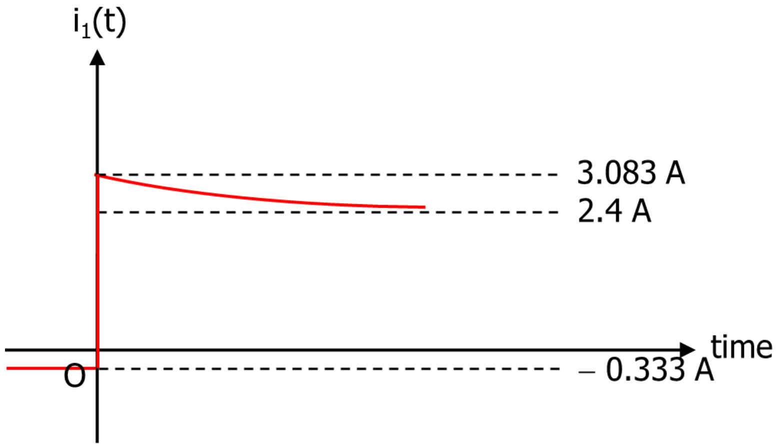
Time constant: the 6-Ω resistor is open-circuited by the zeroed-out current source in the R_{eq} calculation.

$$\tau = L/R_{eq} = 3/(4 + 2||2) = 3/(4 + 1) = 0.6\ \text{s}$$

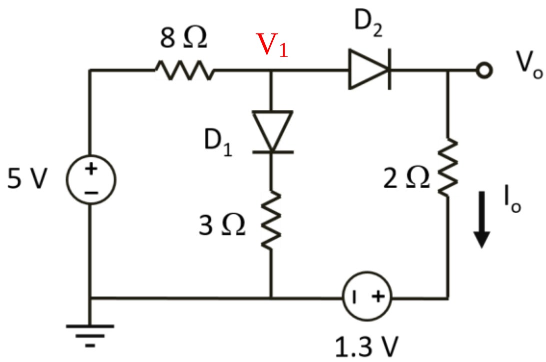
Therefore, for t > 0

$$i_1(t) = 2.4 + (3.083 - 2.4)e^{-\frac{t}{0.6}} = 2.4 + 0.683e^{-1.67t} \text{ V}$$

Following is a plot of $i_1(t)$ starting from t < 0.



Q5. Find V_o and I_o in the circuit below with
(i) ideal diode model,
(ii) offset diode model (V_F = 0.5 V).



(i) Assume both diodes are ON. KCL at the node V_1 yields

$$\frac{V_1 - 5}{8} + \frac{V_1}{3} + \frac{V_1 - 1.3}{2} = 0$$

$$3V_1 - 15 + 8V_1 + 12V_1 - 15.6 = 0$$

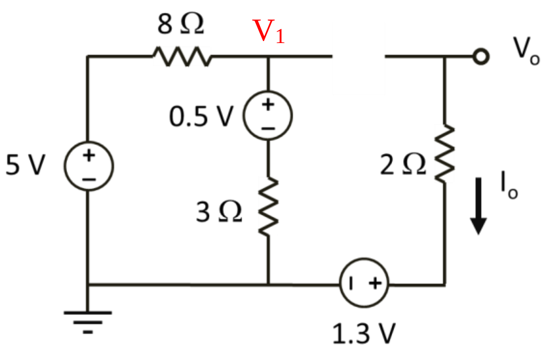
$$23V_1 = 30.6$$

$$V_1 = 1.3304 \text{ V} = V_o$$

$$I_o = \frac{V_o - 1.3}{2} = \frac{1.3304 - 1.3}{2} = 0.0152 \text{ A} > 0$$

The results for V_1, V_o and I_o are consistent with both diodes being ON.

(ii) Assume D_1 ON and D_2 OFF. The circuit diagram looks like this



from which

$$V_o = 1.3\ \text{V}$$
$$I_o = 0\ \text{A}$$

As a check, apply KCL to the node V_1,

$$\frac{V_1 - 5}{8} + \frac{V_1 - 0.5}{3} = 0$$

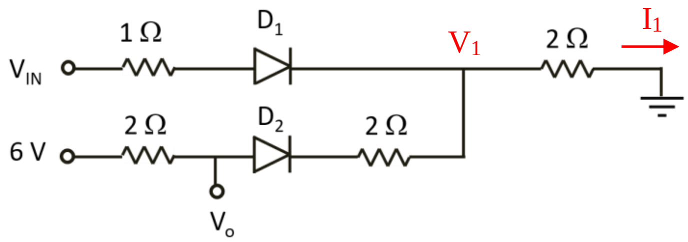
$$3V_1 - 15 + 8V_1 - 4 = 0$$

$$11V_1 = 19\ \text{V}$$

$$V_1 = 1.73\ \text{V} < V_o + V_F$$

This is consistent with D_2 being OFF.

Q6. Plot V_o as a function of V_{IN} for V_{IN} from – 5 V to 25 V in the circuit with
(i) ideal diode model,
(ii) offset diode model (V_F = 0.5 V).



Qualitatively speaking, when V_{IN} starts from low, D_1 is OFF and V_1 is set by the 6-V source. When V_{IN} gets high enough, both D_1 and D_2 are ON and V_1 is set by both V_{IN} and the 6-V source. Finally, when V_{IN} gets sufficiently high, D_2 is OFF and V_1 is set by V_{IN} only.

(i) Ideal diode model:
(a) When D_1 is OFF and D_2 is ON, V_o = 4 V and V_1 = 2 V. This is true for

$$-5\ \text{V} \le V_{IN} < 2\ \text{V}$$

(b) When D_1 is ON and D_2 is OFF, $V_o = 6\ \text{V} < V_1 = 2V_{IN}/3$. This is therefore true for

$$V_{IN} > 6 \times 3/2 = 9\ \text{V}$$

We now have everything we need to do the plot. The following are optional.

(c) $2\text{ V} \le V_{IN} \le 9\text{ V}$, both diodes are ON. Apply KCL to the node V_1,

$$\frac{V_1 - V_{IN}}{1} + \frac{V_1 - 6}{4} + \frac{V_1}{2} = 0$$

$$4V_1 - 4V_{IN} + V_1 - 6 + 2V_1 = 0$$

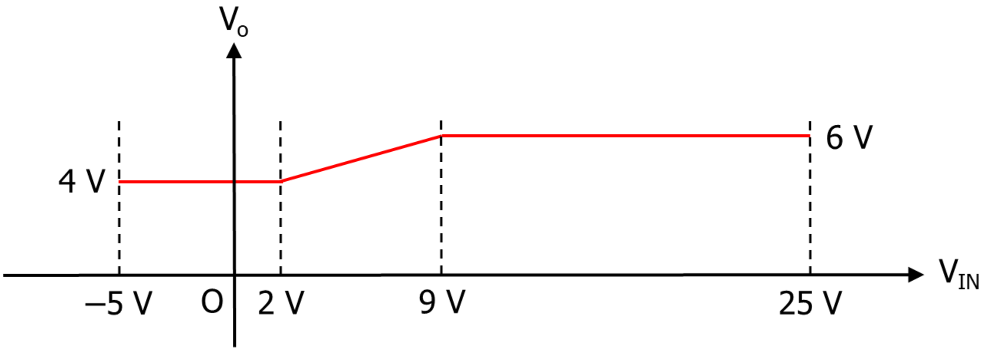
$$7V_1 = 4V_{IN} + 6$$

$$V_1 = \frac{4V_{IN} + 6}{7} \tag{1}$$

Notice that V_o is the center tap between the 6-V source and V_1, and also from (1)

$$V_o = \frac{6 + V_1}{2} = \frac{6 + \frac{4V_{IN} + 6}{7}}{2} = \frac{2}{7}V_{IN} + \frac{24}{7}$$

Following is a plot of V_o vs. V_{IN}.



(ii) Offset diode model ($V_F = 0.5$ V):

(a) When D_1 is OFF and D_2 is ON,

$$I_1 = \frac{6 - 0.5}{2 + 2 + 2} = 0.9167\text{ A}$$

yielding

$$V_1 = 2I_1 = 1.833\text{ V}$$

$$V_o = 6 - 2I_1 = 4.167\text{ V}$$

This is true for

$$-5\text{ V} \le V_{IN} < V_1 + V_F = 1.833 + 0.5 = 2.333\text{ V}$$

(b) When D_1 is ON and D_2 is OFF,

$$I_1 = \frac{V_{IN} - 0.5}{1 + 2}$$

yielding

$$V_1 = 2I_1 = \frac{2}{3}V_{IN} - \frac{1}{3}$$

This is true for $V_o = 6\text{ V} < V_1 + V_F$, or

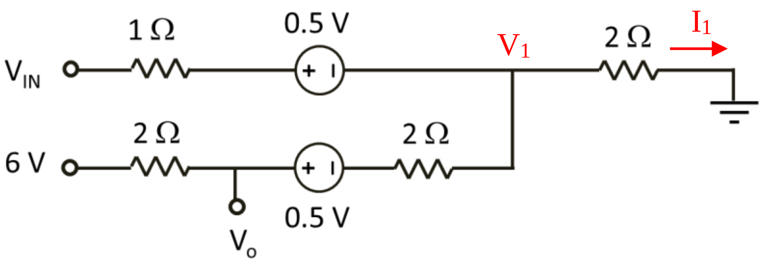
$$\left(\frac{2}{3}V_{IN} - \frac{1}{3}\right) + 0.5 > 6$$

$$2V_{IN} - 1 + 1.5 > 18$$

$$V_{IN} > 8.75 \text{ V}$$

We now have everything we need to do the plot. The following are optional.

(c) For $2.333 \text{ V} \leq V_{IN} \leq 8.75$ V, both diodes are ON. The circuit diagram looks like



Apply KCL to the node V_1,

$$\frac{V_1 + 0.5 - V_{IN}}{1} + \frac{V_1 + 0.5 - 6}{4} + \frac{V_1}{2} = 0$$

$$4V_1 + 2 - 4V_{IN} + V_1 + 0.5 - 6 + 2V_1 = 0$$

$$7V_1 = 4V_{IN} + 3.5$$

$$V_1 = \frac{4V_{IN} + 3.5}{7} \tag{2}$$

Apply KCL to the node V_o and also from (2)

$$\frac{V_o - 6}{2} + \frac{V_o - 0.5 - V_1}{2} = 0$$

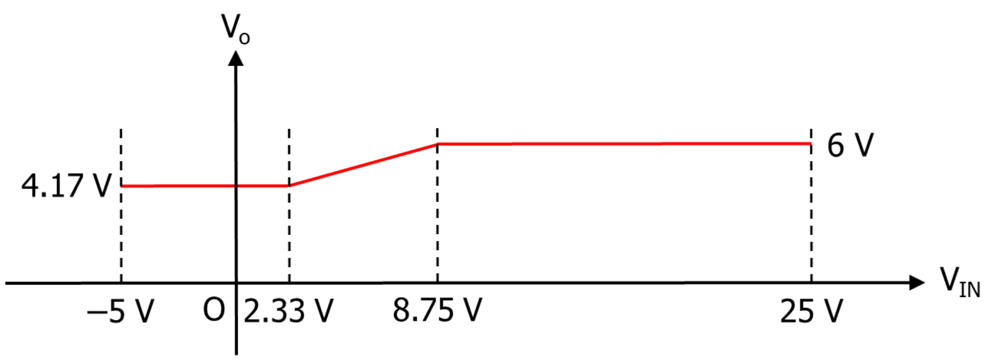
$$V_o - 6 + V_o - 0.5 - \frac{4V_{IN} + 3.5}{7} = 0$$

$$7V_o - 42 + 7V_o - 3.5 - 4V_{IN} - 3.5 = 0$$

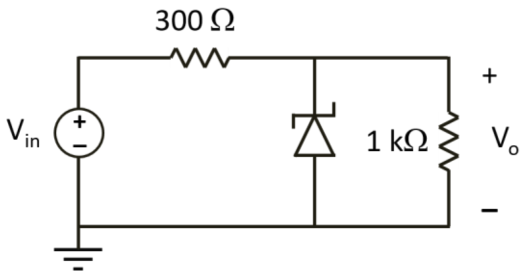
$$14V_o = 4V_{IN} + 49$$

$$V_o = 0.2857V_{IN} + 3.5$$

Following is a plot of V_o vs. V_{IN}.



Q7. In the figure, it shows a Zener diode voltage regulator circuit (V_{Z0} = 5.6 V, R_Z = 10 Ω).
(a) Determine the output voltage V_o if V_{IN} = 6.5 V.
(b) Plot V_o as the function of V_{IN} for 6 V < V_{IN} < 8 V.



Case 1: Zener diode is OFF

$$V_o = V_{in}\left(\frac{1\text{k}}{300 + 1\text{k}}\right) = 0.76923V_{in}$$

This is true so long as $V_o < 5.6$ V, which means $V_{in} < 7.28$ V.

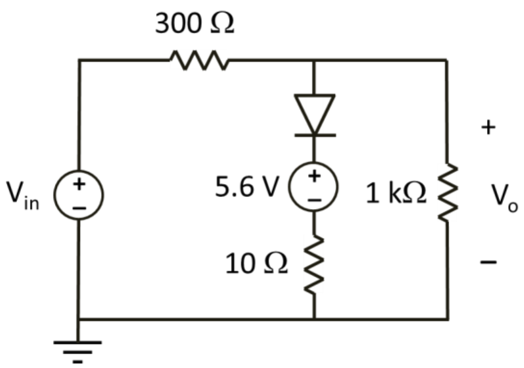
When $V_{in} = 6$ V, $V_o = 4.615$ V.

When $V_{in} = 6.5$ V, $V_o = 5$ V.

When $V_{in} = 7.28$ V, $V_o = 5.6$ V.

Case 2: Zener diode is ON. This happens when $V_o \geq 5.6$ V, which means $V_{in} \geq 7.28$ V.

Replacing the Zener diode by its circuit model, the circuit now looks like this



Apply KCL to the node V_o,

$$\frac{V_o}{1\text{k}} + \frac{V_o - 5.6}{10} + \frac{V_o - V_{in}}{300} = 0$$

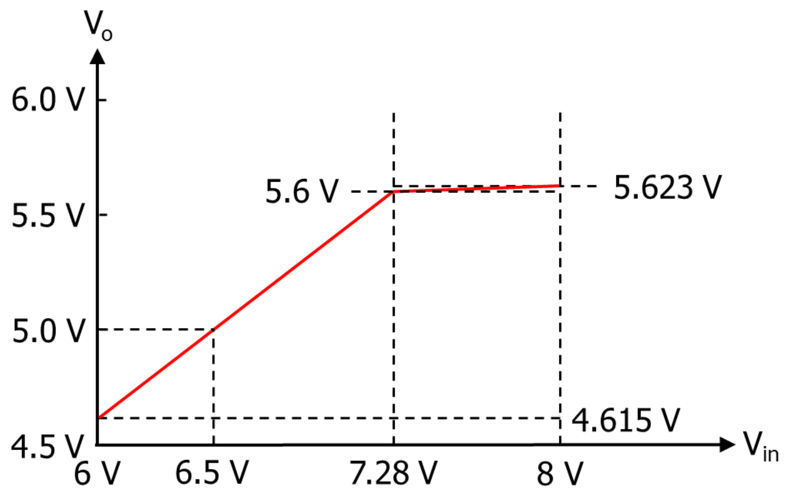
$$3V_o + 300V_o - 1680 + 10V_o - 10V_{in} = 0$$

$$313V_o = 1680 + 10V_{in}$$

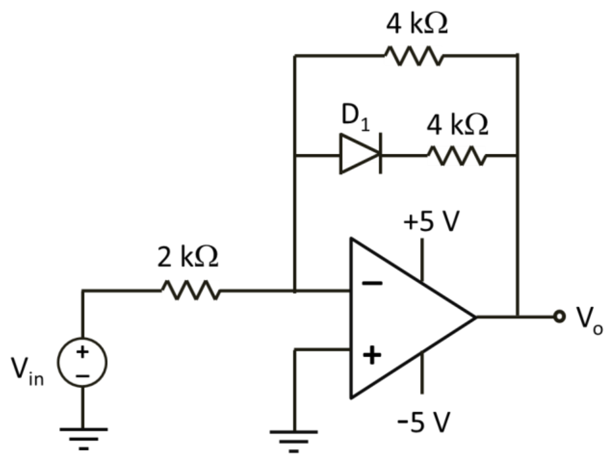
$$V_o = 5.367412 + 0.031949V_{in}$$

When $V_{in} = 8$ V, $V_o = 5.623$ V.

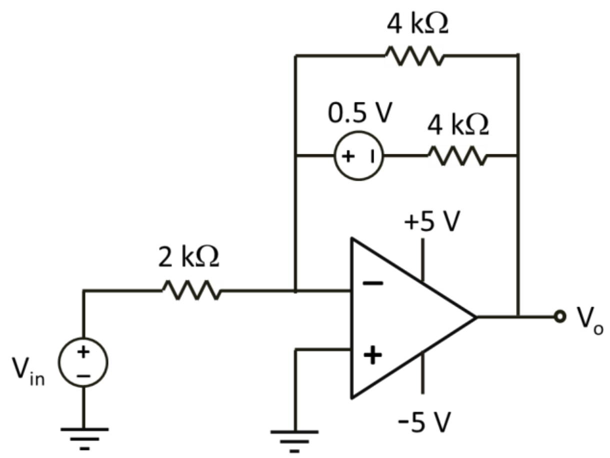
Following is a plot of V_o vs. V_{in}. Once $V_o \geq 5.6$ V, it is regulated to within a narrow range.



Q8. Find V_o assuming ideal op amp and offset diode model ($V_F = 0.5$ V) for the case:
(i) when $V_{in} = 4$ V,
(ii) when $V_{in} = -4$ V.



(i) when $V_{in} = 4$ V, D_1 is ON and the circuit diagram looks like this



Apply KCL to the node V_-, which is equal to V_+ at 0 V.

$$\frac{V_o}{4\text{k}} + \frac{V_o + 0.5}{4\text{k}} = -\frac{V_{in}}{2\text{k}}$$

$$V_o + V_o + 0.5 = -2V_{in}$$

$$V_o = -V_{in} - 0.25 = -4 - 0.25 = -4.25\ \text{V}$$

(ii) when $V_{in} = -4$ V, D_1 is OFF and the circuit is an inverting amplifier with a gain of –2. Hence, V_o would like to go to 8 V. However, the op amp would be saturated, limiting output to

$$V_o = 5\ \text{V}$$