(T)EE2026

Digital Fundamentals

Introduction

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Instructors

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  - see EE2026 webpage on LumiNUS in a few days

Module introduction

Contents

- **Part 1**
  - Number systems
  - Boolean Algebra and logic gates
  - Hardware Description Languages: Verilog
  - Gate-level design and minimization + Verilog
  - Combinational logic circuits and design + Verilog

- **Part 2**
  - Sequential logic circuits + Verilog
  - Combining combinational/sequential building blocks + Verilog
  - Finite State Machines+ Verilog

Course Description

- First course on digital systems
- Introduces fundamental digital logic, digital circuits, and programmable devices
- The course also provides an overview of computer systems
- This course provides students with an understanding of the building blocks of modern digital systems and methods of designing, simulating and realizing such systems
- The emphasis of this module is on understanding the fundamentals of **digital design across different levels of abstraction** using Hardware Description Languages
- Developing valuable design skills for the design of digital systems through FPGAs and state-of-the-art CAD tools, as required by the job market (**exciting projects**)

Expected Learning Outcomes

- **Expected learning outcome (Part 1)**
  - *Be able to perform conversion* between binary, octal, hexadecimal and decimal number systems, and *solve simple problems;*
  - *Understand* Boolean Algebra, and *manipulate and simplify* Boolean functions using theorems and postulates;
  - *Be able to design simple combinational logic circuits* based on Truth table and Karnaugh Map
  - *Be able to design complex combinational logic circuits* using Hardware Description Languages (Verilog) and/or combinational building blocks/IPs
  - *Be able to simulate complex combinational blocks* and verify their proper functionality through behavioural simulation
  - *Be able to design combinational logic circuits* for practical problems/applications

Expected Learning Outcomes

- **Expected learning outcome (Part-2)**
  - *Be able to describe simple sequential logic circuits* based on state transition diagrams
  - *Be able to design complex logic circuits* using Hardware Description Languages (Verilog) and/or sequential/combinational building blocks/IPs
  - *Be able to simulate complex blocks* and verify their proper functionality through behavioural simulation
  - *Be able to design complex logic circuits* for practical problems/applications

Module organization

- **Part-1**
  - 10 lectures (2+1 hours/week)
  - 4 tutorial sessions starting in Week 2 (Check your group and venue)
  - 2 Laboratory sessions, starting in Week 3 (attendance is compulsory)

- **Part-2**
  - 12 lectures (2+1 hours/week)
  - 5 tutorial sessions (Check your group and venue)
  - 4 Laboratory sessions, of which 4 are devoted to the final project (full system on FPGA), starting in Week 8

Module Assessment

- **Part 1 (32.5%)**
  - Lab assignment 1 (combinational circuits): 12.5%
  - Mid-term quiz: 20%
- **Part 2 (32.5%)**
  - Lab assignment 2 (sequential circuits): 12.5%
  - Final quiz: 20%
- **Project (35%)**
  - Project basic features (specified) + enhanced features (open-ended): 35%
- **No final exam ☺**

EE2026 Topics (Part I)

Week	Topics	Remark
Week 1	Introduction/ Number systems (L0+L1)	Module introduction, Position number systems, number system conversion, signed numbers. Arithmetic using signed numbers, BCD, addition using BCD.
Week 2	Boolean Algebra/Verilog (L2+L3)	Theorems, Boolean functions, truth table, SOP/POS form, truth table to SOP or POS, minterm/maxterm, canonical form. Gates & truth table, positive/negative logics and conversion, mixed logic. Intro to Verilog (modules, operators, Boolean expressions).
Week 3	Gate-level design & simplification/Verilog (L4)	Karnaugh map, gate-level simplificaton and implementation. Modeling gates and Boolean functions (dataflow).
Week 4	Gate-level Design & Minimization/Verilog (L5)	Design of combinational logic with minimum complexity
Week 5	Complex combinational logic/Verilog and logic families (L6+L7)	Adders, comparators, decoders/encoders, (de)multiplexers, tri-state logic. Modeling combinational logic (behavioral, structural), simulation, synthesis. Logic families

EE2026 Part II

Week	Topics	Remark
Week 6	Intro to sequential elements	D, SR, JK, T flip-flops, resets, and their Verilog description
Week 7	Verilog for sequential circuits	Verilog description methodology and examples of sequential circuits
Week 8	Counters and registers	Custom Counters, Registers, FF Conversion, registers, flip-flop conversion
Week 9	Design methods for counters and registers	Design methods for general counters and registers
Week 10	Introduction to Finite State Machines (FSM)	Synchronous state machines. State machine structures : Mealy & Moore types. Analysis of state machines. State transition diagrams and synthesis. Top-Down design examples
Week 11	FSM design with architectural elements	Combining FSMs with other architectural elements. Verilog description of FSMs. Design examples.

EE2026 Tutorial Schedule (Part I) (possible updates on LumiNUS)

Week	Tutorials	Assignment
WK1	**No tutorial**	
WK2	Tutorial – 1	
WK3	Tutorial – 2	
WK4	Tutorial – 3	
WK5	Tutorial – 4	
WK6	**No tutorial**	
Recess Week		

- For each tutorial, questions will be posted on LumiNUS the week before, the solutions will be published at the end of the same week

EE2026 Tutorial Schedule (Part II) (possible updates on LumiNUS)

Week	Tutorials	Assignment
WK7	Tutorial – 5	
WK8	Tutorial – 6	
WK9	Tutorial – 7	
WK10	Tutorial – 8	
WK11	Tutorial – 9	
WK12	**No tutorial**	
Recess Week		

- For each tutorial, questions will be posted on LumiNUS the week before, the **solutions** will be published at the end of the same week

EE2026 CA Schedule (tentative: see LumiNUS)

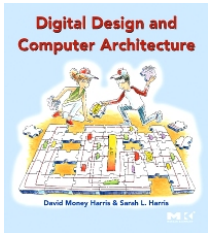
Labs, Projects, Assignments & Quizzes

Lab venue: Digital Electronics (E4-03-07)

Week	Lab (Part 1)	Lab (Part 2)	Quizzes
Week 3	Lab 1 Getting started	-	
Week 4	Lab 2 Combinational circuits		
Week 5		-	
Week 6		Lab 3 – Sequential circuits II	
Recess Week	No lab	No lab	
Week 7		Lab 4 – Sequential circuits II	mid-term quiz
Week 8		Project Lab 1	
Week 9		Project Lab 2	
Week 10		Project Lab 3	
Week 11		(Optional lab session, students work on system integration)	
Week 12		Project Lab 4 / Project evaluation	
Week 13		Project evaluation (if required by class size)	final Quiz

Module information

- **Course materials**
  - LumiNUS (everything about the course)
- **Need help**
  - Discussion Forum under LumiNUS (preferred)
  - Tutors (tutorial questions)
  - TAs and GAs (labs and projects)
    - during lab sessions
  - Face-to-face consultation with lecturer:
    - by appointment, to be taken at the end of each lecture
    - then, the date/time of the appointment is publicized on LumiNUS, so that any student can join
- **Reference book (download from NUS library)**
    - D. Harris, S. Harris, Digital Design and Computer Architecture (1st ed.), Morgan Kaufmann, 2007

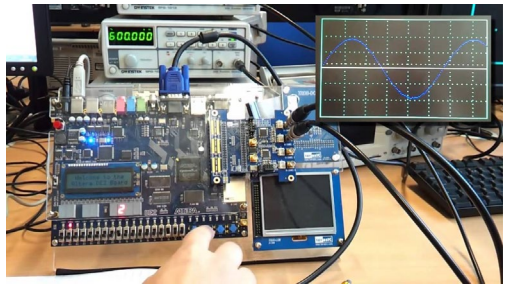


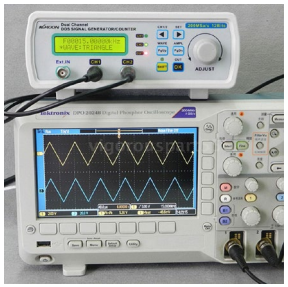
Why studying this module?

- The module is about the fundamentals of digital systems, which is important if you are interested in the design of digital circuits and systems, especially if you plan to specialize in the following areas:
  - Digital integrated circuits (very important)
  - Embedded systems (very important)
- It's the first module about Hardware Description Language (HDL), which is widely used for digital system design and modeling
- You will also learn analytical and problem solving skills through the projects (practical design problems)
- It also serves as prerequisite for other modules at senior levels.

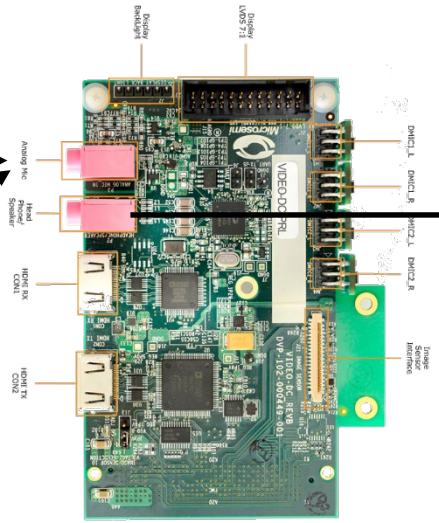
EE2026:
Not Just Another Module…

- **Think & do: strong foundations, real-world design**
  - Industry-relevant project





  - This year: audio processing (in pair, presentation)



your design on FPGA board

EE2026: Quite Unique…

- **Design skills in very high demand**
  - FPGA designer (startups, SMEs, MNCs)
  - Semiconductor industry

AND SO ON AND SO FORTH…

  - Not capital intensive: create YOUR OWN technology/company

EE2026: Quite Unique…

- **Design skills in very high demand**
  - FPGA designer (startups, SMEs, MNCs)
  - Semiconductor industry

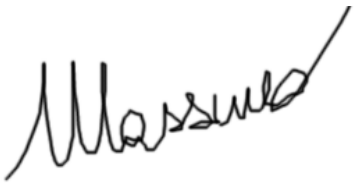
???

Cloud service companies and silicon chip design: are they related at all? Why?

Top

Before Getting Started...

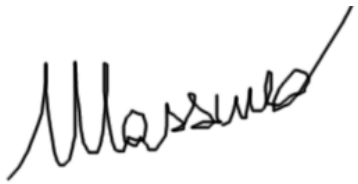
MOTIVATION: WHY ARE WE DOING THIS?



Before Getting Started...

MOTIVATION: WHY ARE WE DOING THIS?

IMPACT: WHAT CAN YOU DO WITH YOUR KNOWLEDGE?

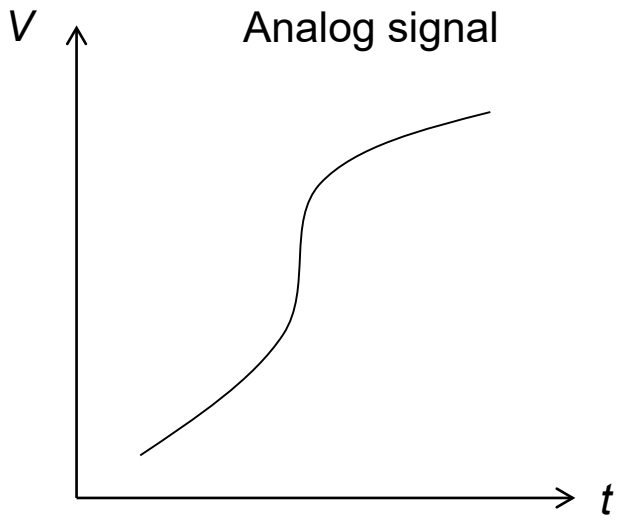


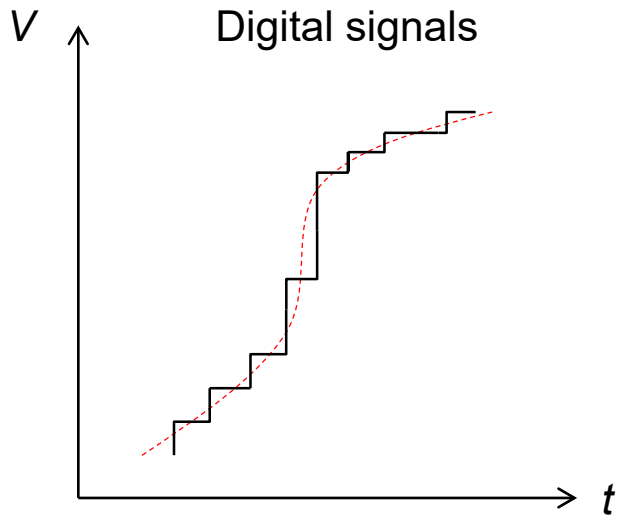
Introduction

1. Analog vs. digital circuit
2. Why digital?
3. Why study this module?

Analog vs. Digital Circuit

- Analog circuit deals with continuous signals
- Digital circuit deals with signals having discrete levels

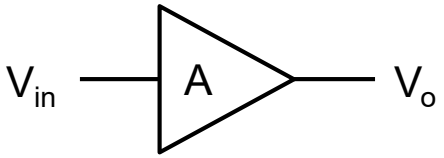




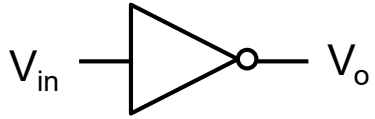
Analog vs. Digital Circuit (cont.)

- Analog circuit is more susceptible to noise
- Digital circuit is a binary system which is much more robust

Analog amplifier



Inverter

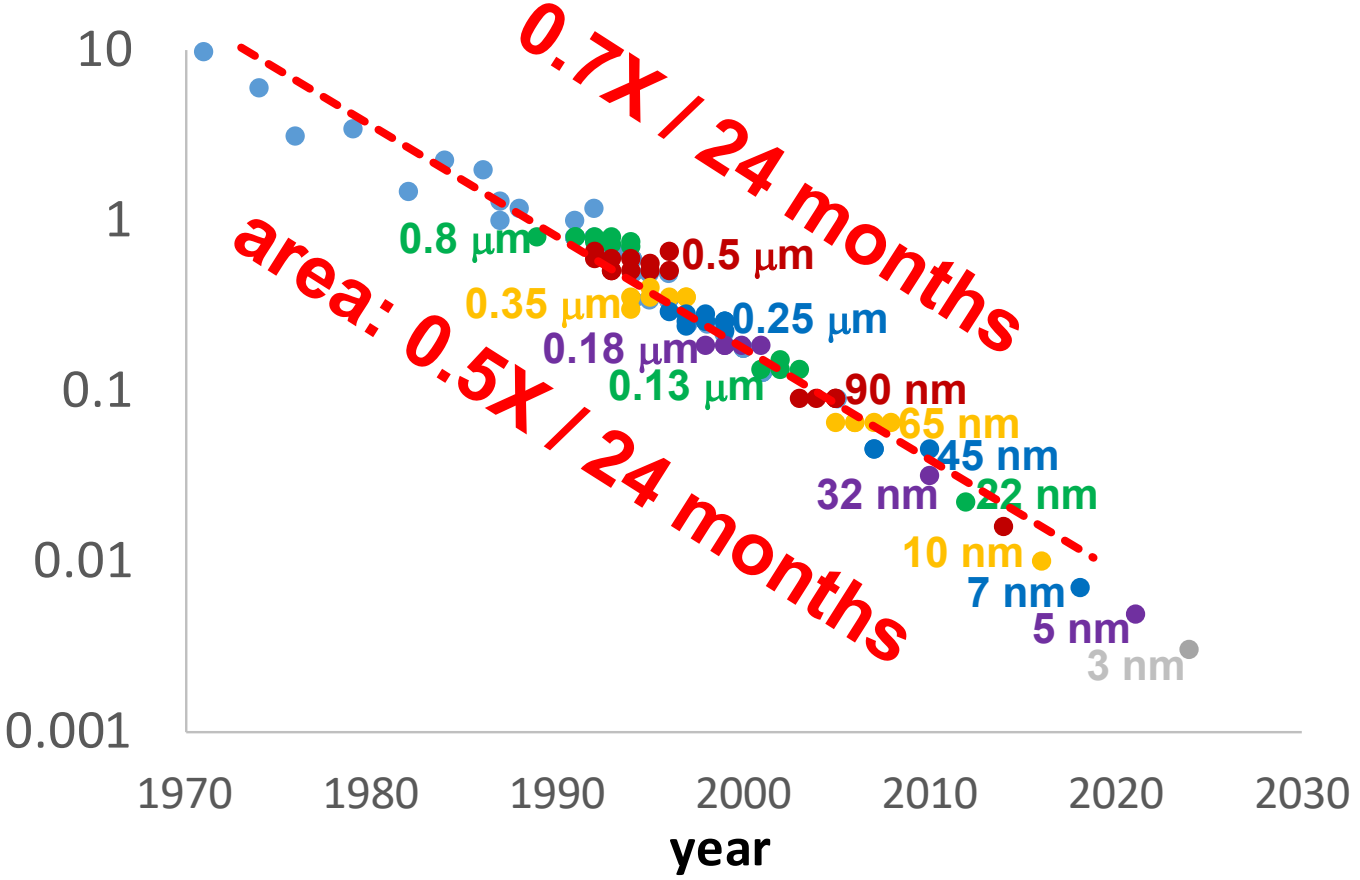


Why digital?

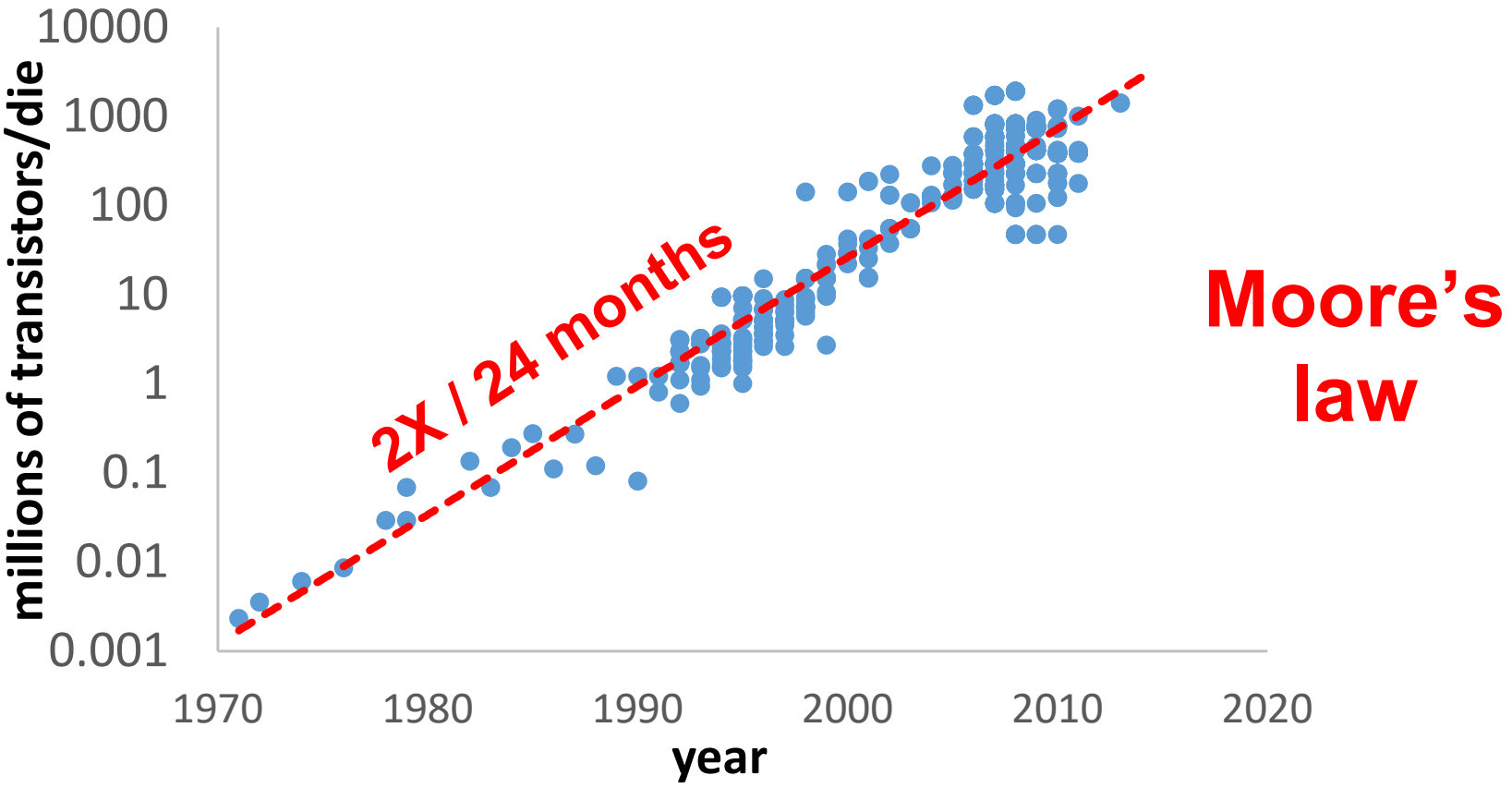
- Robustness (reliability)
- Programmability
- Scalability (in integrated circuit technology)
- Cost

Technology Scaling

- Transistors got smaller over time (at a relentless pace)



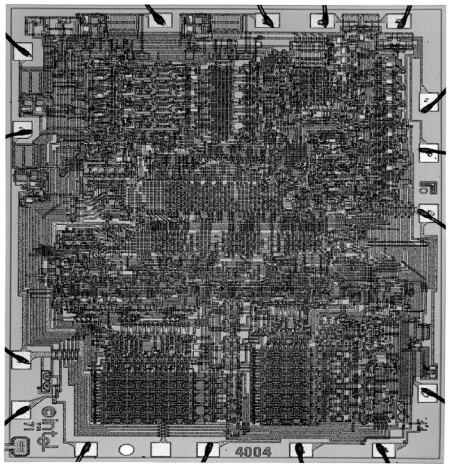
Technology Scaling (cont.)



As more and more transistors can be integrated on a single chip,

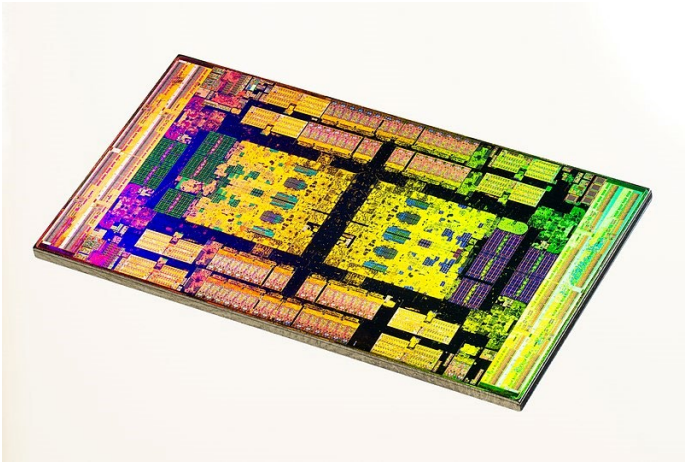
- functionality is increased
- for the same functionality: lower chip area, lower cost per transistor

Technology Scaling (cont.)



1971:

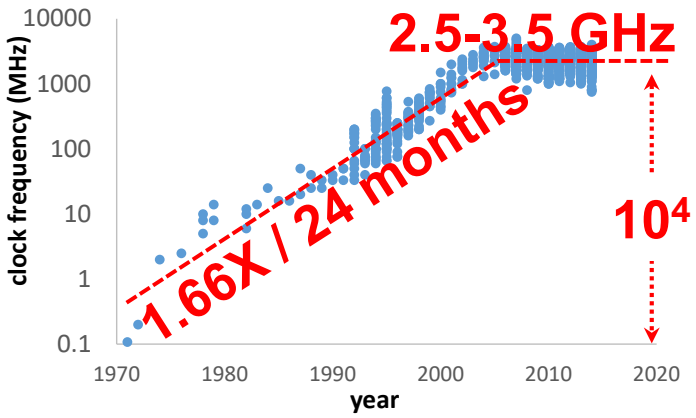
- Intel 4-bit processor in 10 μm PMOS process with 2300 transistors
- Initial clock speed of 108 kHz
- 10μm pMOS technology

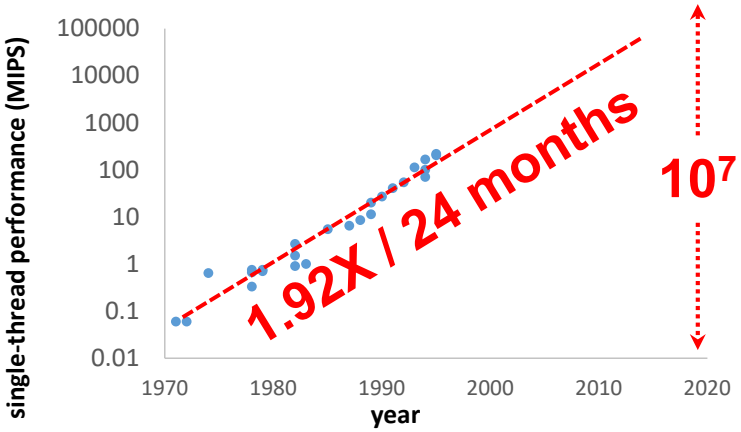


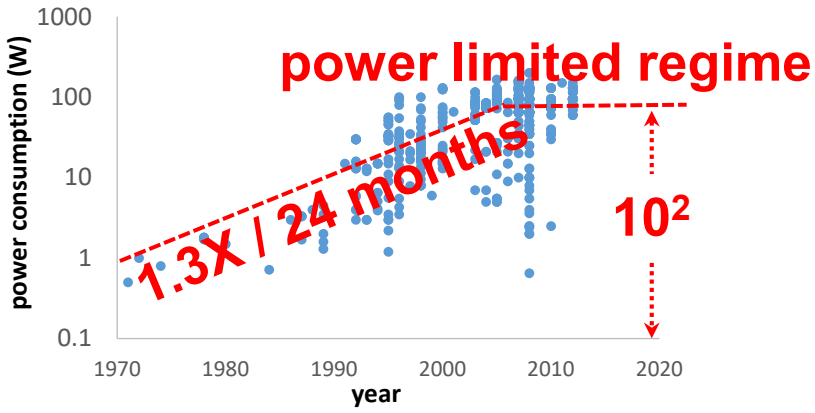
2020:

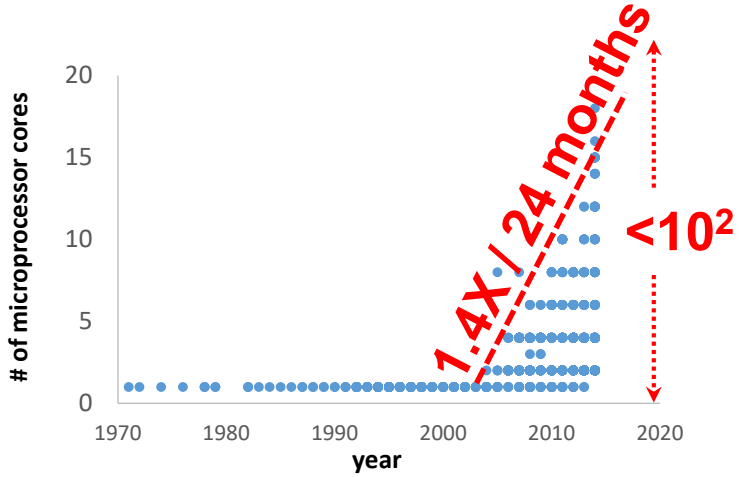
- AMD Epyc Rome 7 nm processor (64 cores, 256MB L3, Zen 2 arch.) 40B transistors
- IBM z15 5.2 GHz clock freq., 12 cores in 14 nm FinFET, 9.2B transistors
- Intel Xeon Platinum 8180 in 14nm CMOS (28 cores), 3.6 GHz, 205 W, 8B transistors
- nVIDIA Ampere, 7nm FinFET, 5 PFLOPS, 54B transistors

Technology Scaling (cont.)









Digital Revolution and Information Age

- 1947 – Invention of transistor
- 1971 – First microprocessor

***Rapid development of digital computing and communication technology brought about the digital revolution and information age**

- 1980s – Personal computers
- 1990s – World Wide Web, digital cameras
- 2000s – Mobile phones, digital TVs, ipod
- 2010 – Smart phones, xPad, cloud computing (accessible everywhere), social networking (constantly connected)
- 2020 – Cloud computing, Internet of things, ultra-low power high-performance mobile computing, ubiquitous computing, immersive computing/augmented reality, gesture recognition...

What type of silicon chips can you find in your pocket (smartphone)? What function do they perform?

Example in Your Pocket (Today)

Application Processor (AP) (microprocessor cores, GPU, memory, video processing…)

Image sensor + pre-processing

LTE modem

Touchscreen controller

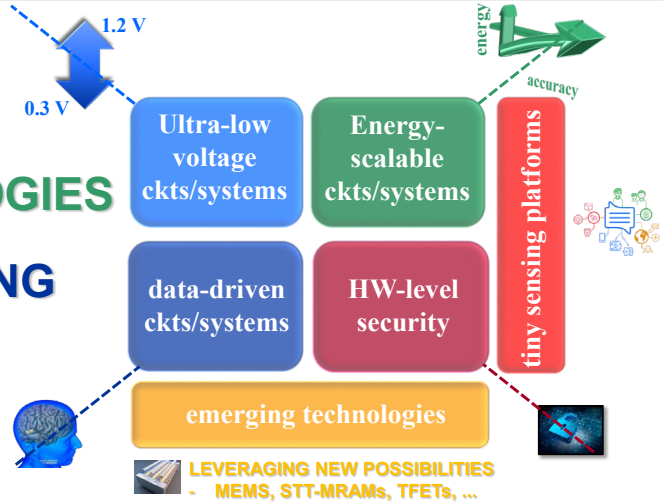
Image sensor + pre-processing

smart battery (charge, wearing, genuineness)

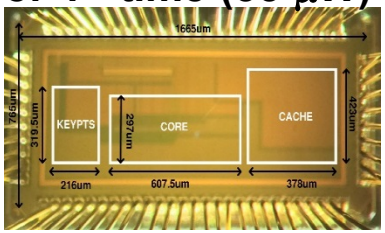
GPS, WiFi, DRAM, Flash, RF transceiver, Power Management, NFC, audio, display power management, FPGA, battery charger, compass, other sensors

Example Available Everywhere (Tomorrow) from GREEN IC Group

http://www.green-ic.org

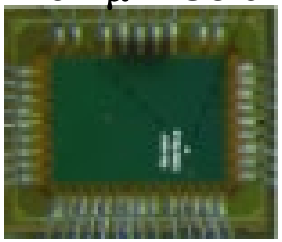


computer vision in IoT for 1st time (55 μW)

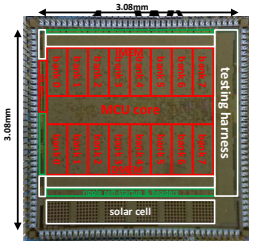


most (cyber)secure "silicon fingerprint"

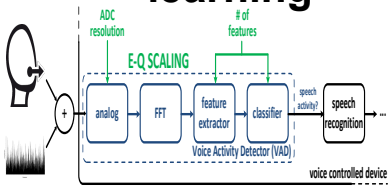
AES in 100 nW (0.1μmx0.1μm solar cell)



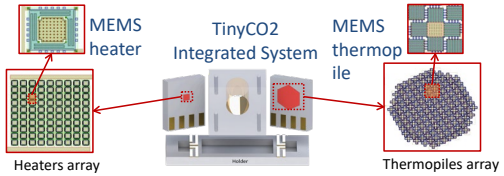
1st lunar-powered chip (power



sub-μW machine learning



1st mm-scale CO2 sensor (perpetual operation)



PRESS

PCWorld ECN HOT CHIPS PHYS.ORG

1st book on chip design for IoT

Continuing Our Conversation

connect over Zoom for consultation and questions right after every 2-h lecture

(see LumiNUS under the "Conferencing" menu)