1. Description

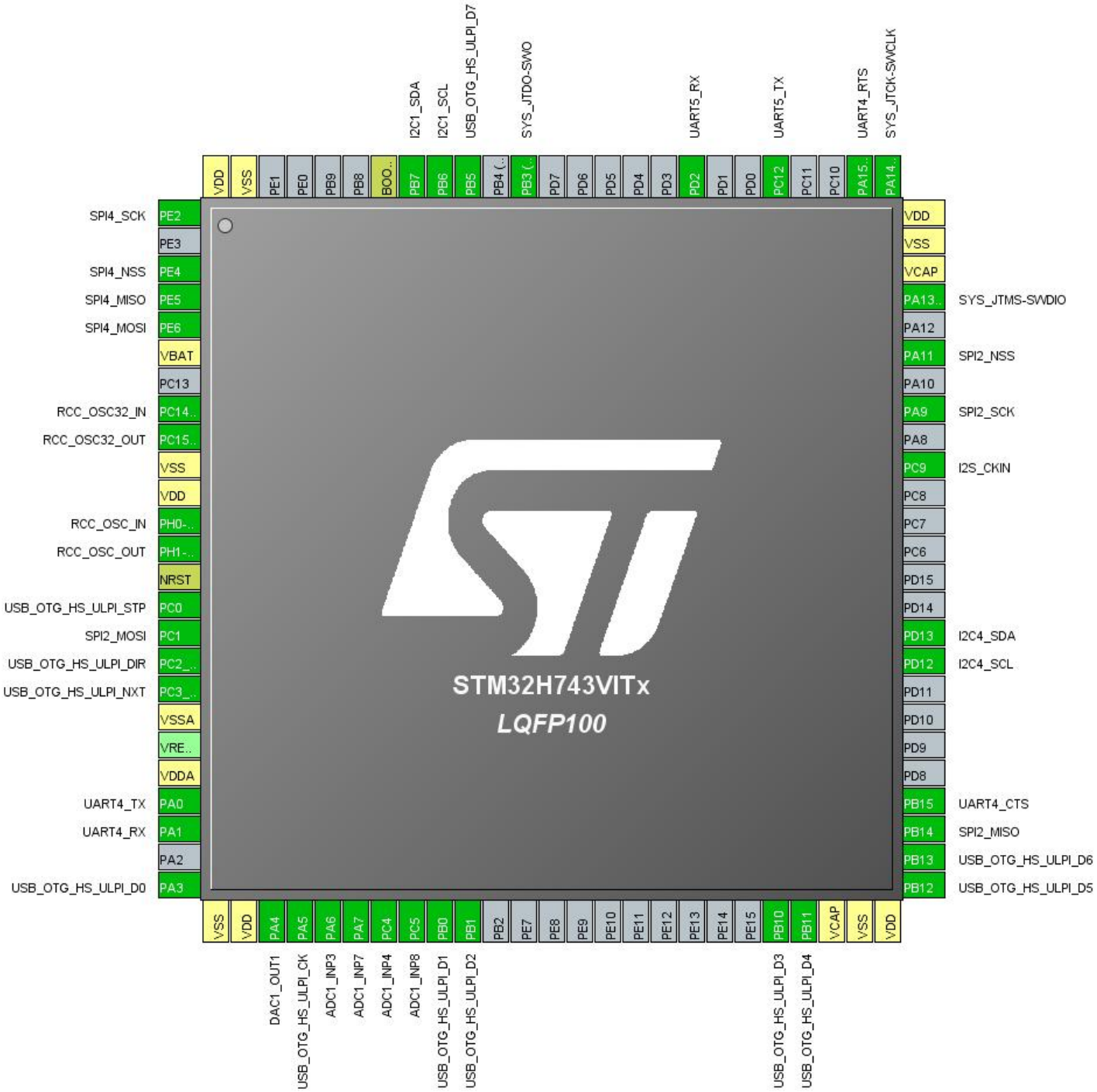
1.1. Project

Project Name	STCubeGenerated
Board Name	custom
Generated with:	STM32CubeMX 5.1.0
Date	03/07/2019

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743VITx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration

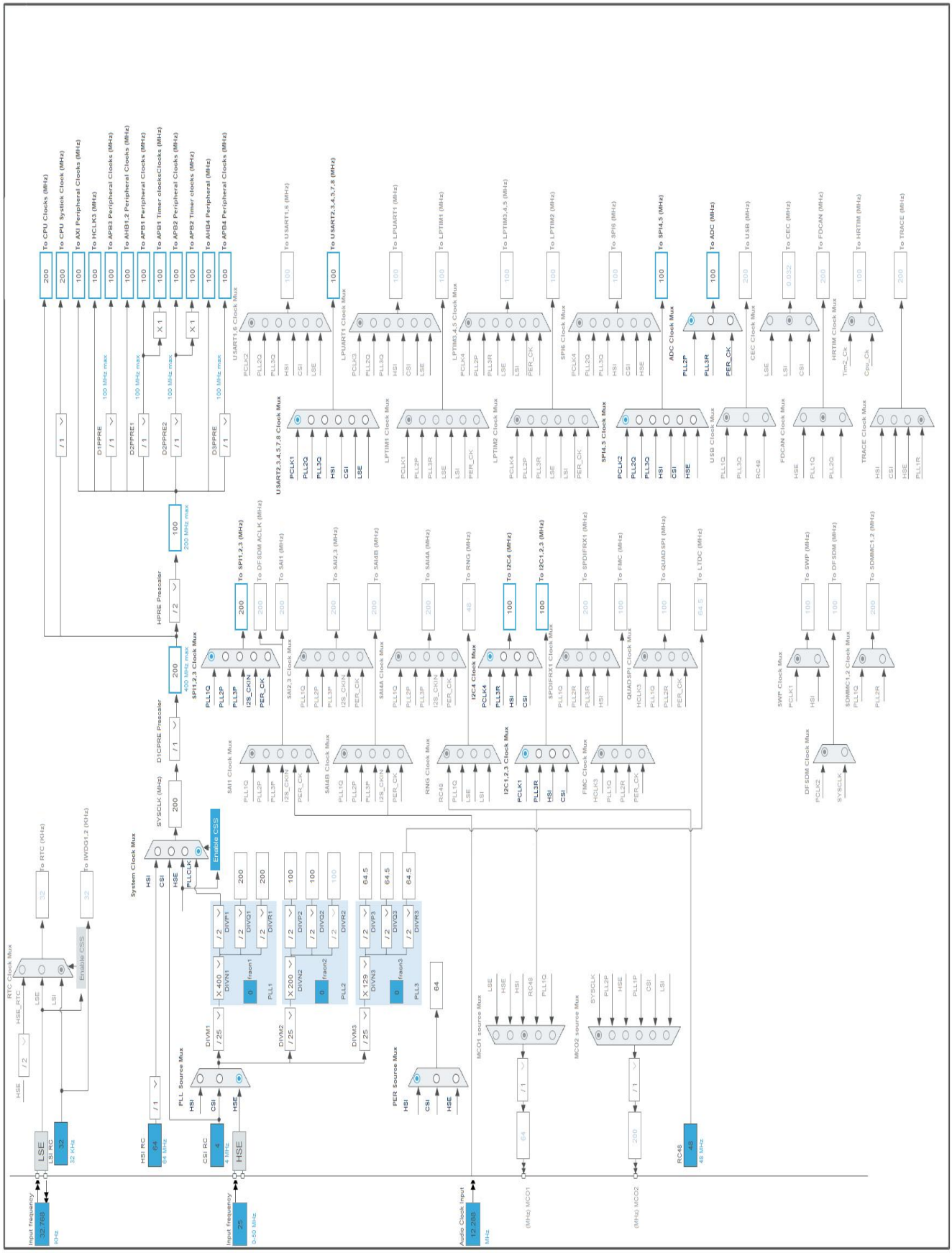


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	
3	PE4	I/O	SPI4_NSS	
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	USB_OTG_HS_ULPI_STP	
16	PC1	I/O	SPI2_MOSI	
17	PC2_C	I/O	USB_OTG_HS_ULPI_DIR	
18	PC3_C	I/O	USB_OTG_HS_ULPI_NXT	
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	UART4_TX	
23	PA1	I/O	UART4_RX	
25	PA3	I/O	USB_OTG_HS_ULPI_D0	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	DAC1_OUT1	
29	PA5	I/O	USB_OTG_HS_ULPI_CK	
30	PA6	I/O	ADC1_INP3	
31	PA7	I/O	ADC1_INP7	
32	PC4	I/O	ADC1_INP4	
33	PC5	I/O	ADC1_INP8	
34	PB0	I/O	USB_OTG_HS_ULPI_D1	
35	PB1	I/O	USB_OTG_HS_ULPI_D2	
46	PB10	I/O	USB_OTG_HS_ULPI_D3	
47	PB11	I/O	USB_OTG_HS_ULPI_D4	
48	VCAP	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	USB_OTG_HS_ULPI_D5	
52	PB13	I/O	USB_OTG_HS_ULPI_D6	
53	PB14	I/O	SPI2_MISO	
54	PB15	I/O	UART4_CTS	
59	PD12	I/O	I2C4_SCL	
60	PD13	I/O	I2C4_SDA	
66	PC9	I/O	I2S_CKIN	
68	PA9	I/O	SPI2_SCK	
70	PA11	I/O	SPI2_NSS	
72	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	
77	PA15 (JTDI)	I/O	UART4_RTS	
80	PC12	I/O	UART5_TX	
83	PD2	I/O	UART5_RX	
89	PB3 (JTDO/TRACESWO)	I/O	SYS_JTDO-SWO	
91	PB5	I/O	USB_OTG_HS_ULPI_D7	
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STCubeGenerated
Project Folder	C:\current\blue-spirit-hd-
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_H7 V1.3.2

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743VITx
Datasheet	030538_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC1

IN3: IN3 Single-ended

IN4: IN4 Single-ended

mode: IN7

mode: IN8

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Boost Mode	Disabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. CORTEX_M7

7.2.1. Parameter Settings:

Cortex Interface Settings:

CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.3. DAC1

OUT1 mode: Connected to external pin only

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

7.4. I2C1

I2C: I2C

7.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.5. I2C4

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

mode: Audio Clock Input (I2S_CKIN)

7.6.1. Parameter Settings:

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	16

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	1 WS (2 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 3

PLL range Parameters:

PLL1 clock Input range	Between 1 and 2 MHz
PLL2 input frequency range	Between 1 and 2 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

7.7. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**100.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.8. SPI4

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**50.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.9. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

7.10. UART4

Mode: Asynchronous

Hardware Flow Control (RS232): CTS/RTS

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.11. UART5

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Prescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. USB_OTG_HS

External Phy: Host_Only

7.12.1. Parameter Settings:

Speed	High Speed 480MBit/s
Enable internal IP DMA	Disabled
Physical interface	External Phy
Use external vbus	Enabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_INP7	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_INP8	Analog mode	No pull-up and no pull-down	n/a	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C4	PD12	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PD13	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PC9	I2S_CKIN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PC1	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE4	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWC	SYS_JTCK-SWCLK	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	LK)					
	PB3 (JTDO/TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	
UART4	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	UART4_CTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15 (JTDI)	UART4_RTS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_HS	PC0	USB_OTG_HS_ULPI_STP	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC2_C	USB_OTG_HS_ULPI_DIR	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC3_C	USB_OTG_HS_ULPI_NXT	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA3	USB_OTG_HS_ULPI_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA5	USB_OTG_HS_ULPI_CK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB0	USB_OTG_HS_ULPI_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB1	USB_OTG_HS_ULPI_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB10	USB_OTG_HS_ULPI_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB11	USB_OTG_HS_ULPI_D4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB12	USB_OTG_HS_ULPI_D5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB13	USB_OTG_HS_ULPI_D6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB5	USB_OTG_HS_ULPI_D7	Alternate Function Push Pull	No pull-up and no pull-down	High	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
I2C1_RX	DMA1_Stream0	Peripheral To Memory	Low
I2C1_TX	DMA1_Stream1	Memory To Peripheral	Low
SPI2_RX	DMA1_Stream2	Peripheral To Memory	Low
SPI2_TX	DMA1_Stream3	Memory To Peripheral	Low
SPI4_RX	DMA1_Stream4	Peripheral To Memory	Low
SPI4_TX	DMA1_Stream5	Memory To Peripheral	Low
UART4_RX	DMA1_Stream6	Peripheral To Memory	Low
UART4_TX	DMA1_Stream7	Memory To Peripheral	Low
UART5_RX	DMA2_Stream0	Peripheral To Memory	Low
UART5_TX	DMA2_Stream1	Memory To Peripheral	Low

I2C1_RX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C1_TX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI2_RX: DMA1_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte

Memory Data Width:	Byte

SPI2_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI4_RX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI4_TX: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_RX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART4_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART5_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART5_TX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. BDMA configuration

DMA request	Stream	Direction	Priority
I2C4_RX	BDMA_Channel0	Peripheral To Memory	Low
I2C4_TX	BDMA_Channel1	Memory To Peripheral	Low

I2C4_RX: BDMA_Channel0 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

I2C4_TX: BDMA_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream2 global interrupt	true	0	0
DMA1 stream3 global interrupt	true	0	0
DMA1 stream4 global interrupt	true	0	0
DMA1 stream5 global interrupt	true	0	0
DMA1 stream6 global interrupt	true	0	0
SPI2 global interrupt	true	0	0
DMA1 stream7 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	0	0
SPI4 global interrupt	true	0	0
BDMA channel0 global interrupt	true	0	0
BDMA channel1 global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
UART4 global interrupt	unused		
UART5 global interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
USB On The Go HS End Point 1 Out global interrupt	unused		
USB On The Go HS End Point 1 In global interrupt	unused		
USB On The Go HS global interrupt	unused		
FPU global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

9. Software Pack Report