

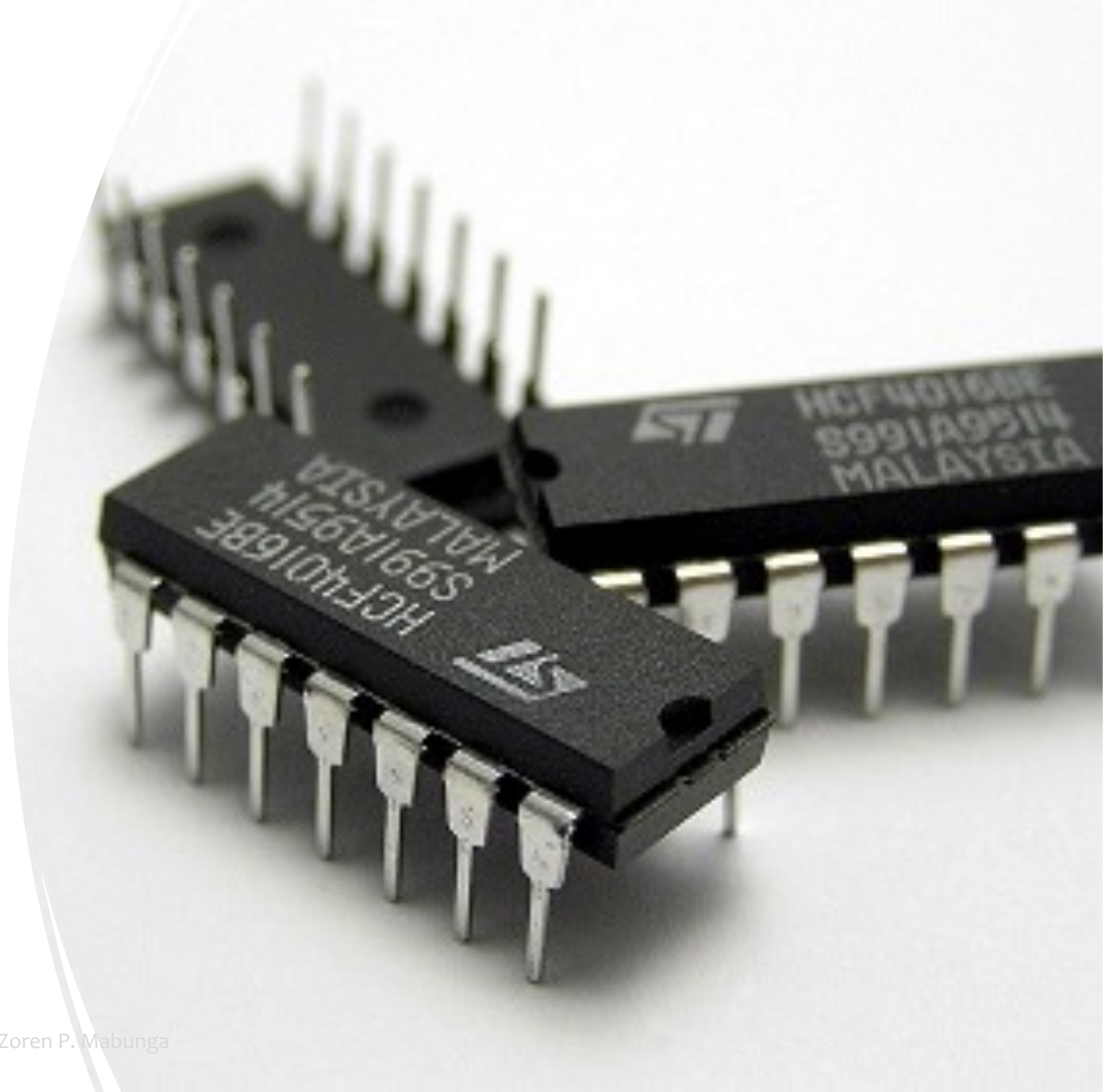


Integrated Circuits

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Digital ICs

- Digital ICs are a collection of resistors, diodes, and transistors fabricated on a single piece of semiconductor material called a substrate, commonly referred to as a chip.



Digital IC types

| Complexity (Level of Integration) | Number of Gates |
|--|------------------------|
| Small-scale integration(SSI) | <10 |
| Medium-scale integration(MSI) | 10 to 99 |
| Large-scale integration(LSI) | 100 to 9999 |
| Very large-scale integration(VLSI) | 10,000 to 99,999 |
| Ultra large-scale integration(ULSI) | 100,000 to 999,999 |
| Giga-scale integration (GSI) | 1,000,000 or more |

Bipolar and Unipolar Digital ICs

- Categorized according to the principal type of electronic component used in their circuitry.
- Bipolar ICs are those that are made using the bipolar junction transistor (PNP or NPN)
- Unipolar ICs are those that use the unipolar field-effect transistors (P-channel and N-channel MOSFETs).

Digital IC Families

1. TTL – a logic family that has been use for a long time
 - common in SSI and MSI chips
2. ECL - has an advantage in systems requiring high speed of operation
3. MOS – suitable for circuits with high component density
4. CMOS – preferable in systems requiring low power consumption
5. DTL - obsolete

TTL Family

| TTL Series | Prefix | Example IC |
|---------------------------------|--------|---------------------|
| Standard TTL | 74 | 7404 (hex inverter) |
| Schottky TTL | 74S | 74S04 |
| Low-power Schottky TTL | 74LS | 74LS04 |
| Advanced Schottky TTL | 74AS | 74AS04 |
| Advanced low-power Schottky TTL | 74ALS | 74ALS04 |

CMOS Family

| CMOS Series | Prefix | Example IC |
|---|--------|------------|
| Metal-gate CMOS | 40 | 4001 |
| Metal-gate, pin-compatible with TTL | 74C | 74C02 |
| Silicon-gate, pin-compatible with TTL, high-speed | 74HC | 74HC02 |
| Silicon-gate, high-speed, pin-compatible and electrically compatible with TTL | 74HCT | 74HCT02 |
| Advanced-performance CMOS, not pin or electrically compatible with TTL | 74AC | 74AC02 |
| Advanced-performance CMOS, not pin but electrically compatible with TTL | 74ACT | 74ACT02 |

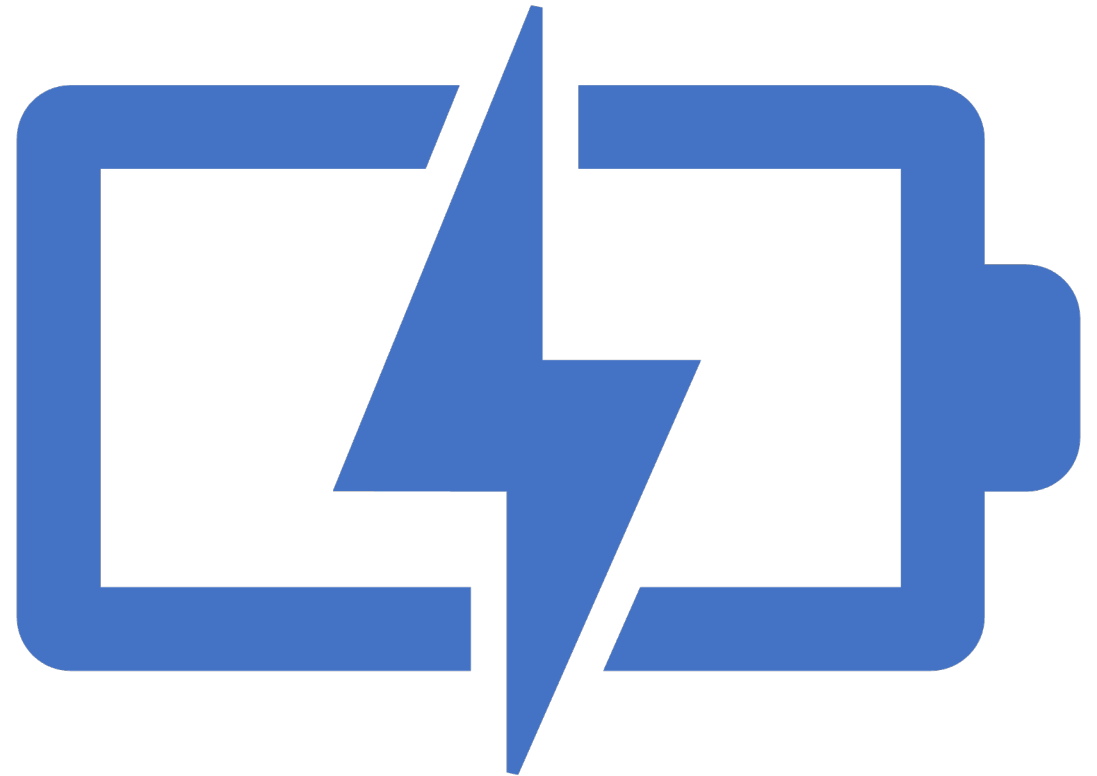


Power and Ground

- To use digital IC, it is necessary to make proper connection to the IC pins.
- Power: labeled V_{cc} for the TTL circuit, labeled V_{DD} for CMOS circuit.
- Ground

Logic-level Voltage Ranges

- For TTL devices, V_{CC} is normally 5V.
- For CMOS circuits, V_{DD} can range from 3-18V.
- For TTL, logic 0 : 0-0.8V, logic 1:2-5V
- For CMOS, logic 0 : 0-1.5V, logic 1:3.5-5V



Unconnected Inputs

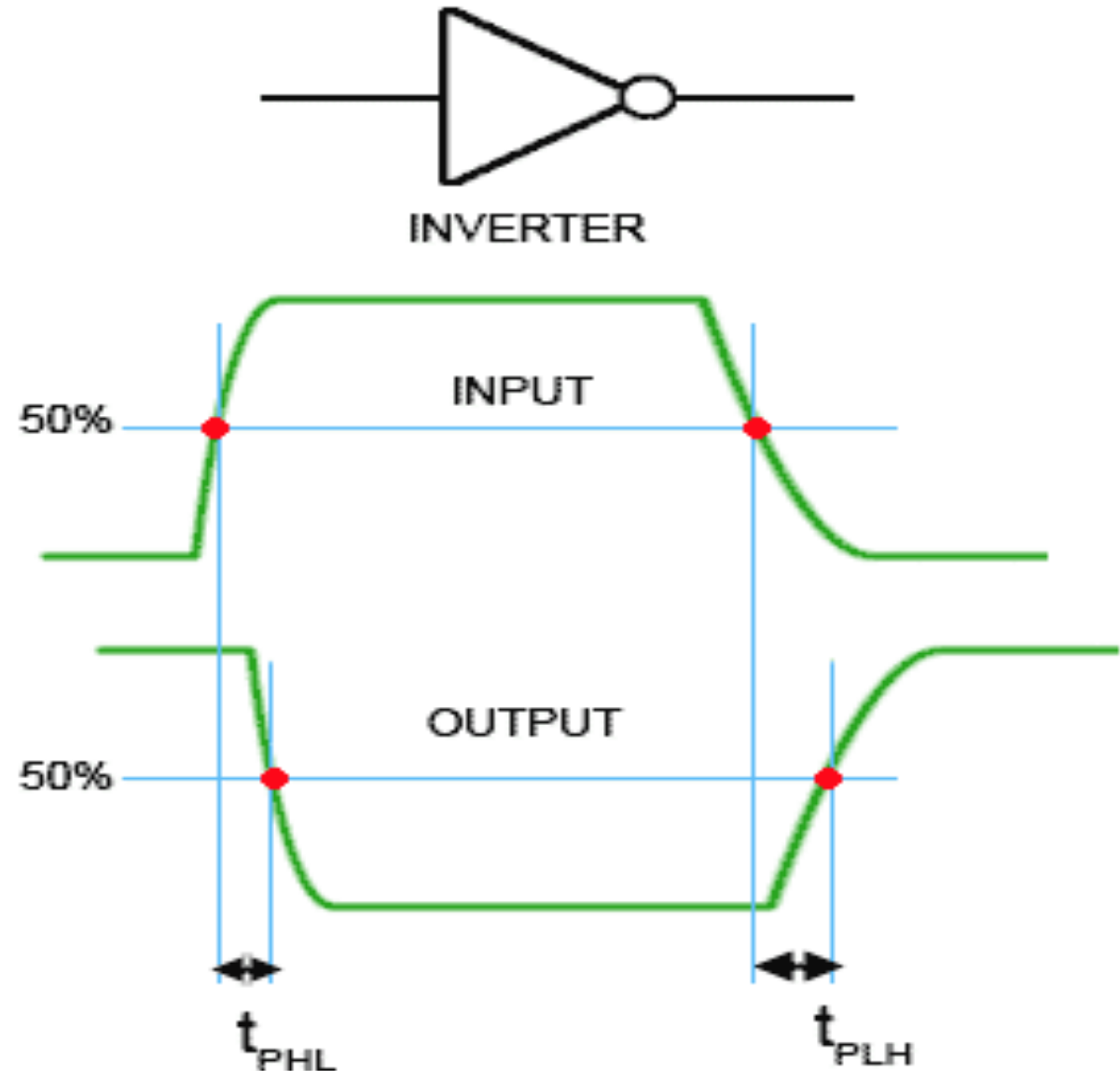
- Also called floating inputs.
- A floating TTL input acts like a logic 1.
- A CMOS input cannot be left floating.

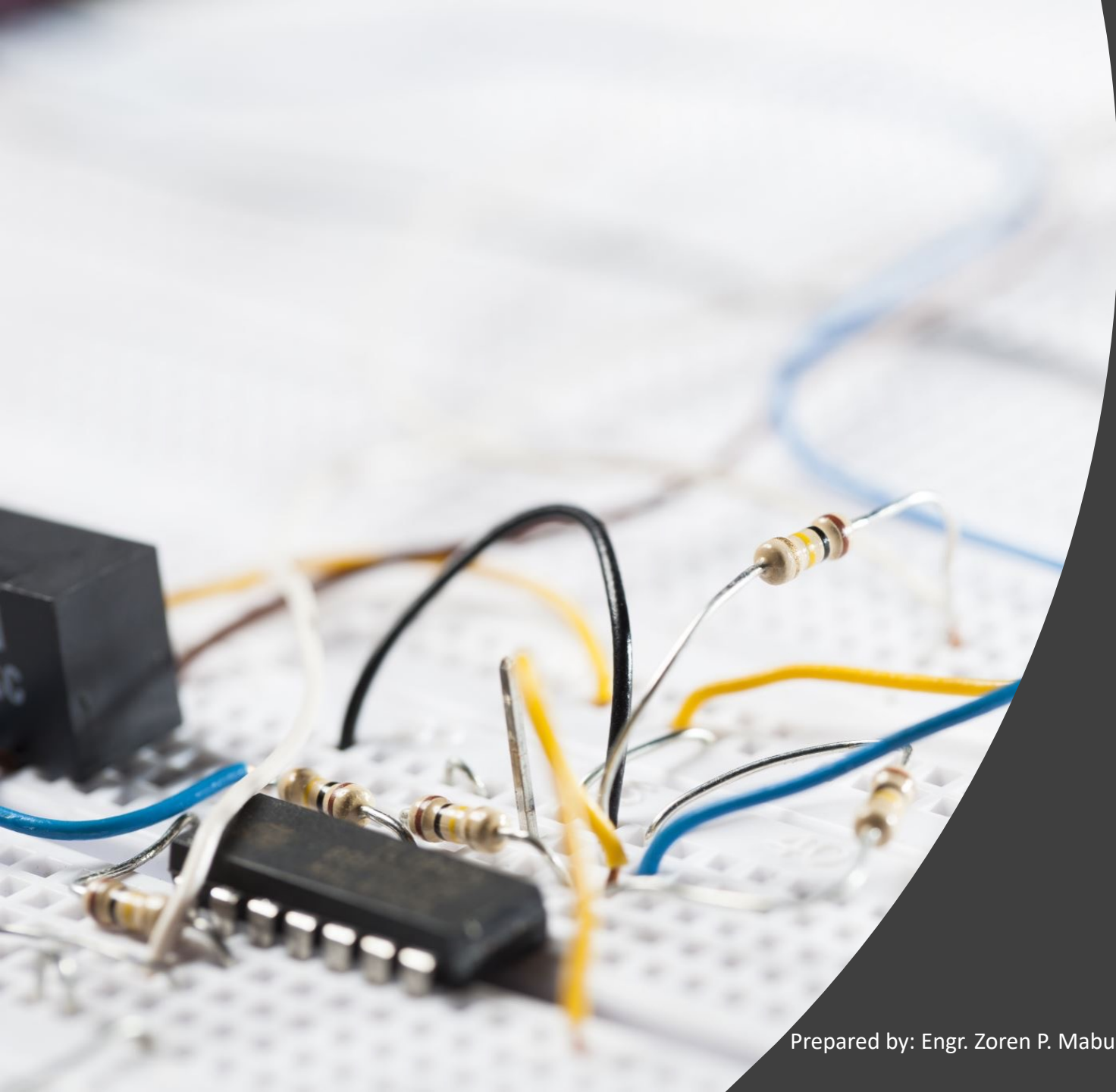


Important Parameters

- 1.Fan-in** – the number of inputs available on a gate
- 2.Fan-out** – the number of standard loads driven by a gate output
- 3.Noise Margin** – maximum extent noise voltage added to an input signal that does not cause an undesirable change in the circuit output.
- 4.Propagation Delay** – The time required for a change in the value of a signal to propagate from an input to an output
- 5.Power Dissipation** – the amount of power drawn from the power supply and consumed by the gate

Propagation Delay Illustration





Combinational Logic Circuits

Prepared by: Engr. Zoren P. Mabunga

Combinational Logic Circuits

- A **combinational logic circuit** consists of input variables, logic gates and output variables.
- This type of logic circuit reacts to values of the signals at their inputs and produce the output signal.

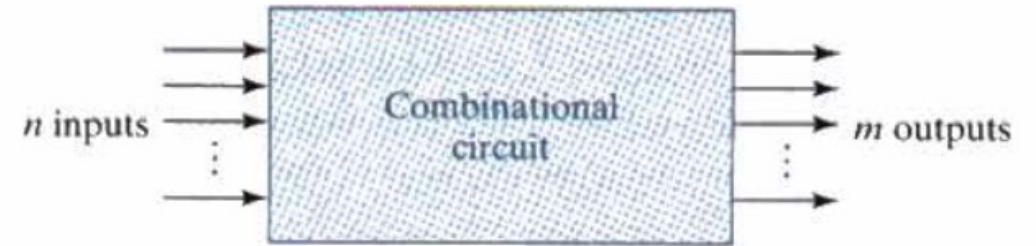


FIGURE 4.1
Block diagram of combinational circuit

Half-Adder

- This circuit needs two binary inputs and two binary outputs.
- The input variables designate the augend and addend bits
- The output variables produce the sum and carry

Table 4.3
Half Adder

| x | y | C | S |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

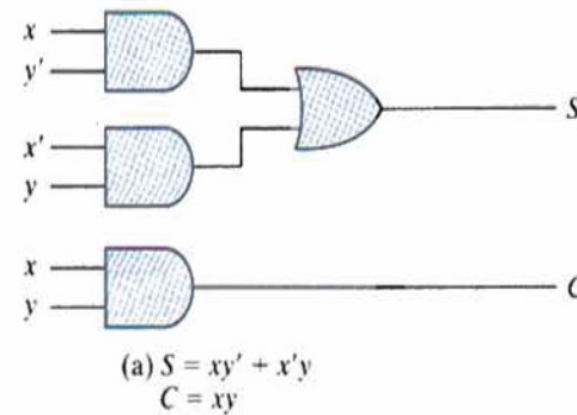
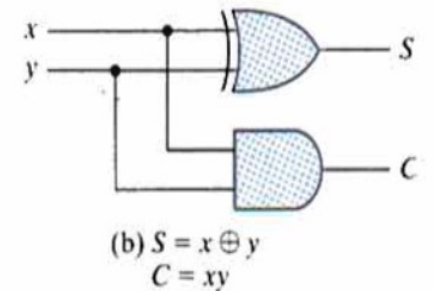


FIGURE 4.5
Implementation of half adder



Full Adder

- A full adder is a combinational logic circuit that performs the arithmetic sum of 3 bits.

Table 4.4
Full Adder

| x | y | z | C | S |
|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

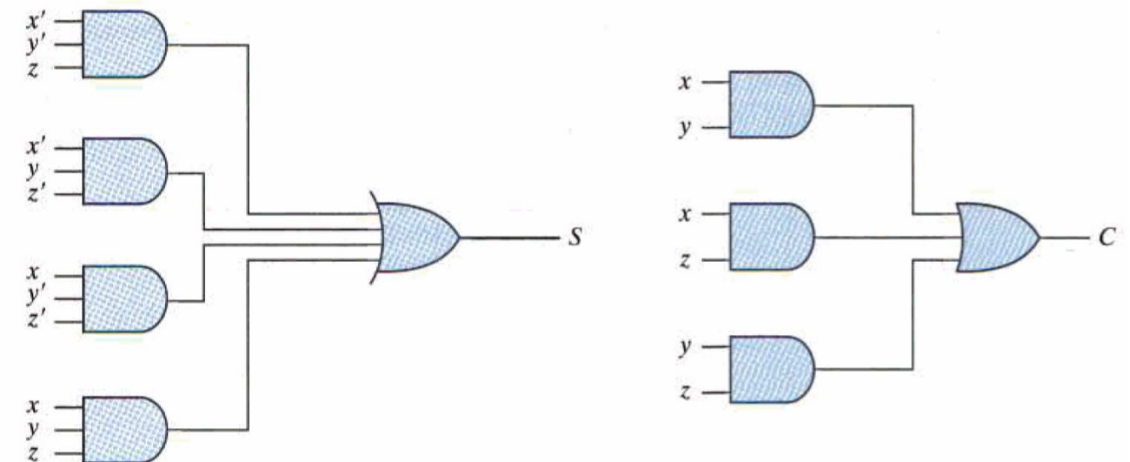


FIGURE 4.7
Implementation of full adder in sum-of-products form

Binary Adder

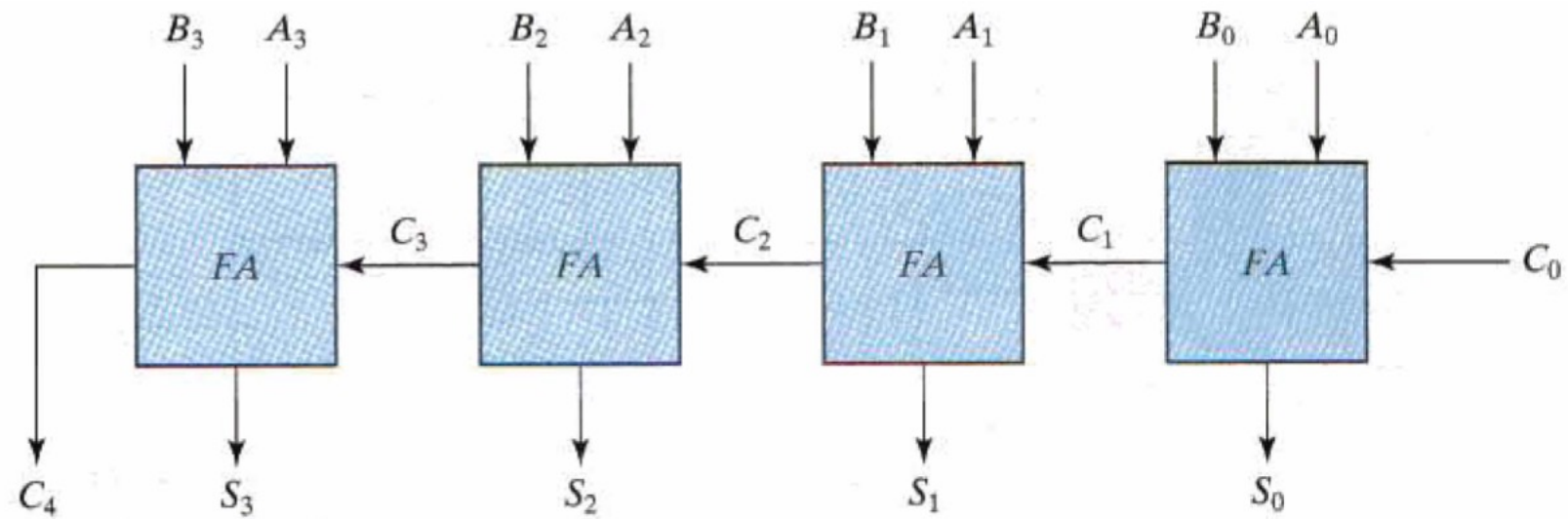
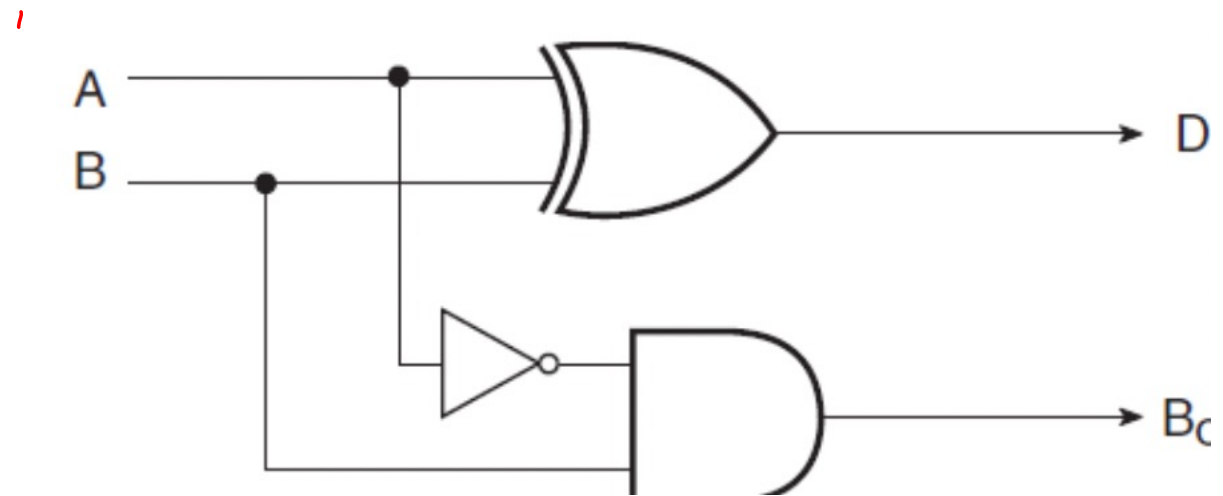


FIGURE 4.9
Four-bit adder

Half Subtractor

- A half subtractor is a combinational logic circuit intended to subtract two single bits and generate two outputs (borrow and difference).

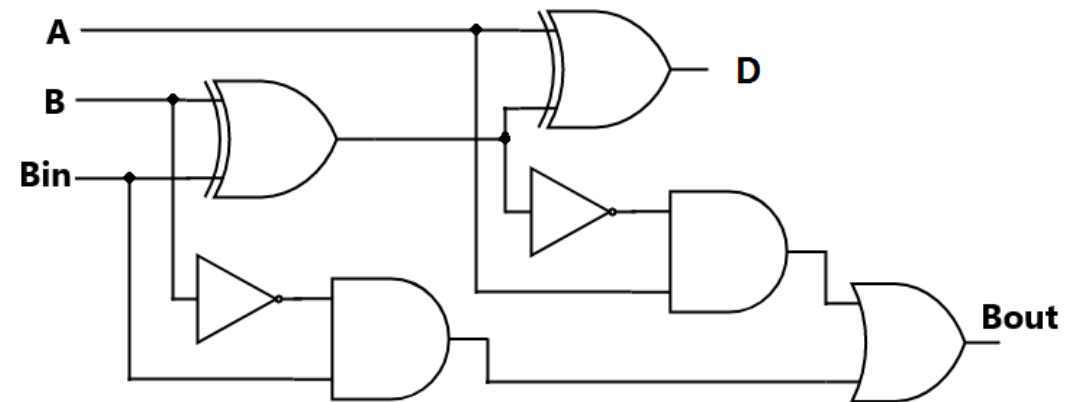
| Inputs | | Outputs | |
|--------|---|---------|--------|
| A | B | Diff | Borrow |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |



Full Subtractor

- A full subtractor is a combinational logic circuit that delivers the subtraction of two bits, one is minuend, and the other is subtrahend considering the borrow of the earlier adjacent lower minuend bit.

| Inputs | | | Outputs | |
|--------|---|----------------------|---------|--------|
| A | B | Borrow _{in} | Diff | Borrow |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |



Decoders

- A **decoder** is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.

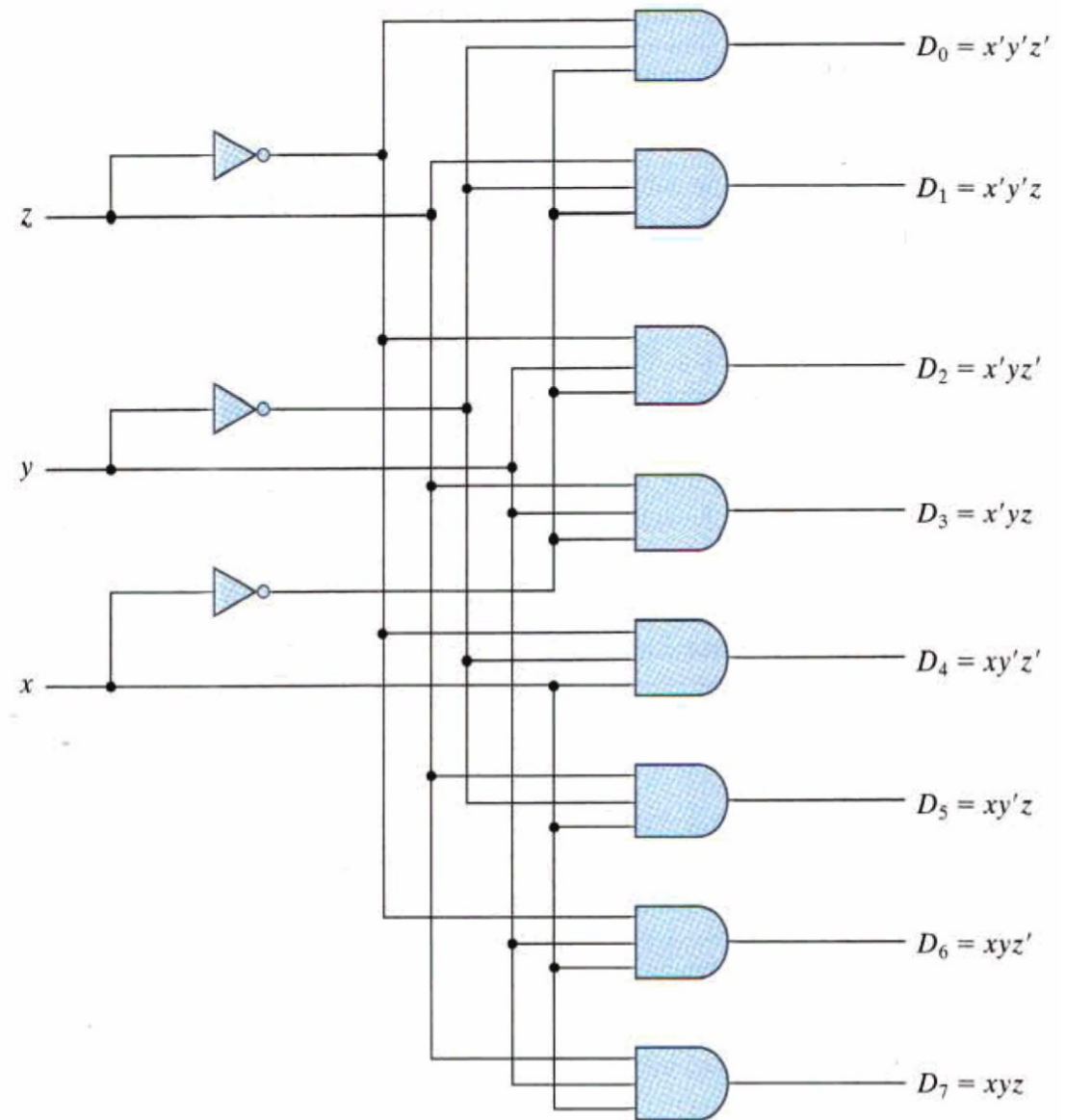
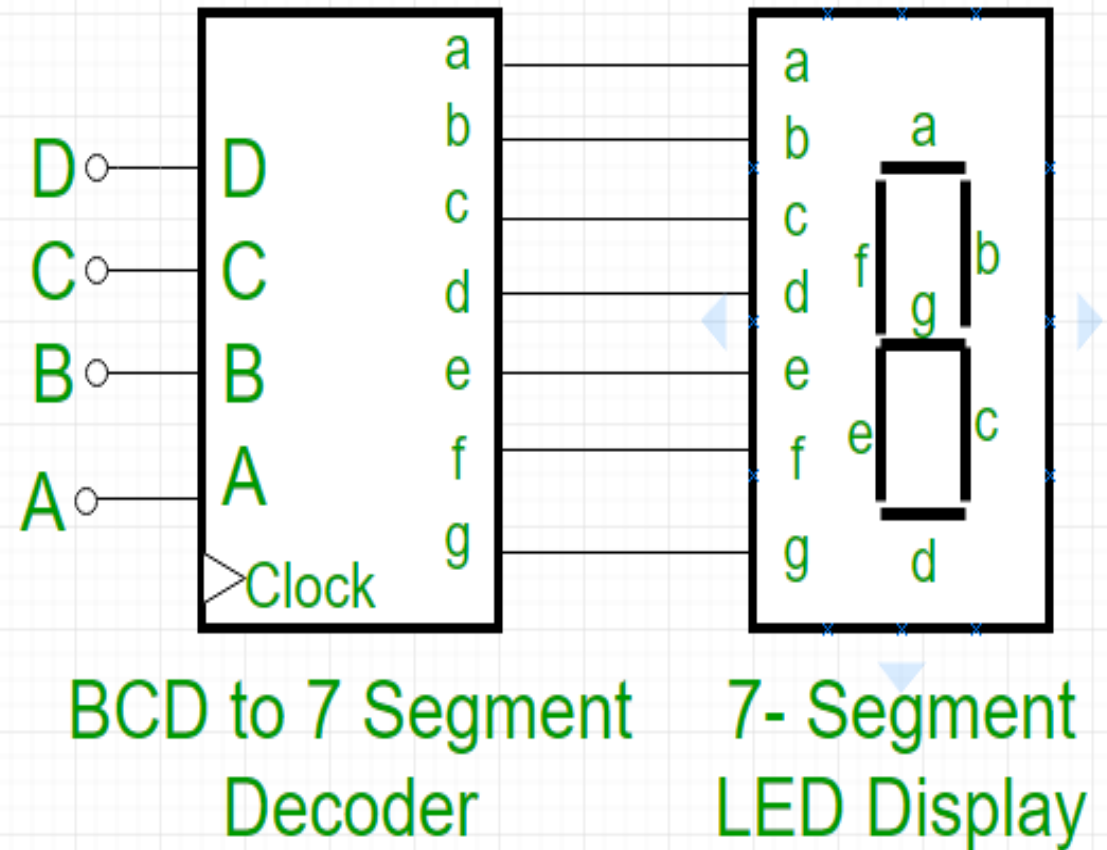


FIGURE 4.18
Three-to-eight-line decoder

BCD to 7-segment Decoder



Encoders

- the opposite of decoders
- it converts m -bit input code to a n -bit output code with $n \leq m \leq 2^n$ such that each valid code word produces a unique output code

Example

- Octal-to-Binary Encoder

□ **TABLE 3-7**
Truth Table for Octal-to-Binary Encoder

| Inputs | | | | | | | | Outputs | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | A ₂ | A ₁ | A ₀ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

Multiplexers

- A multiplexer selects information from an input line and directs the information to an output line
- A typical multiplexer has n control inputs (S_{n-1}, \dots, S_0) called *selection inputs*, 2^n information inputs (I_{2^n-1}, \dots, I_0), and one output Y
- A multiplexer can be designed to have m information inputs with $m < 2^n$ as well as n selection inputs

2-to-1-Line Multiplexer

Since $2 = 2^1$, $n = 1$

The single selection variable S has two values:

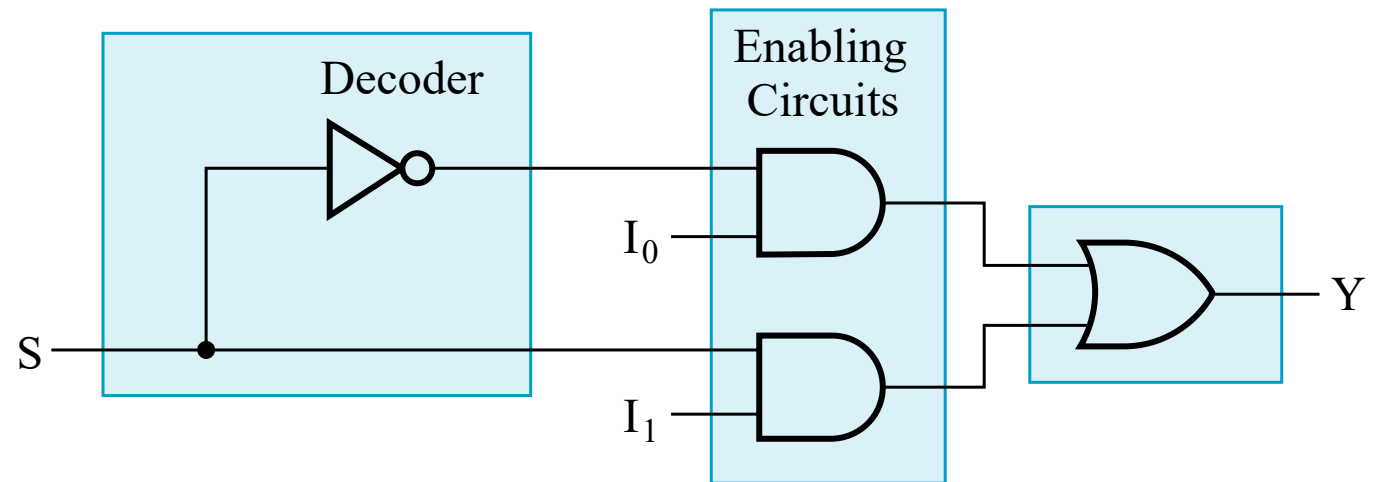
$S = 0$ selects input I_0

$S = 1$ selects input I_1

The equation:

$$Y = I_0 + SI_1$$

The circuit:

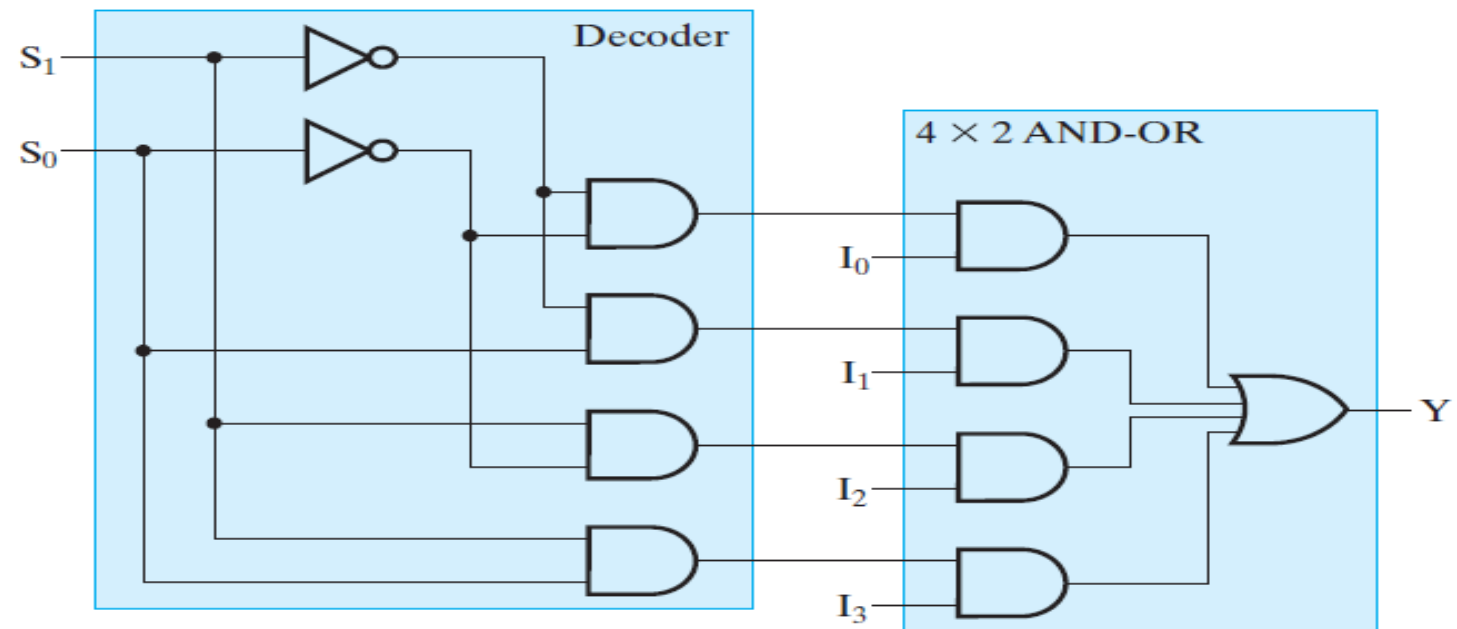


4-to-1-line Multiplexer

- 2-to-2²-line decoder
- 2² × 2 AND-OR

□ **TABLE 3-10**
Condensed Truth Table for 4-to-1-Line Multiplexer

| S ₁ | S ₀ | Y |
|----------------|----------------|----------------|
| 0 | 0 | I ₀ |
| 0 | 1 | I ₁ |
| 1 | 0 | I ₂ |
| 1 | 1 | I ₃ |



Sample MCQs

1. BCD input 1000 is fed to a 7-segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are
 - a) a,b,d
 - b) a,b,c
 - c) All
 - d) a,b,g,c,d

Sample MCQs

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Sample MCQs

2. The output of a half adder is

- a) SUM
- b) CARRY
- c) SUM and CARRY
- d) None of the above

Sample MCQs

2. The output of a half adder is

- a) SUM
- b) CARRY
- c) **SUM and CARRY**
- d) None of the above

Sample MCQs

3. Which device has one input and many outputs?

- a) Multiplexer
- b) Demultiplexer
- c) Counter
- d) Flip-flop

Sample MCQs

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- a) Multiplexer
- b) Demultiplexer**
- c) Counter
- d) Flip-flop

Sample MCQs

4. A 4 : 1 multiplexer requires _____ data select line.

- a) 1
- b) 2
- c) 3
- d) 4

Sample MCQs

4. A 4 : 1 multiplexer requires _____ data select line.

- a) 1
- b) 2**
- c) 3
- d) 4

Sample MCQs

5. In digital circuits Schottky transistors are preferred over normal transistors because of their:

- a) Lower propagation delay
- b) Lower power dissipation
- c) Higher propagation delay
- d) Higher power dissipation

Sample MCQs

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- a) **Lower propagation delay**
- b) Lower power dissipation
- c) Higher propagation delay
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Sample MCQs

6. Which of the following finds application in pocket calculators?

- a) TTL
- b) CMOS
- c) ECL
- d) Both a and c

Sample MCQs

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