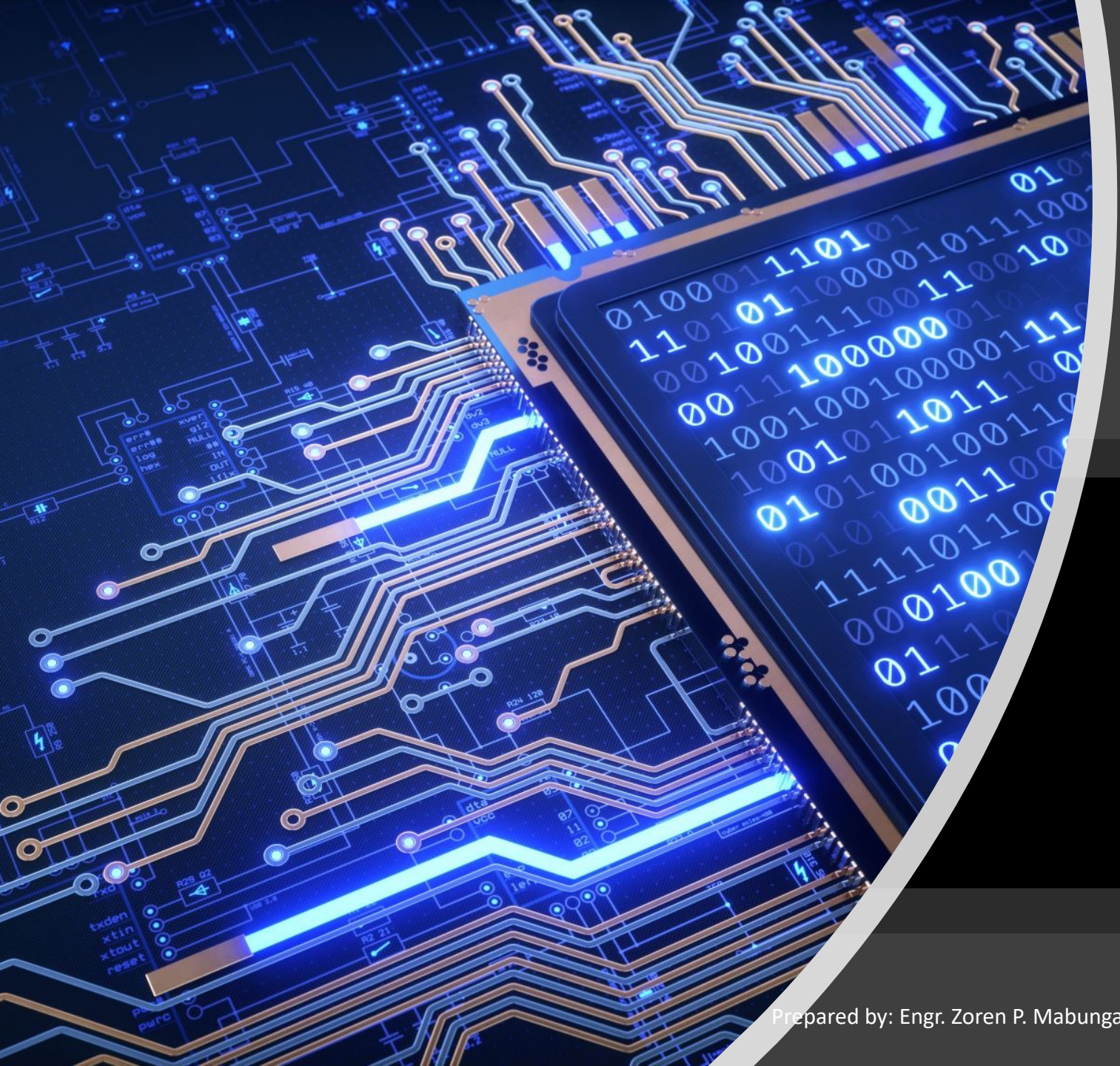

Sequential Logic Circuits

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Two Types of Logic Circuits

1. Combinational Logic Circuit

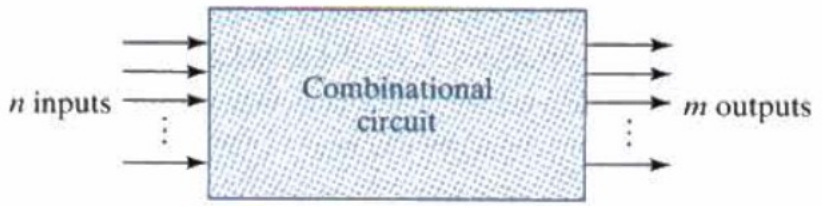


FIGURE 4.1
Block diagram of combinational circuit

2. Sequential Logic Circuit

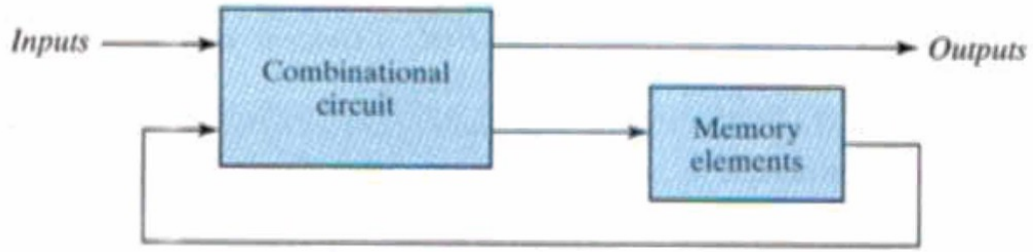
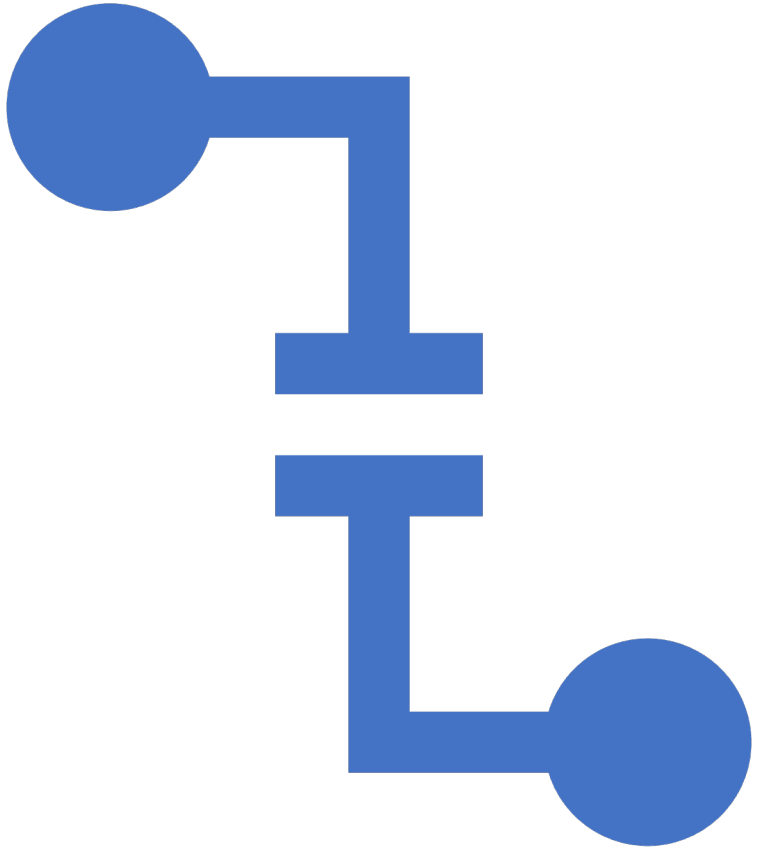


FIGURE 5.1
Block diagram of sequential circuit

Combinational Logic Circuit

- Consists of logic gates whose outputs at any time are determined from only the present combination of inputs.
- Has no memory

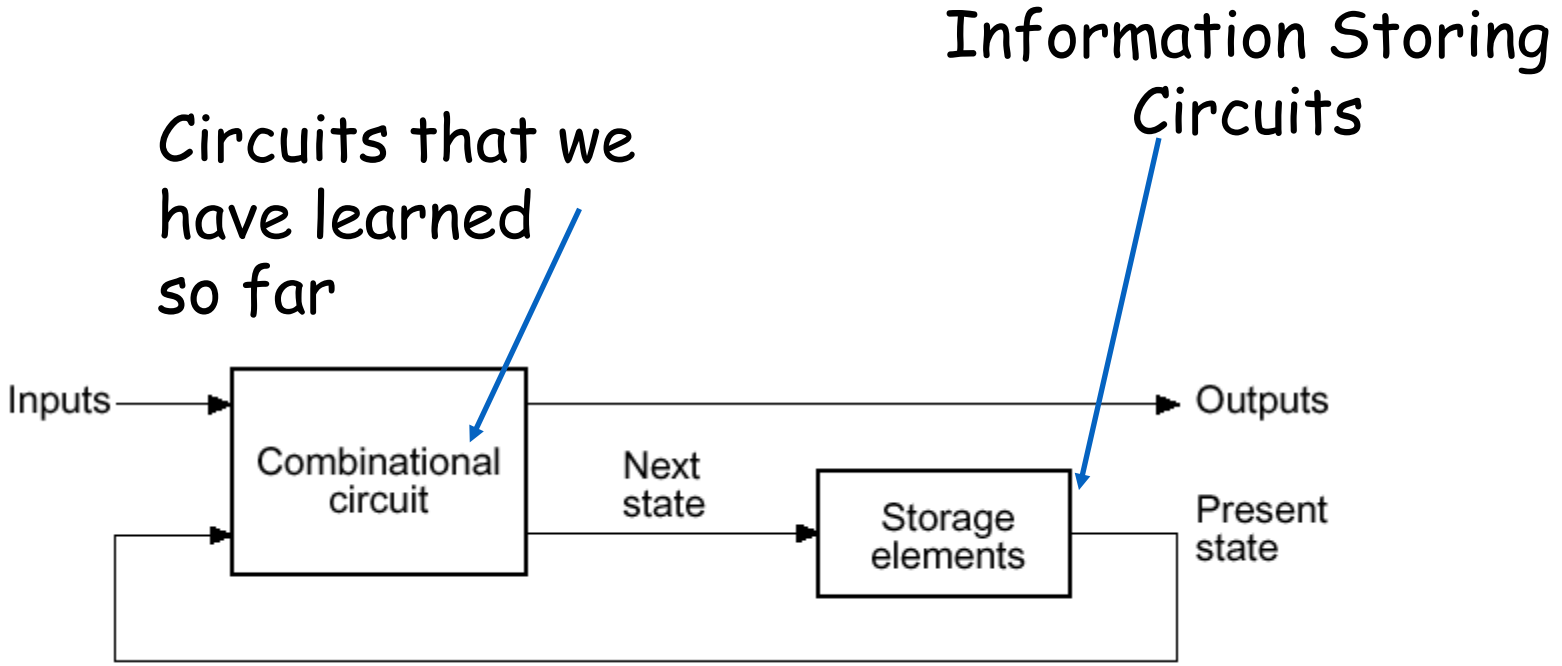


Sequential Logic Circuits

Employ storage elements (flip-flops, latches)

Their outputs are a function of the inputs and the state of the storage elements.

Sequential Logic Circuit



Two types of Sequential Circuit

SYNCHRONOUS SEQUENTIAL CIRCUIT

- A system whose behavior can be defined from the knowledge of its signals at discrete instants of time.
- This type of circuits achieves synchronization by using a timing signal called the clock.

ASYNCHRONOUS SEQUENTIAL CIRCUIT

- Its behavior depends upon the input signals at any instant of time and the order in which the inputs change.

What are Latches?

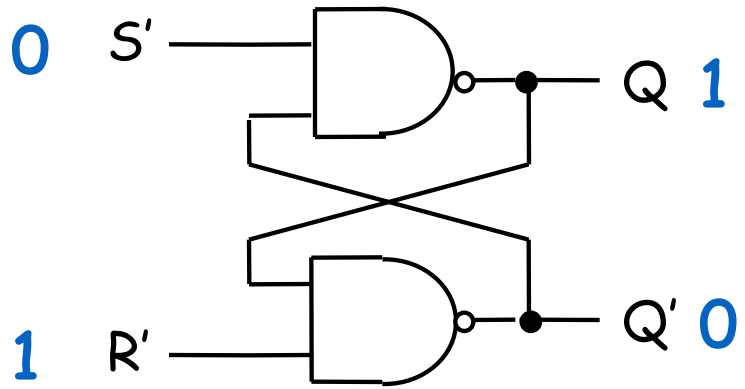
Latches are storage elements that operate with signal levels

Level sensitive devices

Useful for storing binary information and for the design of asynchronous sequential circuits

Building blocks of flip-flops

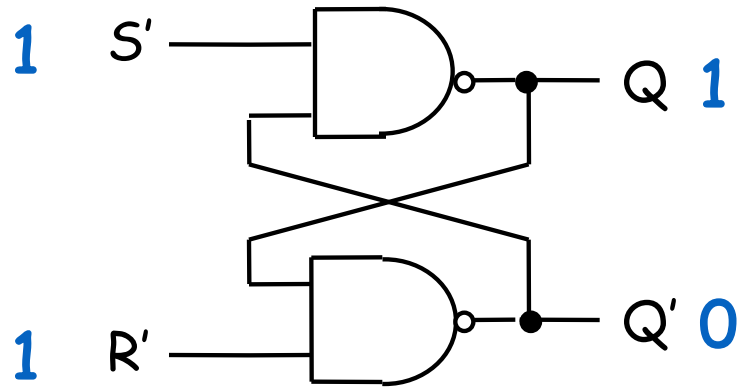
SR Latch (NAND version)



S'	R'	Q	Q'
0	0		
0	1	1	0 Set
1	0		
1	1		

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

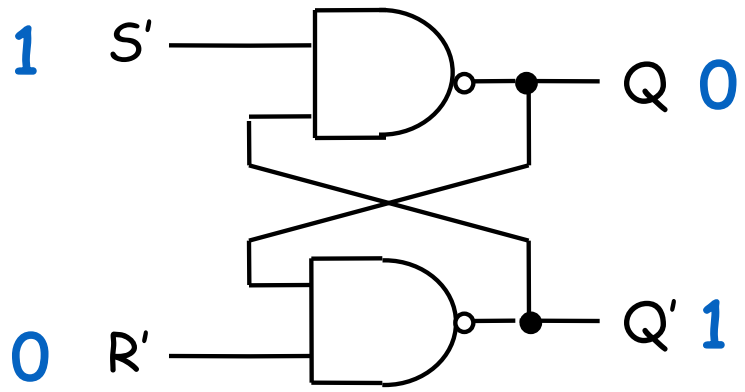
SR Latch (NAND version)



S'	R'	Q	Q'	
0	0			
0	1	1	0	Set
1	0			
1	1	1	0	Hold

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

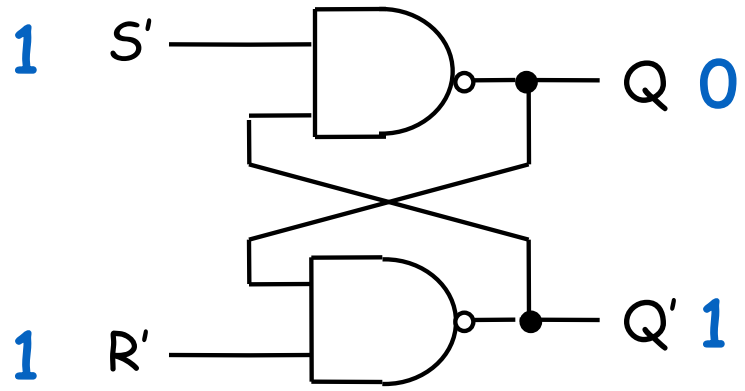
SR Latch (NAND version)



S'	R'	Q	Q'	
0	0			
0	1	1	0	Set
1	0	0	1	Reset
1	1	1	0	Hold

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

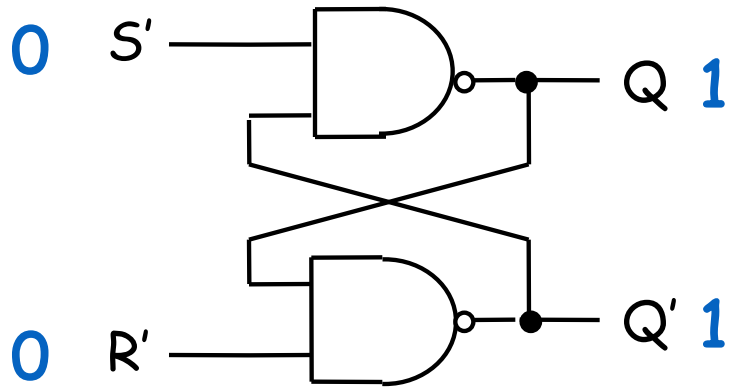
SR Latch (NAND version)



S'	R'	Q	Q'	
0	0			
0	1	1	0	Set
1	0	0	1	Reset
1	1	1	0	Hold
		0	1	Hold

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

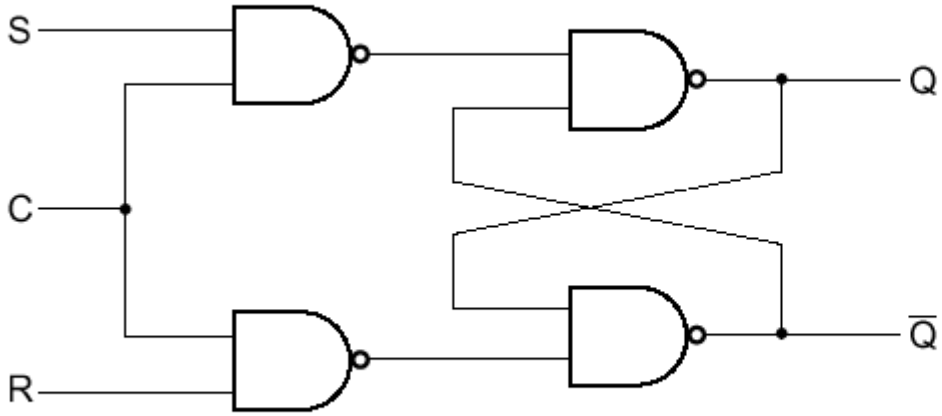
SR Latch (NAND version)



S'	R'	Q	Q'	
0	0	1	1	Disallowed
0	1	1	0	Set
1	0	0	1	Reset
1	1	1	0	Hold
		0	1	Hold

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

SR Latch with Clock signal



(a) Logic diagram

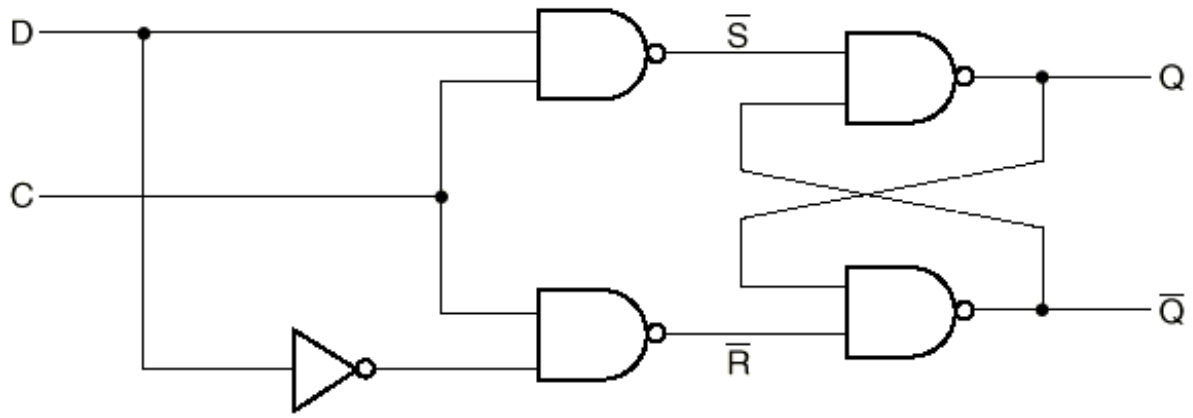
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined

(b) Function table

Latch is sensitive to input changes ONLY when C=1

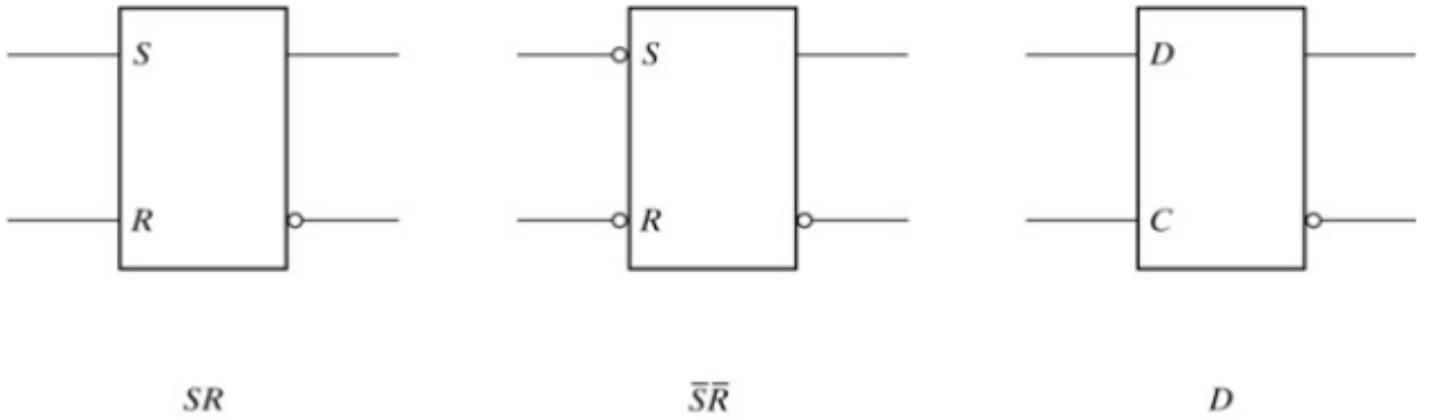
D Latch (Transparent Latch)

- One way to eliminate the undesirable indeterminate state in the RS flip flop is to ensure that inputs S and R are never 1 simultaneously. This is done in the *D latch:*



C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

Graphic Symbols for Latches



FLIP-FLOPS

Storage elements used in clocked sequential circuits

Edge sensitive devices

A binary storage device capable of storing one bit of information.

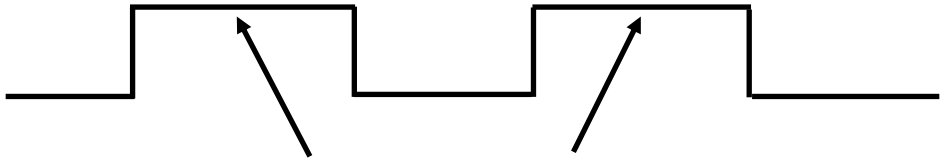
D Flip-Flop, JK Flip-Flop, T Flip-Flop

EDGE-TRIGGERED FLIP FLOPS

Characteristics

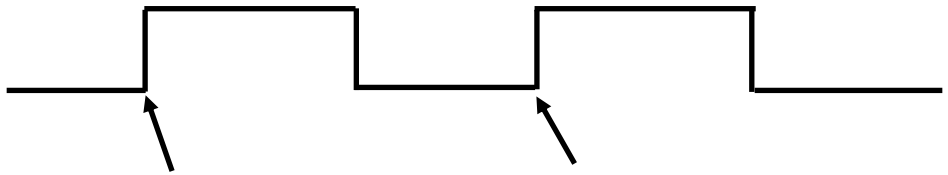
- State transition occurs at the rising edge or falling edge of the clock pulse

Latches



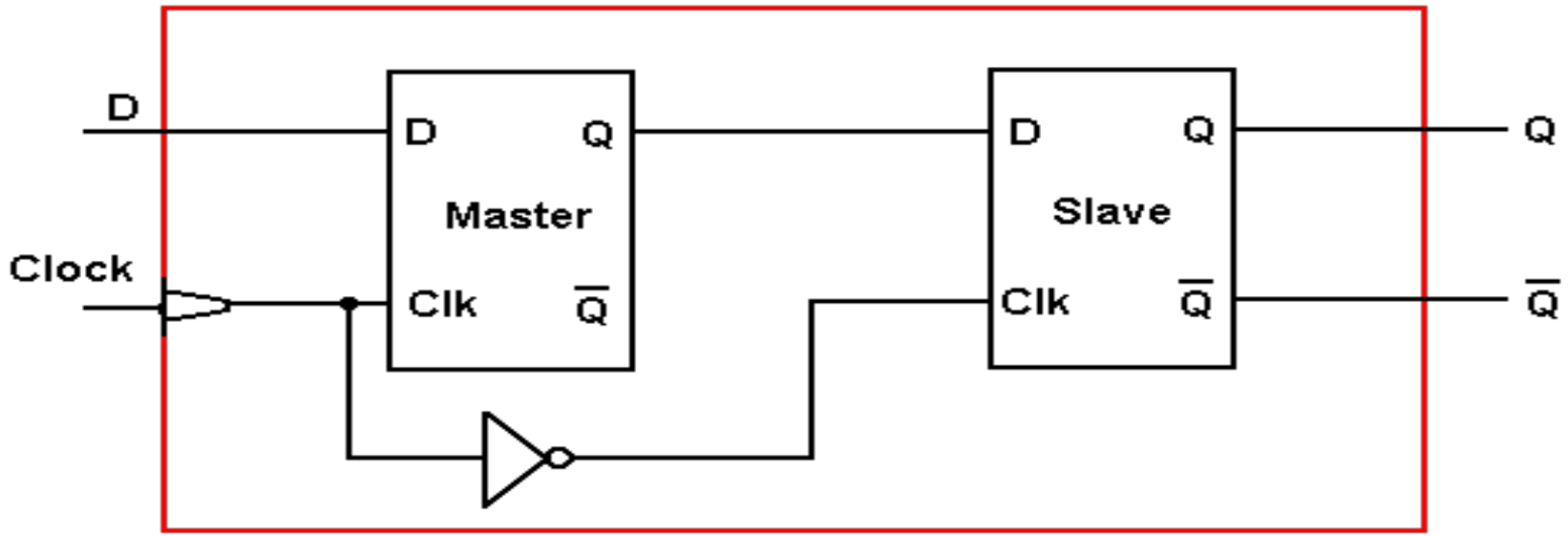
respond to the input only during these periods

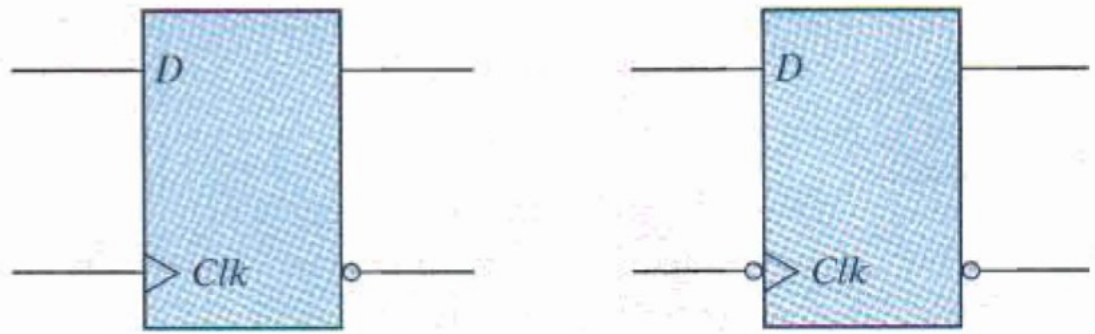
Edge-triggered Flip Flops (positive)



respond to the input only at this time

Concept of Master and Slave Flip-Flop



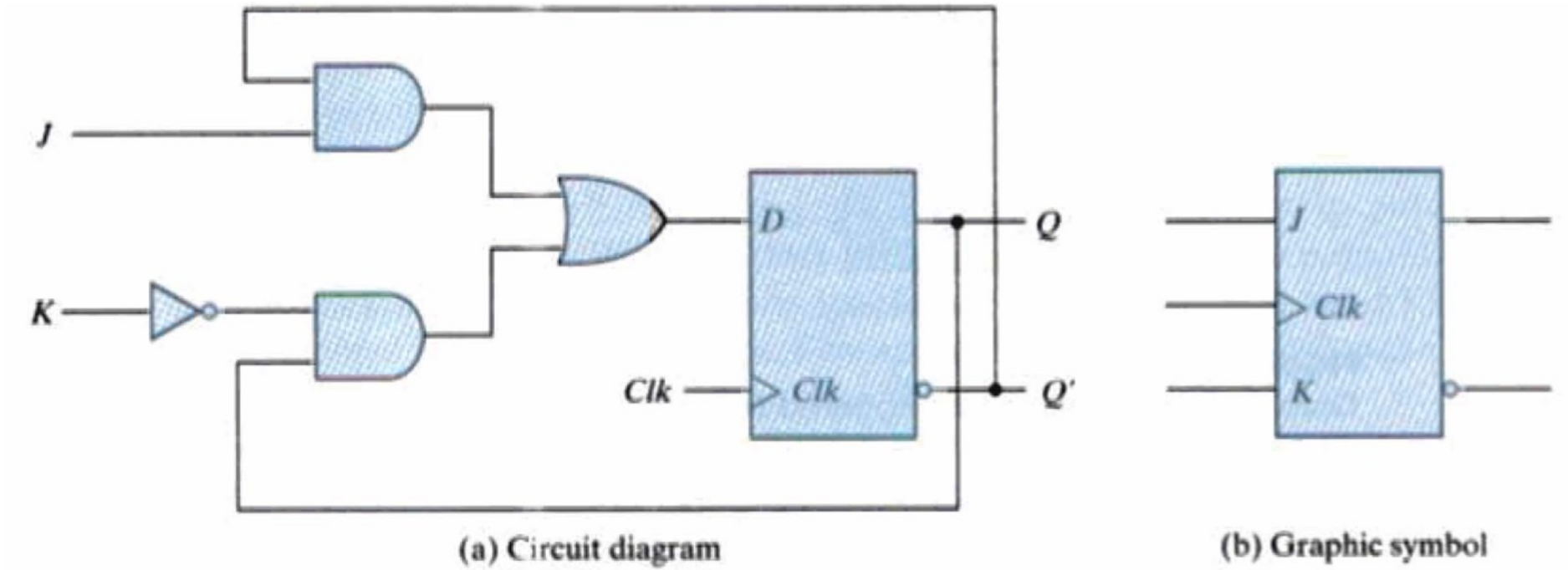


(a) Positive-edge (a) Negative-edge

FIGURE 5.11
Graphic symbol for edge-triggered *D* flip-flop

JK Flip-Flop

- Has 2 inputs



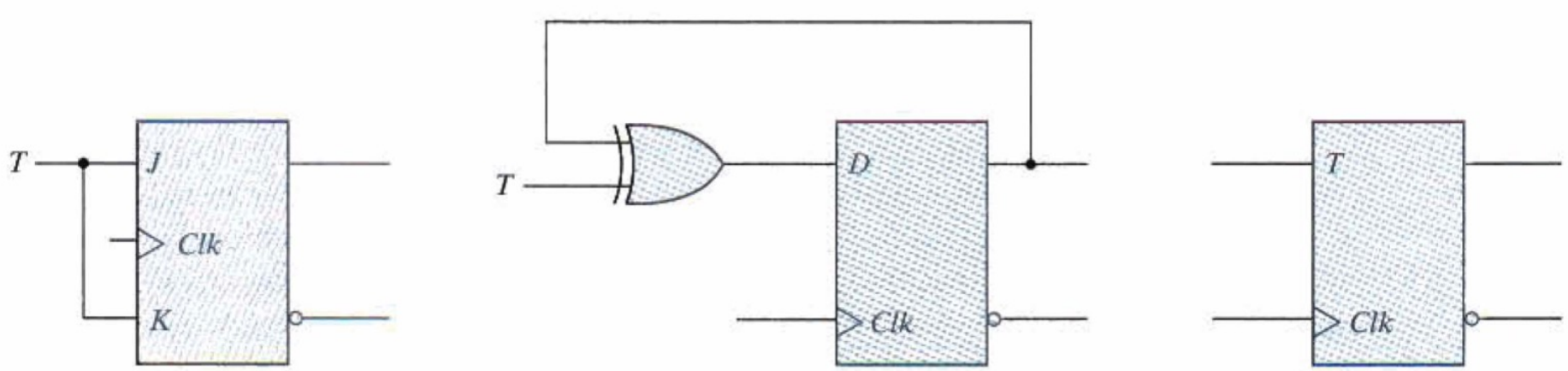
(a) Circuit diagram

(b) Graphic symbol

FIGURE 5.12
JK flip-flop

T Flip-Flop

- A complementing flip-flop
- Obtained from a JK flip-flop when inputs J & K are tied together.
- Useful in binary counters



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

FIGURE 5.13
T flip-flop

Characteristic Table

- Defines the logical properties of a flip-flop by describing its operation in tabular form.
- Q(t) – present state at time t
- Q(t+1) – next state at time t+1

Characteristic Tables (cont.)

D Flip-Flop

D	Q(t+1)	Operation
0	0	Reset
1	1	Set

Characteristic Equation: Q(t+1) = D(t)

Characteristic Tables (cont.)

JK Flip-Flop			
J	K	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

Characteristic Equation: $Q(t+1) = JQ'+K'Q$

Characteristic Tables (cont.)

T Flip-Flop

T	Q(t+1)	Operation
0	Q(t)	No change
1	Q'(t)	complement

Characteristic Equation: $Q(t+1) = T'Q+TQ'$

Analysis of Clocked Sequential Circuits

- A. State Equations
  - Specifies the next state as a function of the present state and inputs
- B. State Table
  - Enumerates the time sequence of inputs, outputs and flip-flop states
- C. State Diagram
  - Graphically shows the time sequence of inputs, outputs and flip-flop states

Example

- Construct the state equations and the equivalent Boolean equation for the output y(t).
- Construct the equivalent state table and state diagram of the sequential circuit.