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# Effective Drive Current in Scaled FinFET and NSFET CMOS Inverters

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**Abstract-**This work investigates the impact of CMOS scaling on the DC effective drive current,  $I_{eff}$  [1],  $I_{eff}=1/2 \times (I_{high}+I_{low})=1/2 \times [I_{ds}(V_{gs}=0.5V_{dd}), V_{ds}=V_{dd})+I_{ds}(V_{gs}=V_{dd}, V_{ds}=V_{dd}/2)]$  of aggressively scaled MOSFETs down to 7nm node technology. FinFET and Nanosheet (NSFET) architectures [2], [3] behave similarly, and  $I_{eff}$  continues to predict the intrinsic delay for aggressively scaled MOSFETs for both device architectures, even for supply-voltages ( $V_{dd}$ ) as low as  $\sim 0.2V$ , where these devices operate in the subthreshold regime. The ratio of  $I_{eff}/I_{on}$ ,  $I_{on}=I_{ds}(V_{ds}=V_{gs}=V_{dd})$ , as a function of  $V_{dd}$ , and threshold voltage ( $V_{th}$ ) show that this ratio can be significantly modulated about a typical value of  $\sim 0.5$ , in a manner that can be easily related to classical MOSFET behavior.

**CMOS Inverter  $I_{eff}/I_{on}$  Characteristic-**Previously it has been shown that  $I_{eff}$  is a more accurate predictor of intrinsic gate delay for sub-90nm node CMOS technologies as opposed to traditional on-current ( $I_{on}$ ) [1]. More recently, transistor scaling has been driven by FinFET, perhaps soon to be followed by NSFETs. A compact-model direct comparison of traditional ( $V_{dd}/I_{dsat}$ ) and ( $V_{dd}/I_{eff}$ ) representing drive impedance ( $R_{SW}$ ) for various technologies including 7nm node FinFET and NSFET (Fig. 1) devices clearly indicates that  $I_{eff}$  is a solid predictor of intrinsic gate delay even for aggressively scaled MOSFETs (Fig. 2). TCAD Ring-Oscillator simulations based on 7nm node FinFET and NSFET platforms (Fig. 3) show that the original  $I_{eff}$  approximation remains accurate for recent technology nodes. Fig. 3 also shows that  $I_{eff}$  can still describe the transistor performance even when  $V_{dd}$  is scaled down to extremely low values, as low as  $\sim 0.2V$ , where these devices are operating near threshold or even in the sub-threshold regime.

**FinFET vs NSFET  $I_{eff}/I_{on}$  Characteristic-**In recent years power reduction has put a much pressure on  $V_{dd}$  scaling, which requires near threshold operation. In order to evaluate the performance of individual transistors,  $I_{eff}/I_{on}$  behavior of 7nm node FinFET and NSFET transistors here are studied for scaled  $V_{dd}$  values. Devices are selected to have similar channel lengths and threshold voltages ( $V_{th}$ ) to allow direct comparison of the device on-state behavior (Fig. 4). Since transistor intrinsic delay is well-connected to the DC  $I_{eff}$ , the  $I_{eff}/I_{on}$  behavior is of interest as it directly relates to stage delay for both above-threshold and below-threshold. Fig. 5 shows the  $V_{dd}$  and  $V_{th}$  dependency of  $I_{eff}/I_{on}$  for FinFET and NSFET transistors. Intuitively,  $V_{th}$  reduction boosts  $I_{eff}/I_{on}$  in both nMOS and pMOS. Note that nMOS FinFET and NSFET behave very similarly, with small positive slope vs  $V_{dd}$ . In contrast, while the average values for the pMOS ratios are quite similar for the two architectures, they show opposite-sign slopes vs  $V_{dd}$ . We identified two mechanisms that can explain this trend. The first is driven by the fact that the primary conduction planes in NSFETs are on (100) surfaces, while those of the FinFET are (110). The lower ( $\sim 1/2 \times$ ) hole mobility associated with the (100) plane can give rise to a higher pinch-off voltage in the pMOS NSFET for higher  $V_{gs}$ , pushing  $I_{high}$  into the triode region of operation. This mechanism would be hidden in bulk planer pFETs due to very large  $DIBL$  in those architectures. The second mechanism can be described through basic phenomenological MOSFET description ( $V_{th}$ ,  $g_m$ ,  $g_{ds}$ , SS,  $DIBL$ ). Fig. 6-9 illustrate the comparison of normalized nMOS and pMOS output characteristics for FinFET and NSFET, when  $V_{dd}$  is set to high and low values of 0.7V and 0.5V respectively. Although, nMOS FinFET and NSFET have an output conductance ( $g_d$ ) mismatch at lower gate voltages, the output characteristics demonstrate an overall comparable on-state behavior (Fig. 6-7). The on-state behavior difference is more pronounced in pMOS devices (Fig. 8-9). pMOS FinFET behaves more like a typical short channel device while pMOS NSFET exhibits long-channel-like behavior. From the device physics point of view, structural differences that drive the electrostatic deviations cannot be the only factor, as the nMOS and pMOS NSFETs have similar subthreshold-slope (SS) and  $DIBL$ . Table 1 shows nMOS and pMOS phenomenological metrics, and it's clear that pMOS NSFET shows one significant parametric difference, namely higher  $g_d/(DIBL \times g_m)$  meaning that  $g_d$  and  $DIBL$  don't have the anticipated correlation.  $g_d$  is expected to be equal to  $DIBL \times g_m$  for a healthy MOSFET. We suspect that channel non-uniformity due to a parallel bulk-channel at the bottom of the NSFET stack is the cause of the pMOS  $I_{eff}/I_{on}$  behavior. A very simple model constructed from the parallel combination of pure Nanosheets with near-ideal  $SS_{sat}$  and low  $DIBL$ , and a bulk MOSFET (see Fig 1), with much higher  $DIBL$  and  $SS_{sat}$ , but with elevated  $V_{th}$ , which 'hides' the subthreshold behavior of this component, is illustrated in Fig. 10. Note that from this simple two-component model, the key feature of high  $g_d/(DIBL \times g_m)$  emerges quiet easily.

**Conclusion-** It is shown that  $I_{eff}$  remains a sound quantitative metric for intrinsic transistor/inverter delay in device architectures and operation regimes needed for scaling below the 7-nm node. This remains true even when supply-voltage ( $V_{dd}$ ) is reduced to or below  $V_{th}$ , making  $I_{eff}$  a valuable metric for low-power/IoT CMOS applications.

**Reference-[1]** M.H. Na, et al., "The Effective Drive Current in CMOS Inverters" IEDM Tech. Digest, , pp. 2.7.1-2.7.4, December 2002. [2] R. Xie, et al., "A 7nm FinFET Technology Featuring EUV Patterning and Dual Strained High Mobility Channels", IEDM Tech. Digest, pp. 2.7.1-2.7.4, December 2016. [3] N. Loubet, et al. "Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET." VLSI Tech. Digest, pp. 230-231, May 2017.

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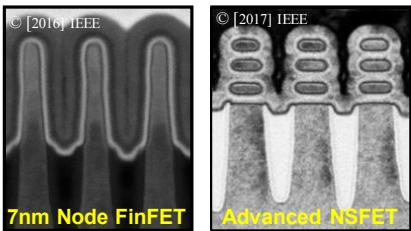


Fig. 1 Cross-sectional TEM images of the FinFET and NSFET devices used in this study [2], [3].

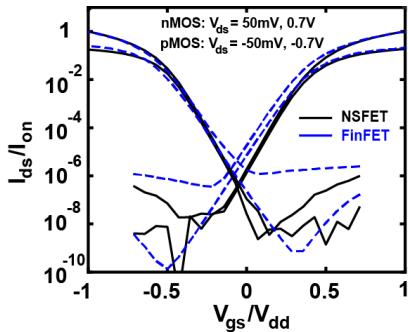


Fig. 4 Normalized transfer characteristics of FinFET and NSFET with matched  $V_{th}$  and  $L_{Gate}$ .

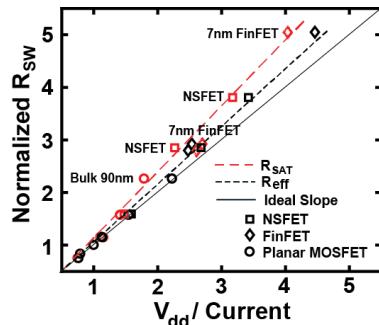


Fig. 2 Extracted  $R_{sw}$  from compact models for 7nm FinFET and NSFET shows that  $I_{eff}$  remains a more accurate delay predictor than  $I_{on}$ , as observed in previously published data.

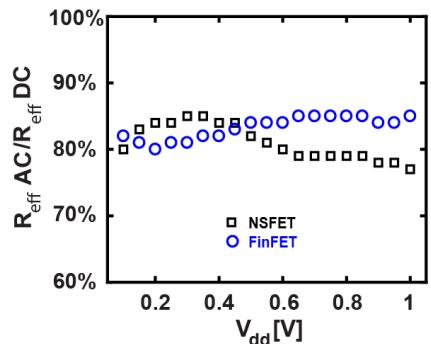


Fig. 3 Compact model based  $R_{eff}$   $AC/R_{eff} DC$  vs  $V_{dd}$  for FinFET and NSFET shows that  $I_{eff}$  remains an accurate predictor of gate delay, even for supply voltages as low as 0.2V.

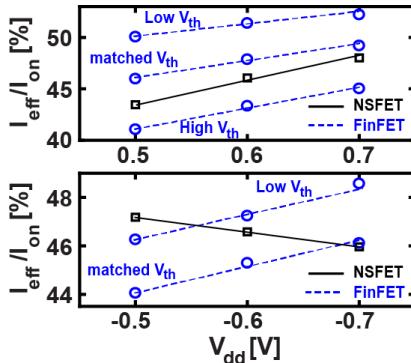


Fig. 5  $I_{eff}/I_{on}$  comparisons for a) nMOS and b) pMOS NSFET and FinFET. pMOS NSFET exhibits reverse voltage dependency. pMOS FinFET  $V_{th}$  is varied to show that this is unable to account for this effect.

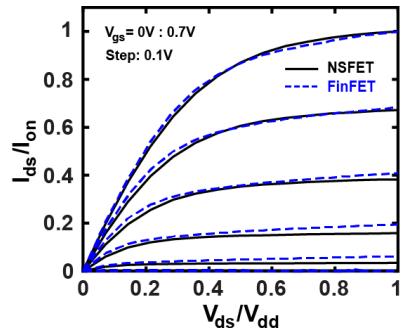


Fig. 6 Normalized output characteristics of nMOS FinFET and NSFET for the  $V_{dd}$  of 0.7V.

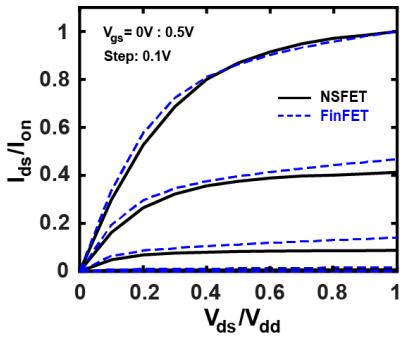


Fig. 7 Normalized output characteristics of nMOS FinFET and NSFET for the  $V_{dd}$  of 0.5V.

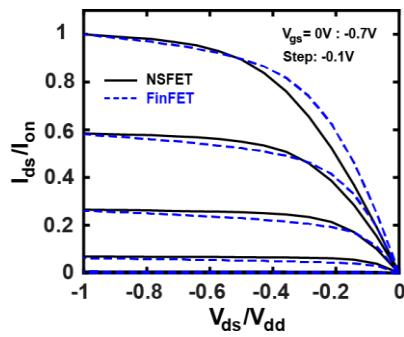


Fig. 8 Normalized output characteristics of pMOS FinFET and NSFET for  $V_{dd}$  of -0.7V.

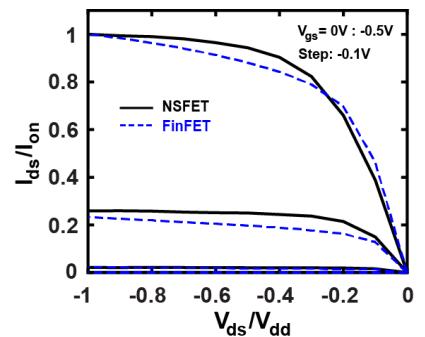


Fig. 9 Normalized output characteristics of pMOS FinFET and NSFET for the  $V_{dd}$  of -0.5V.

	NSFET		FinFET	
	nFET	pFET	nFET	pFET
SS (mV/Decade)	67	63	75	87
DIBL (mV/V)	25	15	52	37
$g_m$ ( $\mu\text{S}$ )	14.30	4.50	5.70	3.44
$g_d$ ( $\mu\text{A}$ )	0.56	0.16	0.40	0.16
$g_d/(g_m \times DIBL)$	1.60	2.31	1.34	1.26

Table 1 Summary of on/off state phenomenological description of FinFET and NSFET transistors.  $g_d/(DIBL \times g_m)$  is typically close to unity; two mechanisms are discussed to account for the larger value in the pMOS NSFET.

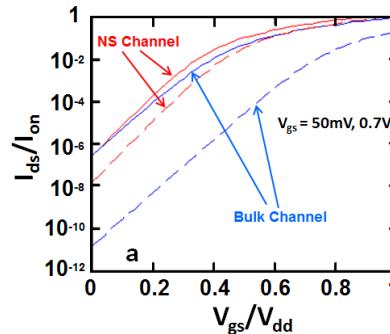


Fig. 10 a) Simulations results for transfer characteristics of a pure NSFET and a buck parasitic device with higher  $V_{th}$ , SS and DIBL. b) The output characteristics clearly show the effect of the parasitic device on the overall on-state behavior.