

Training-Free Parameter Extraction for Compact Device Models Using Sequential Bayesian Optimization With Adaptive Sampling

Om Maheshwari¹, Graduate Student Member, IEEE, Aishwarya Singh¹, Associate Member, IEEE, and Nihar R. Mohapatra¹, Senior Member, IEEE

Abstract—This work presents a computationally efficient approach for extracting compact model parameters with minimal training requirements. Bayesian optimization (BO) is employed in multiple stages to predict the optimum compact model parameters. Initially, the methodology is applied to the MIT virtual source model (MVS 2.0) for extremely thin silicon-on-insulator (ETSOI) devices, nanosheet FETs (NsFETs), and MoS₂-based 2-D material-based FETs (2DFETs). Subsequently, it is demonstrated on the Berkeley short-channel IGFET model (BSIM) common multigate (CMG) compact model for NsFETs. Through sequential processing, adaptive sampling, successive domain reduction, and fine-tuned objective functions, the framework achieves precise and efficient fitting of both global and local model parameters across a range of devices, all in a reduced number of iterations, irrespective of the compact model used.

Index Terms—2-D material-based FET (2DFET), Bayesian optimization (BO), Berkeley short-channel IGFET model (BSIM) common multigate (CMG), compact model, extremely thin silicon-on-insulator (ETSOI), MIT virtual source (MVS) model, nanosheet FET (NsFET), parameter extraction.

I. INTRODUCTION

DEVICE compact models are essential for integrated circuit design, as they represent device behavior through mathematical equations and model parameters, facilitating SPICE simulations. Accurate extraction of these model parameters is crucial to match the modeled device behavior with the measured results while maintaining the integrity of the underlying device physics. Conventionally, extracting and fine-tuning model parameters require expertise and consumes

Received 14 August 2024; revised 19 September 2024; accepted 7 October 2024. Date of publication 25 October 2024; date of current version 2 December 2024. This work was supported in part by the Ministry of Education (Government of India) through Prime Minister's Research Fellowship under Grant 1701656. The review of this article was arranged by Editor Y. Chauhan. (Corresponding author: Om Maheshwari.)

The authors are with the Department of Electrical Engineering, Indian Institute of Technology at Gandhinagar, Gandhinagar, Gujarat 382355, India (e-mail: om.maheshwari@iitgn.ac.in; singh_aishwarya@iitgn.ac.in; nihaar@iitgn.ac.in).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TED.2024.3478177>.

Digital Object Identifier 10.1109/TED.2024.3478177

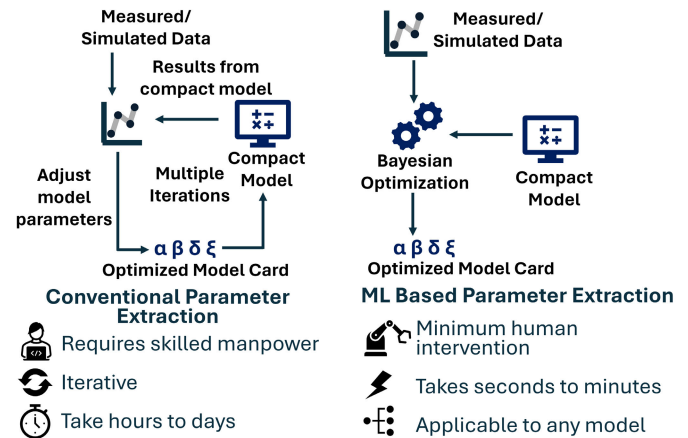


Fig. 1. Parameter extraction strategy using BO. The approach requires no training, is flexible across bias points and across the number of parameters, and converges within a few iterations.

considerable time. The extraction process becomes notably more difficult for scaled devices, such as FinFETs, nanosheet FETs (NsFETs), and 2-D material-based FETs (2DFETs), because of increased complexity in compact models, incorporating quantum confinement and various nonideal effects. For instance, the Berkeley short-channel IGFET model (BSIM) for common multigate (BSIM-CMG) FET has over a thousand parameters for fine-tuning [1], [2].

Machine learning and optimization algorithms hold promise for streamlining the parameter extraction process, alleviating manual efforts (Fig. 1). Recently, there has been a surge in deep-learning (DL)-based approaches [2], [3], [4], [5], capable of predicting compact model parameters from terminal characteristics. However, these methods exhibit significant complexity, often comprising millions of trainable parameters, and demand substantial amounts of training data, thereby imposing a heavy computational burden. In addition, even minor inaccuracies during training can jeopardize the reliability of DL model predictions for critical compact model parameters. Furthermore, the DL models demonstrate limited adaptability to input variations, necessitating specific bias points aligned with pretrained capacitance–voltage (C – V) and current–voltage (I – V) models [2], [3], [4], or simultaneous training of numerous models to achieve such flexibility [5].

The validity of this extraction strategy has only been demonstrated for a narrow range of device dimensions [2], [5]. Furthermore, the DL-based methods lack flexibility to accommodate changes or additions to compact model parameters, necessitating retraining of the model for any such modifications.

In contrast, optimization-based approaches offer a promising avenue to reduce manual effort without the need for additional model training. For instance, Li et al. [6] proposed a genetic algorithm-based optimization strategy for BSIM parameter extraction. However the approach is iterative and computationally expensive. On the other hand, Bayesian optimization (BO), with simple objective functions, presents a computationally efficient alternative to evolutionary algorithms, with fewer tunable parameters within the algorithm [7].

In this study, we introduce a sequential parameter extraction methodology for compact models that utilizes BO. Our approach is distinguished by its simplicity, lack of training requirements, and minimal computational demands. It mirrors the intuitive nature of manual parameter extraction while ensuring the physical validity of the parameters derived. A key feature of our strategy is its flexibility, allowing for adjustments to model parameters at any stage of the extraction process. The methodology employs sequential optimization, adaptive sampling guided by an acquisition function, and successive domain reduction. These techniques synergistically propel the BO method toward precise and efficient parameter extraction. We have validated the effectiveness of our approach using a diverse array of devices, including extremely thin silicon-on-insulator (ETSOI), NsFETs, and MoS₂-based 2-D FETs, demonstrated using the MIT-virtual source model (MVS 2.0) [8], [9]. The extracted parameters consistently produce accurate terminal characteristics within a limited number of iterations. In addition, our method supports predictive analysis of advanced FETs using legacy compact models. We further demonstrate the model-agnostic nature of our algorithm through validation with the BSIM CMG [1] model for NsFETs, confirming its applicability across different compact models.

This article is structured as follows. Section II explains the methodology for compact model parameter extraction, providing a comprehensive overview of the proposed algorithm. Section III presents the validation of parameter extraction results followed by the conclusion in Section IV.

II. METHODOLOGY

A. Compact Model

1) *MVS Compact Model*: We have used the MVS 2.0 model to illustrate our methodology. This model, characterized by charge-based quasi-ballistic transport, is particularly suited for thin-channel devices [8], [9]. Table I lists the compact model parameters for MVS 2.0. For each transistor under consideration, we first identify the known device and material parameters (L , W_{eff} , C_{OX} , m_l , m_t , and $x_{\text{av},0}$) and then extract the subthreshold swing factor (n_0) from either measured or simulated linear transfer characteristics. It is worth noting that while the MVS model was originally formulated for

TABLE I
MVS MODEL PARAMETERS

Symbol	Model Parameter
L	Gate Length
W_{eff}	Effective Width of the channel
C_{OX}	Oxide capacitance
m_l	Longitudinal effective mass
m_t	Transverse effective mass
n_0	Subthreshold swing factor
$x_{\text{av},0}$	Distance between charge centroid from interface at low V_G
$E_{\text{fs}} - \epsilon \Delta 2$	Energy difference between source fermi level and first sub-band
ν	Relative occupancy of $\Delta 2$ sub-bands
B	Quantum mechanical correction factor
μ_{eff}	Effective mobility
$R_{\text{s,d}}$	Source/Drain access resistance
δ	DIBL factor
n_d	Punch through factor
β	Control slope of saturation function
ξ	Coefficient for velocity saturation injection velocity

TABLE II
BSIM CMG MODEL PARAMETERS

Symbol	Model Parameter
QMFACTOR	Prefactor for quantum mechanical (QM) threshold voltage shift correction
QMTCENCV	Prefactor for QM effective width and oxide thickness correction for CV
PQM	Fitting parameter for QM charge centroid (inversion)
PHIG	Gate Workfunction
CIT	Parameter for interface trap
U0	Low Field Mobility
RDSW	Zero bias S/D extension resistance per unit width
UA, EU	Phonon/surface roughness scattering parameter
UD	Coulombic scattering parameter
ETA0	DIBL coefficient
VSAT	Saturation velocity for the saturation region
CDSCD	Drain-bias sensitivity of CDSC
KSATIV	Parameter for long channel Vdsat
MEXP	Smoothing function factor for Vdsat

ETSOI (thin-film) devices with (100)/[100] substrate orientation/transport direction, we have extended its applicability to stacked gate all-around NsFETs with (100)/[110] substrate orientation/transport direction and MoS₂-based 2DFETs. For NsFETs, the conduction effective mass (m_c) in $\Delta 2$ (1), $\Delta 4$ (2) sub-bands, and DOS effective mass (m_{dos}) (3) are modified, whereas for 2DFETs, only mass (m_{dos}) is modified

$$m_{c,\Delta 2} = m_t \quad (1)$$

$$m_{c,\Delta 4} = (m_l + m_t)/2 \quad (2)$$

$$m_{\text{dos}} = 2\sqrt{m_l m_t}. \quad (3)$$

These modified relations enable the applicability of the model for devices with conventional (100)/[110] substrate orientation/transport direction using MVS 2.0 model [10], [11].

2) *BSIM CMG Compact Model*: To demonstrate that the proposed parameter extraction approach is independent of the compact model used, we use BSIM CMG version 112.0.0beta0_4 [1] for modeling NsFETs. The BSIM CMG model offers different modules for different geometric device structures. For NsFETs, we have used GEOMOD = 5, and the structural parameters are gate length $L = 20$ nm and sheet width WGAA = 20 nm, and the sheet thickness TGAA is

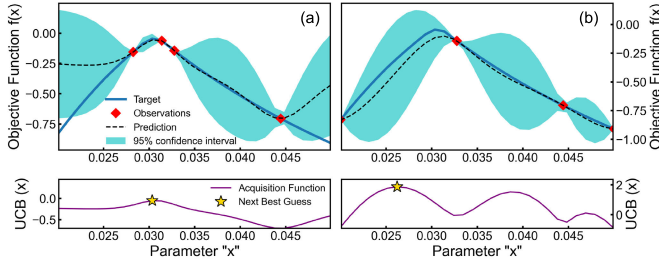


Fig. 2. Gaussian process surrogate model of the objective function and the UCB acquisition function. The samples are drawn near the maximum of the mean value of the surrogate for (a) $\lambda = 0.1$, whereas the samples are drawn in the most uncertain regions in case of (b) $\lambda = 10$.

varied from 5 to 9 nm. Table II lists the key compact model parameters in BSIM CMG, which are to be calibrated.

B. Bayesian Optimization

The BO algorithm constructs a posterior distribution of the objective function using Gaussian processes, aiming to either minimize or maximize it [7]. In each trial, a new value is sampled from the objective function within the parameter domain, guided by the acquisition function. For this study, we employed the upper confidence bound (UCB) acquisition function [12], which is given as follows:

$$\text{UCB}(x) = \mu(x) + \lambda\sigma(x). \quad (4)$$

Here, $\mu(x)$ represents the mean of the surrogate (Gaussian process model), $\sigma(x)$ denotes the standard deviation, and x signifies the model parameter upon which the objective function relies. The next value is sampled at the point where $\text{UCB}(x)$ is maximum. The UCB acquisition function balances exploration and exploitation through the parameter λ . As depicted in Fig. 2, a higher λ encourages sample selection in regions where uncertainty is maximum in the surrogate model [exploration, $\lambda\sigma(x) \gg \mu(x)$], while a lower λ steers the acquisition function toward selecting the next sample where the mean of the current surrogate model is maximum [exploitation, $\mu(x) \gg \lambda\sigma(x)$].

C. Implementation

The different elements, which are implemented to make the proposed parameter extraction strategy accurate and efficient, are described as follows.

1) **Sequential BO:** The model parameters are extracted in four sequential stages of BO, as illustrated in Fig. 3. Of the 16 parameters outlined in Table I for the MVS 2.0 model, seven parameters are predetermined [L , W_{eff} , C_{OX} , m_l , m_t , $x_{\text{av},0}$, and n_0], leaving nine parameters for optimization. The first stage optimization focuses on charge-based parameters, wherein B , v , and $E_{\text{fs}} - \epsilon_{\Delta 2}$ are calibrated using the $C_G - V_G$ characteristics. Subsequently, parameters governing linear transfer characteristics ($E_{\text{fs}} - \epsilon_{\Delta 2}$, μ_{eff} , and $R_{s,d}$) are calibrated, with $E_{\text{fs}} - \epsilon_{\Delta 2}$ readjusted to mitigate any threshold voltage mismatch. In the following stage, parameters, such as n_d , δ , and ξ , are extracted from the saturation transfer characteristics. Finally, β and ξ are fine-tuned based on the output

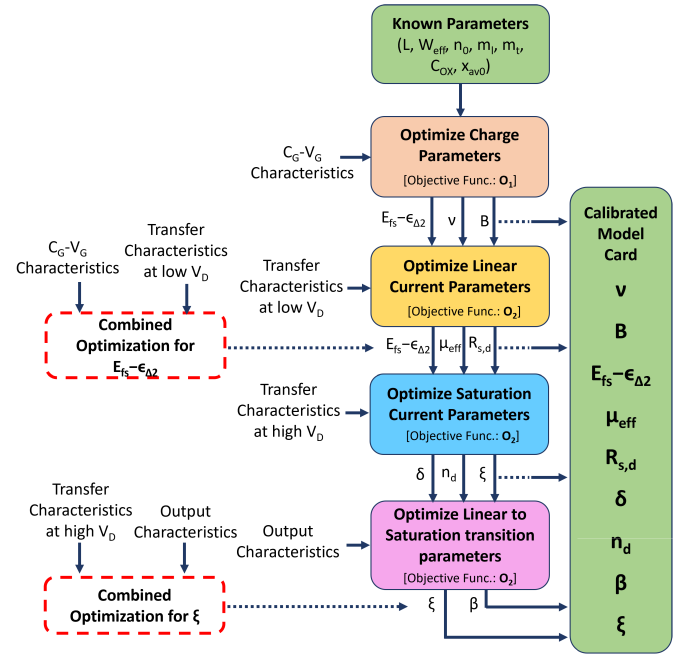


Fig. 3. Sequential BO flow for extraction of MVS model parameters. The extraction is performed in four stages of BO, utilizing measured/simulated $C_G - V_G$ and $I - V$ characteristics and objective functions O_1 (5) and O_2 (6). Parameters coupled across different characteristics are fine-tuned in additional stages.

characteristics. This sequential parameter extraction mirrors manual processes, where electrostatic and transport parameters are sequentially adjusted in different stages. This also ensures the physical validity of the extracted model parameters. Thus, through four sequential stages of BO, a calibrated model card is obtained. Multiple stages can be further added in the sequential BO flow for refinement of parameters coupled across different characteristics, such as $E_{\text{fs}} - \epsilon_{\Delta 2}$ and ξ .

A similar strategy is employed for BSIM CMG model where QMFACTOR, QMTCENCV, PQM, and PHIG are calibrated first for $C_G - V_G$ characteristics, followed by PHIG, CIT, U0, RDSW, UA, EU, and UD for linear $I_D - V_G$ and ETA0, CDSCD, VSAT, and KSATIV in saturation. Along with MEXP, VSAT and KSATIV are refined with output characteristics.

2) **Objective Functions:** The objective function, crucial for the BO process, aims to maximize by minimizing the relative mismatch between modeled and target electrical characteristics. For the $C_G - V_G$ characteristics, it is defined as follows:

$$O_1 = -\frac{1}{N} \sum N \frac{|\Delta C_G|}{C_{G,\text{in}}}. \quad (5)$$

Here, N represents the number of data points in the $C_G - V_G$ curve, $C_{G,\text{in}}$ stands for the measured or simulated gate capacitance (input to the framework), and ΔC_G denotes the difference between modeled gate capacitance and $C_{G,\text{in}}$. For transfer and output characteristics, the objective function is the relative difference between the target and modeled high bias current, low bias current, and slope, expressed as follows:

$$O_2 = -\left(2 \frac{|\Delta I_{\text{HIGH}}|}{I_{\text{HIGH},\text{in}}} + 2 \frac{|\Delta I_{\text{LOW}}|}{I_{\text{LOW},\text{in}}} + \frac{|\Delta \text{slope}|}{\text{slope, in}}\right). \quad (6)$$

Algorithm 1 Bayesian Optimization Loop

```

objective = -error [function  $O_1$  or  $O_2$ ]
Initialize PBounds,  $\lambda$ , BestObj  $\leq -1$ 
while BestObj  $\leq -0.01$  and  $\lambda > 0.1$  do
    acquisition = UCB( $\lambda$ )
    optimizer = Bayesian(objective, PBounds, acquisition)
    results = maximize(optimizer,  $i$  iterations)
    current BestObj, top 5 results  $\leftarrow$  results
    Extract parameters  $\leftarrow$  top 5 results
    PBounds = [ $\alpha$ min(parameters),  $\gamma$ max(parameters)]
    if previous BestObj < current BestObj then
        Extract parameters  $\leftarrow$  previous BestObj
        PBounds = [ $\alpha$ parameters,  $\gamma$ parameters]
    end if
     $\lambda \leftarrow \lambda/2$ 
end while

```

Definitions

BestObj: best value of objective after maximization

PBounds: parameter bounds

α and γ : parameters to adjust PBounds in each iteration

$\alpha \leq 1$, $\gamma \geq 1$

Here, I_{HIGH} and I_{LOW} represent the currents at maximum and minimum bias points, respectively, for the given I - V characteristics. The slope corresponds to the subthreshold slope for transfer characteristics and the saturation slope for output characteristics. The relative mismatch in I_{HIGH} and I_{LOW} is weighted (2 in this work), imposing a higher penalty for mismatches at extreme bias points. It is noteworthy that the objective functions O_1 and O_2 are designed to be negative, as the trajectory of BO aims to maximize the objective function, thereby minimizing the relative error in modeled and experimental electrical characteristics.

3) Algorithm: The algorithm for the BO loop is illustrated in Algorithm 1. This algorithm is deployed at each stage of the sequential BO process to optimize a specific set of parameters.

4) Initialization: For each stage, we start by initializing the model parameter search space or bounds (PBounds) and the acquisition function parameter λ . These parameters are then iteratively refined within the BO loop (Algorithm 1), till the target objective is not achieved with 99% confidence within i iterations. The initial value of λ is set to 10, and it is halved every $i = 15$ iterations, unless the maximized objective function surpasses -0.01 (indicating a relative error between model and input data of less than 1%). If the error fails to converge, the algorithm concludes when $\lambda < 0.1$.

5) Balancing Exploration and Exploitation Through Adaptive Sampling: At the outset of the optimization problem, the initial range of the search space in PBounds tends to be quite broad. Thus, it is advantageous to explore this wide search space initially to identify potential global optima. Therefore, λ in (4) is initialized with a large value, enabling the acquisition function to guide the selection of the next sample where uncertainty is high. As the optimization progresses, the gradual reduction in λ steers the algorithm towards convergence to the best-known optima. This adaptive transition from exploration to exploitation facilitates convergence to a global optimum in

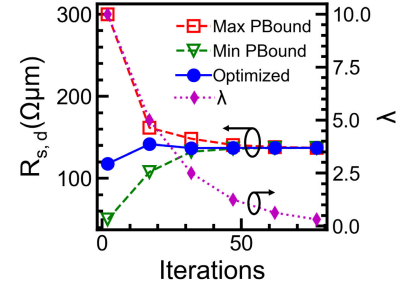


Fig. 4. Domain reduction in PBounds and the optimized value of parameter ($R_{s,d}$) with number of iterations. This helps to achieve the optimized parameter value in lesser iterations. λ is successively reduced from an initial value of 10 to direct the sampling from exploration to exploitation.

fewer iterations, mitigating the risk of the optimizer getting trapped in oscillations during the optimization process.

6) Successive Domain Reduction: PBounds undergo updates every i iterations, where the maximum and minimum parameter values among the best 5 from the previous i iterations are chosen as the limits for the PBounds in the subsequent iterations. This targeted domain reduction within the parameter space significantly contributes to efficiently maximizing the objective function within fewer iterations. This is exemplified in the case of parameter $R_{s,d}$ in Fig. 4, where the domain of the PBounds progressively diminishes with increasing iterations until the algorithm converges to an optimized parameter value. In addition, α and γ serve as scaling factors for tuning the parameter space, offering control over the expansion or contraction of the search space. In this study, typical values of α and γ range between 0.9 and 1 and between 1 and 1.1, respectively.

Thus, the sequential optimization approach not only reduces the number of parameters tuned at each stage, enhancing the performance of the BO process, but also provides an intuitive grasp of the underlying physics governing the predicted model parameters. The optimization efficiency is upheld through domain reduction, while a balance between exploration in the initial iterations and exploitation toward the end is maintained through adaptive sampling in the acquisition function. This optimization-based parameter strategy allows for the flexibility to introduce additional stages or parameters for optimization without the need for generating any additional training data.

III. RESULTS AND DISCUSSION

The proposed parameter extraction strategy is rigorously validated using experimental and simulation data obtained from a variety of devices, including ETSOI FETs, NsFETs, and 2DFETs, spanning different device dimensions. Experimental data from IBM [9], [13], concerning ETSOI devices with a silicon thickness (t_{Si}) of 6 nm and a width of 1 μm , are employed for validation, as shown in Fig. 5. Following the sequential strategy outlined in Fig. 3, we first calibrate the charge-based parameters of MVS model using the C_G - V_G characteristics shown in Fig. 5(a). Subsequently, the model's fit across various gate lengths (L) of 30, 40, and 50 nm is illustrated through the linear, saturation transfer characteristics, and output characteristics presented in Fig. 5(b)-(d), respectively.

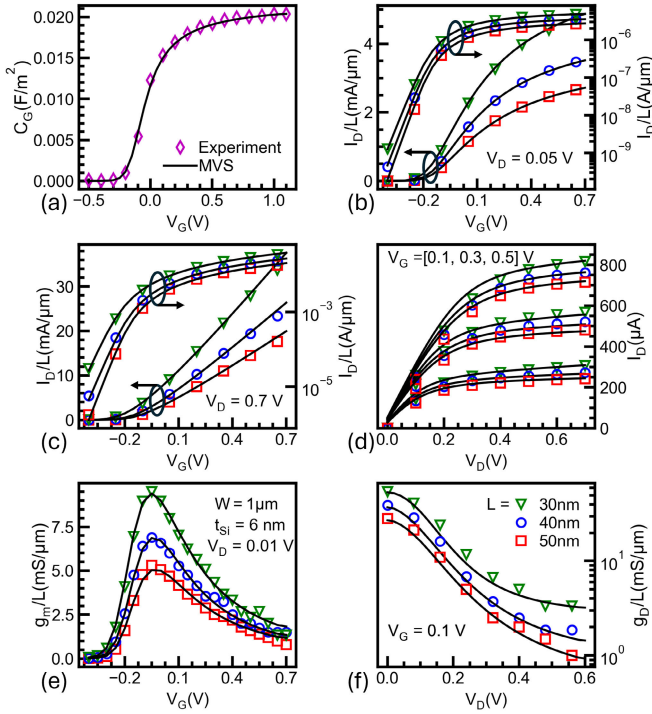


Fig. 5. Validation of parameter extraction strategy for experimental ETSOI device [9], [13] for varying gate length (L). Charge parameters are optimized for obtaining matched (a) gate capacitance, and transport parameters are optimized for (b) linear, (c) saturation transfer characteristics, (d) output characteristics, (e) transconductance, and (f) output conductance. The model is in good agreement with the experiments.

The excellent agreement observed between the model and experimental data [Fig. 5(e) and (f)] underscores the accuracy of the parameters extracted using the proposed methodology, further validating its efficacy.

The parameter extraction method is additionally validated for NsFET device configurations with three sheets, simulated within a well-calibrated TCAD deck. Fig. 6 illustrates the MVS model fit for a 20×20 nm ($L \times W$) NsFET device using the calibrated parameters. Specifically, the plotted (a) C_G - V_G , (b) I_D - V_G linear, (c) I_D - V_G saturation, and (d) I_D - V_D characteristics across varying sheet thickness t_{Si} demonstrate good agreement between the model and simulation. Furthermore, we analyze the trends in the predicted physical parameters [Fig. 7(a) ν , (b) $E_{fs}-\epsilon_{\Delta 2}$, (c) μ_{eff} , and (d) $R_{s,d}$] for different t_{Si} values. The parameter ν , indicating the probability of occupancy of $\Delta 2$ sub-bands, and $E_{fs}-\epsilon_{\Delta 2}$, relating to the threshold voltage of the device, both increase with a reduction in t_{Si} . This confirms that the predicted parameters align with the theories of quantum confinement [14]. The reduction in effective mobility (μ_{eff}) with decreasing t_{Si} is consistent with experimental research findings [15]. In addition, the decrease in source-drain access resistance $R_{s,d}$ with increasing t_{Si} is valid, as the nanosheet's cross-sectional area increases with t_{Si} .

Fig. 8(a) presents the simulated and modeled C_G - V_G characteristics of NsFETs with different gate lengths (L) at low V_D . The C_G - V_G model parameters B and ν remain fixed for a given technology and do not vary with L . The observed

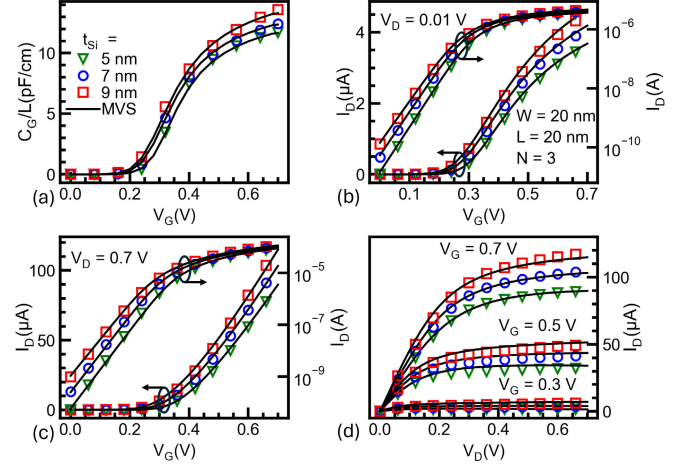


Fig. 6. Validation of parameter extraction strategy using MVS for NsFET device for varying sheet thickness (t_{Si}). Charge parameters are optimized for obtaining matched (a) gate capacitance, and transport parameters are optimized for (b) linear, (c) saturation transfer characteristics, and (d) output characteristics.

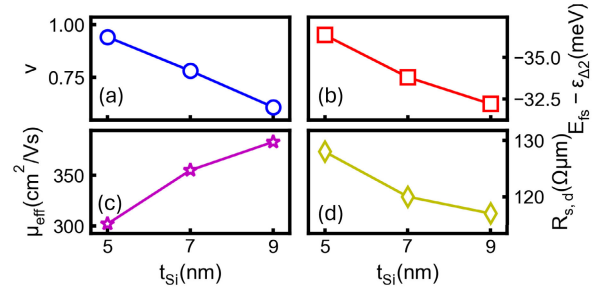


Fig. 7. Optimized physical parameters in the MVS model (a) ν , (b) $E_{fs}-\epsilon_{\Delta 2}$, (c) μ_{eff} , and (d) $R_{s,d}$ for varying t_{Si} . The trends in the predicted parameters are in agreement with the underlying device physics.

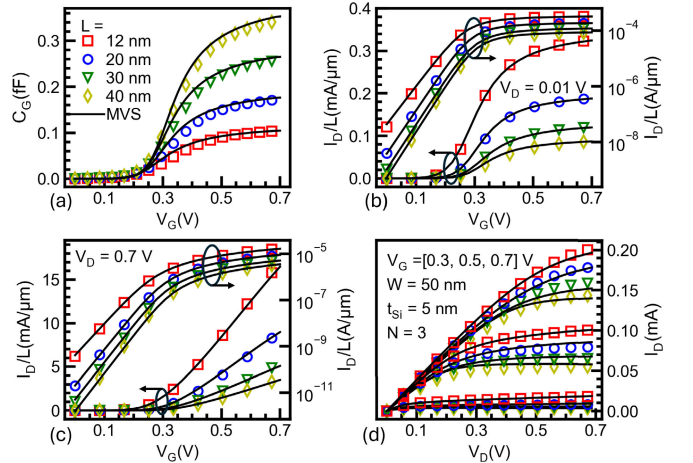


Fig. 8. Simulated and modeled results for NsFET across different values of L . (a) Gate capacitance, (b) linear, (c) saturation transfer characteristics, and (d) output characteristics. The accurate match in the simulated and modeled characteristics verifies the optimal fitting of the MVS model parameters.

agreement between the model and simulation data ensures global fitting of these parameters. Moreover, the linear and saturation transfer characteristics are aligned with TCAD

TABLE III
COMPARISON OF THE PROPOSED PARAMETER EXTRACTION STRATEGIES WITH THE LITERATURE

Method	Training Set Size	Model Size/Complexity	Applicable Parameter Range	Parameter/Bias Flexibility	Applicable Device	Applicable Model	Parameters Extracted
DL [2]	5×10^4	5.95×10^5 trainable parameters	Within training domain	No/No	10 nm FinFET	BSIM CMG	4 (C-V), 8 (I-V)
DL [3]	3×10^5	8.77×10^7 trainable parameters	Within training domain	No/No	14 nm FinFET	BSIM CMG	16 (I-V)
DL [4]	1.2×10^5	2.4×10^6 trainable parameters	Within training domain	No/No	HEMT	ASM HEMT	10 (I-V)
DL [5]	1×10^5	multiple models, 100 neurons each	Within training domain	No/Yes	14 nm FinFET	BSIM CMG	6 (C-V), 12 (I-V)
This work	0	Same as Compact Model	Entire parameter space	Yes/Yes	Demonstrated for ET-SOI, NsFET, 2DFET	Any, demonstrated MVS, BSIM CMG	9 MVS, 15 BSIM CMG

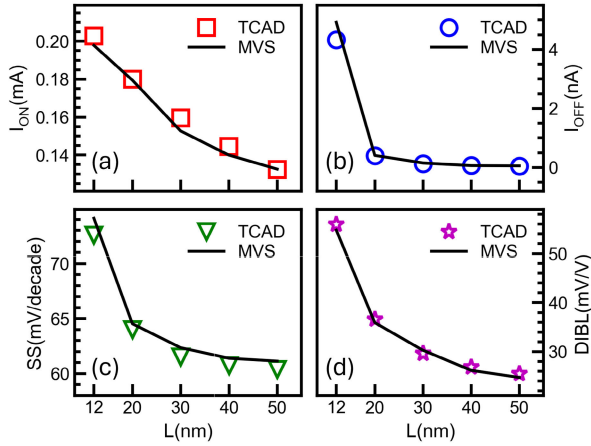


Fig. 9. Variation of (a) ON current (I_{ON}), (b) OFF current (I_{OFF}), (c) subthreshold swing (SS), and (d) DIBL across L in NsFETs for the MVS model and TCAD. The extracted model card is accurate and is able to capture the exact trends of the figures of merit.

data for the calibrated μ_{eff} , $E_{fs}-\epsilon_{\Delta 2}$, $R_{s,d}$, δ , n_d , and ξ , as illustrated in Fig. 8(b) and (c), respectively. In addition, the optimized value of β guarantees the fidelity of the modeled output characteristics in the linear-to-saturation transition region [Fig. 8(d)]. Because of the objective function O_2 (6), the slope and endpoint currents are also accurately modeled. This validation is further confirmed in Fig. 9, which exhibits strong agreement in key performance metrics, such as ON-current (I_{ON}), OFF-current (I_{OFF}), subthreshold swing (SS), and drain-induced barrier lowering (DIBL) between the model and the simulated data points across varying L . The collective results from Figs. 6 to 9 underscore the successful optimization of parameters to achieve an excellent model fit across a range of NsFET devices, from thick to thin and long to short. Thus, a complete calibrated model card for NsFETs can be efficiently prepared using multistage sequential BO within minutes. Furthermore, to showcase the adaptability of the parameter extraction approach, we have also calibrated model parameters for 2-D short channel MoS₂ FET (Fig. 10) [16]. The device characteristics were obtained from ab initio quantum-transport simulations. Employing the same approach outlined in Fig. 3 and Algorithm 1, we extracted model parameters for the 2DFET. The results depicted in Fig. 10 exhibit outstanding agreement with the simulated characteristics. It is noteworthy that even in the absence of output

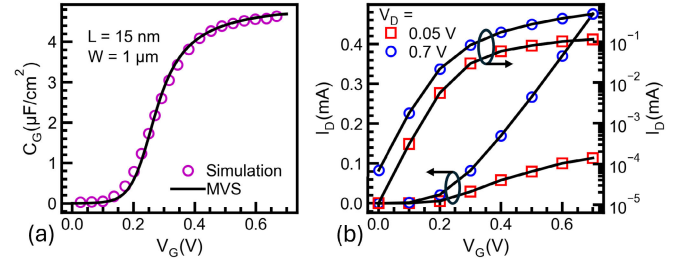


Fig. 10. (a) Gate capacitance for MoS₂ FET modeled with MVS using the proposed parameter extraction strategy. (b) Transfer characteristics of 2DFET. The model is well calibrated for the 2DFET simulation data.

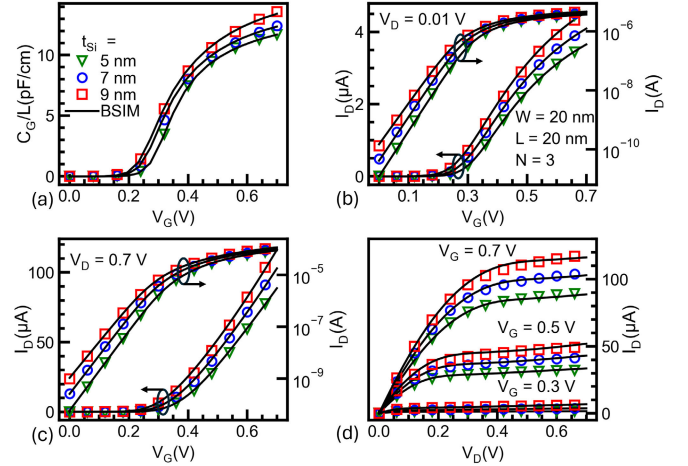


Fig. 11. Calibrated (a) gate capacitance, (b) linear transfer characteristics, (c) saturation transfer characteristics, and (d) output characteristics using BSIM CMG compact model for NsFET device for varying sheet thickness (t_{si}).

characteristics, the parameters β and ξ are optimized from the transfer characteristics in the saturation region. This versatility in adjusting the optimization of parameters according to the available simulation or experimental data renders the approach highly adaptable for predictive analysis of diverse devices.

To demonstrate the versatility of the parameter extraction strategy, BSIM CMG compact model parameters listed in Table II are calibrated for NsFETs with varying sheet thickness, using the proposed parameter extraction strategy. This is shown in Fig. 11.

Fig. 12(a) illustrates the objective function across the number of trials for various BO trajectories. All trajectories

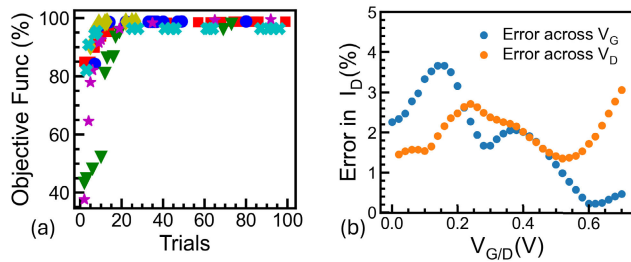


Fig. 12. (a) Objective function across the number of BO iterations. (b) Average relative error in modeling current-voltage characteristics for NsFETs. Sequential approach with adaptive sampling and domain reduction efficiently maximize the objective function in a few number of trials, resulting in accurate parameters.

effectively maximize the objective function, demonstrating a significant reduction in mismatch error [Fig. 12(b)] between the model and experimental data within just a few trials. This optimization efficiency can be attributed to the sequential strategy, adaptive sampling, and successive domain reduction. On a Ryzen 5 4600 H laptop CPU, each BO iteration in BSIM CMG takes 1–2 s, with the optimization of one sequence requiring 70–90 s. In contrast, for MVS, each iteration takes only 0.2–0.3 s, and optimizing one sequence takes 10–15 s.

Table III provides a summary of the advantages offered by the proposed approach of parameter extraction using BO over the DL-based approaches documented in the literature [2], [3], [4], [5]. Note that, DL methods entail significant training costs and suffer from rigidity in the model. These models are characterized by complexity, with numerous nodes and hidden layers, often comprising tens or hundreds of thousands of trainable parameters. In contrast, the approach presented in this work maintains practical model complexity similar to that of the compact model, since no additional models are trained. Furthermore, DL models require substantial complexity adjustments to accommodate electrical characteristics without structured bias variation. Moreover, retraining of the DL model is necessary whenever additional parameters need to be included or excluded in the parameter extraction scheme. The proposed approach effectively addresses these drawbacks, as it requires no training and offers flexibility at every stage of the parameter extraction process. This flexibility enables predictive analysis of emerging devices using decade-old models, thus enhancing versatility and practicality.

IV. CONCLUSION

In summary, we proposed a flexible and training-free approach to extract the compact model parameters efficiently using BO. Our methodology was demonstrated on the MVS and BSIM CMG model, showcasing its applicability and effectiveness. By employing simple yet accurate objective functions, we ensured the extraction of optimal model parameters. The sequential optimization process, coupled with adaptive sampling and successive domain reduction, proved instrumental in achieving parameter optimization within a few iterations. Extensive validation across ETSOI, NsFETs, and

MoS₂-based 2DFETs affirmed the robustness and versatility of our parameter extraction methodology. The sequential BO strategy offers an intuitive alternative to manual calibration. However, unlike manual methods, our approach enables the preparation of a complete calibrated model within minutes because of the efficiency of the proposed algorithm.

REFERENCES

- [1] G. Pahwa, A. Pampori, C. K. Dabhi, and D. Rajasekharan, “BSIMCMG 112.0.0beta0 4 multi-gate MOSFET compact model, technical manual,” Dept. Elect. Eng. Comput. Sci., Univ. California, Berkeley, Berkeley, CA, USA, Tech. Rep. 112.0.0beta0_4, 2024.
- [2] M. Kao, F. Chavez, S. Khandelwal, and C. Hu, “Deep learning-based BSIM-CMG parameter extraction for 10-nm FinFET,” *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4765–4768, Aug. 2022.
- [3] F. Chavez, C.-T. Tung, M.-Y. Kao, C. Hu, J.-H. Chen, and S. Khandelwal, “Deep learning-based I-V global parameter extraction for BSIM-CMG,” *Solid-State Electron.*, vol. 209, Nov. 2023, Art. no. 108766. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S003811012300179X>
- [4] F. Chavez, D. T. Davis, N. C. Miller, and S. Khandelwal, “Deep learning-based ASM-HEMT I-V parameter extraction,” *IEEE Electron Device Lett.*, vol. 43, no. 10, pp. 1633–1636, Oct. 2022.
- [5] A. Ashai, A. Jadhav, A. K. Behera, S. Roy, A. Dasgupta, and B. Sarkar, “Deep learning-based fast BSIM-CMG parameter extraction for general input dataset,” *IEEE Trans. Electron Devices*, vol. 70, no. 7, pp. 3437–3441, Jul. 2023.
- [6] Y. Li, “An automatic parameter extraction technique for advanced CMOS device modeling using genetic algorithm,” *Microelectron. Eng.*, vol. 84, no. 2, pp. 260–272, Feb. 2007. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0167931706003078>
- [7] M. Pelikan, D. E. Goldberg, and E. Cantú-Paz, “BOA: The Bayesian optimization algorithm,” in *Proc. 1st Annu. Conf. Genet. Evol. Comput. Conf. (GECCO)*, vol. 1. San Francisco, CA, USA: Morgan Kaufmann Publishers, 1999, pp. 525–532.
- [8] S. Rakheja, M. S. Lundstrom, and D. A. Antoniadis, “An improved virtual-source-based transport model for quasi-ballistic transistors—Part I: Capturing effects of carrier degeneracy, drain-bias dependence of gate capacitance, and nonlinear channel-access resistance,” *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2786–2793, Sep. 2015.
- [9] S. Rakheja, M. S. Lundstrom, and D. A. Antoniadis, “An improved virtual-source-based transport model for quasi-ballistic transistors—Part II: Experimental verification,” *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2794–2801, Sep. 2015.
- [10] A. Singh, M. D. Ganeriwala, R. Kaur, and N. R. Mohapatra, “A simplified approach to include confinement induced band structure changes into the NsFET compact model,” in *Proc. IEEE Int. Conf. Emerg. Electron. (ICEE)*, Dec. 2022, pp. 1–5.
- [11] Y. Liu, N. Neophytou, T. Low, G. Klimeck, and M. S. Lundstrom, “A tight-binding study of the ballistic injection velocity for ultrathin-body SOI MOSFETs,” *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 866–871, Mar. 2008.
- [12] F. Nogueira. (2014). *Bayesian Optimization: Open Source Constrained Global Optimization Tool for Python*. [Online]. Available: <https://github.com/bayesian-optimization/BayesianOptimization>
- [13] A. Majumdar and D. A. Antoniadis, “Analysis of carrier transport in short-channel MOSFETs,” *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 351–358, Feb. 2014.
- [14] R. Kaur and N. R. Mohapatra, “Comprehensive analysis of sheet thickness scaling on the performance of nanosheet nFETs,” *IEEE Trans. Electron Devices*, vol. 71, no. 5, pp. 2856–2862, May 2024.
- [15] S. Mochizuki et al., “Evaluation of (110) versus (001) channel orientation for improved nFET/pFET device performance trade-off in gate-all-around nanosheet technology,” in *IEDM Tech. Dig.*, vol. 26, Dec. 2023, pp. 1–4.
- [16] O. Maheshwari, J. Cao, Y. Lee, M. Luisier, and T. Agarwal, “Radio frequency performance of high mobility 2D monolayer Au₂S-based transistors,” in *Proc. 7th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Mar. 2023, pp. 1–3.