An Analytical Model for the Effective Drive Current in CMOS Circuits

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***Abstract*— Inverter delay is often evaluated as CV_{dd}/I_{eff}, where C is the load capacitance, V_{dd} is the supply voltage, and I_{eff} is the effective drive current derived by approximating the inverter switching trajectory with a linear model. The I_{eff} model utilizes high and low drain currents conventionally measured in wafer acceptance tests and does not require extraction of any parameters. Ease of use combined with reasonable accuracy (∼15%) is the main reason for wide application of CV_{dd}/I_{eff} delay metrics. However, CV_{dd}/I_{eff} expression produces large errors when applied to another two important basic circuits: nand and nor. This is because nand and nor circuits contain transistor series connections not accounted for in the inverter model. In this paper, an analytical solution for the transistor series connection influence on the discharge/charge operation in nand/nor circuits is provided. The model for nand/nor effective drive current (denoted as I_{stack}) developed in this paper maintains simplicity of the original I_{eff} expression. It requires only one additional measurement of the linear current. Model accuracy was assessed by comparing to extensive SPICE delay simulations of nand and nor circuits designed using state-of-the-art MOS technologies. Comparison results show that CV_{dd}/I_{stack} equation provides ∼15% accuracy for nand/nor circuits in line with CV_{dd}/I_{eff} accuracy for inverter. In an era of emphasis on low-power design, the developed model presents convenient means of exploring design space when optimizing circuit supply voltage for low-power operation.**

***Index Terms*— CMOS, delay, effective drive current, low-power design, NAND, NOR.**

I. Introduction

FOR predicting CMOS circuit speed, a simple metrics based on device dc current is widely used. In this metrics, the circuit delay is expressed as CV_{dd}/I, where C is the load capacitance, V_{dd} is the supply voltage, and I is the transistor current of a CMOS logic circuit. An effective drive current I_{eff} [1], instead of I_{ON} or I_{dsat}, is used for specifying transistor charging and discharging capability that determines circuit speed. The I_{eff} definition is based on the accurate approximation of transistor behavior during inverter switching [1].

The reason for the widespread application of CV_{dd}/I_{eff} delay model is its ease of use: the model contains no fitting parameters and, except for the conventional current measurements, does not require elaborate procedures for parameter extraction. Nevertheless, the model provides reasonable accuracy ($<\sim$15%) to make it useful in device development and circuit design. In addition, I_{eff} definition is technology independent and is widely used in studies of technology fundamentals and for explaining advanced device concepts [2]–[4].

The I_{eff} expression is based on analysis of the switching trajectory of MOS transistors. It is developed by approximating the inverter switching trajectory using two current points

$$I_L = I_{ds}\left(V_{gs} = \frac{V_{dd}}{2}, V_{ds} = V_{dd}\right) \tag{1}$$

and

$$I_H = I_{ds}(V_{gs} = V_{dd}, V_{ds} = V_{dd}/2) \tag{2}$$

where I_L and I_H are the transistor low and high currents, I_{ds} is the transistor drain-to-source current, and V_{gs}, V_{ds}, and V_{dd} are the gate-to-source voltage, drain-to-source voltage, and power supply voltage, respectively. I_L = The effective drive current is expressed as [1]

$$I_{eff} = \frac{I_H + I_L}{2}. \tag{3}$$

Due to the simplicity of the effective drive current equation little effort is required for its calculation.

More accurate expression for the inverter effective drive current was developed in [5] using three current points to provide a better approximation for current switching trajectory. A four-point model to account for the special properties of nanoscale Si and carbon nanotube FETs was developed in [6]. With research effort continuing, in recent papers, the effective current methodology was extended to the area of pass-gate transistors in [7] and inverter-transmission gate structure in [8]. An effective current model for near-threshold CMOS circuits was presented in [9].

The effective drive current expression (3) produces larger errors for delay when applied to NAND and NOR circuits. In NAND/NOR circuits, discharge/charge current flows through the series connection of nMOS/pMOS transistors. Drain-to-source voltage for the switching transistor is lower than V_{dd} and changes during operation. Therefore, current flowing during NAND/NOR operation is lower than (3).

Critical paths of CMOS circuits typically comprise large numbers of NAND and NOR circuits. Accurate and easy-to-use effective drive current models for NAND/NOR logic gates

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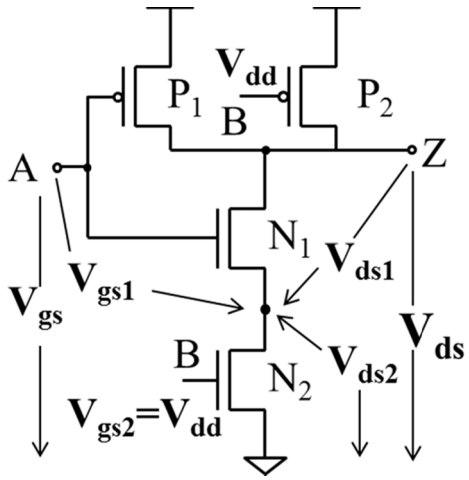

Fig. 1. NAND2 schematic and voltage notation.

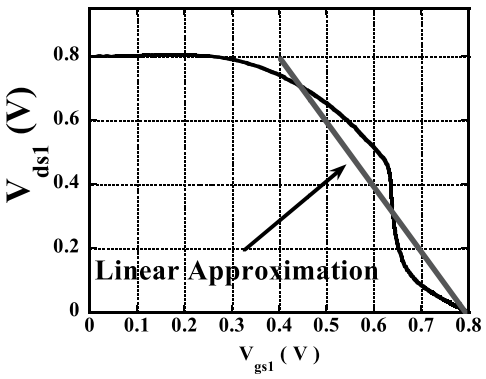

Fig. 2. N1 transistor V_{ds1} dependence on voltage V_{gs1} and its straight-line approximation.

are of great importance for circuit evaluation. An effective drive current model applicable to NAND and NOR circuits was developed in [10] using fitting of current approximation equation to SPICE simulation results. Extensive SPICE simulations are required to determine parameters of such model. In this paper, we provide a closed-form analytical solution for effective drive current in NAND and NOR circuits by extending approach of [1] to account for the effect of transistor series connection without the use of fitting parameters.

The issue of low-power design is critical in modern semiconductor technology. Reducing the supply voltage is the key to low-power operation [11]. However, reducing V_{dd} increases the circuit delay. The developed model provides convenient means of exploring circuit design space over a continuous range of supply voltages when optimizing circuit supply voltage for low-power operation.

This paper is organized as follows. In Section II, first, we derive the effective drive current model for NAND2 case. Then, we generalize the effective current equation for n-input NAND. Finally, we develop the effective current equation for n-input NOR. Section III presents verification results. The analytical model is compared to SPICE simulation results for circuits designed using state-of-the-art FinFET technology over a wide range of supply voltages and fan-outs.

II. Effective Drive Current Derivation for NAND/NOR Circuits

In this section, first, the discharge process in NAND gate is considered, and an analytical expression for the NAND fall delay is developed by analyzing the discharge current through the series connected nMOS transistors. Second, the charge process in NOR gate is considered, and an analytical expression for the NOR rise delay is obtained by analyzing the charge current through the series connected pMOS transistors.

NAND2 schematic and notation for voltages applied to its terminals are depicted in Fig. 1. Ring oscillator mode of operation as defined in [1] is assumed. V_{dd} is applied to the terminal B of the circuit. The input voltage at terminal A is swept from low to high, and output voltage changes from high to low. It is known that sweeping input voltage at B terminal or sweeping input voltages at both terminals simultaneously will produce shorter delays. We characterize circuit by its largest delay and, therefore, limit our discussion to the case shown in Fig. 1.

Delay time is defined as the time required for the output to reach 50% of its final output level when the input changes to 50% of its final input level. The delay time is expressed as

$$\tau = \int_{V_{dd}}^{V_{dd}/2} \frac{C dV_{ds}}{I_{ds}(V_{gs}, V_{ds})}, \quad \frac{V_{dd}}{2} \le V_{gs} \le V_{dd} \tag{4}$$

where C is a calculated load capacitance.

When input voltage at terminal A is swept from low to high, transistor N1 operates in the saturation region, while transistor N2 operates in the linear region. Since our goal is to derive closed-form and simple equation for I_{eff} we use a linear approximation for $I_{ds}(V_{gs1}$ and $V_{ds1})$ of the transistor N1

$$I_{ds} = I_{dsat} + g_m(V_{gs1} - V_{dd}) + g_{ds}(V_{ds1} - V_{dd}) \tag{5}$$

where I_{dsat} is the transistor saturation current, g_m denotes transconductance and g_{ds} denotes conductance. Any higher order approximation produces models intractable analytically.

Since transistor N2 operates in the linear region we can describe current $I_{ds}(V_{gs2}$ and $V_{ds2})$ for transistor N2 as

$$I_{ds} = \frac{I_{dlin}}{V_{dlin}} V_{ds2} \tag{6}$$

where I_{dlin} is the linear current measured at $V_{gs} = V_{dd}$, $V_{ds} = V_{dlin}$, and V_{dlin} is the low voltage of several dozen millivolts.

Next, in Fig. 2 dependence of the source-to-drain voltage V_{ds1} on the input voltage V_{gs1} is shown for transistor N1. To achieve analytical solution, this dependence is approximated by a straight line depicted in Fig. 2

$$V_{ds1} = \frac{3}{2} V_{dd} - V_{gs1}. \tag{7}$$

This approximation was selected since only the linear function can provide a closed-form model for the effective drive current. The validity of this approximation is investigated in Section III.

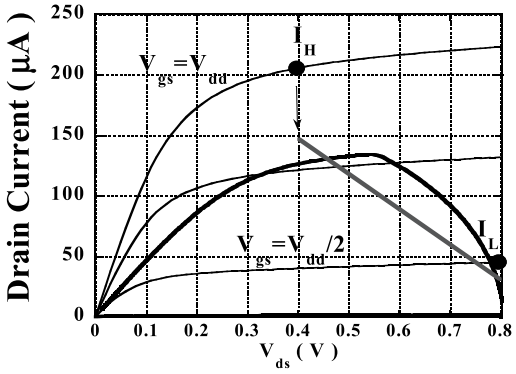

Fig. 3. Switching trajectory of NAND2 circuit as a function of the output voltage and its straight-line approximation. The approximation current is reduced compared to the inverter case.

In addition to (5)–(7), note that the circuit output voltage V_{ds} is a sum of V_{ds1} and V_{ds2} voltages

$$V_{ds} = V_{ds1} + V_{ds2}. \tag{8}$$

From (8), V_{ds1} is expressed as a function of V_{ds} and V_{ds2}. This expression is then used in (7) and expression for V_{gs1} as a function of V_{ds} and V_{ds2} is obtained. Substituting these two expressions into (5) provides I_{ds} as a function of V_{ds} and V_{ds2}. Then, (6) is used to eliminate V_{ds2} and I_{ds} is expressed as a function of V_{ds} only

$$I_{ds} = \frac{1}{1 + \frac{(I_H - I_L)}{I_{dlin}} \frac{2V_{dlin}}{V_{dd}}} \times [I_{dsat} + (g_{ds} - g_m)V_{ds} + (0.5g_m - g_{ds})V_{dd}]. \tag{9}$$

For the inverter case discussed in [1], I_{ds} approximation is expressed as

$$I_{ds} = I_{dsat} + (g_{ds} - g_m)V_{ds} + (0.5g_m - g_{ds})V_{dd}. \tag{10}$$

Therefore, discharge current in NAND2 is reduced in comparison to inverter by

$$K = 1 + \frac{2(I_H - I_L)}{I_{dlin}\frac{V_{dd}}{V_{dlin}}} \tag{11}$$

where I_L and I_H are defined by (1) and (2), and I_{dlin} is the linear current measured at $V_{gs} = V_{dd}$, $V_{ds} = V_{dlin}$. Fig. 3 shows a switching trajectory of NAND2 circuit as a function of the output voltage and trajectory approximation by (9). The approximation current is reduced compared to the inverter case since the straight line no longer goes through I_L and I_H points.

The delay time (4) now can be rewritten as

$$\tau = \int_{V_{dd}}^{V_{dd}/2} \frac{C dV_{ds}}{I_{ds}(V_{ds})}. \tag{12}$$

Performing integration of (12) delivers

$$\tau = \frac{CV_{dd}}{2} \cdot \frac{1 + \frac{I_H - I_L}{I_{dlin}} \cdot \frac{2V_{dlin}}{V_{dd}}}{I_H - I_L} \cdot \ln\left(\frac{I_H}{I_L}\right). \tag{13}$$

Substituting

$$\ln\left(\frac{I_H}{I_L}\right) = \frac{2(I_H - I_L)}{I_H + I_L} \tag{14}$$

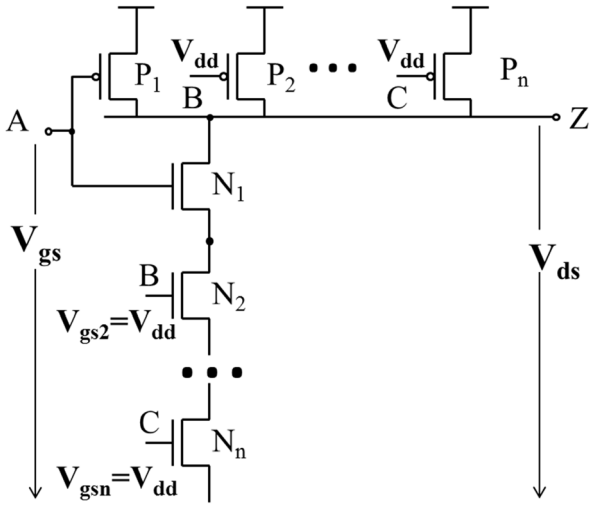

Fig. 4. n-input NAND schematic.

into (13) expresses delay time as a function of I_{eff}

$$\tau = \frac{CV_{dd}}{2} \cdot \frac{1 + \frac{I_H - I_L}{I_{dlin}} \cdot \frac{2V_{dlin}}{V_{dd}}}{I_{eff}}. \tag{15}$$

To distinguish with inverter case and in line with definition in [10], the effective drive current flowing through the series connection of transistors is denoted as I_{stack} or the stack current

$$I_{stack} = \frac{I_{eff}}{1 + \frac{I_H - I_L}{I_{dlin}} \cdot \frac{2V_{dlin}}{V_{dd}}}. \tag{16}$$

Equation (16) can be rewritten as

$$I_{stack} = I_{eff}/K \tag{17}$$

where the coefficient K is defined by (11). Then, NAND2 delay is expressed as

$$\tau = \frac{CV_{dd}}{2I_{stack}}. \tag{18}$$

Next, we discuss an n-input NAND circuit shown in Fig. 4. The same as in the two-input NAND analysis, input signal at terminal A changes from low to high and high voltage is applied to all other inputs. To evaluate delay time, we replace n-input NAND circuit with two-input NAND circuit shown in Fig. 5.

Assuming that source–drain voltage difference for individual transistors $N_2, N_3, \ldots, N_n$ in Fig. 4 is small, we evaluate source–drain voltage of transistor N2 in Fig. 5 as $(n-1)V_{ds2}$. The analysis described previously for two-input NAND can be applied to the circuit in Fig. 5. It shows that the stack current can be again expressed by (17) where K now is defined as

$$K = 1 + \frac{2(n-1)(I_H - I_L)}{I_{dlin}\frac{V_{dd}}{V_{dlin}}} \tag{19}$$

and n is the number of NAND circuit inputs.

Note that the above-mentioned derivation can also be employed when the input voltage of N2 in Fig. 1 is swept and V_{DD} is applied to the input terminal of N1. With the proper

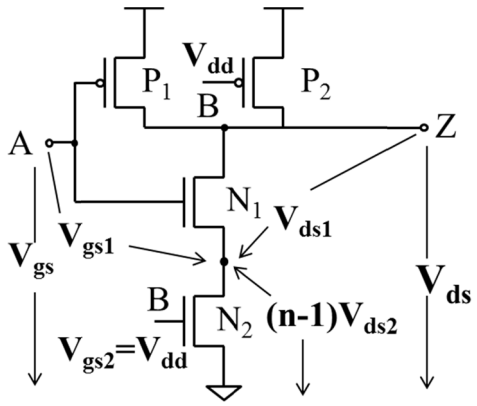

Fig. 5. NAND2 schematic for analysis of the n-input circuit operation.

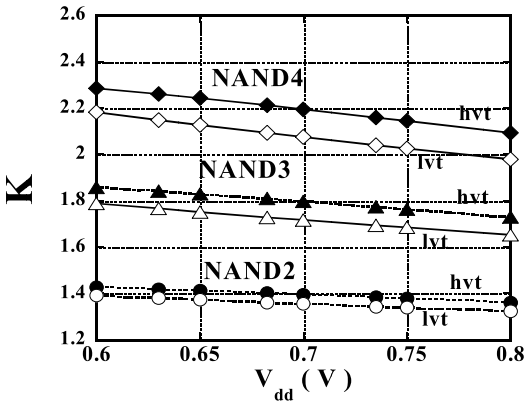

Fig. 6. K-values for calculating fall delays of NAND2, NAND3, and NAND4.

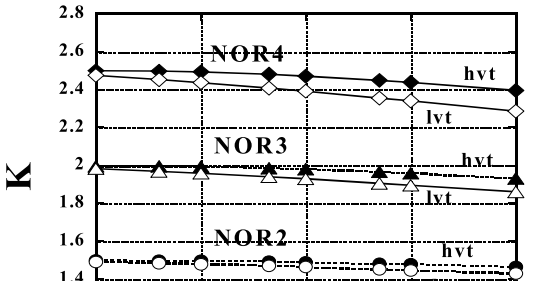

Fig. 7. K-values for calculating rise delays of NOR2, NOR3, and NOR4 circuits.

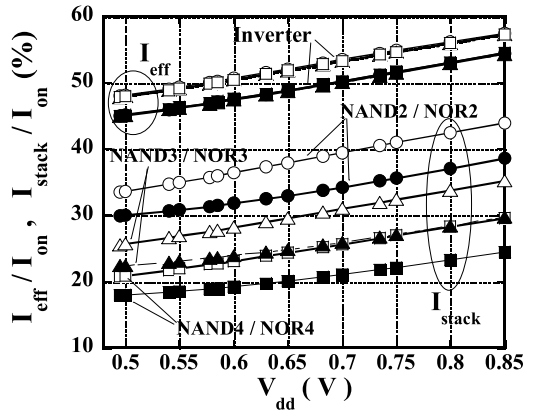

Fig. 8. Dependence of I_{eff}/I_{ON} and I_{stack}/I_{ON} on V_{dd}. Open symbols: nMOS. Filled symbols: pMOS.

change of notation, (5) will describe operation of N2 and (6) operation of N1. The expression for I_{stack} is

$$I_{stack} = \frac{I_{H\,N2} + I_{LN2}}{2 + \frac{4(n-1)(I_{H\,N2} - I_{L\,N2})}{I_{dlin\,N2}\frac{V_{dd}}{V_{dlin}}}} \tag{20}$$

where $I_{H\,N2}$, $I_{L\,N2}$, and I_{dlinN2} are the high, low, and linear currents for N2.

Next, the low–high transition in NOR gate is discussed. Similar to NAND, delay of NOR is defined by (4). During low–high transition, the charge current flows through series-connected pMOS transistors. The analysis (5)–(16) can be repeated for these pMOSFETs. Such analysis shows that the stack current of n-input NOR circuit is again described by (17) and (19) where currents and voltages refer now to pMOSFETs. Rise time of n-input NOR circuit is again expressed by (18).

K-values in (17) show how much discharge current in n-input NAND circuit or charge current in n-input NOR circuit is reduced due to transistor series connection in comparison to the inverter case. As an example, K-values were calculated as a function of V_{dd} for 7-nm FinFET technology. In Fig. 6, typical K-values for NAND and in Fig. 7 for NOR circuits are shown. Results for lower V_{th} transistors and higher V_{th} transistors are demonstrated. K-values increase with increasing of NAND/NOR number of inputs and, therefore, the stack current rapidly decreases. For NAND2 circuit K is around 1.4, for NAND3 K is around 1.8, and for NAND4 K is around 2.2. FOR NOR2 circuit K is around 1.5, for NOR3 K is around 2, and for NOR4 K is around 2.5. In addition, Figs. 6 and 7 show dependence of K-values on V_{dd} and transistor threshold voltage. Figs. 6 and 7 demonstrate that dependence of K on V_{dd} and V_{th} is not large. Dependence of I_{eff}/I_{ON} and I_{stack}/I_{ON} on V_{dd} is provided in Fig. 8. The ratio of I_{stack}/I_{ON} for NAND/NOR circuits is smaller than that of the ratio of I_{eff}/I_{ON} for inverters and decreases with increasing the input number.

III. Model Verification

In this section, the stack current model is compared to SPICE simulations and it is demonstrated that (17)–(19) provide reasonably accurate approximations of delays in comparison to SPICE results. NAND and NOR circuits designed using 7-nm FinFET technology were simulated and circuit delays were calculated as a function of the supply voltage V_{dd} for fan-out = 3. The circuit used in SPICE simulations consists of input pulse generator, NAND/NOR, and load circuits.

In Fig. 9, NAND2 fall and NOR2 rise delays simulated by means of SPICE and their approximations calculated using transistor I_{eff} or I_{stack} are shown. Since I_{eff} model does not account for the effect of the nMOS transistor series connection in NAND discharge process, fall delays evaluated using I_{eff} are significantly smaller than SPICE results. In a similar way, because I_{eff} model reflects inverter operation

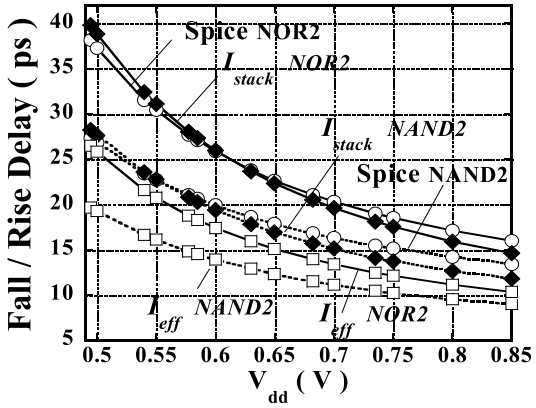

Fig. 9. Comparison of I_{stack}, I_{eff}-based models to SPICE simulation results for NAND2 fall and NOR2 rise delays.

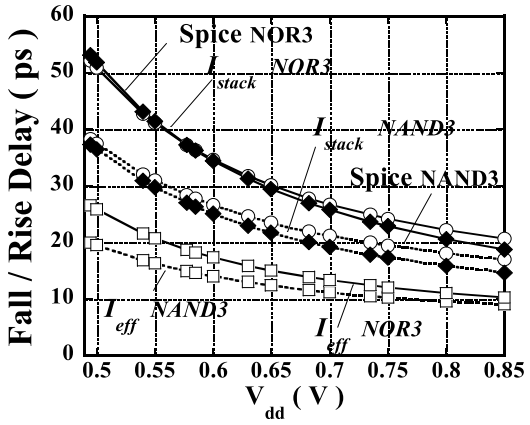

Fig. 11. Comparison of I_{stack}, I_{eff}-based models to SPICE simulation results for NAND3 fall and NOR3 rise delays.

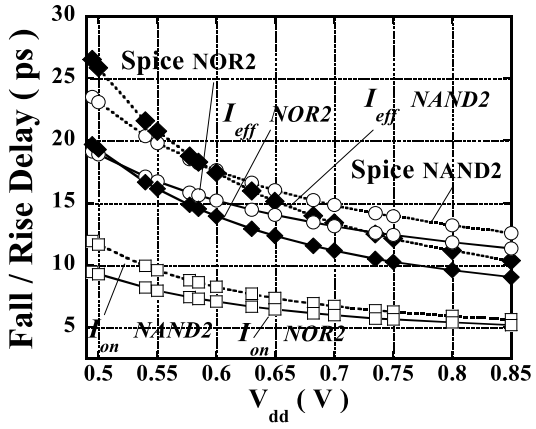

Fig. 10. Comparison of I_{eff}, I_{ON}-based models to SPICE simulation results for NAND2 rise and NOR2 fall delays.

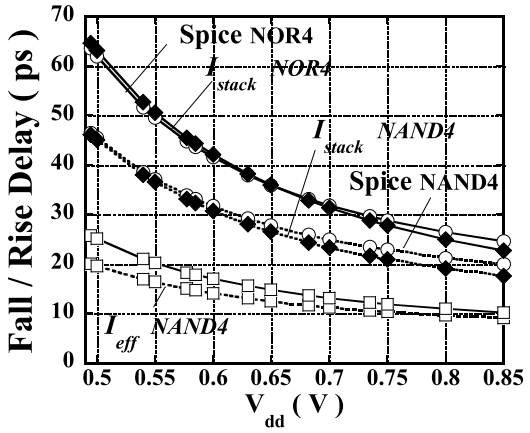

Fig. 12. Comparison of I_{stack}, I_{eff}-based models to SPICE simulation results for NAND4 fall and NOR4 rise delays.

only and does not account for the effect of the pMOS transistor series connection in the NOR charge process, rise delays evaluated using I_{eff} are significantly smaller than SPICE results. When I_{stack} values are used good agreement with SPICE is achieved in a wide range of supply voltages. In addition, in Fig. 10, comparison of NAND2 rise and NOR2 fall delays to SPICE simulation results is provided. Since NAND/NOR circuits do not contain pMOS/nMOS transistors connected in series, pMOS/nMOS I_{eff}-based models accurately describe NAND charge/NOR discharge processes and provide good agreement with SPICE simulation. Fig. 10 also demonstrates large improvement over I_{ON} approximation. It is possible to say that I_{stack} model provides improvement over I_{eff} in approximating NAND fall/NOR rise delays similar to improvement over I_{ON} achieved by introduction of I_{eff} for inverters.

In Fig. 11, NAND3 fall and NOR3 rise delays simulated by means of SPICE, and their I_{eff} or I_{stack} approximations are shown. Comparison results are similar to the two-input case and demonstrate good accuracy of the I_{stack} model.

Next, in Fig. 12, accuracy of the I_{stack} approximations for NAND4 fall and NOR4 rise delays is examined. With the increasing number of inputs, NAND fall/NOR rise delays become larger and I_{stack} model correctly accounts for this effect.

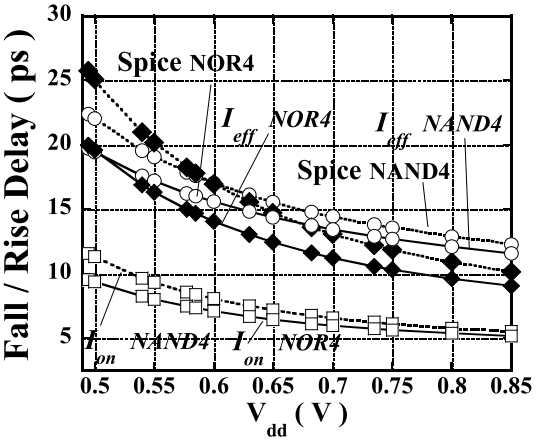

Fig. 13. Comparison of I_{stack}, I_{eff}-based models to SPICE simulation results for NAND4 rise and NOR4 fall delays.

In Fig. 13, comparison of NAND4 rise and NOR4 fall delays is provided. In contrast to NAND4 fall/NOR4 rise delay increase, NAND4 rise/NOR4 fall delays exhibit little change compared to NAND2/NOR2 results shown in Fig. 10 and can be approximated well using I_{eff} model.

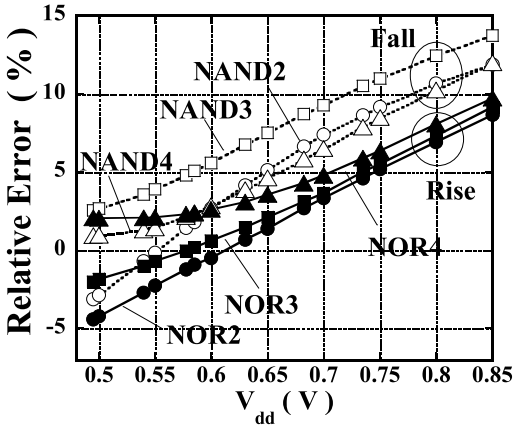

Fig. 14. Relative error of NANDfall/NOR rise delay calculation using I_{stack} in comparison to SPICE simulation results for circuits with fan-out = 3 load as a function of V_{dd}.

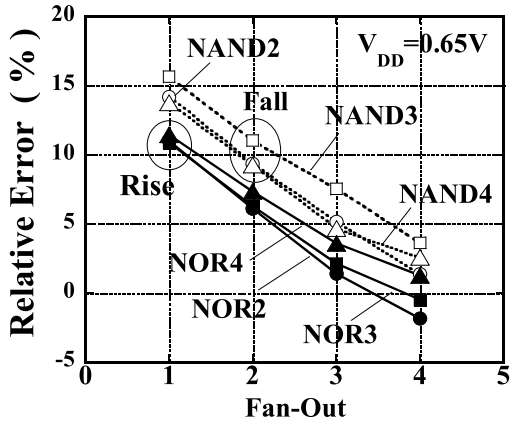

Fig. 15. Relative error of NAND fall/NOR rise delay calculation using I_{stack} in comparison to SPICE simulation results at $V_{dd} = 0.65$ V as a function of fan-out.

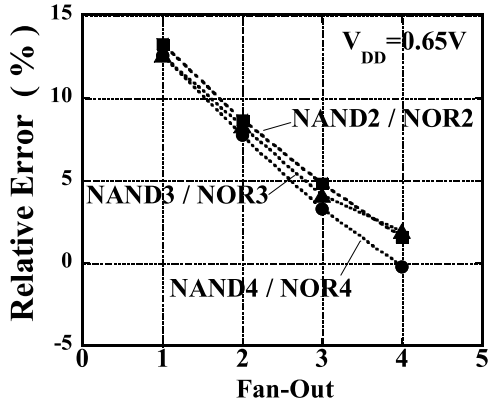

Fig. 16. Relative error of NAND/NOR circuit delay calculation using I_{stack} in comparison to SPICE simulation results at $V_{dd} = 0.65$ V as a function of fan-out.

The relative error of I_{stack} approximation for NAND fall/NOR rise delays is shown in Fig. 14 as a function of number of inputs and V_{dd}. Relative error increases with increasing V_{dd} but does not exceed 15%. This accuracy is similar to the accuracy of inverter delay approximation by means of I_{eff} [1]. Relative error increases with increasing V_{DD} due to the larger error of the linear approximation (5) for a larger voltage range. In Fig. 15, the relative error of I_{stack} approximation for NAND fall/NOR rise delays is shown as a function of fan-out and number of inputs for $V_{dd} = 0.65$ V. For important cases of fan-out = 3 and fan-out = 4, the relative error is below 10%. Fig. 16 demonstrates good accuracy for delay approximations of NAND/NOR circuits.

IV. Conclusion

The effective drive current I_{stack} model developed in this paper provides a simple and easy-to-use method for fast prediction of NAND/NOR circuit delays with reasonable accuracy (relative error $<\sim$15%) in a wide range of supply voltages and fan-outs. The model does not require complicated parameter extraction procedures and uses transistor currents which are routinely measured at the wafer acceptance tests during circuit fabrication. The model can also be used for process-voltage-temperature variability analysis.

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