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An Analytical Model for the CMOS Inverter

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***Abstract*— A new analytical model for the CMOS inverter is introduced. This model results by solving analytically the differential equation which describes the inverter operation. It uses new simplified transistor current expressions which are developed taking into account the nanoscale effects and also considering temperature as a parameter. Expressions for the output voltage are derived, which are then used for capturing the output and supply currents, making the model compatible with CCS technology requirements. The proposed model is parametric according to the input signal slew, output load, transistor widths, supply voltage, temperature and process parameters. It presents an average error less than 3% for the typical case.**

Keywords—Inverter modeling; transistor current model; timing model; output current model; simulation, CCS technology

I. INTRODUCTION

A current based modeling approach has been used by the industry lately for the timing and power analysis of integrated circuits [1-3]. This approach has proven very effective in modeling the nano-scale effects of current technologies. The Composite Current Source (CCS) model for timing, power and noise, enables efficient characterization for cell library creators in the sense of .lib files. Based on circuit simulation, the CCS modeling approach can provide an accuracy of 2% when compared to BSIM [2]. However, it needs large files for keeping pre-characterized data of the library cells. Furthermore, the pre-characterization phase is a time consuming procedure resulting from the fact that it is based on real circuit simulations. The use of .lib files for timing analysis and power estimation imposes time-consuming accesses, while an additional step for the simulation compiler is needed in order to transform .lib data to the circuit characteristics (e.g. propagation delay, output slew, power consumption). Also, extrapolation is needed in case the studied circuit configuration does not fall upon the configurations described by the .lib files.

Instead of the simulative approach, many analytical models have been proposed to describe the propagation delay and the power consumption of the CMOS inverter in closed mathematical forms [4-6]. These models preserve a parametric view of the behavior of the inverter and can be used for very fast characterization, compared to SPICE simulations, of any configuration, that spans to a reasonable range of design parameter values. Furthermore, analytical expressions for the circuit characteristics facilitate the development of predictive models regarding variability effects, an important issue in nano-scale technologies.

In this paper, a new model for the propagation delay and current consumption for bulk CMOS gates is proposed, which takes into account most of the nano-scale effects. This model is developed for the CMOS inverter and is fully parametric to the input slew, the output load, the transistor sizes, the supply voltage, temperature and process parameters. According to the authors' knowledge, this is the first effort that an analytical model has been developed considering all these parameters. The following approach is based on solving the differential equation which describes the inverter operation. According to [7] the study of any logic gate can be reduced to the study of an equivalent inverter, thus increasing the applicability of the proposed model.

A simplified but still accurate transistor drain current model, for both the strong and the weak inversion regime, is derived first, which takes into account nano-scale effects, such as carrier velocity saturation, channel length modulation, the DIBL effect, the narrow width effect and the impact of temperature on the silicon energy band gap, intrinsic carrier density and mobility. The drain current in the sub-threshold region is also taken into account. All the drain current expressions are described as a function of temperature, which plays a significant role in the performance of the circuits. A 45 nm PTM technology is employed for the validation of the proposed transistor current model.

The proposed inverter model is about a hundred times faster in terms of calculation speed compared to HSPICE simulations, while it eliminates the need of storing large library files. The average error in the propagation delay for the nominal case (V_{DD}=1V, T=25^{o}C) is less than 3%, for input rise and fall cases. The proposed model preserves its accuracy with an average error of less than 5% when different values of the supply voltage are applied. Furthermore, it provides the supply and output current values needed in CCS library files to exploit the current EDA technology for timing and power analysis.

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II. Transistor Current Model

The transistor drain current model presented in [6] is used as the basis for our proposal, since it is considered appropriate for analytical approaches. However, in the model of [6] the threshold voltage V_T and DIBL factor n_{DIBL} are fitting parameters. To increase the compactness of the inverter model, it is modified in order to include analytical expressions for V_T and n_{DIBL} Also, the modified drain current model is extended to include the temperature dependence of the device parameters. Furthermore, in our model the subthreshold current is also taken into consideration.

The threshold voltage expression of an n-channel MOSFET is given by [8]

$$V_{Tlong} = V_{fb} + 2\varphi_f + \frac{qN_A t_{dep}}{\varepsilon_{ox}/t_{ox}} \quad (1)$$

where V_{fb} is the metal-semiconductor work function difference, φ_f is the Fermi potential, N_A is the channel concentration, t_{ox} is the gate oxide thickness and t_{dep} is the maximum depletion depth allowed for the doping concentration N_A, given by the

$$t_{dep} = \sqrt{\frac{4\varepsilon_{Si}\varphi_f}{qN_A}} \quad (2)$$

In our analysis, we consider the charge density in the gate oxide to be negligible. By shrinking the device dimensions, the so called short channel effects (SCE) affect the transistor function and the parameters of the threshold voltage V_T, DIBL effect n_{DIBL} and the ideality factor n, are given by [9]

$$V_T = V_{T0} - n_{DIBL}V_{DS}$$

$$n_{DIBL} = 0.8\left(\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\right)\left(\frac{t_{ox}t_{dep}}{L^2}\right)\left[1+\left(\frac{x_j}{L}\right)^2\right] \quad (3)$$

$$n = 1 + n_{factor}\left(\frac{\varepsilon_{Si}t_{ox}}{t_{dep}\varepsilon_{oX}}\right) + \left(\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\right)\left(1+\frac{3t_{dep}}{4L}\right)\left(\frac{t_{ox}x_j}{L^2}\right)\sqrt{1+2V_{DS}}$$

where x_j is the source/drain junction depth and V_{T0} is given by

$$V_{T0} = V_{Tlong} - 0.64\left(\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\right)\left(\frac{t_{ox}t_{dep}}{L^2}\right)\left[1+\left(\frac{x_j}{L}\right)^2\right] \quad (4)$$

Finally, the modified expressions of the transistor current are:

$$I = \begin{cases} I_O\left(1-\frac{W_m}{W}\right)e^{\frac{V_{GS}-V_T}{n(kT/q)}}\left(1-e^{-\frac{V_{DS}}{kT/q}}\right), & V_{GS} < V_T \\ B\left(1-\frac{W_m}{W}\right)\left(\frac{V_{GS}-V_T}{V_{T0}}\right)^a \frac{V_{DS}}{V_{DSAT}}, & V_{DS} \le V_{DSAT} \\ B\left(1-\frac{W_m}{W}\right)\left(\frac{V_{GS}-V_T}{V_{T0}}\right)^a [1+\lambda(V_{DS}-V_{DSAT})], & V_{DS} > V_{DSAT} \end{cases} \quad (5)$$

where the first expression represents the subthreshold drain current, while the other two represent the drain current for below (linear) and above (saturation) V_{dsat} operation. W_m is a linear expression of W, to model the narrow width effect. The expressions for I_o, B and V_{dsat} are given by:

$$I_o = \left(\frac{W}{L}\right)\mu C_{ox}\left(\frac{nkT}{q}\right)^2$$

$$B = \left(\frac{W}{L}\right)\mu C_{ox}V_{T0}^2 \quad (6)$$

$$V_{DSAT} = K\left(\frac{V_{GS}-V_T}{V_{T0}}\right)^2$$

where the temperature dependence of the electron mobility, is expressed as

$$\mu \propto T^{-2.4} \quad (7)$$

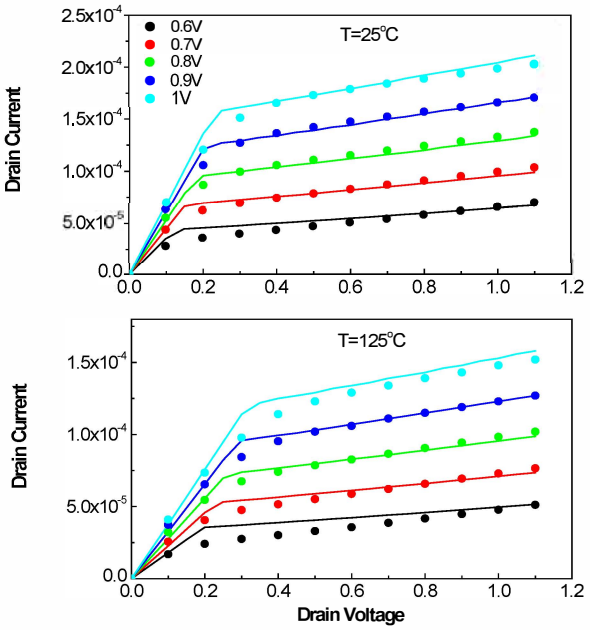

Fig. 1. Comparison of our modified model (lines) with simulation results (dots) for a device with W=200nm and for two different temperatures.

In Fig. 1, the comparison of the DC characteristics of our model with HSPICE results for the PTM 45nm technology [10] and for different temperature values are presented. The device is a bulk n-MOSFET with a 50 nm channel length and 200 nm channel width. For this case, W_m=172nm (in eq. (5)). The accuracy of the drain current model is validated by HSPICE simulation results.

The parameters used in this model, for width values ranging from 100nm to 400nm and temperatures from 0°C up to 125°C, are presented in Table I.

TABLE I: PARAMETER VALUES FOR DIFFERENT WIDTHS, W, AND TEMPERATURES, T

W=100-400nm	K	m	α	λ	n_{factor}
T=0°C	0.133	0.7	1.24	0.3	3
T=25°C	0.131		1.46		2.5
T=50°C	0.127		1.58		2
T=75°C	0.124		1.68		1.5
T=100°C	0.12		1.74		1
T=125°C	0.118		1.78		0.5

III. MODELING THE OPERATION OF THE INVERTER

The inverter structure to be analyzed is shown in Fig. 2. Parasitic capacitances are also shown. C_m is the coupling capacitance between input and output node, corresponding to the gate-to-drain capacitance of both transistors. C_{db} corresponds to the drain-to-bulk junction capacitance and presents a critical role in the accuracy of the model. C_{out} corresponds to the output load capacitance.

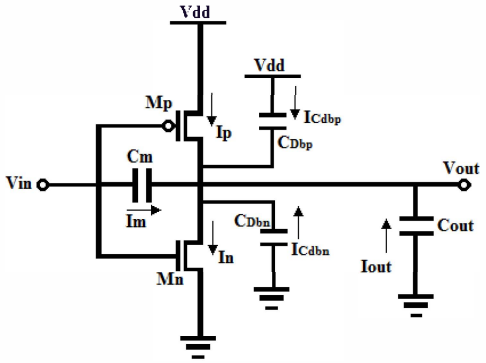

Fig.2. Studied Topology for the inverter

An analytical model that describes the output voltage waveform as well as the supply and output currents is created. To derive the model, the following differential equation needs to be solved. It resulted by applying the Kirchhoff's current law at the output node:

$$I_n + C_{dbn}\frac{dV_{out}}{dt} = I_p - C_{out}\frac{dV_{out}}{dt} + C_m\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) - C_{dbp}\frac{dV_{out}}{dt} \qquad (8)$$

where I_n, I_p are the transistors' currents. The equation is solved for both, rising and falling input ramp signals. A parametric slew is considered for the input signals. The appropriate average values are defined for parasitic capacitances, according to the transistor operation mode, as they resulted by HSPICE simulations. Parametric expressions for the output voltage are derived for every region of operation capturing the entire output transition of the inverter.

The differential equation is initially modified according to the appropriate expressions of eq. (5) for the NMOS and PMOS transistors currents with respect to the working operation mode. Then it is solved giving the output transition. The structure of the solution flow for a rising input ramp is given in Fig. 3. A similar flow for the falling input ramp exists. A simplified version of the model with less parameterization and without the extensions of output and supply currents has been presented with detail in [11]. In Fig. 3 the various operation regions and the corresponding transition conditions are presented. Since the proposed model has been developed for an industrial library with a wide range of parameter values, some adjustments compared to that of [11] where conducted in order to preserve the required accuracy.

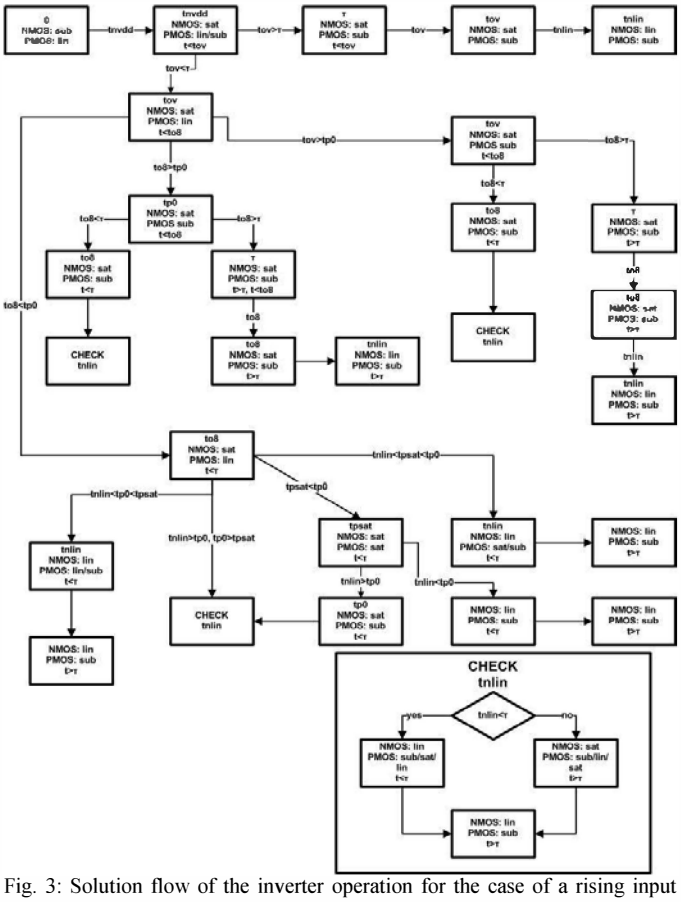

Fig. 3: Solution flow of the inverter operation for the case of a rising input ramp.

Special attention has been issued for the calculation of the output voltage in the overshooting/undershooting regions as well as the duration of these regions. As depicted in Fig. 5, 6 the overshooting/undershooting region corresponds to a significant fraction of the total transition time of the inverter. To simplify the analysis in these regions, the current of the short-circuiting transistor has been neglected since its drain-to-source voltage is almost zero.

First order Taylor approximations for both transistors' currents in the conducting mode has been used in the occasions where the differential equation couldn't be solved. A new region,

where both transistors are in saturation, has been included. Also, another region just after the overshooting/undershooting up to the time of 20% change in the output voltage has been included. In this region, the V_{DS} was considered constant and the solution of the differential equation was feasible using the approximation

$$B(V_{GS} - V_T)^a \rightarrow a_1 B V_{GS} - a_2 V_T \quad (9)$$

The coefficients a_1 and a_2 have been calculated to minimize the average transformation error. By this way a significant increase in the accuracy of the approximation of the output voltage expression derivative was achieved ensuring the accuracy of the following steps.

Finally, a parametric expression for the output voltage according to the input transition time, output load, transistor width, supply voltage and temperature has been derived. Using the expression of the output voltage, the expression of the output current in C_{out} is provided by $I_{out} = C_{out}\, dV_{out}/dt$. The current from the supply voltage can be calculated by

$$I_{Vdd} = I_P \pm C_{gsp}\frac{dV_{in}}{dt} - C_{dbp}\frac{dV_{out}}{dt} \quad (10)$$

where "+" or "-" are used for the case of falling or rising inputs, respectively. C_{gs} is the gate-to-source capacitance. In the case of a rising input the current though the transistor, I_P becomes comparable with that through the capacitances C_{gsp} and C_{dbp} as depicted in Fig. 4. In Fig. 4 the charge (integration of the current) that flows through the PMOS, Q_P, is compared to that through the capacitance C_{gsp}, Q_{cgsp}, and the junction capacitance C_{dbp}, Q_{cdbp}. It is clear that a more precise calculation method for the parasitic capacitances is required for an accurate estimation of the supply current I_{Vdd}. Therefore, parametric expressions for the parasitic capacitances have been defined in all the regions of operation shown in Fig. 3. In this way, the proposed model can become compatible to the CCS environment. Closed forms of the propagation delay and the output waveform slope are also provided.

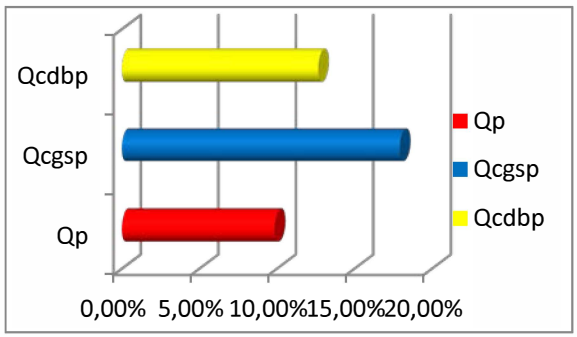

Fig. 4: Comparison of the portion of the charge through the transistor, C_{gsp} and C_{dbp} in relation to the charge stored in C_{out}

IV. EVALUATION OF THE MODEL - RESULTS

The proposed model is used for the characterization of the NangateOpenCellLibrary [12] for the 45nm PTM technology [10]. It is designed to satisfy all the corners defined in .lib files and shown in Table II. Also, in this Table the range of the parameters supply voltage, temperature and NMOS transistor width is shown. According to the library, $W_p = 1.5W_n$.

TABLE II. PARAMETER CORNERS AND RANGES

Input slew, τ *(ps)*	2.9, 12, 43, 102, 195, 325, 496
Load capacitance, C_{out} (fF)	0.37, 1.9, 3.8, 7.6, 15.1, 30.3, 60.6
NMOS transistor width, W_n *(nm),* (range)	90 - 400
Supply voltage, V_{DD} (V), (range)	0.7 - 1.25
Temperature, T (°C), (range)	0 - 125

In Fig. 5 the output voltage waveform for a rising input and V_{DD}=1V, T=25°C, τ=43ns, C_{out}= 3f and W_n=150nm, is shown. In Fig. 6 the output voltage waveform for a falling input and the same configuration is shown. The corresponding HSPICE simulation results are also shown in dotted lines. In both cases the accuracy of the proposed model is obvious.

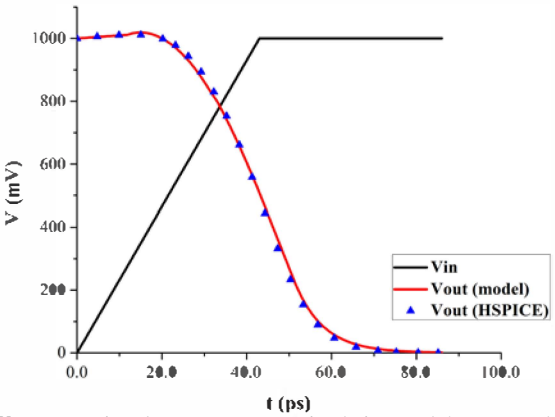

Fig. 5. V_{out} comparison between HSPICE simulations and the proposed model for a rising input case

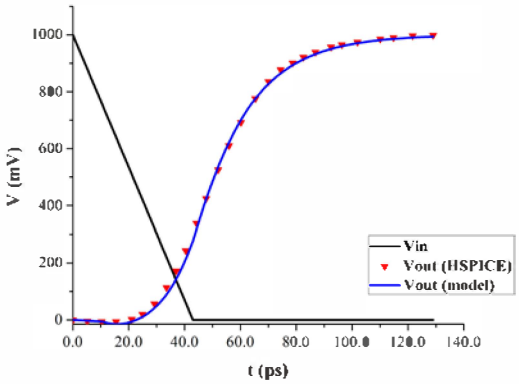

Fig. 6: V_{out} comparison between HSPICE simulations and the proposed model for a falling input case

In Table III and IV, comparisons for the propagation delay are provided for various design corners for $T = 25^oC$ and $T = 125^oC$ respectively. An average error of 3% with a maximum less than 10% is presented in all the corners for the typical case (V_{DD}=1V, T=25°C). For T=25°C and in whole the range of the V_{DD} (0.7V-1,25V) the average error increases to 4,5% while for different values of T the error is about 8%. This increased error for different values of V_{DD} and T is due to the approximations used for the parasitic capacitances which are strongly depended on these parameters but also in the accuracy of eq. (5), and the use of Taylor approximations for the solution of eq. (8).

TABLE III. EVALUATION RESULTS REGARDING PROPAGATION DELAY FOR T=25°C

$V_{DD} = 0.7V$							
$W(nm)$	$C_{out}(fF)$	τ 10ps			τ 100ps		
		HSPICE	Model	Error	HSPICE	Model	Error
100	0.5	10.9ps	11.5ps	5.5%	33ps	31.7ps	3.9%
	15	145ps	146ps	0.7%	170ps	166ps	2.4%
400	0.5	7.7ps	8.2ps	6.5%	24.2ps	25ps	3.3%
	15	39ps	40.1ps	2.8%	64.9ps	63.5ps	2.2%
$V_{DD} = 1V$							
$W(nm)$	$C_{out}(fF)$	τ 10ps			τ 100ps		
		HSPICE	Model	Error	HSPICE	HSPICE	Model
100	0.5	7.1ps	7.5ps	5.6%	13.7ps	13ps	5.4%
	15	88.3ps	88.3ps	0%	106ps	107ps	0.9%
400	0.5	4.7ps	5.1ps	8.5%	7ps	7.1ps	1.4%
	15	24ps	25ps	4.2%	41.4ps	41.4ps	0%

TABLE IV. EVALUATION RESULTS REGARDING PROPAGATION DELAY FOR T=125°C

$V_{DD} = 0.7V$							
$W(nm)$	$C_{out}(fF)$	τ 10ps			τ 100ps		
		HSPICE	Model	Error	HSPICE	Model	Error
100	0.5	14.7ps	15.4ps	4.8%	38.1ps	37.7ps	1%
	15	206ps	194ps	3.8%	232ps	220ps	5.2%
400	0.5	9.6ps	10.5ps	9.3%	28ps	30.5ps	8.9%
	15	54.2ps	54.8ps	1.1%	79ps	75ps	5%
$V_{DD} = 1V$							
$W(nm)$	$C_{out}(fF)$	τ 10ps			τ 100ps		
		HSPICE	Model	Error	HSPICE	Model	Error
100	0.5	9ps	8.9ps	1.1%	17.5ps	16ps	9.4%
	15	121ps	116ps	4.1%	139ps	133ps	4.3%
400	0.5	5.9ps	6.2ps	5%	9.6ps	9.3ps	3.1%
	15	32.3ps	32.2ps	0.3%	49.8ps	47.2ps	5.2%

In Fig. 7 the estimated values for the output current, I_{out}, in specific time points, are provided with the output current waveform as it results from HSPICE simulation. They refer to a circuit configuration: $W_N = 200nm$, $C_{out} = 1fF$, $\tau = 80ps$, $V_{DD} = 1V$, $T = 25^oC$. The output and supply current waveforms can be depicted by hundreds of points. However, to reduce simulation time, a minimal number of points from the current waveform are calculated. There is a trade-off between accuracy and simulation time as reflected by the number of points saved. The time points for which the current values are provided where selected so that the output current waveform can be accurately reconstructed. An average number of 10 points were adequately enough for all the cases. They correspond to the end of the regions of operation as depicted in Fig. 3 (as described in [11]) and for some cases at the middle of them. Connecting with lines the output current points in Fig. 7 and integrating over time, an estimation of the charge is obtained which may be used as a yardstick for the evaluation of the output current estimates. In Fig. 8 the values for the supply current for a rising input and the same configuration with that of Fig. 7 is provided. The accuracy is obvious. These current values for all the design corners are used in the CCS technology. In Table V the maximum output current value and the time point when it occurs, are compared with that of HSPICE simulations. In Table VI the consumed charge (integration of the current) is compared with the theoretic value, Q=$C_{out}V_{DD}$.

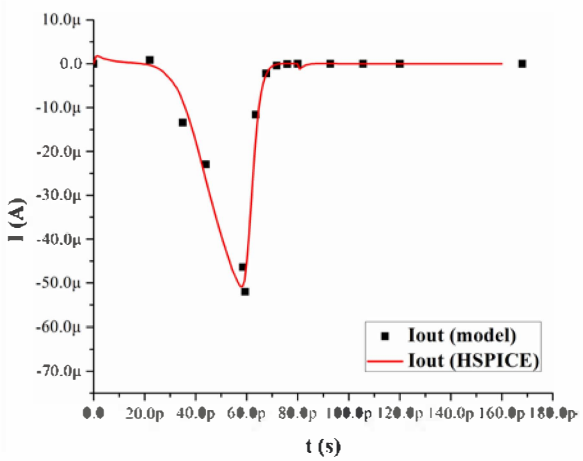

Fig. 7. Output current values compared to HSPICE output current waveform

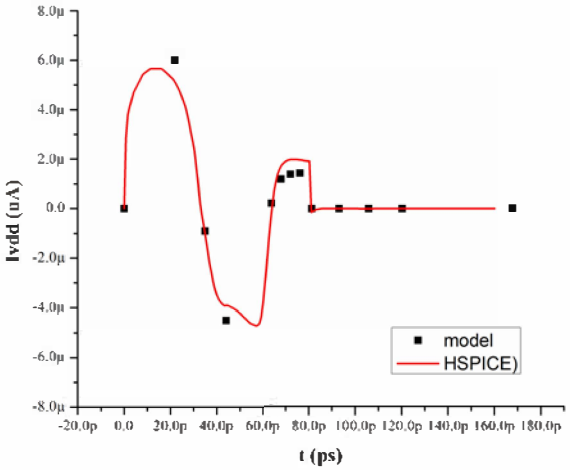

Fig. 8. Supply current values compared to HSPICE supply current waveform

TABLE V: EVALUATION RESULTS REGARDING THE MAXIMUM OF THE OUTPUT CURRENT (T=25°C, W=200nm)

V_{DD} (V)	C_{out} (fF)	τ (ps)	I_{max} (μA)			t_{max} (ps)		
			model	Hspice	error %	model	HSPICE	error %
0.7	0.5	10	46.4	45.5	2	10	10	0%
		100	16.2	16	1.3	86.1	82.5	4.4%
	5	10	82.4	79.3	3.9	10	10	0%
		100	63.6	68.5	7.1	100	100	0%
1	0.5	10	96	98.1	2.1	10	10	0%
		100	26.4	26.3	0.4	60.2	64.9	4.2%
	5	10	175	179	2.2	10	10	0%
		100	116	120	3.3	93.9	91.1	3.1%

A C++ code has been produced for the proposed model and compiled in a Linux environment. A class has been created for each region of operation and in each class the voltage expressions were calculated. To quantify the speed advantage of the proposed model versus HSPICE a fair comparison regarding the CPU time needed for the calculation of the output voltage waveform of both approaches was set up. For various cases an acceleration of 90-150 times was determined.

TABLE VI: EVALUATION RESULTS REGARDING THE INTEGRAL OF THE OUTPUT CURRENT (T=25°C, W=200nm)

V_{DD} (V)	C_{out} (fF)	τ (ps)	Consumed charge (fC)		
			model	Q=$C_{out}V_{DD}$	error
0.7	0.5	10	0.356	0.35	1.7
		100	0.4	0.35	12.5%
	5	10	3.2	3.5	8.6%
		100	3.68	3.5	5.1%
1	0.5	10	0.5	0.5	0%
		100	0.59	0.5	18%
	5	10	4.5	5	10%
		100	4.5	5	10%

V. CONCLUSIONS

An analytical model for the CMOS inverter was presented. The output voltage waveform was expressed as a function of the input signal slew, output voltage, transistor widths, supply voltage, temperature and process parameters. Based on the output voltage, waveforms for the supply and output currents are provided making this model compatible with CCS technology. The model has been evaluated for an industrial library for the 45nm PTM technology and for a wide range of parameter values. For the typical case the average error is less than 3% while it increases to 4.5% for different values of supply voltage and 8% for different values of temperature. A speed up of two orders of magnitude is presented in comparison to HSPICE.

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