The Effective Drive Current in CMOS Inverters

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ABSTRACT

A simple but accurate expression for the effective drive current, I_{eff}, for CMOS inverter delay is obtained. We show that the choice $I_{eff} = (I_H + I_L)/2$, where $I_L = I_{ds}(V_{gs}=V_{dd}/2, V_{ds}=V_{dd})$, and $I_H = I_{ds}(V_{gs}=V_{dd}, V_{ds}=V_{dd}/2)$ is defined, accurately predicts inverter delay when tested against compact models over a variety of conditions and against hardware results in 90nm node technology. Furthermore this definition of I_{eff} accurately captures the delay behavior of non-traditionally scaled devices, where mobility and V_T/V_{dd} are scaled in neither a regular nor uniform manner.

INTRODUCTION

The expression CV/I has been widely used as a simple means of approximating a CMOS inverter delay, τ_{pd}, where C is a calculated load capacitance, $V=V_{dd}$ is the power supply voltage, and I is taken as $I_{dsat}= I_{ds}(V_{gs}=V_{ds}=V_{dd})$ (1-3). Recently, attempts to improve over use of I_{dsat} as I_{eff} have been made, but the results are not simple, nor has a general validity been demonstrated (4-5). In Fig. 1, CV_{dd}/I_{dsat} is compared to compact-model drive impedance, Rsw, for inverters for several devices/technologies. While overall agreement is good, notable exceptions occur. The widths of devices in the inverters are scaled with technology, and thus Rsw tends to be higher for more-advanced technologies. Fig. 2 shows a plot of I_{ds}/I_{dsat} as a function of V_{ds}/V_{dd} for IBM technologies from .8μm to .25μm CMOS devices; the scaling of these devices was such that the normalized plots nearly overlay, resulting in good tracking between CV_{dd}/I_{dsat} and τ_{pd}. Deviations from the trend may be driven by significant deviations from uniform scaling, such as thicker gate oxide, or higher threshold voltage, than typical values for the V_{dd} in use. In Fig. 3 a case where the threshold voltage, V_T, was not lowered in proportion to V_{dd} illustrates the shortcomings that accompany the use of I_{dsat} in non-fully scaled situations. The normalized I_{ds}/I_{dsat} currents substantially fail to overlay, leading to large inaccuracies in the CV/I assessment. Limitations on gate oxide and subthreshold leakage, as well as innovations such as high-mobility devices are expected to further drive CMOS FET scaling such that I_{dsat} will significantly lose accuracy as an indicator of τ_{pd}.

INVERTER DELAY

We show typical Vin and Vout using three inverters as a function of time in Fig. 4; τ_{pd} is defined as the average of the falling and rising delays. We examine Vout, the output voltage of an inverter, vs. Vin, its input voltage, in Fig 5. Vin was swept from ground to V_{dd} and then back to ground using three cases: 1. quasi-static, dVin/dt<< I_{dsat}/C, 2. the ring-oscillator condition, where Vin(t) = Vout(t+2τ_{pd}) and 3. high-speed where dVin/dt >> I_{dsat}/C. Use of I_{dsat} as I_{eff} is equivalent to following trajectory 3, while the desired result lies along trajectory 2. I_{eff} arguments based on the quasi-static trajectory 1, can be seen to be misleading. In Fig. 6 trajectory 2 has been mapped to $I_{ds}(t)$ vs. $V_{ds}(t)$, and is compared to the FET characteristic. A convenient choice of integration for τ_{pd} runs from Vin=$V_{dd}/2$ to Vout=$V_{dd}/2$, yielding

$$\tau_{pd} = \int_{V_{gs}=V_{dd}/2}^{V_{ds}=V_{dd}/2} \frac{C dV_{ds}}{I_{ds}(V_{gs}, V_{ds})}. \quad (1)$$

(along trajectory 2)

In Fig. 7 several technologies are plotted in a similar fashion as in Fig. 6, except that for each technology I_{ds} and V_{ds} are normalized by I_{dsat} and V_{dd}, respectively. The intersection of an inverter trajectory with its $V_{gs}=V_{dd}/2$ device characteristic is the starting point for its τ_{pd} integral, while the end point for the integral is at its $V_{ds}=V_{dd}/2$ characteristic. To evaluate this integral we linearize the $I_{ds}(V_{gs},V_{ds})$ equation by,

$$I_{ds} = I_{dsat} + g_m(V_{gs} - V_{dd}) + g_{ds}(V_{ds} - V_{dd}) \quad (2)$$

which is illustrated in Fig. 8. We also approximate the inverter trajectory 2 by

$$V_{ds}(t) = (3/2)\,V_{dd} - V_{gs}(t), \quad (3)$$

also shown in Fig 8. The integration of (1) is now trivial:

$$\tau_{pd} = \frac{CV_{dd}}{2(I_H - I_L)} \ln\left(\frac{I_H}{I_L}\right). \quad (4)$$

To further simplify (4), we expand the logarithm and define I_{eff},

$$\frac{1}{(I_H - I_L)} \ln\left(\frac{I_H}{I_L}\right) \approx \frac{2}{(I_H + I_L)} \equiv \frac{1}{I_{eff}}, \quad \text{where } I_H/I_L \le 3, \quad (5)$$

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so that it satisfies $\tau_{pd} = \frac{CV_{dd}}{2} \frac{1}{I_{eff}}$.

In the region for $I_H/I_L>3$, we extend the simplified expression (5),

$$I_{eff} = \frac{(I_H + I_L)}{2}. \quad (6)$$

EVALUATION OF I_{EFF}

To verify our approximation, we would like to remove C from the equation, since it presents yet another variable, not addressed by this work. In Fig. 9 τ_{pd} is plotted against Cload, where Cload is varied for a given inverter and the slope defines the drive impedance, Rsw. Rsw should then be proportional to V_{dd}/I_{eff}, regardless of technology/device details.

In Fig. 10 Rsw was extracted from compact models for the same technologies as those used in Fig. 1, and was compared to V_{dd}/I_{eff}. Also shown is V_{dd}/I_{dsat}, for comparison. A substantially improved agreement is seen when I_{eff} is used. In Fig. 11, V_T and V_{dd} were independently varied in compact models and the modeled Rsw was compared to V_{dd}/I_{eff}. The results indicate that I_{eff} accurately predicts the Rsw for large values of V_T/V_{dd}, which is of interest for power-constrained CMOS. Similarly, Fig. 12 shows a comparison where low-field mobility was independently varied, showing that I_{eff} can capture performance benefits of strained silicon devices. As a further test, in Fig 13, saturation velocity was varied independently, and again I_{eff} proved true. Thus even though the devices are highly non-uniform in their scaling, I_{eff} continues to predict the value of Rsw well.

In Fig. 14 experimental ring oscillator delays and device currents for 90-nm technology were measured at various V_{dd}s to show the correlation between the delay and V_{dd}/I_{eff}. We expect Rsw to be directly proportional to the measured delay, since Cload should be relatively constant. Even at low V_{dd} where V_T/V_{dd} issue becomes significant, I_{eff} continues to agree well with the data. Moreover, the normalized slope of V_{dd}/I_{eff} vs. delay is very close to unity and hence to the ideal case.

The approximation in (5) was used throughout this work for I_{eff}. For some cases examined, particularly those where $I_H/I_L>3$, the approximation contributes more than 10% error to the evaluation of I_{eff}, yet the agreement of simulation-based and hardware-based data with (6) continues to be quite good in this regime. We suspect that this unjustified agreement is due to cancellation of the earlier approximation to the voltage trajectory, Fig. 8. This should prove a fruitful region for future investigation

CONCLUSION

In conclusion, a simple yet accurate expression for the effective drive current for CMOS inverter delays was derived. This expression was validated with both compact model delay analysis and with hardware-based data from ring oscillators. We find our I_{eff} expression accurate over a wide range of variables and technology scales. Therefore we expect that advanced technology options will demand its adoption in lieu of of I_{dsat} to enable accurate and rapid assessment of an inverter delay.

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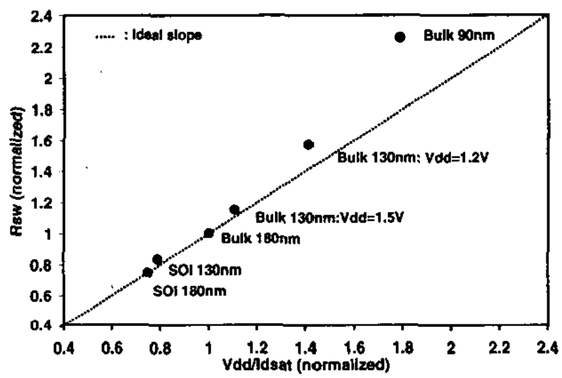

Fig. 1. CV_{dd}/I_{dsat} is compared to simulated compact-model Rsw for various technologies. Note that device widths are scaled according to the technology scaling; this results in increasing Rsw with scaling.

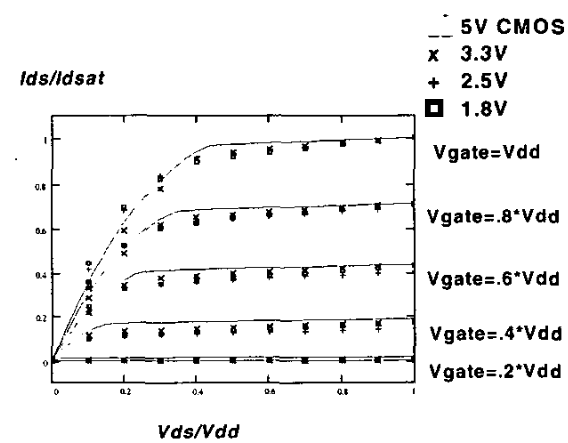

Fig. 2. NMOS I_{ds}/I_{dsat} vs. V_{ds}/V_{dd} are plotted for IBM technologies from 800 nm to 250 nm CMOS devices.

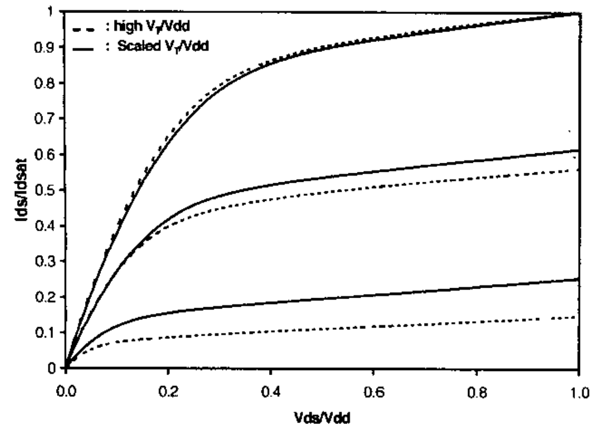

Fig. 3. I_{ds}/I_{dsat} as a function of V_{ds}/V_{dd} is compared for the cases of high V_T/V_{dd} and scaled V_T/V_{dd} devices.

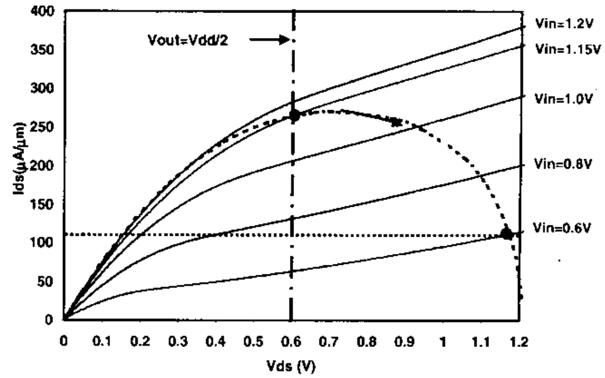

Fig. 6. Trajectory 2 is mapped to I_{ds} (t) as a function of V_{ds}(t) for 130-nm technology. The example is PFET and V_{dd} is 1.2V.

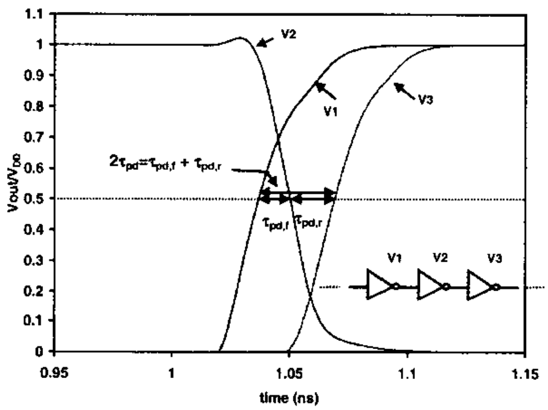

Fig. 4. Typical Vin and Vout using three inverters are shown.

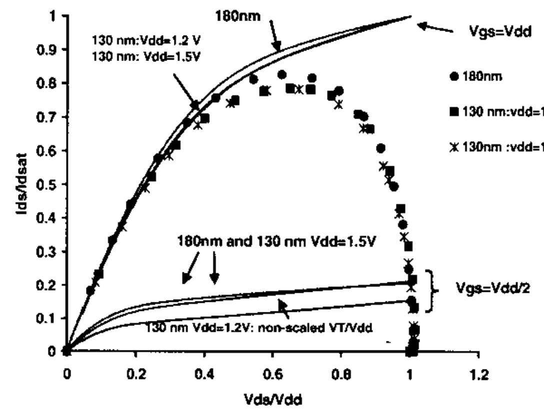

Fig. 7. Several technologies are plotted for I_{ds}/I_{dsat} vs. V_{ds}/V_{dd}. The lines are for I_{ds} vs. V_{ds} at $V_{gs}=V_{dd}/2$ and at $V_{gs}=V_{dd}$ for the technologies.

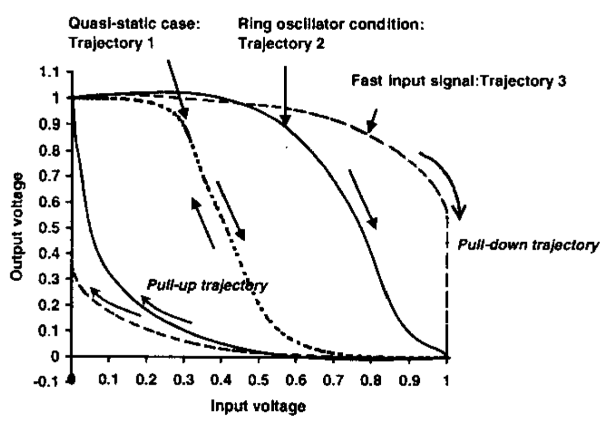

Fig. 5. Vout is plotted as a function Vin for various trajectories.
Trajectory 1: Quasi-static case, Trajectory 2: Ring oscillator condition where Vin(t)=Vout(t+$2\tau_{pd}$), Trajectory 3: Very fast input case (the use of I_{dsat} as I_{eff} is equivalent to this trajectory).

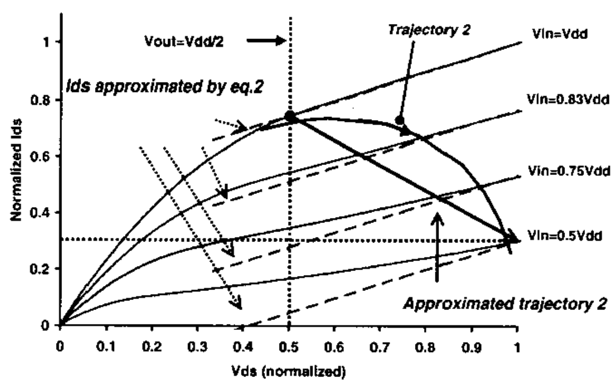

Fig. 8. I_{ds}/I_{dsat} vs. V_{ds}/V_{dd} is shown. The dashed lines are I_{ds} approximated by Eq.2, and the approximated trajectory 2 is also plotted.

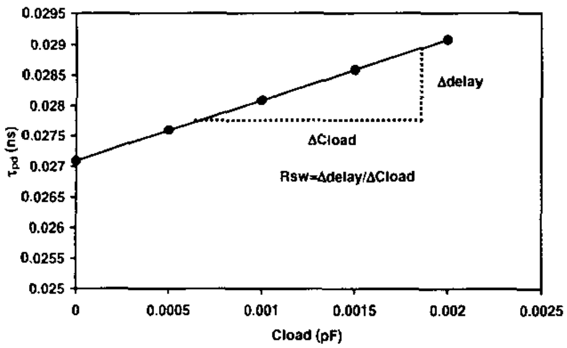

Fig. 9. The definition of switching resistance, Rsw, is shown. Rsw is extracted from the slope of τ_{pd} vs. Cload.

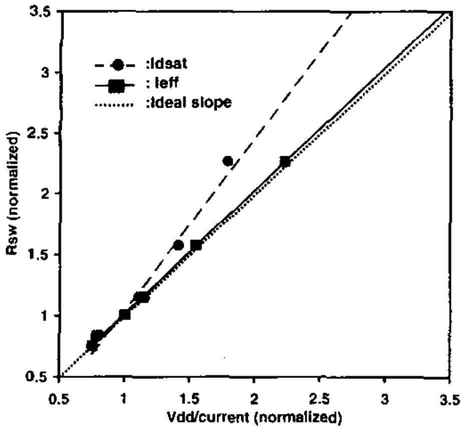

Fig. 10. Rsw is extracted from compact models for various technologies used in Fig. 1.

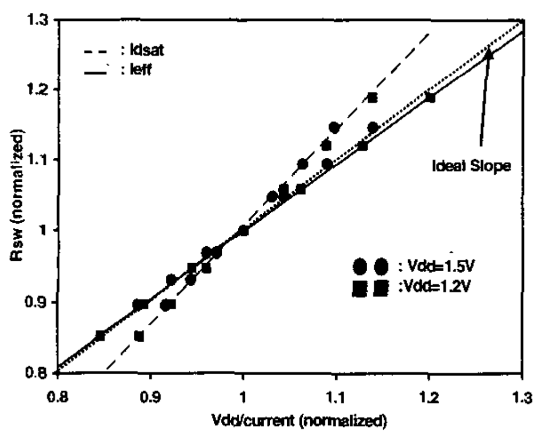

Fig. 11. Rsw is extracted from compact models with various conditions of V_T/V_{dd}. The dashed line shows the trend for Rsw vs. I_{dsat}, while the solid one is for Rsw vs. I_{eff}. The 130 nm technology is shown in the plot with different power supply V_{dd}.

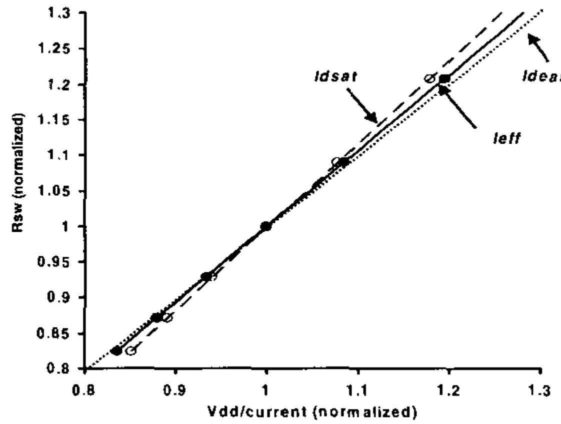

Fig. 12. Rsw is extracted from compact models when the mobility is changed. The dashed line shows the trend for Rsw vs. I_{dsat}, while the solid one is for Rsw vs. I_{eff}.

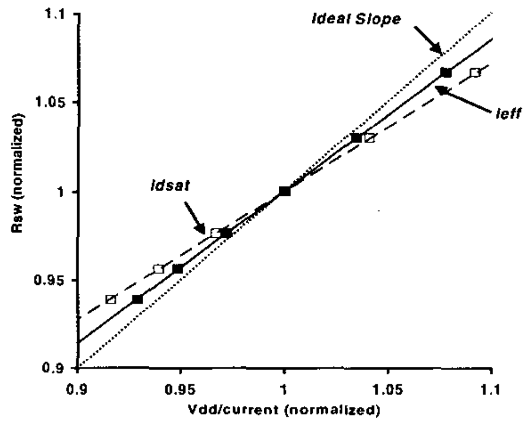

Fig. 13. Rsw is extracted from compact models when the saturation velocity is changed. The dashed line shows the trend for Rsw vs. I_{dsat}, while the solid one is for Rsw vs. I_{eff}.

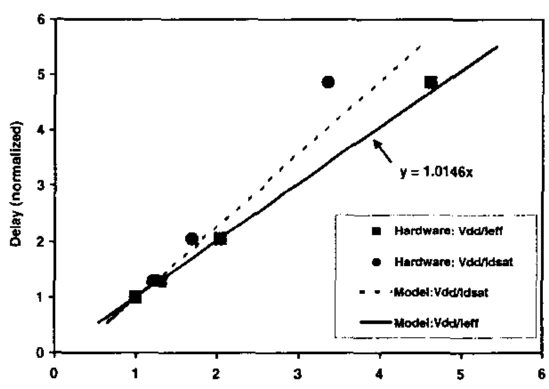

Fig. 14. Experimental ring oscillator delays and device currents for 90-nm technology were measured at various V_{dd}. The measured delays are directly correlated with Rsw since the Cload remains relatively constant.