Project Write Up

Project Course Code: EE299
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Project Title: Machine Learning Driven Device Co-Optimization

Problem Statement:-
The CMOS inverter, the smallest and most widely used logic circuit in CMOS technology, serves as the focus of this work. The goal is to predict and optimize the inverter design, including Width (W), Length (L), and Number of Transistors (N), to meet specified power and delay requirements for advanced Nanosheet FET and CFET-based technologies.

The work would include the following steps:-

(a) Develop an analytical model for inverter delay and power as functions of key parameters such as effective current and capacitance.

(b) Validate the analytical model through mixed-mode simulations(using TCAD or Cadence) to ensure accuracy and reliability under various operating conditions

Future Work:-

(a) Build a deep neural network (DNN)-based forward model to predict current and capacitance values for given inverter design parameters (W, L, N)

(b) Implement advanced optimization techniques such as grid search, Bayesian optimization, or evolutionary algorithms to achieve efficient inverse design for the desired power and delay requirements.

This approach leverages a combination of analytical modeling, simulation, and machine learning to enable accurate and efficient design optimization for next-generation CMOS technologies.

Here Is the Final Project Presentation Link: CLICK HERE

Motivation:-

As CMOS devices scale down, emerging architectures like CFETs (Complementary Field-Effect Transistors) offer vertical stacking (NMOS over PMOS) to improve density and performance. However, with increased non-linearity and tighter power/delay constraints, traditional manual design-space exploration becomes inefficient.

This project focuses on **co-optimizing CFET-based inverter circuits** using physics-based analytical modeling and, later, machine learning. The key trade-offs involve maximizing speed (minimizing delay) while minimizing power consumption, both static and dynamic.

Approach:-

Implemented and compared three classical models for the calculation of delay using current modelling:-

- **One-point model**
- **Two-point model -** *reference link*
- **Three-point model -** *reference link*

Proposed a new **transient-current-based model** by averaging the actual current over a full switching cycle, leading to better agreement with the simulated delay.

One Point Model:-

- Uses the equation such that $I_{effective}$ is taken as I_{ON}
- I_{ON} was taken as $I_{dsat} = I_d(V_{GS}=V_{DD}, V_{DS} = V_{DD})$

Two Point Model:-

$I_{effective(NMOS)} = (I_{NL} + I_{NH})/2$

$I_{effective(PMOS)} = (I_{PL} + I_{PH})/2$

$\tau_{PHL} = C_L V_{DD} / 2I_{effective(NMOS)}$

$\tau_{PLH} = C_L V_{DD} / 2I_{effective(PMOS)}$

$\tau_P = (\tau_{PLH} + \tau_{PHL})/2$

$I_H = I_{ds}$ ($V_{GS} = V_{dd}$ and $V_{DS} = 0.5V_{dd}$)

$I_L = I_{ds}$ ($V_{GS} = 0.5\ V_{dd}$ and $V_{DS} = V_{dd}$)

Three Point Model:-

$$I_{effective(NMOS)} = (I_{NL} + I_{NH} + I_{NM})/3$$

$$I_{effective(PMOS)} = (I_{PL} + I_{PH} + I_{PM})/3$$

$$\tau_{PHL} = C_L V_{DD} / 2I_{effective(NMOS)}$$
$$\tau_{PLH} = C_L V_{DD} / 2I_{effective(PMOS)}$$
$$\tau_P = (\tau_{PLH} + \tau_{PHL})/2$$

$$I_H = I_{ds}\ (V_{GS} = V_{DD} \text{ and } V_{DS} = 0.5V_{DD})$$

$$I_L = I_{ds}\ (V_{GS} = 0.5\ V_{DD} \text{ and } V_{DS} = V_{dd})$$

$$\mathbf{I_M = I_{ds}(V_{GS}=0.75\ V_{DD},\ V_{DS}=0.75\ V_{DD}).}$$

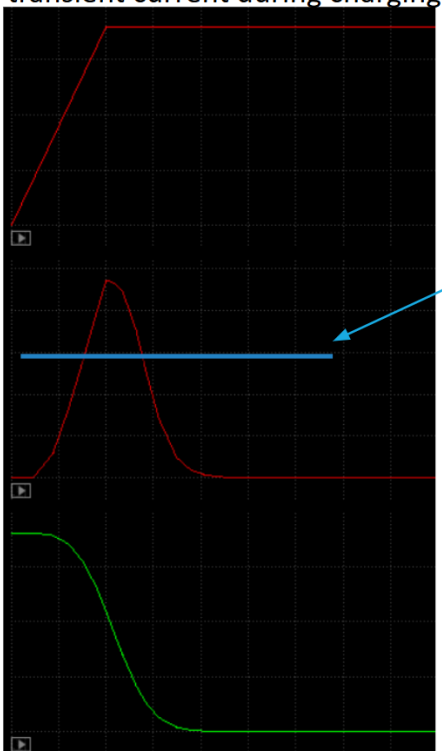
Second Approach :-

Find the average transient current during charging and discharging and fit it to get $I_{effective}$

Input Pulse Going Low to High =>

NMOS transient current =>

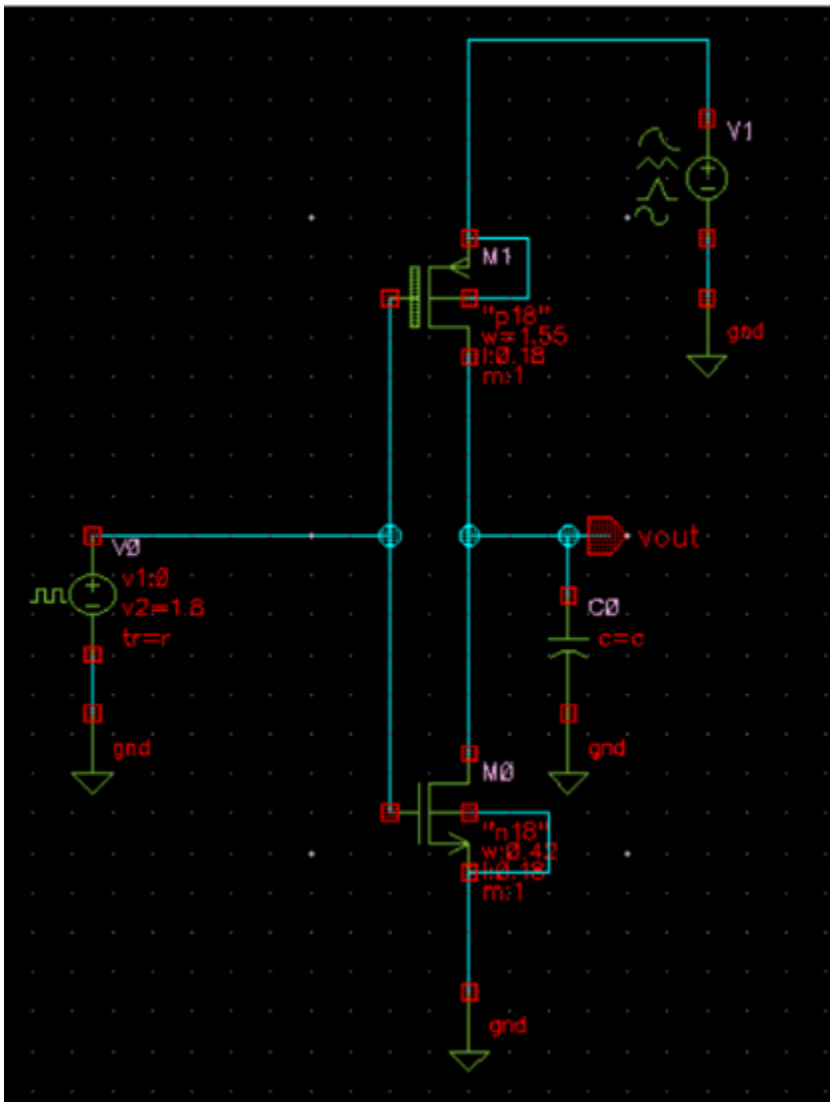
Output Voltage Going High to Low =>



Average Value of Current

(similarly we can do for PMOS)

Tool Used: Cadence Virtuoso ADE Suite

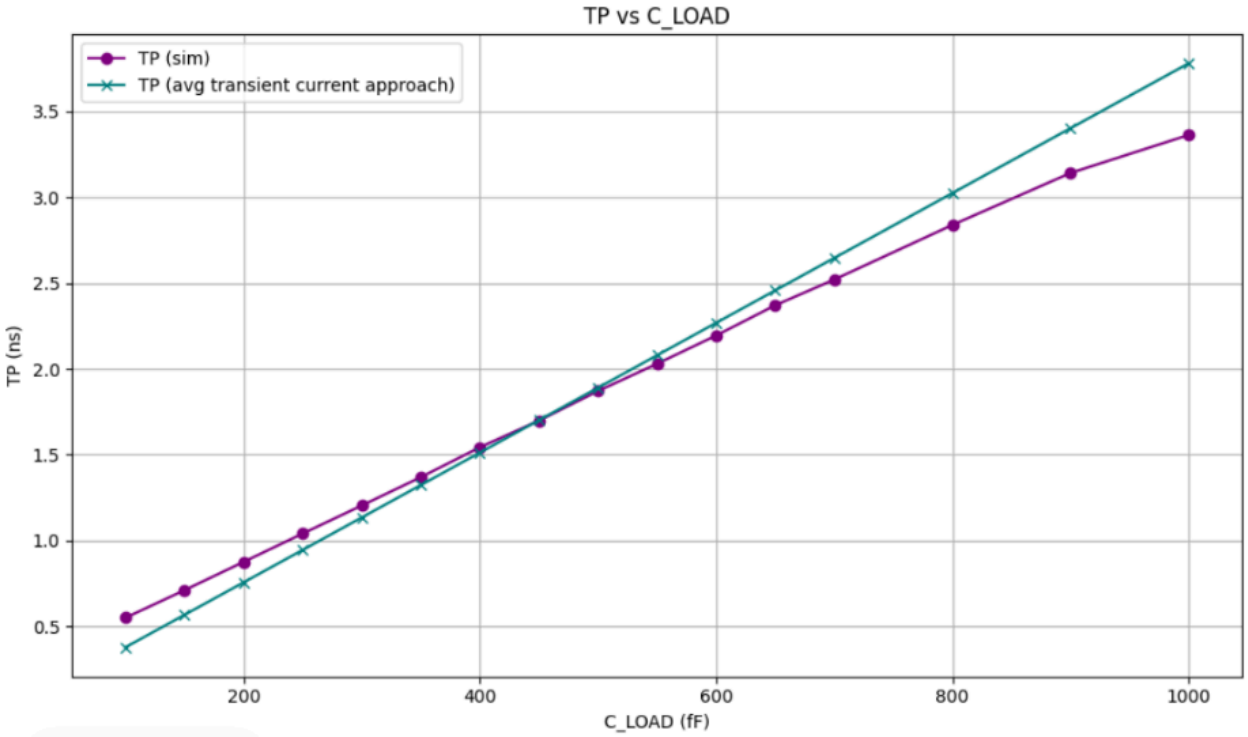


Results :-

C_{load} (fF)	τ_{PHL}(ns)(sim)	τ_{PLH} (ns)(sim)	τ_P(ns)(sim)	Error % onepoint	Error % twopoint	Error % threepoint
100	0.585	0.515	0.55	48.20609455	1.687545455	1.243636364
150	0.7706	0.651	0.7108	39.88467642	14.10773073	14.62296005
200	0.958	0.793	0.8755	34.92484752	23.52221588	24.07995431
250	1.14	0.941	1.0405	31.55538683	29.9179481	30.50456511
300	1.33	1.078	1.204	29.01998007	34.73052326	35.33887043
350	1.52	1.218	1.369	27.17073192	38.24066837	38.86486486
400	1.71093	1.3755	1.543215	26.16285352	40.15376989	40.78660459
450	1.8934	1.5036	1.6985	24.52757374	43.25777156	43.90462173
500	2.0809	1.6612	1.87105	23.87523583	44.49600492	45.14844606
550	2.27	1.79	2.03	22.8194266	46.50008621	47.16157635
600	2.47	1.919	2.1945	22.11442789	47.83827751	48.50580998
650	2.65799	2.0833	2.370645	21.89331933	48.2579741	48.92740161
700	2.831	2.21	2.5205	20.88611942	50.16978774	50.84784765
800	3.2132	2.4641	2.83865	19.71775879	52.38750815	53.0755817
900	3.62	2.663	3.1415	18.38935795	54.90900844	55.60846729
1000	3.96	2.766	3.363	15.29393993	60.78456735	61.51055605

Significant Error Observed when Classical Models were used

- **Averaging of the transient current showed better results**



Worst Case error = 30%
Best Case Error = 0.15%

Future Work:-

- Gathering more data from TCAD Mix Mode Simulations
- Develop a physics-based ML model to train the parameters using the formulated model
- Implement the model for scaling across technologies
- Apply methodology to different logic gates and circuits beyond the inverter.