Shreyas Pathak

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Electrical engineering graduate with a strong focus on front end VLSI design, RTL development, verification, and design for testability. Skilled in SystemVerilog, FPGA prototyping, simulation workflows, and digital logic design, complemented by hands-on project experience and continuous self learning. Adept at collaborating on complex engineering challenges and committed to delivering precision, reliability, and performance in every design.

Skills

Software & Programming tools: MS Office, AutoCAD/Solidworks, Matlab/Simulink/ RStudio, Android Studio, UVM, Python/C++/Java, SystemVerilog/Verilog-A/AMS, Git, Gradle, Google Tests, Cadence Virtuoso, LTSpice, Synopsys VCS

Hardware & System Design: FPGA programming, Raspberry Pi, PLC (LAD, SFC) and HMI programming

Professional & Analytical: Project Management, Risk Management, Data Analysis, Technical Communication

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Education

University of British Columbia, Okanagan **September 2020 - April 2025**
Bachelor of Applied Sciences - Electrical Engineering

Relevant Courses*: Engineering Drawings and CAD/CAM, Embedded System Design, Energy System Transition, Microelectronics, Motor Drive Systems, Power Electronics, Engineering Project Management*

Technical Projects

16-bit Arithmetic Logic Unit (ALU) Design, University of British Columbia, Okanagan **January 2025 - April 2025**

- Designed a 16-bit ALU using SystemVerilog, supporting arithmetic/logical operations and a custom 16-bit instruction format with opcode and register addressing.
- Developed a comprehensive testbench for simulation and verification; analyzed signal behavior using EPWave waveform viewer on EDAPlayground.
- Applied digital design principles and modular HDL practices to implement and verify ALU functionality in a hardware simulation environment.

Engraving Machine Control System, University of British Columbia, Okanagan **September 2024 - December 2024**

- Designed and implemented a state feedback controller for an engraving machine by analyzing system states and transfer functions to achieve precise and stable performance.
- Conducted detailed system controllability and stability analysis using Matlab, employing simulation tools and methods to ensure performance and reliability.
- Enhanced system performance by significantly reducing Integral Squared Error (ISE), achieving accurate tracking of desired outputs through integrated feedback and feedforward control strategies.

Analog Integrated Circuit Design Project, University of British Columbia, Okanagan **January 2024 - April 2024**

- Developed and optimized low-pass filters and differential amplifiers using Cadence simulation software, achieving precise cutoff frequencies, improved gain stability, and robust circuit designs.
- Conducted detailed parametric analyses to fine-tune resistance, capacitance, and gain, ensuring accurate operation and enhanced reliability under varying circuit conditions.
- Integrated switched-capacitor filters to replace resistors, achieving an estimated 20% improvement in noise reduction and gain stability, particularly in high-frequency applications.

Digital Logic and FPGA Design, University of British Columbia, Okanagan **January 2022 - April 2022**

- Designed and simulated combinational and sequential circuits including ripple-carry adders, 2's complement logic, and FSMs using SystemVerilog in Intel Quartus.
- Developed modular Verilog designs for arithmetic and control logic, validated through simulation and FPGA testing.
- Optimized circuit designs for accurate signal behavior from logic gates to synthesized hardware.

Certificates

BCG GenAI **May 2025**

- Completed a job simulation for BCG's GenAI team, developing a Python-based chatbot that provided financial insights using rule-based logic and SEC filings (10-K, 10-Q).
- Applied pandas for data extraction and manipulation, and translated complex financial data into clear, user-friendly responses through structured logic.

Volunteer Experience

- ***The Pink Back Project UBCO*** - Supported donation drives, care packages, and campus events to reduce inequalities.
- ***Teach One campaign*** - Taught underprivileged individuals,crafted personalized learning plans to empower their future.