

1. At the integrated circuit level what are the 3 principle constituents of a computer system
 - Gates:
For data processing
 - Memory cells:
for data storage
 - Interconnection among the elements:
For data movement
2. Explain the Moore's law
 - Moore's law posits that the number of transistors per square inch on an integrated circuit doubles every after two years. Although the doubling of transistors increases the power of computers, the cost of computer gets halved.
3. List and explain the key characteristics of computer family
 - **Similar or identical instruction set**; in many cases, the set of machine instructions is supported in all members of the family. Thus, the program that runs on one machine runs on another
 - **Similar or identical operating system**; the same basic operating is available for all family members
 - **Number of input or output ports; increase** from low to high
 - **Increasing memory size**; increase from low to high
 - **Increasing cost; increases** from low to high

4. A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

Solution:-

CPI is the average Clocks per instructions =

$$45000 + (2 \times 32000) + (2 \times 15000) + (8000 \times 2) / (100\ 000) = 155 / 100 = 1.55$$

$$\text{MIPS} = 40 \text{ M clocks / sec} \times (1 / 1.55 \text{ clocks per instruction}) = 40 / 1.55 / 1000000 =$$

25.8 MIPS

$$\text{Execution time} = (100\ 000 \text{ instructions}) \times 1.55 \text{ CPI} = 155\ 000 \text{ cycles} \times 1 / 40 \text{ M sec} = 0.003875 = 3.87 \text{ ns}$$

Stallings: CPI = 1.55; MIPS rate = 25.8; Execution time = 3.87 ns.

- a. On the IAS, what would the machine code instruction look like to load the contents of memory address 2?

Op Code | operand(Address)

.....

00 0001 | 000 000 0010

- b. How many trips to memory does the CPU need to make to complete this instruction during the instruction cycle?

At the beginning, the CPU must get instruction from the memory. The instruction contains the address of the data to be loaded. The data will be loaded which are located at this address. This is another memory call.

During the execution time of the instruction, there will be two memory accesses.

6. On the IAS, describe in English the process that the CPU must undertake to read a value from memory and to write a value to memory in terms of what is put into the MAR, MBR, address bus, data bus, and control bus

To the value from memory, the CPU puts the address of the value it wants in the the MAR. The CPU then asserts the read control line to memory and places the address on the address bus. Memory places the content of the memory location on the data bus this data is then transferred to the MDR. To write a value to memory, the CPU puts the address of the value it wants to write into the MAR. the CPU also place the data it wants to write into the MDR. The CPU then asserts the write control line to memory and places the address on the address bus. Memory transfers the data on the data bus into the corresponding memory location.

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MODULE NAME: COMPUTER SYSTEMS ARCHITECTURE AND OPERATION

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