Combinational Testing

Definitions

Singular Cover

- Minimal set of input signal assignments needed to represent essential prime implicants of a KMAP

D Frontier

- Comprises of gates whose output value is X and atleast 1 of its i/p is D or overline{D}
- Any gate in D frontier can be used for fault propagation

Unique D Drive

- If there is one 1 gate is D frontier, fault effect has to be propagated through that gate

J Frontier

- Gates whose output value is known (0 or 1) but its inputs are not yet computed
- Any gate in J frontier can be used for justification

D Algorithm

Procedure

1. Unique D Drive
2. Backward Implication
3. Propagate D Through D frontier
4. Backward Implication

PDFC (Primitive D Cube for a Fault)

Specify minimal input conditions
- Applied to gate input to produce error at the gate output
- Used in fault activation

PDC (Propagation D Cube)

TC (Test Cube)

Test cube is a partially specified Boolean values for testing a fault

Pros

- Guarantee to generate a pattern for the testable fault

Cons

- Assignment of values is allowed for internal signals
- Backtracking could occur at each gate
- Very large search space

PODEM (Path Oriented Decision Making Algorithm)

PODEM choose what input to be chosen based on difficulty level as given by the controllability measures.

SCOAP (Sandia Controllability Observability Analysis Program)

- CC1 - The controllability to assert 1 at a net
- CC0 - The controllability to assert 0 at a net

CO (Combinational Observability)

- CO(a) - The observability of an input (a) as seen from the output

Sequential Circuit Testing

Procedure

1. Initialisation of FFs
2. Activating of fault
3. Propagation of fault

Algebra

Roth's Algebra (5 Values)

- Initial algebra for testing out circuits with five values

- Possible Values - 1 (`1/1`), 0 (`0/0`), D (`1/0`), D ~ (`0/1`), X (`X/X`)

Muth's Algebra (9 Values)

- Roth's 5 valued algebra was insufficient for testing sequential circuits
- Added these values :- G0 (`0/x`), G1(`1/X`), F0(`X/0`), F1(`X/1`)

Types of Sequential ATPG ckts

- Cyclic Circuit
  - There is feedback in the s-graph
- Acyclic Circuit
  - There is no feedback in the s-graph
  - Can be tested easily by time frame expansion method

Theorems

- Given a cycle free structure, the fault free and faulty circuit with a non-FF fault are always initialisable
- A test for a non-FF fault can always be found in $d_seq + 1$ time frames, unless it is untestable

Simplified Model

Assumptions

- Single SaFs
- FFs are treated as ideal memory elements
  - Internal faults in FFs are not modeled
  - Faults in clk signal are ignored
  - only i/p and o/p of FFs are considered

Time Frame Expansion

- Unroll the ckt with respect to each time frame (each posedge of the clock)
- Efficient for acyclic circuits

Simulation Based Methods

- Use vector spaces to find all the test vectors iteratively
- Algorithms:

- Contest
- Genetic

Contest Algorithm

Intro

- Concurrent test generator
- Search for test is guided by cost functions

Phases

- Initialisation - No faults targetted, Compute Cost functions (True value simulator)
- Concurrent Phase - all faults targetted, cost function (Concurrent fault simulator)
- Single fault phase - faults targetted one at a time, cost function (by true value simulator) and dynamic testability analysis