

Opcode Table of the Minimal 8-Bit CPU

description	no operand (A)	immediate	abs address	rel address	word at abs adr	(SP + rel offset)
Load A from		LDI (0x0b)	LDA (0x15)	LDR (0x21)		LDS (0x2c)
Store A to			STA (0x16)	STR (0x22)		STS (0x2d)
Clear			CLA (0x17)	CLR (0x23)	CLW (0x32)	
Negate	NEG (0x0c)		NEA (0x18)	NER (0x24)	NEW (0x33)	
Increment	INC (0x0d)		INA (0x19)	INR (0x25)	INW (0x34)	
Decrement	DEC (0x0e)		DEA (0x1a)	DER (0x26)	DEW (0x35)	
Add		ADI (0x0f)	ADA (0x1b)	ADR (0x27)	ADW (0x36)	
Subtract		SBI (0x10)	SBA (0x1c)	SBR (0x28)	SBW (0x37)	
Compare		CPI (0x11)	CPA (0x1d)	CPR (0x29)		
Add with Carry		ACI (0x12)	ACA (0x1e)	ACR (0x2a)	ACW (0x38)	
Sub with Carry		SCI (0x13)	SCA (0x1f)	SCR (0x2b)	SCW (0x39)	
Jump to			JPA (0x14)	JPR (0x20)		
Jump to subroutine			JPS (0x30)			

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No Operation	NOP (0x00)					
Wait on Terminal Input	WIN (0x01)					
Output A to Terminal	OUT (0x02)					
Clear Carry In Flag	CLC (0x03)					
Set Carry In Flag	SEC (0x04)					
Logical NOT	NOT (0x05)					
Logical Shift Left	LSL (0x06)					
Rotate Shift Left	ROL (0x07)					
Logical Shift Right	LSR (0x08)					
Rotate Shift Right	ROR (0x09)					
Arithmetic Shift Right	ASR (0x0a)					
Return from Subroutine	RTS (0x31)					
Push on Stack	PHS (0x2e)					
Pull from Stack	PLS (0x2f)					

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Branch on Carry Set			BCS (0x3d)			
Branch on Carry Clear			BCC (0x3c)			
Branch on minus			BMI (0x3f)			
Branch on plus			BPL (0x3e)			
Branch if Zero			BEQ (0x3b)			
Branch if not Zero			BNE (0x3a)			