

Page Table Issue (2) – Size

- 32-bit address space
- 4 kB page size

* Linear page tables are too big

$$|offset| = \log_2(4 \text{ kB}) = 12 \quad |VPN| = 32 - 12 = 20 \text{ bits}$$

$$\# \text{ entries in the page table} = 2^{20}$$

$$5\text{-bytes} = |pte|$$

$$|page \text{ table}| = 5 \text{ bytes} * 2^{20} = \underline{\underline{5 \text{ MB}}} \text{ per process}$$

~100 processes active at once in a system
 \Rightarrow 500 MB for all page tables

Solving Size: Solution #1

Simple Solution: .. why not inc^r the sz of a page?

- Internal fragmentation

Solving Size: Solution #2 Motivation

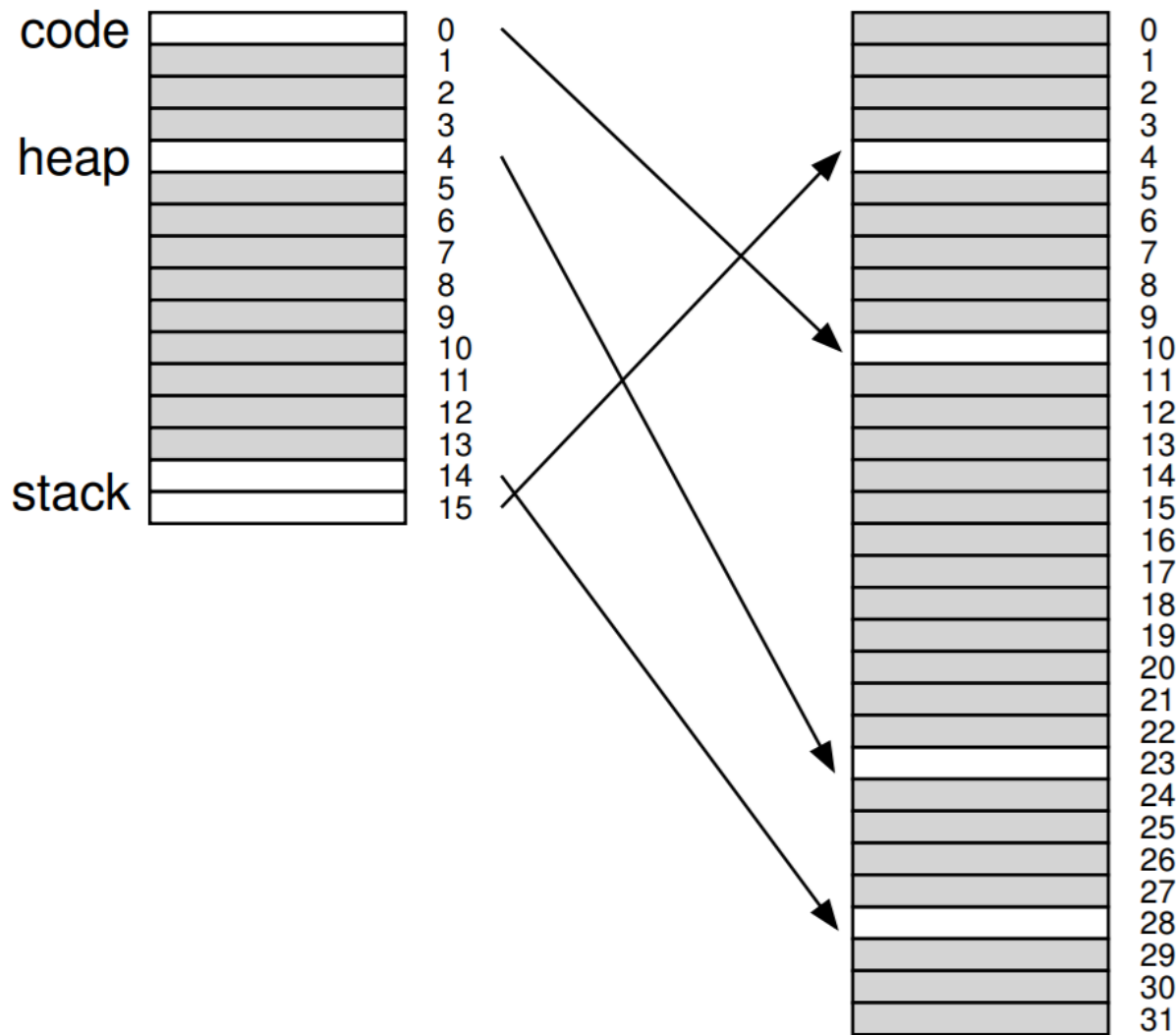
Consider:

- 16 kB address space
- 1 kB pages
- the stack and heap small

Solving Size: Solution #2 Motivation

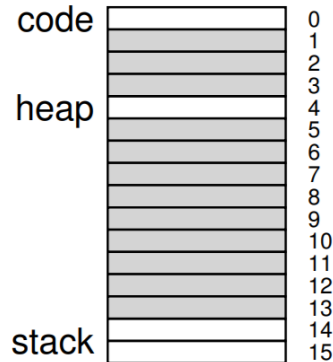
Virtual Address Space

Physical Memory

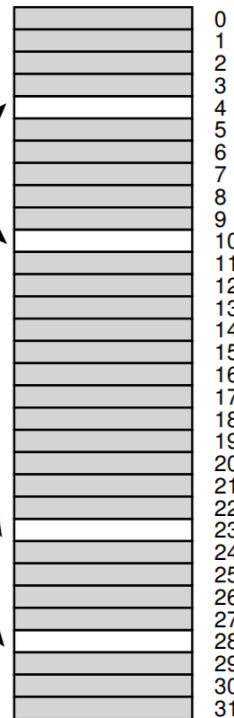


Solving Size: Solution #2 Motivation

Virtual Address Space



Physical Memory



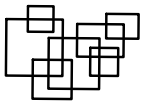
PFN	valid	prot
10	1	r-x
-	0	—
-	0	—
-	0	—
23	1	rw-
-	0	—
-	0	—
-	0	—
-	0	—
-	0	—
-	0	—
-	0	—
-	0	—
-	0	—
28	1	rw-
4	1	rw-

a sparse address space
leads to lots of invalid
entries in the page table
wasted space ←

Solving Size: Solution #2

Combine paging with segmentation / segmented paging)

1. Break up a process into different sized segments
2. Break up segments into fixed sized pages
 - e/a seg has its own page table
 - all entries in a page table are valid b/c we hv variable length page tables



seg table ^{↑?} stores location of page table

Solution #2 Visual

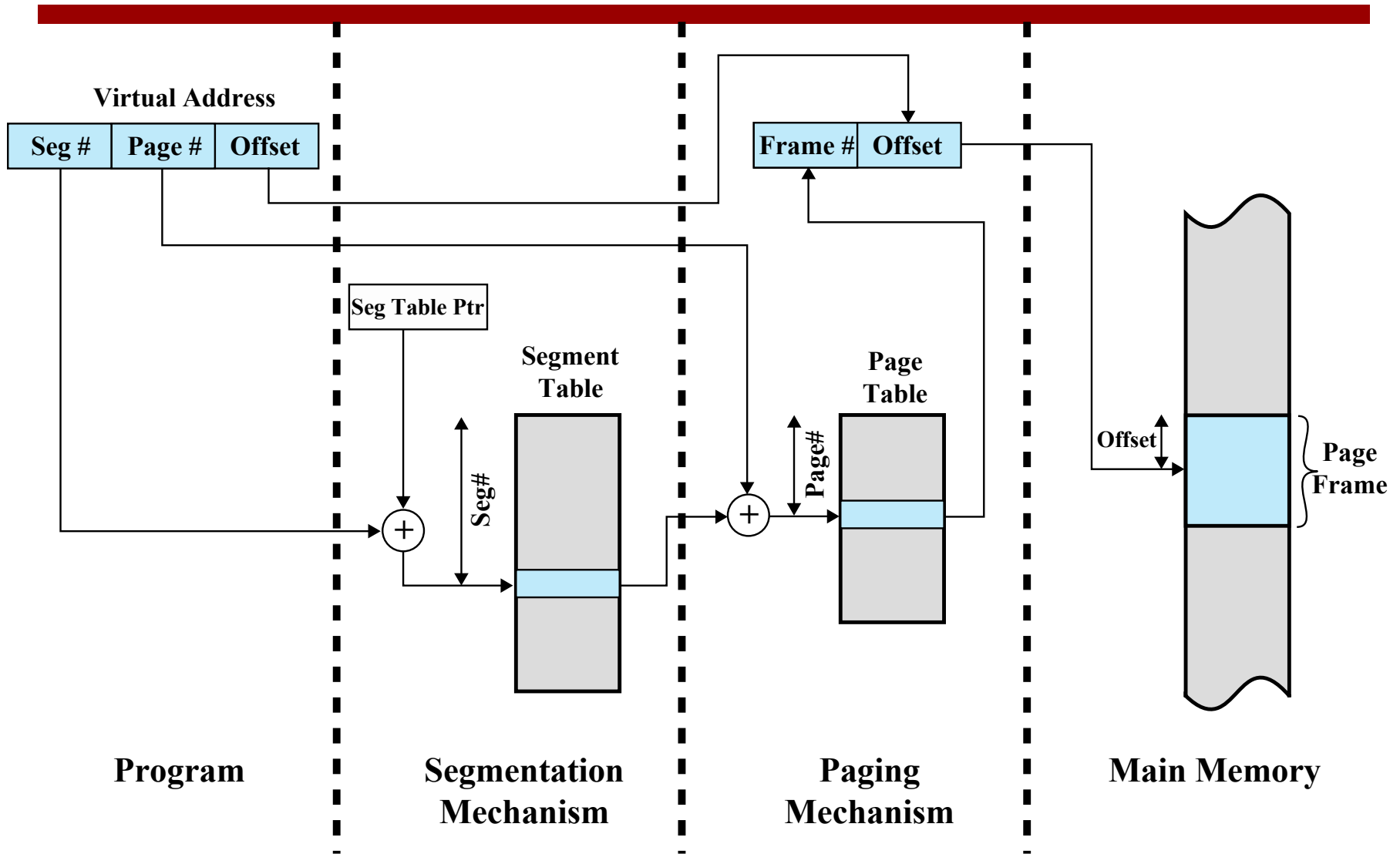


Figure 8.12 Address Translation in a Segmentation/Paging System

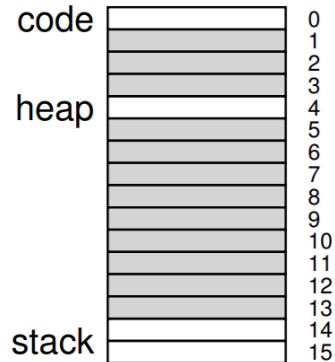
Solution #2 Analysis

+space efficiency - page tables only store valid entries

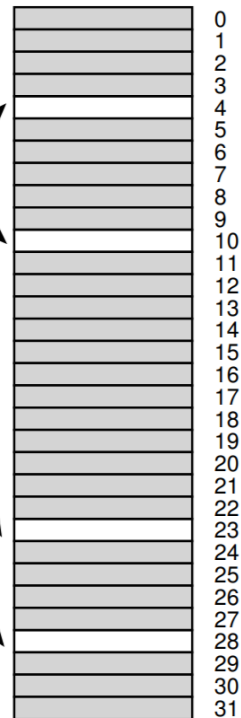
- External fragmentation - due to variable length page tables

Solution #3: Motivation

Virtual Address Space



Physical Memory



goal: don't
store invalid
entries

PFN	valid	prot
10	1	r-x
-	0	---
-	0	---
-	0	---
23	1	rw-
-	0	---
-	0	---
-	0	---
-	0	---
-	0	---
-	0	---
-	0	---
-	0	---
-	0	---
28	1	rw-
4	1	rw-

Solution #3

Main Idea: Multi-level paging

1. Break up the page table into fixed sized chunks
2. If all entries in a chunk are invalid, don't allocate the chunk

⇒ store in page directory

High-Level Example

Given:

- $|page| = 64 \text{ bytes}$
- $|virtual \text{ address space}| = 16 \text{ KB}$ $2^{10} \cdot 16 = 2^{10} \cdot 2^4 = 2^{14}$
- $|page \text{ table entry}| = 4 \text{ bytes}$

Calculate:

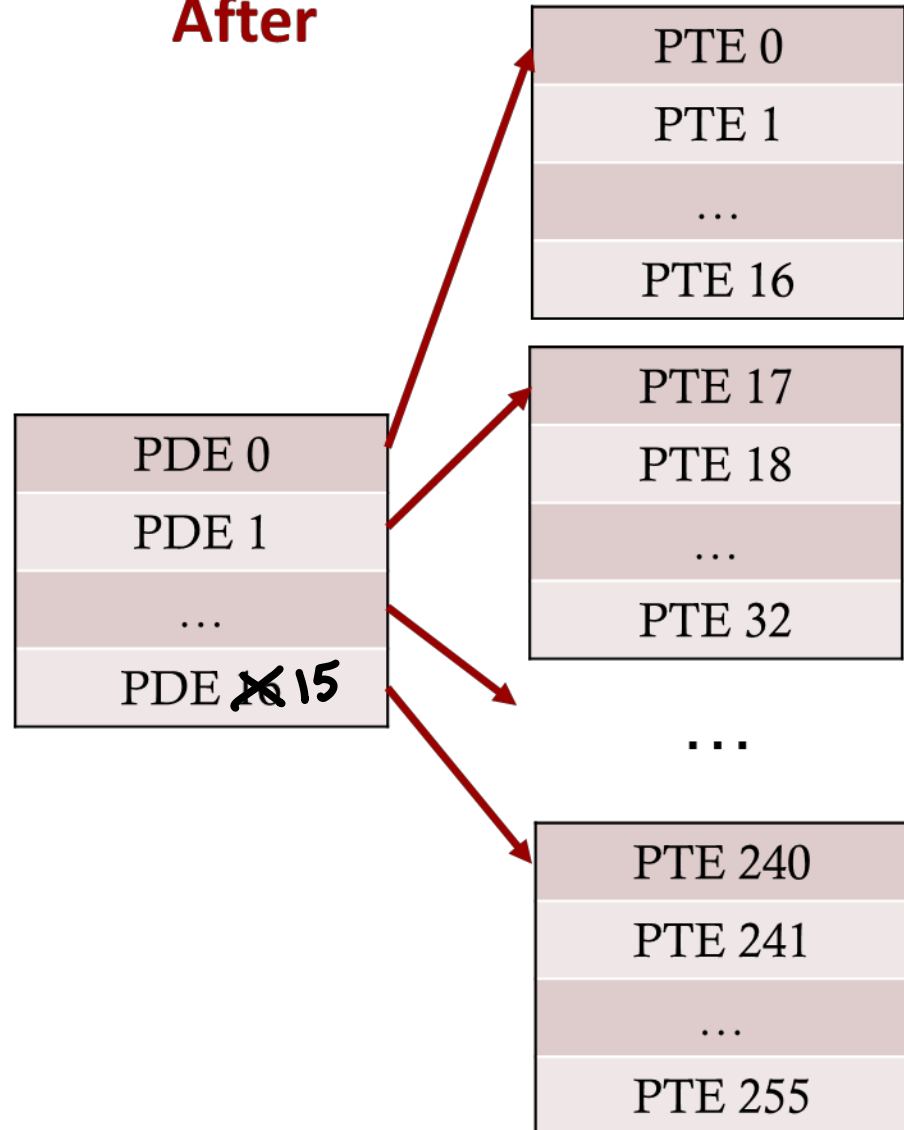
1. $|virtual \text{ address}| = ?$ $\log_2(16 \text{ KB}) = 14$
2. $|offset| = ?$ $\log_2(64 \text{ B}) = 6$
3. $|VPN| = ?$ $14 - 6 = 8$
4. $\# \text{ entries in page table} = ?$ $2^8 = 256$
5. $|page \text{ table}| = ? = 256 \cdot 4 \text{ B} = 1 \text{ KB}$
6. $\# \text{ chunks (pages)} = \frac{|page \text{ table}|}{|page|} = 16 \text{ pages} = \# \text{ entries in page directory}$

High-Level Example

Before

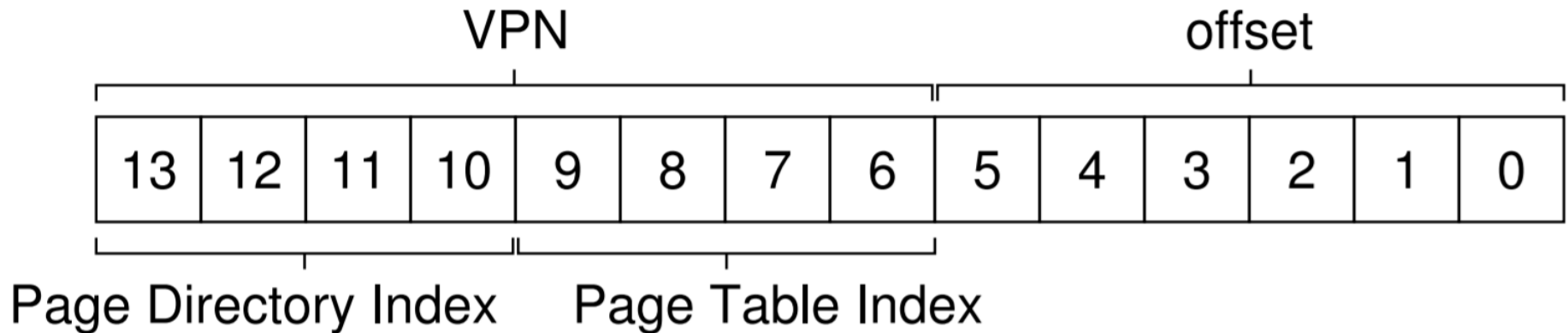
PTE 0
PTE 1
PTE 2
PTE 3
PTE 4
PTE 5
PTE 6
...
PTE 252
PTE 253
PTE 254
PTE 255

After

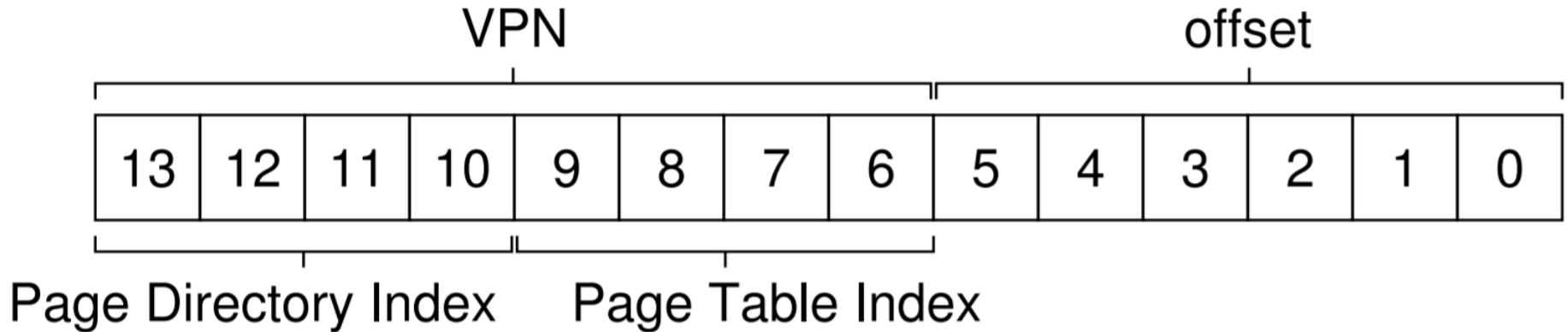


Address Translation #1

- $|\text{page directory}| = 16 \text{ entries} \Rightarrow \log_2(16) = 4 \text{ bits}$
- $|\text{page table pieces}| = 16 \text{ entries} \Rightarrow$



Address Translation #2



1. Check page directory
2. if valid = 1, keep looking, check next level
3. form physical address

Address Translation Visual

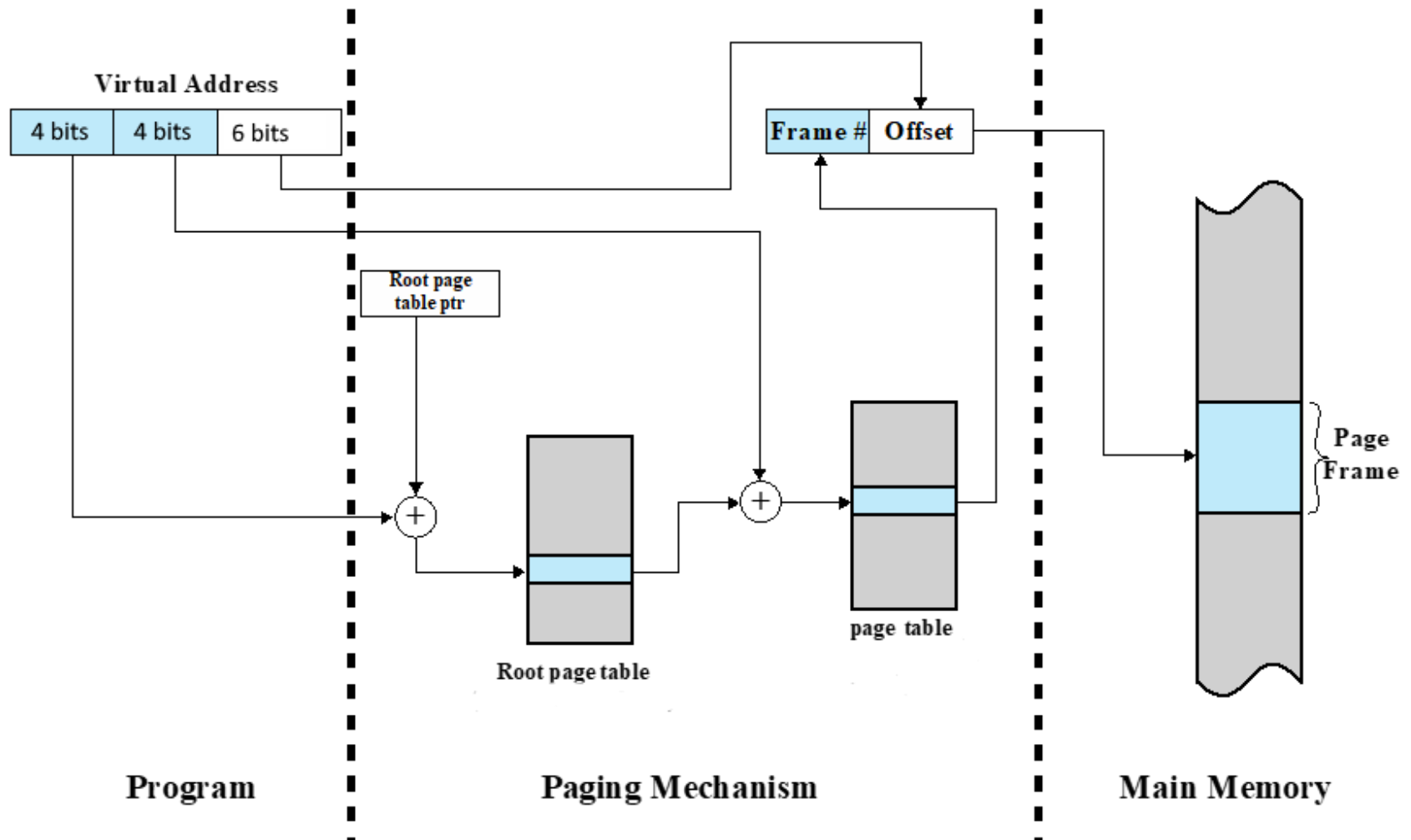


Figure 8.4 Address Translation in a Two-Level Paging System

Address Translation Steps (w/ TLB)

1. form VPN
2. check TLB *translation lookaside buffer*
 - Hit *≈ 99%*
 - a) check protection bits
 - b) if good → form phys address
 - Miss
 - a) form address of page directory entry (PDE)
 - b) *fetch PDE*
 - c) if valid → form addr of PTB
 - d) *fetch PTB*
 - e) check valid & protect bits
 - f) if good → form phys address & update TLB
3. fetch phys address

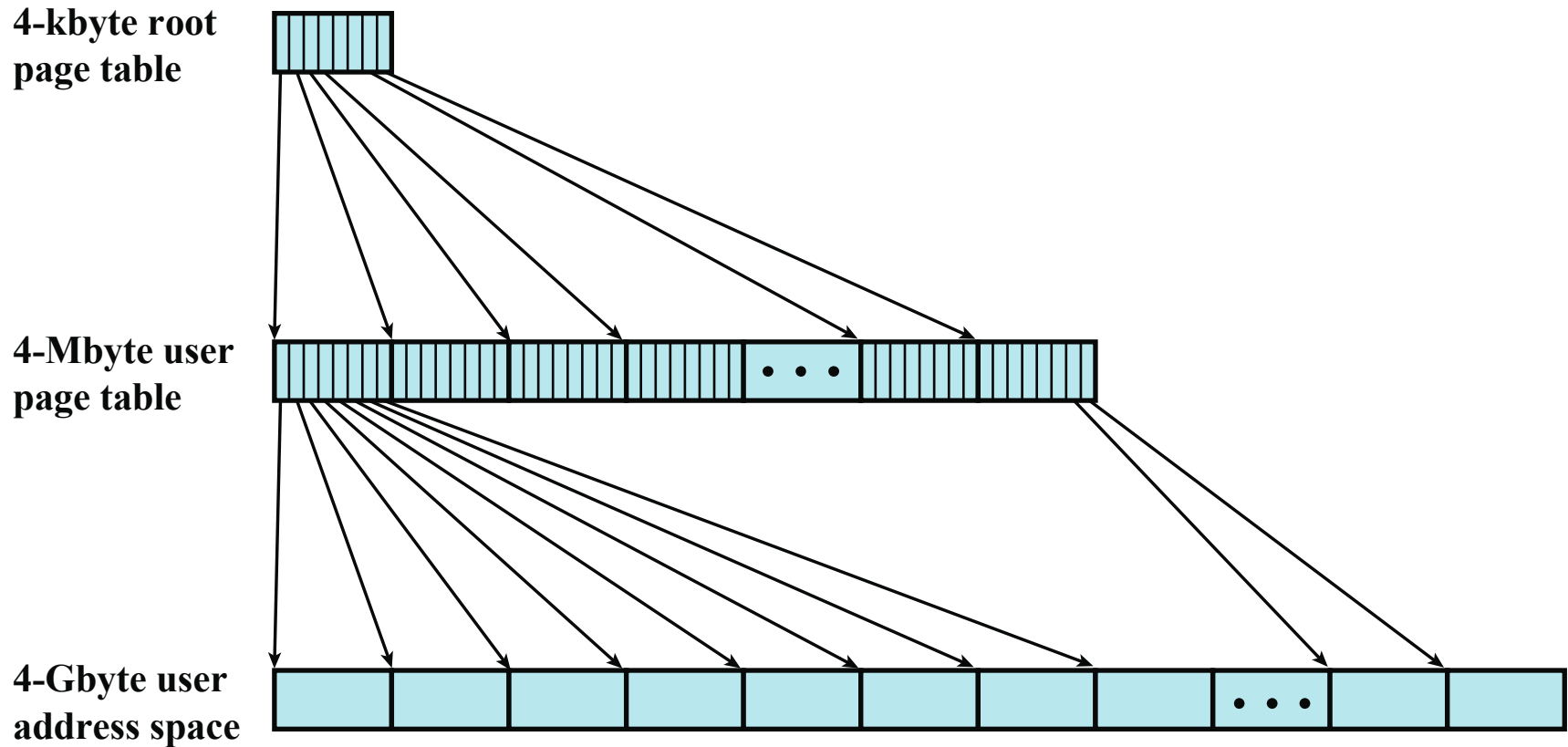
*increased
miss penalty*

We're Not Done Yet!

So far, we've assumed only *two* levels:

1. page Directory
2. pieces of page table
 \Rightarrow do this again?

Three-Levels Visual



Solution (3) Analysis

+ extremely space efficient

- increased penalty of TLB misses

x86! does this
(realworld)

Solution (4)

Inverted Page Table: (Hash table)

- One page table, total
 - Index by frame number
 - Hash (VPN) \longrightarrow PFN (index of PTE)
- VPNs are not globally unique! unique per proc.
- 1) Hash (VPN, pid) \mapsto PFN (ind of PTE)
- 2) store proc id in page table & "chain"

4) form phys addr

Solution (4) Analysis

- + page table size is fixed
 - dependent on # of frames,
 - dependent on sz of phys mem
- Difficult to implement "sharing"
- Hash funct. must be implemented in hardware

powerpc uses
this

Solving Space: Summary

use a complex
data structure

Learning Group Time

(Maybe)