-- - 1

An Overview of the Risk Posed by Thermal Neutrons to the Reliability of Computing Devices

Daniel Oliveira, Sean Blanchard, Nathan DeBardeleben, Fernando F. dos Santos, Gabriel Piscoya Dávila, Philippe Navaux, Stephen Wender, Carlo Cazzaniga, Christopher Frost, Robert Baumann, Paolo Rech

Abstract—The high performance, high efficiency, and low cost of Commercial Off-The-Shelf (COTS) devices make them attractive also for applications with strict reliability constraints. Today, COTS devices are adopted in HPC and safety-critical applications such as autonomous driving. Unfortunately, we cannot assume that COTS chips manufacturing process does not include the cheap natural Boron, that could makes them highly susceptible to thermal (low energy) neutrons.

Through radiation beam experiments, using high-energy and low-energy neutrons, it has been shown that thermal neutrons are a significant threat to COTS device reliability. The evaluation includes AMD APU, three different NVIDIA GPUs, an Intel accelerator, and an FPGA executing a relevant set of algorithms. Besides the sensitivity of the devices to thermal neutrons it is also fundamental to consider the thermal neutron flux in different scenarios such as weather, concrete walls and floors, or even HPC liquid cooling systems. Correlating beam experiments and neutron detector data, it is shown that thermal neutrons FIT rate could be comparable or even higher than the high energy neutron FIT rate.

I. Introduction

Commercial Off-The-Shelf (COTS) devices are designed and produced to improve performances and efficiency at the lowest possible cost. Reliability is of second importance, as long as the quality of service is sufficient for the average user. Building a device to the highest achievable levels of reliability conflicts with the low margins of the markets that consume these parts. Most consumers of COTS parts are primarily interested in performance and low price and would not understand a higher prize in exchange for higher reliability. The COTS part is suppose to be intrinsically sufficiently reliable, in other words, reliability is not seen a feature but an intrinsic characteristic [1], [2].

On the other hand, reliability is one of the most important characteristics for devices in the field of High Performance Computing (HPC) and safety-critical applications [3], [4], [5]. As an unreliable system can negatively affect not only the throughput of a computer but also the correctness of operations, it is fundamental to increase reliability through redundancies in improved manufacturing processes, chip architectures, transistor layout changes, or other software/hardware hardening solutions [1]. This added reliability clearly comes at an added cost in terms of engineering, more costly manufacturing, and increased power consumption. Only specialized safety critical industries, such as aerospace or medical, are today willing to pay the additional cost of highly reliable parts. The HPC community is forced to build systems using COTS parts, because of its strict performance and power

consumption constrains, forcing a constant struggle between the drive for ever increasing efficiency and the potential of lower scientific productivity due to lower reliability [6]. The automotive market is also peculiar, as reliability must be paramount (although not seen as a feature by the consumer) but the competitiveness of the market forces the production cost to be as low as possible. The rising interest of autonomous vehicles, that require extremely high computing capabilities, exacerbates this paradox.

In this paper we review the latest discoveries and the challenges associated with the reliability risk to HPC systems and safety-critical applications that comes from high energy and thermal neutrons. We refer in particular, to [7], [8], where authors propose an experimental evaluation of the sensitivity of various devices to high energy and thermal neutrons as well as an estimation of the error rates in various applications scenarios. It is well known that ${}^{10}B$ has a large capture cross section for thermal neutrons and the resulting excited state of ¹⁰B decays into Lithium-7 and a 1.47 MeV alpha particle [1], [2]. This alpha particle, which has high energy. is known to be a threat for computing devices, as it can generate transient faults. It is just the presence of ^{10}B that increases significantly the susceptibility of the device to thermal neutrons, thus removing completely Boron or using depleted ¹¹B would solve the problem and guarantee the device to be immune to thermal neutrons. However, this solution would significantly increase the manufacturing cost. Such a cost increase is unjustified for COTS devices, for which reliability is not as important as performances, efficiency, and yield. Using a costly manufacturing process would make the device more reliable but most of the customers of COTS devices will not appreciate the difference and would not understand the increased product price. As these COTS devices are today used in many applications for which reliability is a critical issue, such as HPC servers and automotive applications, it is fundamental to understand the error rate induced by also thermal neutrons, without assuming that ^{10}B is absent. The details of how ^{10}B is used in modern chips are proprietary and not publicly available. The only way to evaluate Boron concentration in a chip, and the associated increased sensitivity to thermal neutrons, is through controlled radiation exposure. We studied the effects of high energy and thermal neutrons on modern computing devices executing a representative set of benchmarks.

As shown in [8], modern data centers contain large masses of materials that can potentially increase the flux of thermal neutrons, in the form of concrete slab floors, cinder block walls, and water cooling units. In order to accurately estimate the effects of thermal neutrons we deployed a neutron detector to measure the natural background rate variation due to materials used in a modern data center. The measurements reported in [8] indicate that these materials can increase the thermal neutron counts, and thus the COTS device's error rate, by as much as 20%. When dealing with a self-driven car, other aspects should be considered, as the humidity in the air and the fuel in the tank, both of which can increase the thermal neutron flux.

What is established is that COTS devices are to be considered vulnerable to thermal neutrons. For some devices, the probability for thermal neutrons to generate an error can be even higher than the probability due to high energy neutrons. The main contributions of our research are: (1) a methodology to experimentally evaluate the sensitivity of computing devices to high energy vs. thermal neutrons; (2) an estimation of the flux of thermal neutrons as affected by various materials, such as concrete walls and water; (3) the evaluation, based on both (1) and (2), of computing devices error rate due to thermal neutrons.

II. BACKGROUND AND RELATED WORKS

Radiation is a known cause of upsets in computers [9]. The interaction of particles, primarily neutrons for terrestrial machines, with transistors can reverse the value of the bits stored in memory or create current spikes in logic operations. These faults can create an undetected error known as Silent Data Corruption (SDC), or create a Detected Unrecoverable Error (DUE). It is well known that thermal neutrons can affect electronic devices [2], [10]; however, only devices containing ^{10}B are susceptible to thermal neutrons. Approximately 20% of naturally occurring Boron is ^{10}B with the rest primarily being ^{11}B . Depleted Boron, where the ^{10}B content is low, is expensive in large quantities and generally not used in COTS parts.

Recently, ^{10}B was found in the manufacturing process of COTS devices [11]. It is worth noting that ^{10}B presence does not depend on the technology node but on the quality of the manufacturing process (smaller transistors will have less Boron, but also less Silicon. The Boron/Silicon percentage is not necessarily reduced). As devices produced for the user market are now employed in HPC and safety-critical applications, we must expect ^{10}B to be present. Some previous work has studied the sensitivity of SRAM and FPGA devices to thermal neutrons [12], [13], [14]. Weulersse et al. [15] compared the error rates of some memories (SRAM, CLB, caches) induced by thermal neutrons, 60MeV protons, and 14MeV neutrons.

A. High Energy and Thermal Neutrons

High energy neutrons, or fast neutrons, are neutrons with energies that range from 1 to over 1,000 MeV are known to disturb the function of electronic devices and are considered a main cause of faults in terrestrial electronic devices [2], [1]. The flux of high energy neutrons in the atmosphere has been thoroughly studied since Hess' discovery [16], [17]. The

flux is known to vary across the surface, as a consequence of the earth's magnetic field, and increases exponentially with altitude, reaching a maximum at about 60,000 ft. Under normal solar conditions, the fast neutron flux is almost constant for a given latitude, longitude, and altitude.

Thermal neutrons, or slow neutrons, are low energy neutrons (lower than 0.5 eV), produced by the moderation of high energy neutrons in materials or the emission of neutrons from nuclear decay. The flux of thermal neutrons, in contrast to high energy neutrons, can be difficult to predict as it strongly depends on the environmental conditions as well the presence of other materials (primarily hydrogen containing) in the device's immediate surroundings (like concrete, water, a fuel tank, etc..) in addition to latitude, longitude, and altitude. Various authors have made calculations to evaluate thermal fluxes in realistic cases [10], [18], [19], [20]. As a result, when predicting the error rate caused by thermal neutrons, it is essential to measure rates in realistic settings.

We have built and deployed a neutron detector in order to have a precise understanding of the thermal neutron flux inside a representative data center. We measured the rates of thermal neutrons in the proximity of water, and demonstrate that cooling water, for instance, can increase the thermal neutron flux (and thus error rate) by up to 20%.

B. Supercomputer Cooling

One of the main challenges in designing HPC systems is the dissipation of heat. A modern supercomputer can push more than 750 watts per square foot which can easily overwhelm traditional cooling systems [21]. One notable and growing trend in data centers is the use of liquid cooling [22]. Eight of today's Top10 supercomputers use some form of liquid cooling [23]. These surrounding materials, as demonstrated in Section V, act as a moderator for neutrons energy and, thus, increase the thermal neutron flux.

C. Motivation

As mentioned, it is mainly the presence of ^{10}B in the manufacturing process that makes a device susceptible to thermal neutrons [11]. Reducing the amount of ^{10}B could reduce the sensitivity of the device to thermal neutrons accordingly and using purified Boron would make the device immune to thermal neutrons induced effect.

Nevertheless, the use of purified Boron increases the manufacturing process and, thus, the final product cost. Such an increased cost is unjustified for consumer electronics, as the (high energy or thermal) neutrons error rate is sufficiently low not to be considered a major concern for user applications (video editing, gaming, and so forth). Having a more expensive product to ensure high reliability is not appealing for the consumer and manufacturers are investing in improving performances and efficiency as well as in improving the yield.

Lately, applications for which reliability is indeed a major concern, as cloud computing, High Performance Computing, and automotive applications, have started to be powered by COTS devices. The choice of using COTS in these applications is dictated by the need of extremely high computational

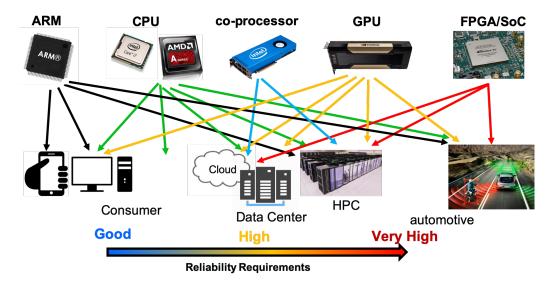


Fig. 1: High energy and thermal neutrons normalized cross sections for AMD APU and FPGA.

requirements with low power budget. The automotive market is a corner case. To implement an autonomous vehicle it is necessary to detect objects in real time, and this is normally achieved though Convolutional Neural Networks (CNNs) that are very computational demanding. Moreover, high computational efficiency is preferred in order not to exceed the vehicle power budget. Finally, the manufacturing cost is a highly sensible variable as the automotive market is highly competitive. As a result, the device selected to execute CNNs for autonomous vehicle must be efficient, with high performances, and low-cost as a COTS device. Nevertheless, reliability must be paramount, and this must include the thermal neutron component.

Figure 1 shows an abstract view of the current COTS devices market situation. There are various computing architectures available in the market, from low power ARM embedded processors to high end CPU, accelerators as coprocessors or GPUs, and programmable or application-specific devices (FPGAs or ASICs). Each of these devices has its own computing characteristics and cost. Most producers are willing to increase the yield by adopting the same architecture for various application domains, from consumer electronic, to cloud serves, HPC, and autonomous vehicles. Nevertheless, the strategy works only if the COTS device reliability is carefully evaluated and found to be sufficient for the project requirements.

 ^{10}B , which is the main topic of this paper, is one of the main variables in the reliability evaluation of COTS devices. As said, manufacturers do not have interest in using the more expensive purified Boron for their devices as this could put them in a weaker market position and reduce their yield. On the other hand, when the COTS device is employed as part of a project that has high reliability requirements it is mandatory to evaluate also its thermal neutrons induced error rate. We cannot assume that a device that was not produced to be highly reliable is ^{10}B free.

As mentioned, the second very important aspect of thermal

neutrons reliability evaluation, besides the presence of ^{10}B and the device sensitivity to thermal neutrons, is the thermal neutron flux. While the high-energy neutrons flux has been extensively studied and is assumed to be relatively constant (but dependent on the location), the thermal neutrons flux is extremely variable. Humidity, location, materials in proximity of the computing device (such as water, wood, concrete, gasoline, and so forth) are among the several factors that can significantly modify the thermal neuron flux and, then, the final FIT rate of the COTS device. As an example, when it rains the error rate of a device detecting objects in a car can be significantly higher than during a sunny day, in a supercomputer devices placed close to the water-cooling pipes can experience a higher fault rate than other nodes. It is the goal of this paper to understand also the variability of the error rate of devices based on some of these variables.

III. METHODOLOGY

In this section, we present the experimental methodology that should be used to measure the sensitivity of electronic devices to thermal and high energy neutrons. We describe the available neutron sources as well as the computing devices selected and the codes executed.

A. Devices

To evaluate the sensitivity of thermal and high energy neutrons it is fundamental to test various COTS devices. The devices selected should be used in all the different domains described in Section II-C. For the co-processor, explicitly manufactured for HPC and data centers, we tested an **Intel Xeon Phi**, built using a 22nm Intel's 3-D Tri-gate technology. We also tested two **NVIDIA GPUs** that are used in all domains: NVIDIA K20 manufactured in a 28nm TSMC CMOS technology, NVIDIA TitanX fabricated in a 16nm TSMC FinFET technology. An **AMD Accelerated Processing Unit (APU)**, manufactured in a 28nm SHP Bulk Process at Global Foundries is a hybrid device that can also be used in

all domains. The APU integrates CPU and GPU in the same chip. Finally, Zynq-7000 is the **FPGA** tested, fabricated in a 28nm TSMC technology.

B. Codes

The code selection needs to consider the devices in which they are going to be executed. They have a wide range of architectural and computational characteristics. Then, to have a fair evaluation, we selected codes that are efficient for each device, so we can reduce the bias in the reliability evaluation toward devices that are more efficient for the codes.

A matrix multiplication, LUD, LavaMD, and HotSpot were selected for Xeon Phi and GPUs. These codes are highly arithmetic codes that solve linear algebra and finite difference methods, which are executed efficiently in HPC devices. For APU, which is a heterogeneous device, we use SC, CED, and BFS that are made specifically for such devices. Finally, we also tested YOLO and MNIST to represent neural networks. These neural networks were tested in GPUs and FPGAs to evaluate the impact on self-driven vehicles.

C. Radiation Experiments Setup

The amount of ^{10}B involved in the manufacturing process is part of the industry sensitive data and is definitely not publicly available. Actually, the quantity of Boron can even vary from a batch of devices to another. That said, a customer can ask (paying) to the fab to reduce the amount of Boron or to use high quality products to significantly reduced the amount of ^{10}B . When evaluating the reliability of COTS devices for applications in which reliability matters, thermal neutrons should be considered. Radiation experiments are the only way to evaluate if the device meets the project reliability requirements considering also thermal neutrons. To achieve this evaluation it is necessary to expose the device to both high energy and thermal neutrons, comparing the sensitivity of the device to both kind of neutrons.

There are some facilities that allow to measure the realistic error rates of computing devices to high energy neutrons, such as the Los Alamos National Lab's Los Alamos Neutron Science Center in the US or the ChipIR facility of the Rutherford Appleton Lab in the UK. Thermal neutrons are used for physics of matter studies and there are not dedicated beam line for the test of electronic devices. However, as shown in [8], it is possible to adapt thermal neutrons facilities for the test of computing systems. Reactors, such as the ones available in nuclear power plants, are also excellent controlled sources for thermal neutrons.

D. Thermal Neutrons Detector

The measure of the flux of termal neutrons is very challenging, as it varies depending on the environmental conditions and on the material in the proximity of the device. In [8], we deployed Tin-II, which is a thermal neutron detector designed at LANL, to measure the actual thermal neutrons flux in certain conditions. Tin-II will be used to evaluate the thermal neutrons flux inside the Trinity supercomputer at LANL. We

used Tin-II to evaluate the effect of surrounding materials in modern data centers on thermal neutrons flux. We evaluated the impact of liquid cooling by counting thermal neutrons with and without a box containing 2 inches of water close to the detector. The count difference, shown in detail in Section V, indicates the water influence in the thermal neutrons flux.

IV. CROSS SECTION RESULTS

In this section, we show the average cross sections results from ChipIR and ROTAX experiments. The detailed results, including a study of the different trend for different algorithms, are presented in [8]. It is important to note that we used the same device and setup for both experiments. As we show, the thermal neutrons cross section is far from being negligible, which indicates the presence of ^{10}B in the silicon doping.

Figure 2 compares the sensitivity of high energy and thermal neutron cross sections. We divide the high energy cross section by the thermal neutron one, to provide the ratio between the cross sections. In other words, a cross section ratio of one implies that a device is as sensitive to thermal neutrons as to high energy ones; a ratio of 10.14, as for the SDCs on Xeon Phi means that, for that device, a high energy neutron has a 10.14x higher probability to generate an SDC than a thermal neutron. The higher the ration, the lower the sensitivity to thermal neutrons as compared to high energy neutrons.

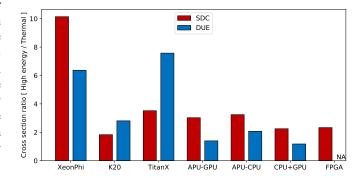


Fig. 2: Average cross section ratio for all devices.

For **Xeon Phi**, the ratio is 10.14x for SDCs and 6.37x for DUEs as shown in Figure 2. Thus, for each SDC caused by thermal neutrons, we have about 10 SDCs caused by high energy ones. This low sensitivity to thermal neutrons indicates that Xeon Phi uses little or depleted Boron in the manufacturing of the devices.

NVIDIA GPUs SDC ratio is about 2x to 3x for K20 and TitanX, respectively. For DUE, the difference is more substantial, with K20 presenting a ration of 3x while TitanX has a ratio of 7x. TitanX is manufactured using FinFET, while K20 still uses CMOS planar transistors, which may indicate that FinFET devices are less susceptible to thermal neutrons than CMOS ones.

The APU embeds a GPU and a CPU that can work simultaneously. We test the heterogeneous codes as executed on the GPU only, on the CPU only, and distributing concurrently 50% of the workload to the CPU and 50% to the GPU (CPU+GPU). The **AMD APU**, as shown in Figure 2, has a SDC ratio

similar to NVIDIA GPUs and a much worse DUE ratio. It is worth noting that when GPU is active, the DUE is even worse and about 1.18x for CPU+GPU. This GPU sensitivity to DUE may indicate that the mechanism responsible for communication and synchronism between CPU and GPU is particularly sensitive to thermal neutrons.

Finally, for **FPGA**, the SDC cross section ratio is 2.33x, indicating that for each thermal neutron SDC we observe about two high energy SDCs. Thus, similar to NVIDIA GPUs and AMD APU, the thermal neutron sensitivity is far from negligible and should not be neglected. It is worth noting that neutron-induced errors in the configuration memory of SRAM FPGAs have a *persistent* effect, in the sense that a corruption changes the implemented circuit until a new bitstream is loaded in the device. The observation of an error at the FPGA output indicates that the bitstream has probably been corrupted.

V. NEUTRON FLUXES DISCUSSION

The cross section, measured with beam experiments, represents the sensitivity of a device to thermal or high energy neutrons. However, to have an understanding of the actual error rate, one needs to consider the background radiation fluxes of high energy and thermal neutrons where the device will be located. Error rates are then calculated by multiplying the measured cross sections by the neutron fluxes. We report and discuss FIT rates in [8].

The flux for high energy neutrons in the atmosphere can be precisely estimated considering the altitude, longitude, latitude, and solar activity. However, the environment and the materials that surround a device significantly impact neutron flux and energy. For instance, the rain droplets of thunderstorms act as moderators slowing high energy neutrons into thermal ones. The thermal neutron flux, as measured in [10], can be $2\times$ higher during a thunderstorm than on a sunny day. Liquid cooling systems can also have the side effect of significantly increasing the proportion of thermal neutrons that hit a device.

For autonomous vehicles, it is even harder to estimate the thermal neutron flux since the environment can drastically change. For instance, the road material, weather condition, and how much fuel the vehicle has in the tank may impact the neutron flux. Besides, as humans are composed primarily of water (an excellent neutron moderator), the number of passengers will change the thermal neutron flux.

To empirically measure the impact of materials in the thermal neutron flux in a data center, we placed the Tin-II detector (details in Section III-D) in a building similar to the one containing the Trinity supercomputer. We collected data over the course of several days, then placed 2 inches of water in a box over the detector starting on 20^{th} April 2019. Figure 3 shows that when water is placed over the detector the thermal neutron counts abruptly increase of about 24%. This increase shows that the presence of water in the cooling system can significantly increase the rates of thermal neutrons in a system, which in turn will increase the rates in the devices sensitive to those neutrons as seen in section IV. Considering

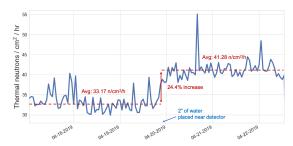


Fig. 3: Tin-II thermal neutron detector measurements with two inches of water placed over detector on 20^{th} April 2019.

only the liquid cooling and a concrete floor for a data center, we estimate that the thermal neutron contribution for the total FIT rate of a device can be as high as 40% [8].

In contrast to high energy neutrons, thermal neutrons flux can be effectively reduced, shielding the device with thin layers of cadmium or some inches of Boron plastic. However, cadmium is highly toxic and should not be heated and, then, it cannot be placed in the proximity of an HPC device or a cooling system. Boron plastic also thermally isolates the device, which makes it impractical to be used as a shield between the cooling system (one of the most efficient sources of thermal neutrons) and the device.

VI. CONCLUSIONS

In this work, we give an overview and some initial experimental results on the differences between high energy and thermal neutron sensitivity. We evaluate modern computing devices used in domains such as HPC to consumer and autonomous vehicles. We show that thermal neutron sensitivity is far from negligible for most COTS devices. For instance, the DUE caused by thermal neutrons is as probable as the DUE caused by high energy neutrons in the APU device.

We also discuss the neutron fluxes and how the surrounding material may increase the thermal neutron flux. We demonstrate through a thermal neutron detector that water from cooling systems can increase up to 20% the thermal neutron flux. Finally, we report in [8] that the thermal neutron contribution to the total error rate can be up to 40%.

ACKNOWLEDGEMENT

Authors would like to thank Gus Sinnis for their This support. precious help and work is based experiments performed thanks to the STFC on (DOI: 10.5286/ISIS.E.RB2000036 DOI: 10.5286/ISIS.E.RB1900122), and was partially sponsored by the Laboratory Directed Research and Development program of Los Alamos National Laboratory under project numbers: 20190499ER and 20180017ER, by CAPES/PVE - Finance Code 001, the EU H2020 Programme, and from MCTI/RNP-Brazil under the HPC4E project, grant agreement n 689772, and by the project FAPERGS 17/2551-0001 2020. Document approved for release with the code LA-UR-20-23268.

REFERENCES

- J. Ziegler and H. Puchner, SER-history, Trends and Challenges: A Guide for Designing with Memory ICs. Cypress, 2004.
- [2] R. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *Device and Materials Reliability, IEEE Transactions on*, vol. 5, no. 3, pp. 305–316, Sept 2005.
- [3] R. Lucas, "Top ten exascale research challenges," in DOE ASCAC Subcommittee Report, 2014.
- [4] A. Cohen, X. Shen, J. Torrellas, J. Tuck, Y. Zhou, S. Adve, I. Akturk, S. Bagchi, R. Balasubramonian, R. Barik, M. Beck, R. Bodik, A. Butt, L. Ceze, H. Chen, Y. Chen, T. Chilimbi, M. Christodorescu, J. Criswell, C. Ding, Y. Ding, S. Dwarkadas, E. Elmroth, P. Gibbons, X. Guo, R. Gupta, G. Heiser, H. Hoffman, J. Huang, H. Hunter, J. Kim, S. King, J. Larus, C. Liu, S. Lu, B. Lucia, S. Maleki, S. Mazumdar, I. Neamtiu, K. Pingali, P. Rech, M. Scott, Y. Solihin, D. Song, J. Szefer, D. Tsafrir, B. Urgaonkar, M. Wolf, Y. Xie, J. Zhao, L. Zhong, and Y. Zhu, "Interdisciplinary research challenges in computer systems for the 2020s," National Science Foundation, USA, Tech. Rep., 2018.
- [5] J. Dongarra, H. Meuer, and E. Strohmaier, "ISO26262 Standard," 2015.[Online]. Available: https://www.iso.org/obp/ui/#iso:std:iso:26262:-1: ed-1:v1:en
- [6] M. Snir, R. W. Wisniewski, J. A. Abraham, S. V. Adve, S. Bagchi, P. Balaji, J. Belak, P. Bose, F. Cappello, B. Carlson et al., "Addressing failures in exascale computing," *International Journal of High Perfor*mance Computing Applications, p. 1094342014522573, 2014.
- [7] D. Oliveira, S. Blanchard, N. DeBardeleben, F. F. dos Santos, G. P. Davila, P. Navaux, C. Cazzaniga, C. Frost, R. C. Baumann, and P. Rech, "Thermal neutrons: a possible threat for supercomputers and safety critical applications," in 25th IEEE European Test Symposium (ETS'20). IEEE, 2020.
- [8] D. Oliveira, S. Blanchard, N. DeBardeleben, F. F. dos Santos, G. P. Davila, P. Navaux, A. Favalli, O. Schappert, S. Wender, C. Cazzaniga, C. Frost, and P. Rech, "Thermal neutrons: a possible threat for supercomputer reliability." Springer, 2020.
- [9] JEDEC, "Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices," JEDEC Standard, Tech. Rep. JESD89A, 2006.
- [10] J. Dirk, M. E. Nelson, J. F. Ziegler, A. Thompson, and T. H. Zabel, "Terrestrial thermal neutrons," *IEEE Transactions on Nuclear Science*, vol. 50, no. 6, pp. 2060–2064, 2003.
- [20] R. Sheu and S. Jiang, "Cosmic-ray-induced neutron spectra and effective dose rates near air/ground and air/water interfaces in taiwan," *Health physics*, vol. 84, no. 1, pp. 92–99, 2003.

- [11] S.-J. Wen, S. Pai, R. Wong, M. Romain, and N. Tam, "B10 finding and correlation to thermal neutron soft error rate sensitivity for srams in the sub-micron technology," in 2010 IEEE International Integrated Reliability Workshop Final Report. IEEE, 2010, pp. 31–33.
- [12] S. Lee, I. Kim, S. Ha, C.-s. Yu, J. Noh, S. Pae, and J. Park, "Radiation-induced soft error rate analyses for 14 nm finfet sram devices," in 2015 IEEE International Reliability Physics Symposium, IEEE. IEEE, 2015, pp. 4B-1.
- [13] Y.-P. Fang and A. S. Oates, "Characterization of single bit and multiple cell soft error events in planar and finfet srams," *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 132–137, 2016.
- [14] P. Maillard, M. Hart, J. Barton, P. Jain, and J. Karp, "Neutron, 64 mev proton, thermal neutron and alpha single-event upset characterization of xilinx 20nm ultrascale kintex fpga," in 2015 IEEE Radiation Effects Data Workshop (REDW). IEEE, 2015, pp. 1–5.
- [15] C. Weulersse, S. Houssany, N. Guibbaud, J. Segura-Ruiz, J. Beaucour, F. Miller, and M. Mazurek, "Contribution of thermal neutrons to soft error rate," *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 1851–1857, 2018.
- [16] V. F. Hess, "Über den ursprung der durchdringenden strahlung," Z. Phys., vol. 14, p. 610, 1913.
- [17] J. F. Ziegler, "Terrestrial cosmic rays," *IBM Journal of Research and Development*, vol. 40, no. 1, pp. 19–39, Jan 1996.
- [18] A. Hands, P. Morris, K. Ryden, C. Dyer, P. Truscott, A. Chugg, and S. Parker, "Single event effects in power mosfets due to atmospheric and thermal neutrons," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 2687–2694, 2011.
- [19] R. Baumann, "Soft error characterization and modeling methodologies at texas instruments," in *Proc. Semiconductor Research Council 4th Topical Conf. Reliability.[CD-Rom] SemaTech CD-ROM.* USA: SemaTech, 2000, pp. 0043–3283.
- [21] M. K. Patterson and D. Fenwick, "The state of datacenter cooling," Intel Corporation White Paper. Available at http://download.intel.com/technology/eep/data-center-efficiency/stateofdate-center-cooling. pdf, 2008.
- [22] A. Capozzoli and G. Primiceri, "Cooling systems in data centers: state of art and emerging technologies," *Energy Procedia*, vol. 83, pp. 484–493, 2015.
- [23] J. Dongarra, H. Meuer, and E. Strohmaier, "TOP500 Supercomputer Sites: November 2018," 2018. [Online]. Available: http://www.top500.