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IMX219PQH5
Module Design Reference Manual v2.2

Mobile Imaging Business Division
Device Solution Business Group
Sony Corporation

- Chip Physical Information

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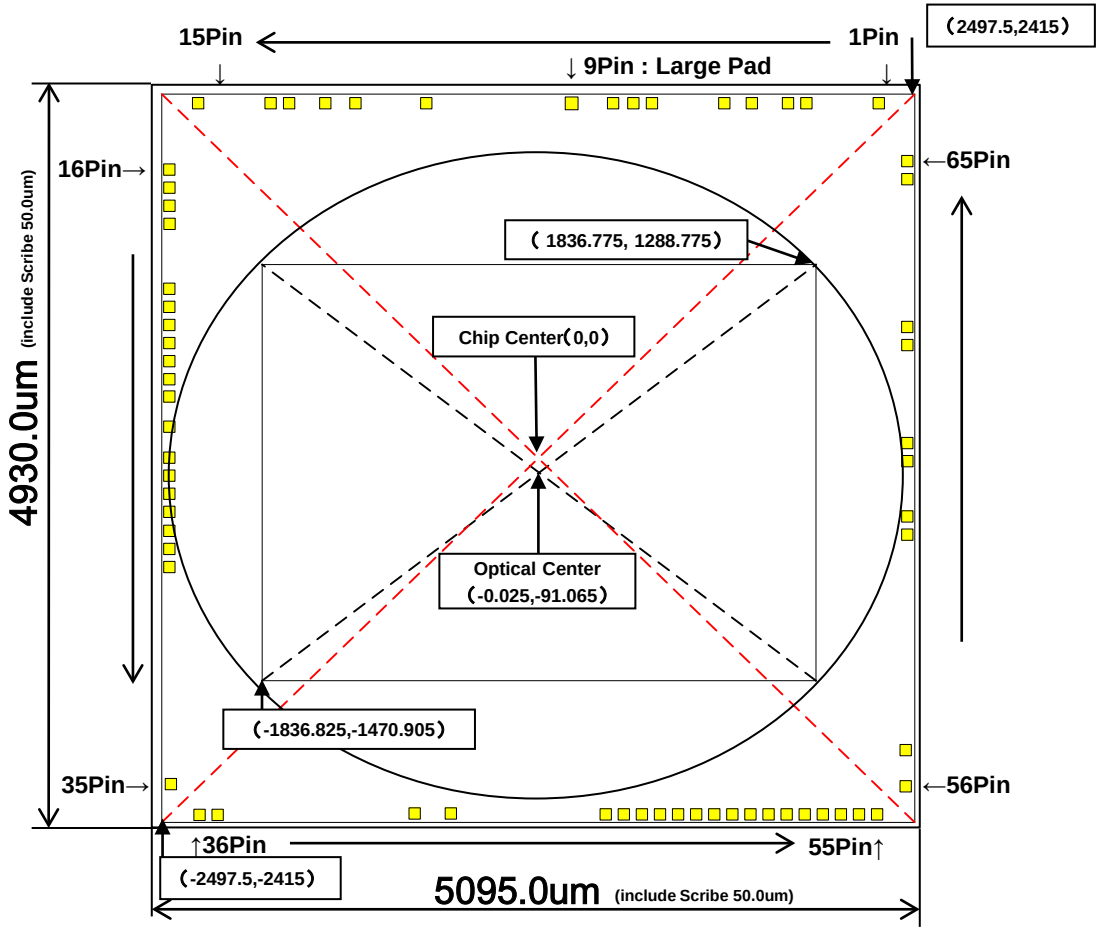
Excel file:IMX219ES_PADLocation_130523_0.xlsx

Chip size (after dicing) :5.070(H)X4.905(V) ±0.035 mm

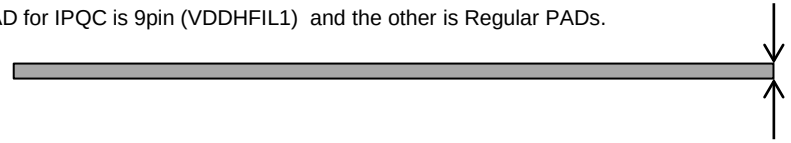
Chip thickness :0.150mm ±0.015 mm

2013/4/26					
No	Port name	Chip center origin		Chip left bottom side origin w/o scribe	
		Xcoordinate [um]	Ycoordinate [um]	Xcoordinate [um]	Ycoordinate [um]
right top corner					
1	VDDLSC1	2247.50	2355.00	4745.00	4770.00
2	VSSLSC1	1767.50	2355.00	4265.00	4770.00
3	VDDHCM1	1647.50	2355.00	4145.00	4770.00
4	VSSHCM1	1407.50	2355.00	3905.00	4770.00
5	VSSLCN1	1167.50	2355.00	3665.00	4770.00
6	VDDLCN1	687.50	2355.00	3185.00	4770.00
7	VSSLDM1	567.50	2355.00	3065.00	4770.00
8	VSSLSC2	447.50	2355.00	2945.00	4770.00
9	VDDHFIL1	167.50	2356.00	2665.00	4771.00
10	VDDLCN2	-727.50	2355.00	1770.00	4770.00
11	VSSLCN2	-1207.50	2355.00	1290.00	4770.00
12	VSSHCM2	-1407.50	2355.00	1090.00	4770.00
13	VDDHCM2	-1647.50	2355.00	850.00	4770.00
14	VSSLSC3	-1767.50	2355.00	730.00	4770.00
15	VDDLSC3	-2247.50	2355.00	250.00	4770.00
left top corner					
16	VCP	-2447.50	1915.00	50.00	4330.00
17	VBO	-2447.50	1795.00	50.00	4210.00
18	VSSHSN1	-2447.50	1675.00	50.00	4090.00
19	VDDHSN1	-2447.50	1555.00	50.00	3970.00
20	VSSLSC4	-2447.50	1125.00	50.00	3540.00
21	POREN	-2447.50	1005.00	50.00	3420.00
22	XCLR	-2447.50	885.00	50.00	3300.00
23	TENABLE	-2447.50	765.00	50.00	3180.00
24	GPO	-2447.50	645.00	50.00	3060.00
25	FSTROBE	-2447.50	525.00	50.00	2940.00
26	SDA	-2447.50	405.00	50.00	2820.00
27	SCL	-2447.50	205.00	50.00	2620.00
28	TEST1	-2447.50	5.00	50.00	2420.00
29	SWTCK	-2447.50	-115.00	50.00	2300.00
30	INCK	-2447.50	-235.00	50.00	2180.00
31	VDDMCO	-2447.50	-355.00	50.00	2060.00
32	VSSLSC5	-2447.50	-480.00	50.00	1935.00
33	VDDLSC5	-2447.50	-600.00	50.00	1815.00
34	VDDHFIL2	-2447.50	-726.00	50.00	1689.00
35	VDDLSC6	-2447.50	-2165.00	50.00	250.00
left bottom corner					
36	VSSLSC6	-2247.50	-2365.00	250.00	50.00
37	VSSLDM2	-2127.50	-2365.00	370.00	50.00
38	VDDLSC7	-807.50	-2365.00	1690.00	50.00
39	VSSLSC7	-567.50	-2365.00	1930.00	50.00
40	VDDLIO1	447.50	-2365.00	2945.00	50.00
41	VSSLIO1	567.50	-2365.00	3065.00	50.00
42	DMO1N	687.50	-2365.00	3185.00	50.00
43	DMO1P	807.50	-2365.00	3305.00	50.00
44	DMO2N	927.50	-2365.00	3425.00	50.00
45	DMO2P	1047.50	-2365.00	3545.00	50.00
46	VSSLIO2	1167.50	-2365.00	3665.00	50.00
47	DCKN	1287.50	-2365.00	3785.00	50.00
48	DCKP	1407.50	-2365.00	3905.00	50.00
49	VSSLIO3	1527.50	-2365.00	4025.00	50.00
50	DMO3N	1647.50	-2365.00	4145.00	50.00
51	DMO3P	1767.50	-2365.00	4265.00	50.00
52	DMO4N	1887.50	-2365.00	4385.00	50.00
53	DMO4P	2007.50	-2365.00	4505.00	50.00
54	VSSLIO4	2127.50	-2365.00	4625.00	50.00
55	VDDLIO2	2247.50	-2365.00	4745.00	50.00
right bottom corner					
56	VSSLSC8	2447.50	-2165.00	4945.00	250.00
57	VDDLSC8	2447.50	-1925.00	4945.00	490.00
58	VSSHPL	2447.50	-507.00	4945.00	1908.00
59	VDDHPL	2447.50	-387.00	4945.00	2028.00
60	TVCDSIN	2447.50	-20.00	4945.00	2395.00
61	TVMON	2447.50	100.00	4945.00	2515.00
62	VSSHAN	2447.50	750.00	4945.00	3165.00
63	VDDHAN	2447.50	870.00	4945.00	3285.00
64	VDDHSN2	2447.50	1850.00	4945.00	4265.00
65	VSSHSN2	2447.50	1970.00	4945.00	4385.00

- Chip Physical Information



※1 Actual size of a chip will be smaller than indicated when dicing (scribe) is taken into account
※2 Some PADs are located in image circle.
※3 Large PAD for IPQC is 9pin (VDDHFIL1) and the other is Regular PADs.



Thickness

150 um ± 15um

- Pin Information

Pin No.	Symbol	I/O	A/D	Description	Remarks
1	VDDLSC1	Power	D	1.2 V Power	
2	VSSLSC1	GND	D	1.2 V GND	
3	VDDHCM1	Power	A	2.8 V Power	
4	VSSHCM1	GND	A	2.8 V GND	
5	VSSLCN1	GND	D	1.2 V GND	
6	VDDLCN1	Power	D	1.2 V Power	
7	VSSLDM1			Dummy	NC
8	VSSLSC2	GND	D	1.2 V GND	
9	VDDHFIL1	Power	A	2.8 V Power	$=V_{ANA}$
10	VDDLCN2	Power	D	1.2 V Power	
11	VSSLCN2	GND	D	1.2 V GND	
12	VSSHCM2	GND	A	2.8 V GND	
13	VDDHCM2	Power	A	2.8 V Power	
14	VSSLSC3	GND	D	1.2 V GND	
15	VDDLSC3	Power	D	1.2 V Power	
16	VCP	O	A	Analog Output	connect to capacitor(2.2uF)
17	VBO	O	A	Analog Output	connect to capacitor(1.0uF)
18	VSSHSN1	GND	A	2.8 V GND	
19	VDDHSN1	Power	A	2.8 V Power	
20	VSSLSC4	GND	D	1.2 V GND	
21	POREN	I	D	Digital Input	Connect to VDIG
22	XCLR	I	D	Digital Input	
23	TENABLE	I	D	Digital Input	NC
24	GPO	O	D	Digital Output	
25	FSTROBE	O	D	Digital Output	
26	SDA	I/O	D	Digital Input/Output	
27	SCL	I	D	Digital Input	
28	TEST1	I	D	Digital Input	NC
29	SWTCK	I	D	Digital Input	NC
30	INCK	I	D	Digital Input	
31	VDDMCO	Power	D	1.8 V Power	
32	VSSLSC5	GND	D	1.2 V GND	
33	VDDLSC5	Power	D	1.2 V Power	
34	VDDHFIL2	Power	A	2.8 V Power	$=V_{ANA}$
35	VDDLSC6	Power	D	1.2 V Power	
36	VSSLSC6	GND	D	1.2 V GND	
37	VSSLDM2			Dummy	NC
38	VDDLSC7	Power	D	1.2 V Power	
39	VSSLSC7	GND	D	1.2 V GND	
40	VDDLIO1	Power	D	1.2 V Power	
41	VSSLIO1	GND	D	1.2 V GND	
42	DMO1N	O	D	Digital Output	
43	DMO1P	O	D	Digital Output	
44	DMO2N	O	D	Digital Output	
45	DMO2P	O	D	Digital Output	
46	VSSLIO2	GND	D	1.2 V GND	
47	DCKN	O	D	Digital Output	
48	DCKP	O	D	Digital Output	
49	VSSLIO3	GND	D	1.2 V GND	
50	DMO3N	O	D	Digital Output	
51	DMO3P	O	D	Digital Output	
52	DMO4N	O	D	Digital Output	
53	DMO4P	O	D	Digital Output	
54	VSSLIO4	GND	D	1.2 V GND	
55	VDDLIO2	Power	D	1.2 V Power	
56	VSSLSC8	GND	D	1.2 V GND	
57	VDDLSC8	Power	D	1.2 V Power	
58	VSSHPL	GND	D	2.8 V GND	
59	VDDHPL	Power	D	2.8 V Power	
60	TVCDSIN	I	A	Analog Input	NC , For test
61	TVMON	O	A	Analog Output	NC , For test
62	VSSHAN	GND	A	2.8 V GND	
63	VDDHAN	Power	A	2.8 V Power	
64	VDDHSN2	Power	A	2.8 V Power	
65	VSSHSN2	GND	A	2.8 V GND	

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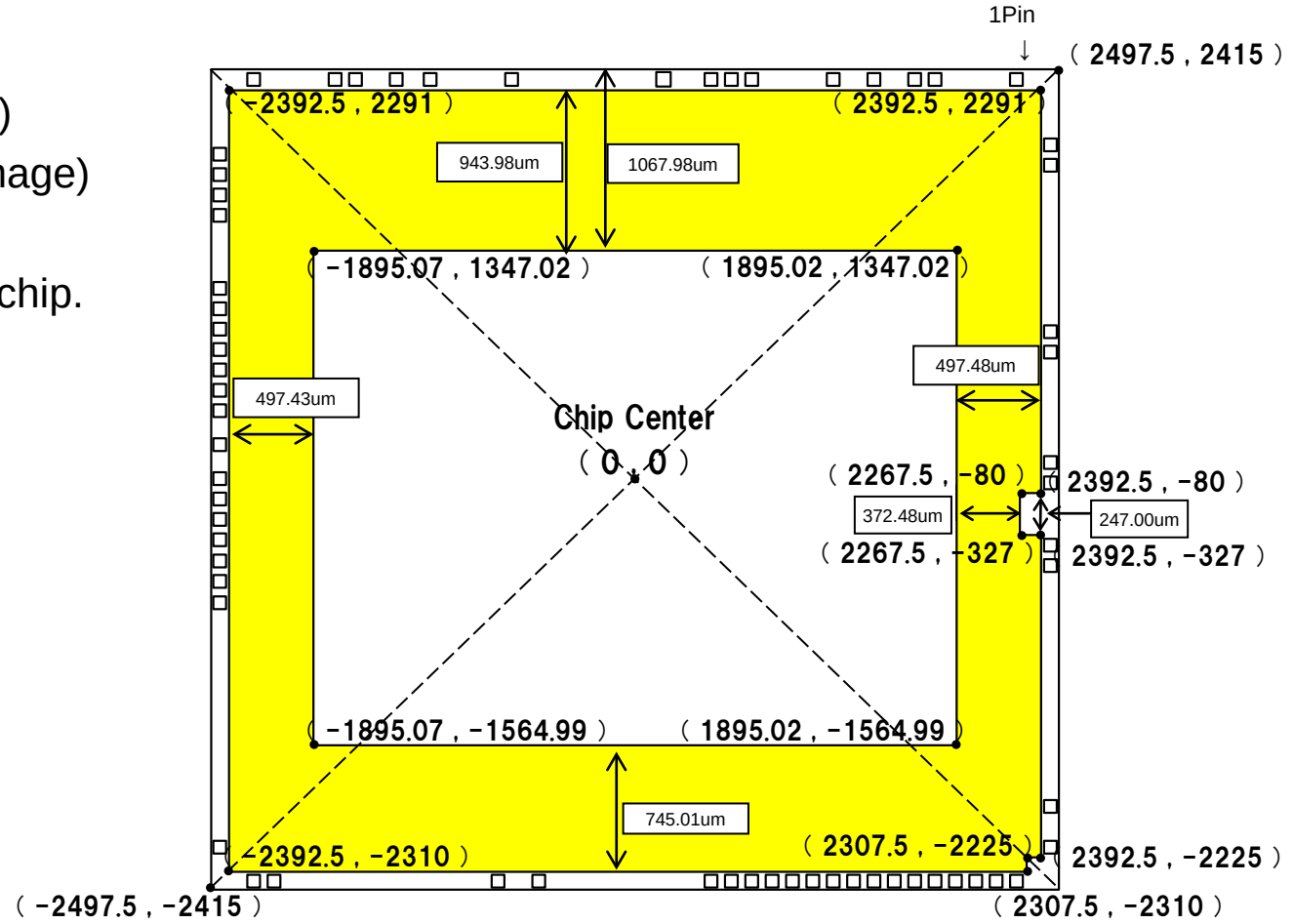
Undesirable Area for the Contact of Collet

-Edge of Chip (Dust generation)
-Unit Cell Area (Pixel damage)
-Die Pad (Electrostatic destruction)
-Around the Die Pad (Coating damage)

※Collet should not touch edge of chip.

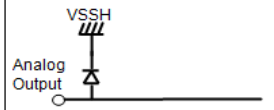
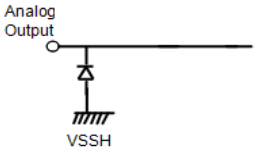
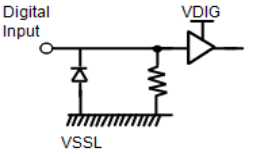
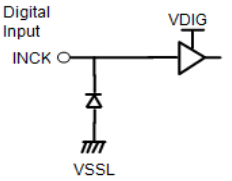
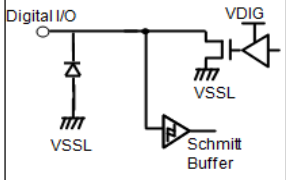
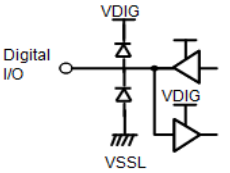
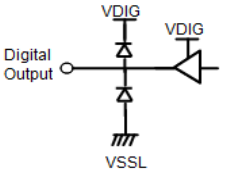
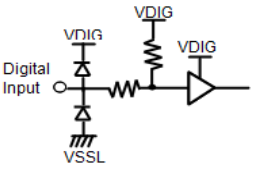
Possible Collet contact area



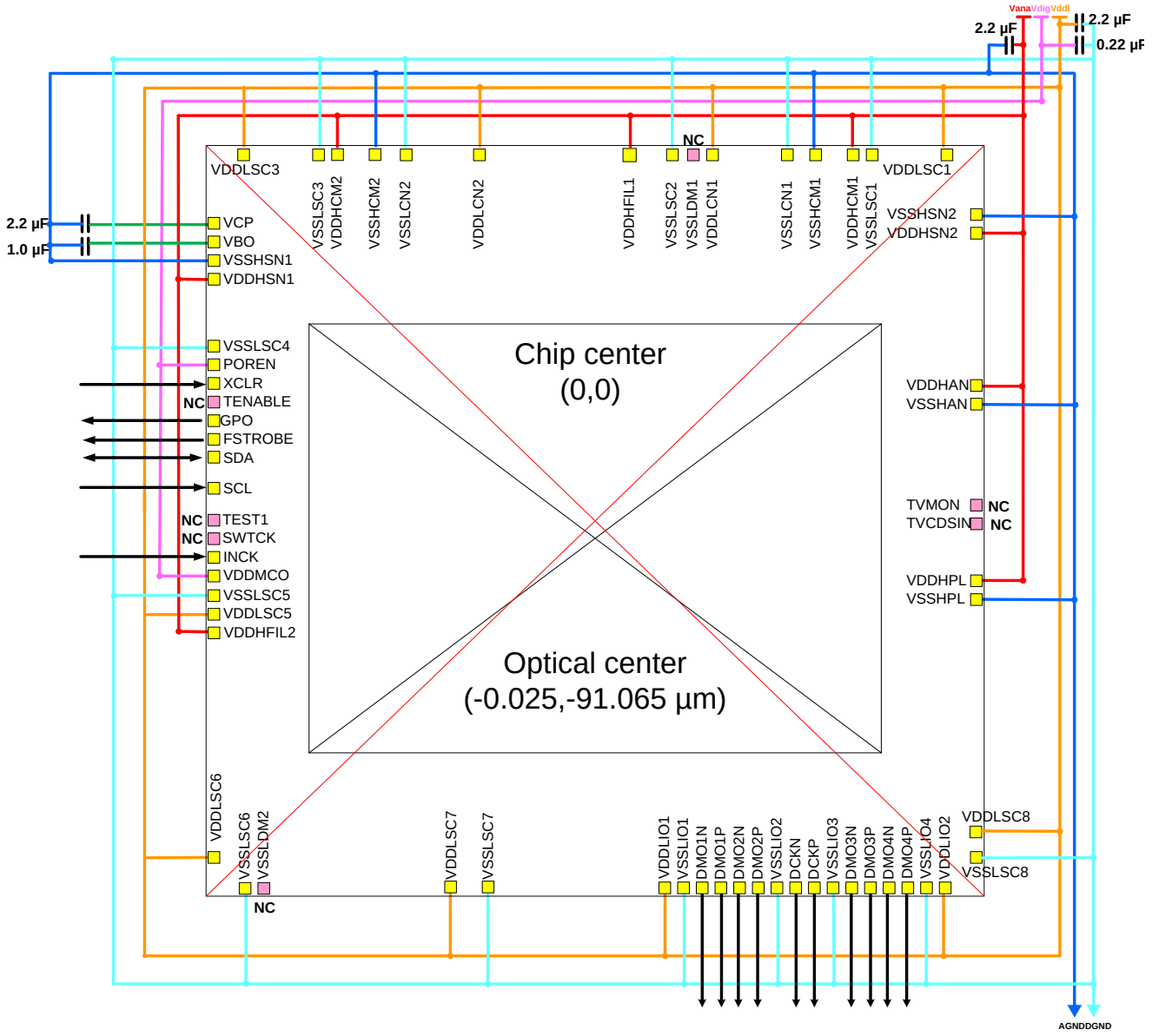
- Pin Status List

Name	Description of the purpose	Type (I, I/O, O)	Power off	HW STB	SW STB
DCKP	MIPI output (CLK+)	O	HiZ	Low	Low
DCKN	MIPI output (CLK-)	O	HiZ	Low	Low
DMO1P	MIPI output (Data+)	O	HiZ	Low	Low
DMO1N	MIPI output (Data-)	O	HiZ	Low	Low
DMO2P	MIPI output (Data+)	O	HiZ	Low	Low
DMO2N	MIPI output (Data-)	O	HiZ	Low	Low
DMO3P	MIPI output (Data+)	O	HiZ	Low	Low
DMO3N	MIPI output (Data-)	O	HiZ	Low	Low
DMO4P	MIPI output (Data+)	O	HiZ	Low	Low
DMO4N	MIPI output (Data-)	O	HiZ	Low	Low
VCP	Charge pomp output	O	HiZ	HiZ	-1.2V
VBO	Power supply output	O	HiZ	HiZ	High(2.8V)
GPO	General purpose output	I/O	HiZ	Low	HiZ (※1)
FSTROBE	Flash strobe	O	HiZ	HiZ	HiZ
SCL	I2C Clock	I/O	HiZ	HiZ	HiZ
SDA	I2C Data	I/O	HiZ	HiZ	Hiz
POREN	For Test(Connect to VDIG)	I	HiZ	High	High
INCK	Image sensor clock	I	HiZ	HiZ	HiZ
XCLR	Image sensor reset	I	Low	Low	High (1.8V)
TENABLE	NC , For test	I	HiZ	Low	Low
TEST1	NC , For test	I	HiZ	Low	Low
SWTCK	NC , For test	I	HiZ	Low	Low
TVCDSIN	NC , For test	I	HiZ	HiZ	HiZ
TVMON	NC , For test	O	HiZ	HiZ	HiZ
DVDD	Digital Power 0.95V	Power	HiZ	High(1.2V)	High(1.2V)
IOVDD	I/O Power 1.8V	Power	HiZ	High(1.8V)	High(1.8V)
AVDD	Analog Power 2.8V	Power	HiZ	High(2.8V)	High(2.8V)
AGND	Analog GND	GND	AGND	AGND	AGND
DGND	Digital GND	GND	DGND	DGND	DGND

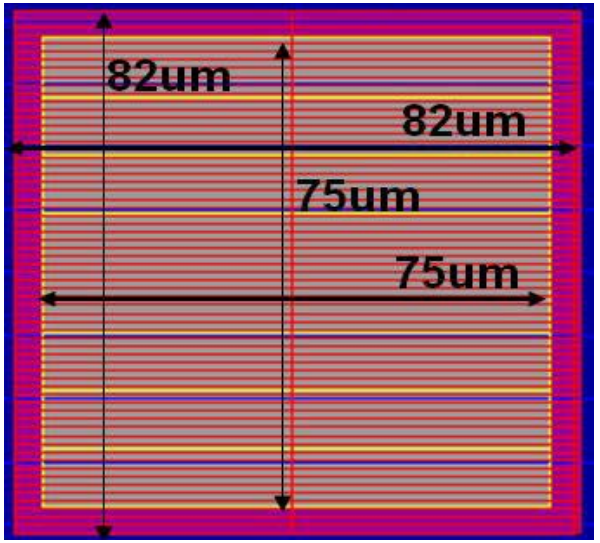
※1: Please connect to GND , when GPO function is not enable.

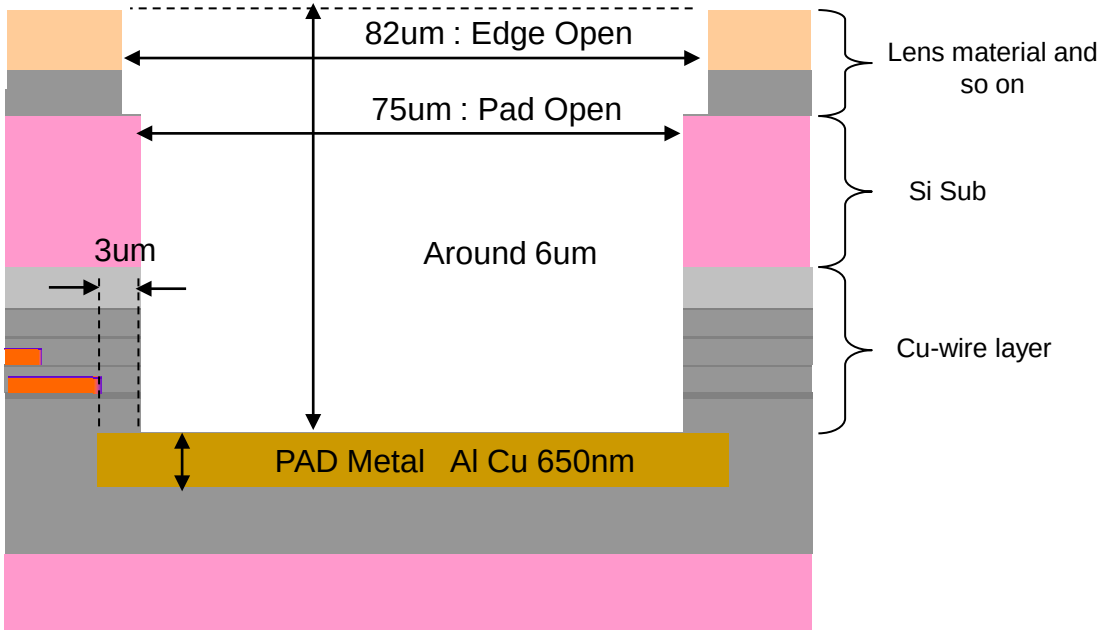
Symbol	Equivalent circuit	Symbol	Equivalent circuit
VCP		VBO	
XCLR		INCK	
SDA SCL		GPO	
FSTROBE		POREN	

VDDH: 2.8 V power supply, VDIG: 1.8 V power supply, VDDL: 1.2 V power supply
VSSH: 2.8 V GND, VSSL: 1.2 V GND


Vana Vdig Vddl
2.2 µF
2.2 µF
0.22 µF
NC
VDDLSC3
VDDLSC1
VSSLSC3
VDDHCM2
VSSHCM2
VSSLCN2
VDDLCN2
VDDHFIL1
VSSLSC2
VSSLDM1
VDDLCN1
VSSLCN1
VSSHCM1
VDDHCM1
VSSLSC1
2.2 µF
1.0 µF
VCP
VBO
VSSHSN1
VDDHSN1
VSSHSN2
VDDHSN2
VSSLSC4
POREN
XCLR
NC TENABLE
GPO
FSTROBE
SDA
SCL
NC TEST1
NC SWTCK
INCK
VDDMCO
VSSLSC5
VDDLSC5
VDDHFIL2
Chip center
(0,0)
Optical center
(-0.025,-91.065 µm)
VDDHAN
VSSHAN
TVMON NC
TVCDSIN NC
VDDHPL
VSSHPL
VDDLSC6
VSSLSC6
VSSLDM2
NC
VDDLSC7
VSSLSC7
VDDLIO1
VSSLIO1
DMO1N
DMO1P
DMO2N
DMO2P
VSSLIO2
DCKN
DCKP
VSSLIO3
DMO3N
DMO3P
DMO4N
DMO4P
VSSLIO4
VDDLIO2
VDDLSC8
VSSLSC8
AGNDDGND

- PAD Structure

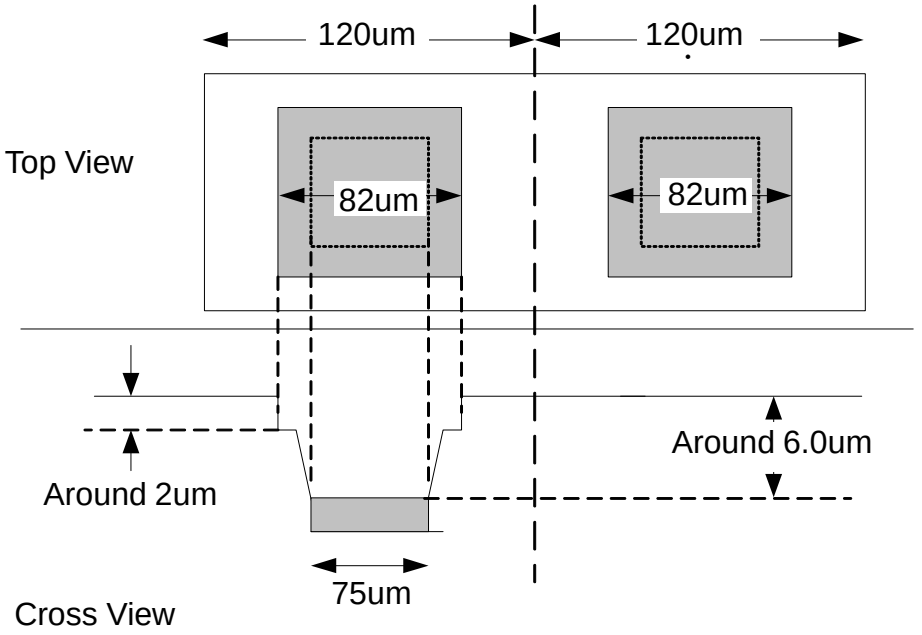




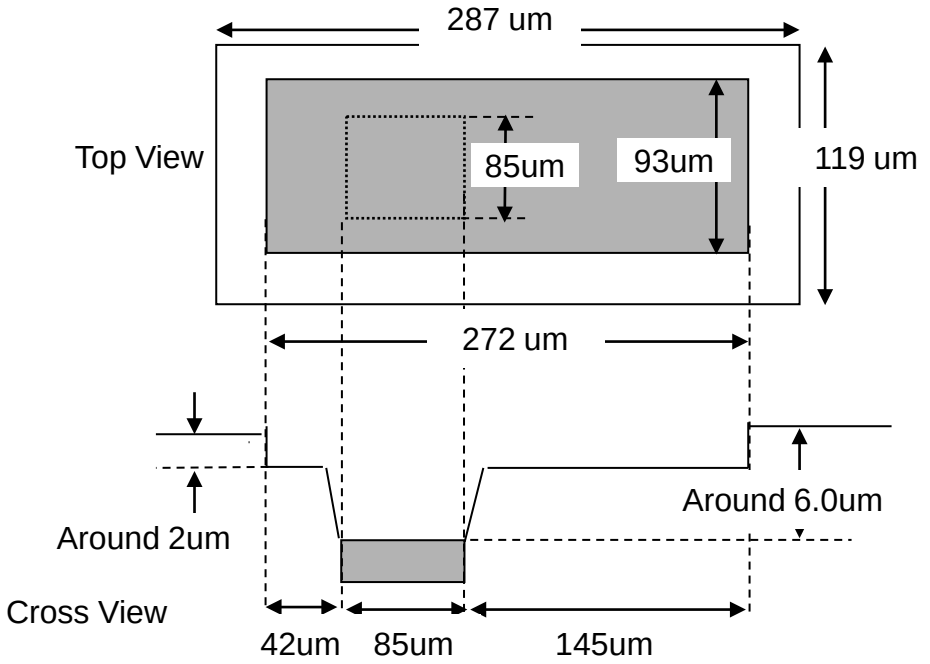
■ : Edge between PAD metal and TOP lens layer
■ : PAD open metal zone

- Pad structure

【Regular Pad】



【IPQC Pad】



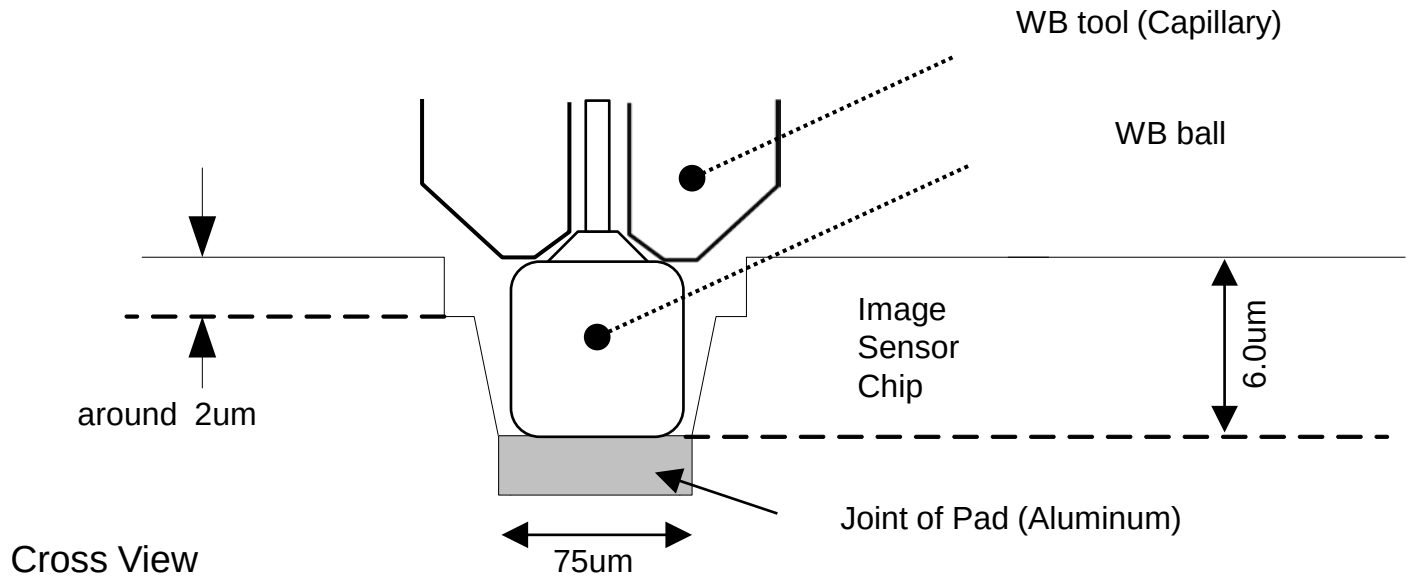
- Sony recommend to adjust the shape of bonding ball, because of the depth of Pad.

- IMX219 has one IPQC Pad. (9pin, VDDHFIL1)
- It is useful to check share strength. But it is not representative the other PAD's share strength, because it is depend on module bender's applied condition.

Since the distance from "Joint of PAD" (Aluminum) to surface of Image sensor chip is deep. Please pay attention to choose appropriate WB tooling and the condition.

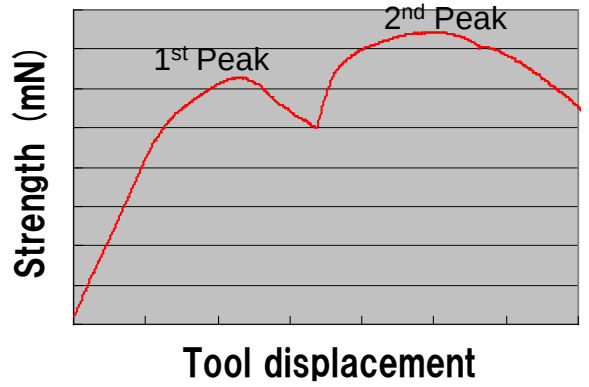
For example :

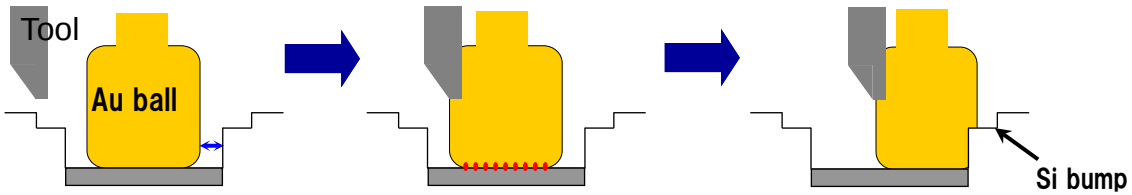
1) **WB tooling(Capillary)**
2) **Diameter and thickness for WB ball**



When measuring share strength, there is possibility that 2nd peak becomes higher than 1st peak related to the depth of PAD. 1st peak shows strength of joint and 2nd peak shows strength at pinching Au ball between tool and PAD wall that is placed in the opposite side of measurement start point. If acquiring Max value of strength at measuring Share strength, there is possibility that the value is not proper strength of joint. So please check profile of Strength waveform-Tool displacement and take in the 1st peak as below illustration.

■Illustration of Strength waveform and double peaks



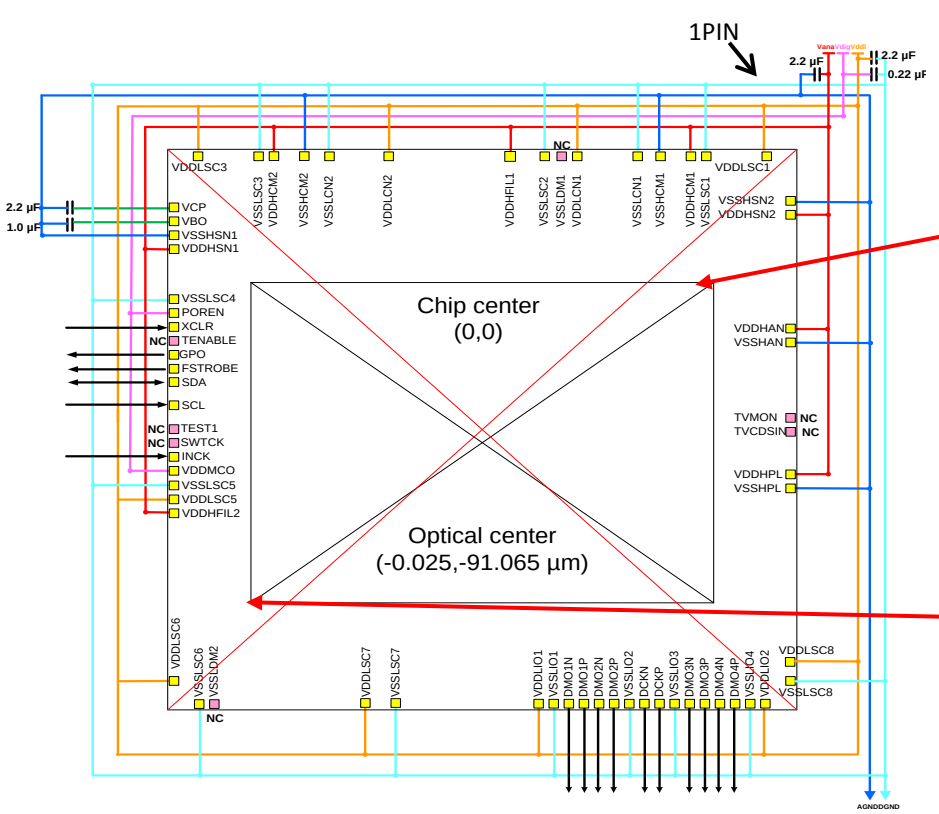


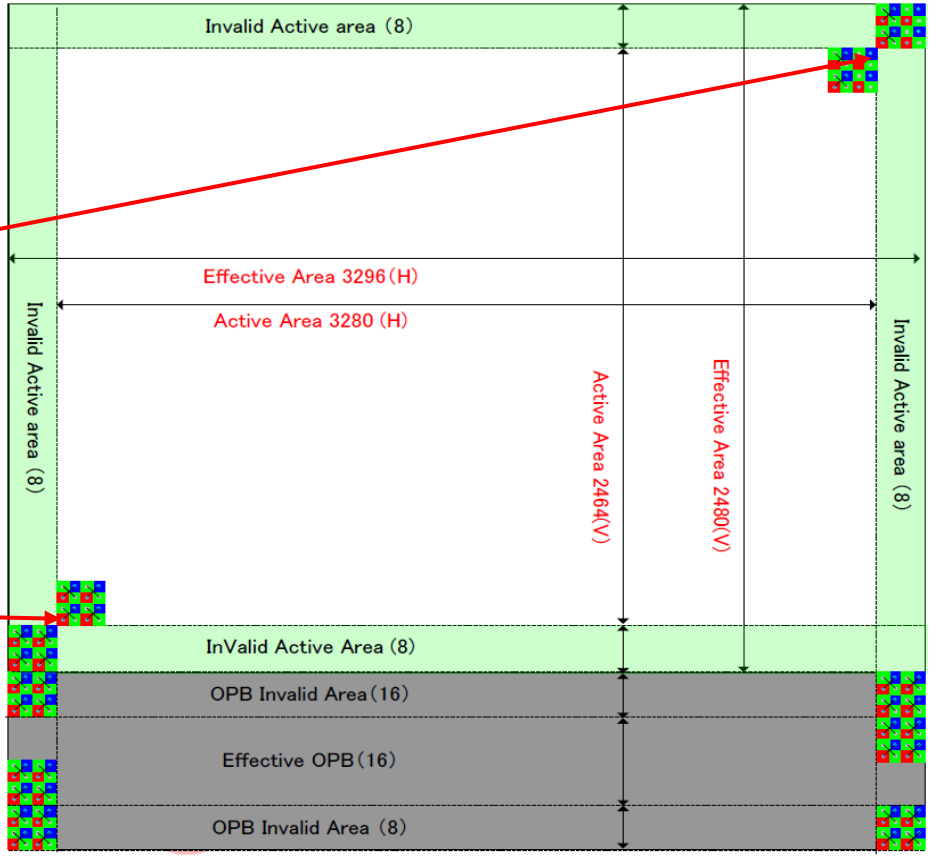
【before measurement】

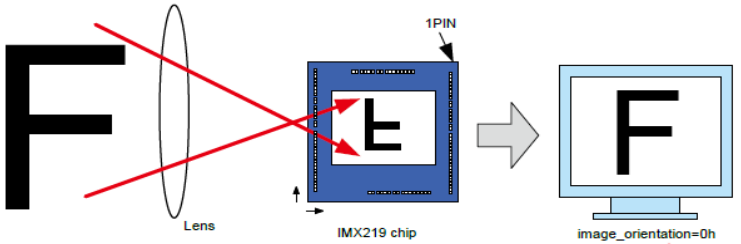
【1st Peak】
Strength of joint

【2nd Peak】
Strength at pinching Au ball between tool and PAD wall

- Pixel Array Information







(Datasheet)

10-1 Absolute Maximum Ratings

Table 40 Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage (analogue)	V_{ANA}	-0.3		3.3	V	
Supply voltage (Core)	V_{DDL}	-0.3		2.0	V	
Supply voltage (IF)	V_{DIG}	-0.3		3.3	V	
Input voltage	V_I	-0.3		3.3	V	
Output voltage	V_O	-0.3		3.3	V	
Operating temperature (function)	Topr	-20		60	°C	Junction temperature
Storage temperature	Tstg	-30		80	°C	Junction temperature
Performance guarantee temperature	Tspec	-20		60	°C	Junction temperature

10-2 Recommended Operating Conditions

Table 41 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage (analogue)	V_{ANA}	2.6	2.8	3.0	V	
Supply voltage (Core)	V_{DDL}	1.08	1.2	1.3	V	
Supply voltage (IF)	V_{DIG}	1.62	1.8	1.98	V	

- PSRR characteristics

PSRR [dB] is defined by the following equation.
It is to see level of pattern (seam) noise on the picture caused by ripple noises on power supplies (VANA/VDDL).

$$\mathrm{PSRR} = 20 \cdot \log_{10}\left(\frac{\sqrt{\sigma_a{}^2 - \sigma_b{}^2}}{\frac{V_{inpp}}{2\sqrt{2}}} \right)$$

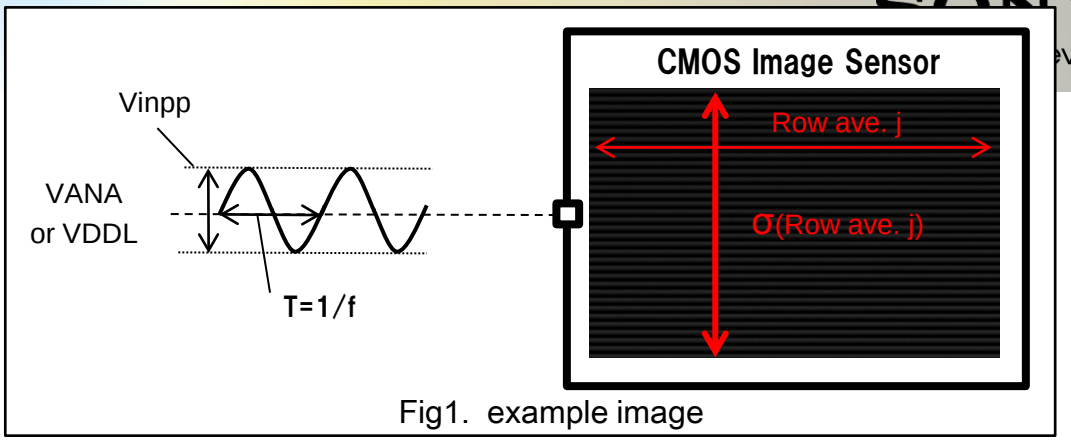


Fig1. example image

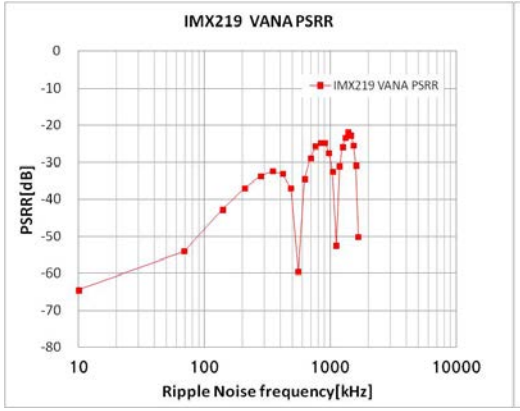
Where:

Vinpp: Peak to peak voltage of input ripple on analog or digital power supply

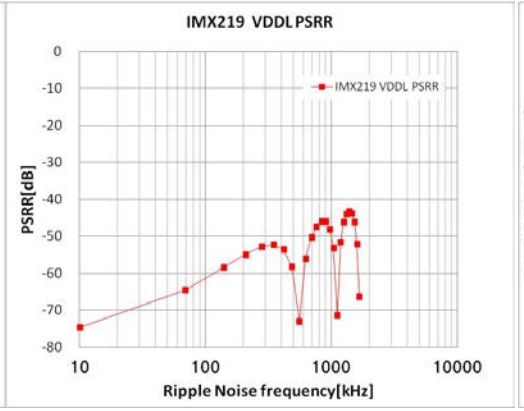
σa: Standard deviation of row averages at Gr pixels [Vrms] by capturing a frame which has ripple noises.

σb: Standard deviation of row average at Gr pixels [Vrms] by capturing a frame which has no ripple noises.

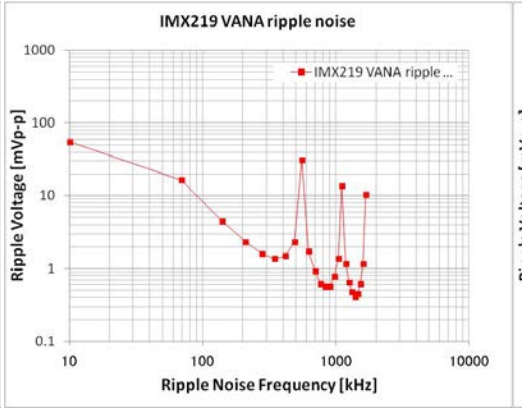
The following figures show typical performance level at measurement condition. PSRR is based on the measured value while the acceptable ripple noise plots are calculated using the measurement data. In this case acceptable noise level is set as 1/10 of random noise of the sensor. Please suppress power supply noise to level less than Vinpp-t.



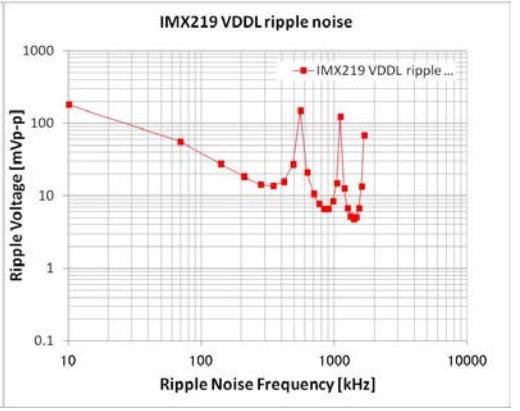
PSRR characteristic of VANA



PSRR characteristic of VDDL



Vinpp-t characteristic of VANA



Vinpp-t characteristic of VDDL

(Vinpp-t is the value that PSRR noise becomes a one-tenth of random noise)*

- Power Consumption

(Datasheet)

(V_{ANA} = 3.0 V, V_{DDL} = 1.3 V, V_{DIG} = 1.98 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Comment
Current consumption (Full,30 frame/s)	IVAVA_strm		33	38	mA	VTmax is max speed read out from pixel array CSI2 4 lanes, V_{ANA} current
	IVDDL_strm		100	160	mA	VTmax is max speed read out from pixel array CSI2 4 lanes, V_{DDL} current Defect Correction, L.S.C. function off
HW-Standby current	ISTB_ana			50	µA	XCLR = Lo, V_{ANA} current
	ISTB_dig			10	µA	XCLR = Lo, V_{DIG} current
	ISTB_Iddl			50	µA	XCLR = Lo, V_{DDL} current

Note) Measurement conditions

- Power Consumption on each mode (Reference data)

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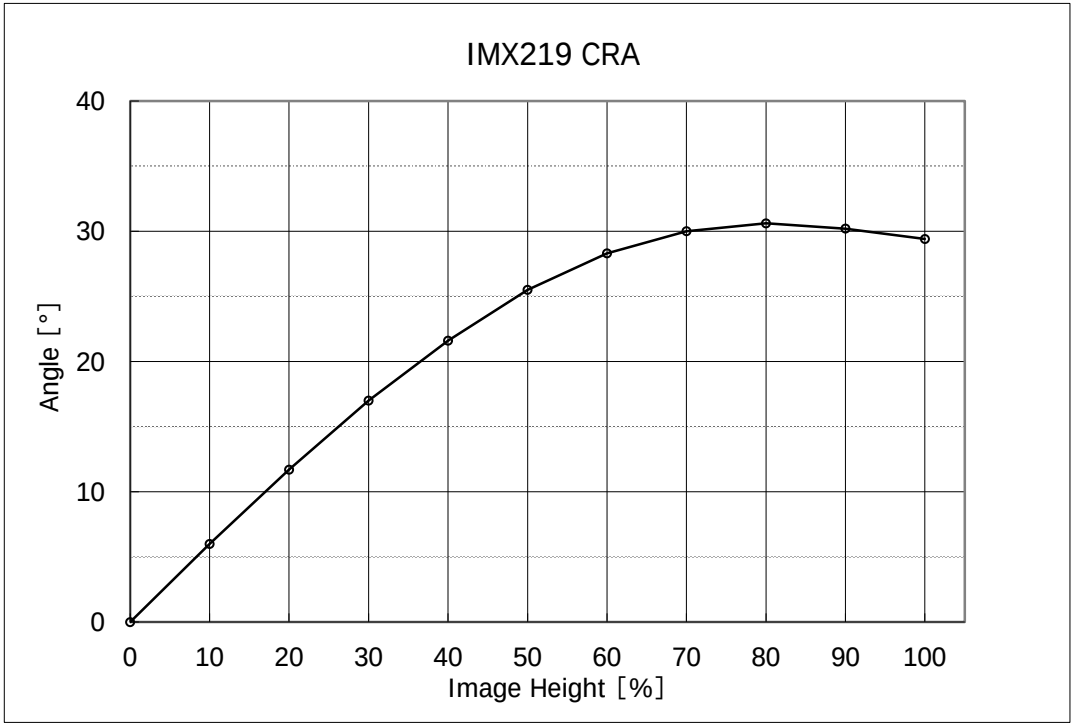
			#1	#2	#3	#4	#5	#6	#7
			Max 4:3	Max 16:9	2x2binned 16:9	4x4binned 16:9	1080p	720p	Max 4:3 2lane
Video Timing (In)			3280x2464	3280x1844	1640x920	820x460	1920x1080	1408x792	3280x2464
Sensor Resolution (Out)			3280x2464	3280x1844	3280x1840	3280x1840	1920x1080	2816x1584	3280x2464
Max Frame Rate			30fps	30fps	120fps	120fps	60fps	180fps	21fps
Data Format			RAW10	RAW10	RAW10	RAW10	RAW10	RAW10	RAW10
Input Clock Frequency			12MHz	12MHz	12MHz	12MHz	12MHz	12MHz	12MHz
VT_PLL			702MHz	702MHz	702MHz	702MHz	702MHz	702MHz	456MHz
VT_PIX			140.4MHz	140.4MHz	140.4MHz	140.4MHz	140.4MHz	140.4MHz	91.2MHz
Row Time (or LLPCK)			(10b)	(10b)	(10b)	(10b)	(10b)	(10b)	(10b)
ADC Resolution			10bit	10bit	10bit	10bit	10bit	10bit	10bit
MIPI lanes			4	4	4	4	4	4	2
MIPI Speed (/lane)			726Mbps	726Mbps	726Mbps	726Mbps	726Mbps	726Mbps	912Mbps
Typical meas. Condition (*)	VANA	mW	84.25	67.42	88.36	104.53	78.06	107.74	85.64
	VDIG	mW	0.03	0.03	0.03	0.03	0.03	0.03	0.03
	VDDL	mW	113.03	96.73	96.61	100.15	101.81	108.63	95.67
Total		mW	197.31	164.18	185.00	204.71	179.89	216.40	181.34

* Typical meas. Condition : VANA=2.8V, VDIG=1.8V, VDDL=1.2V, Tj = 25℃

- CRA Characteristics of Recommended Lens

Image Height		Target CRA (degree)
[%]	[mm]	
0.0	0.00	0.0
10.0	0.23	6.0
20.0	0.46	11.7
30.0	0.69	17.0
40.0	0.91	21.6
50.0	1.14	25.5
60.0	1.37	28.3
70.0	1.60	30.0
80.0	1.83	30.6
90.0	2.06	30.2
100.0	2.29	29.4



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General description

This document describes shading characteristics of the image senor for luminance (G) and chromaticity (B/G, R/G). The purpose of its usage is to visually and quantitatively know about performance shift (herein after referred as “ΔCRA” = Lens CRA – sensor CRA).

The luminance shading can be evaluated with the plot titled as “G” and the color shading can be evaluated with the plot “R/G” and “B/G”.

Based on this document , please judge whether the lens used by customer matches this image sensor.

However, minus (-) side shift of the lens CRA is generally less impact to the shading performance, please refer to the individual ΔCRA-Shading Performance plot for the final judgment.

- IMX219 ΔCRA - Shading Characteristics of “G” Pixel

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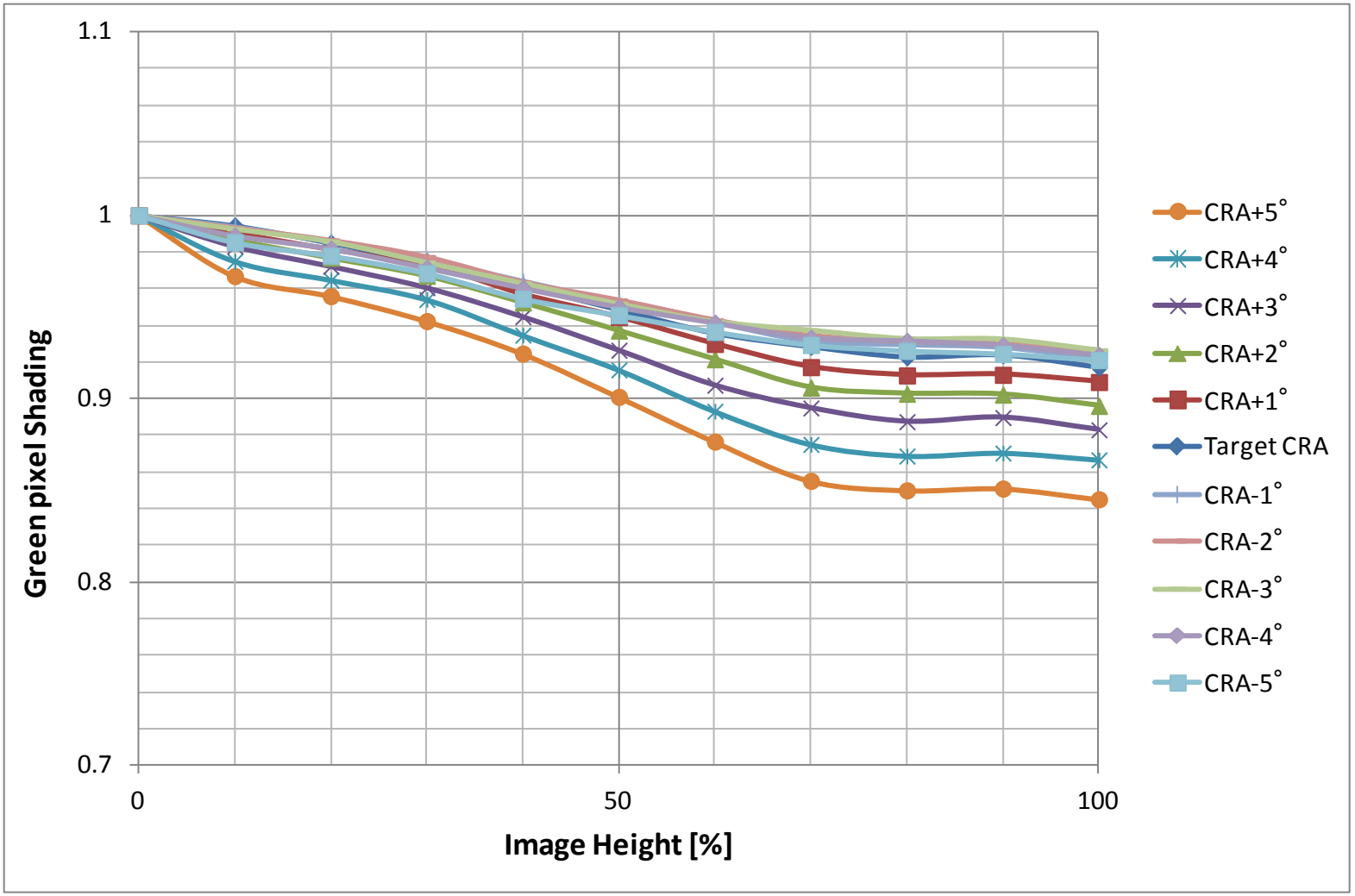
* Measurement with the white light source.



Note : In case of IMX219, minus(-) shift of ⊿CRA is much less risk than plus(+) side.

- IMX219 ΔCRA - Shading Characteristics of “B/G”

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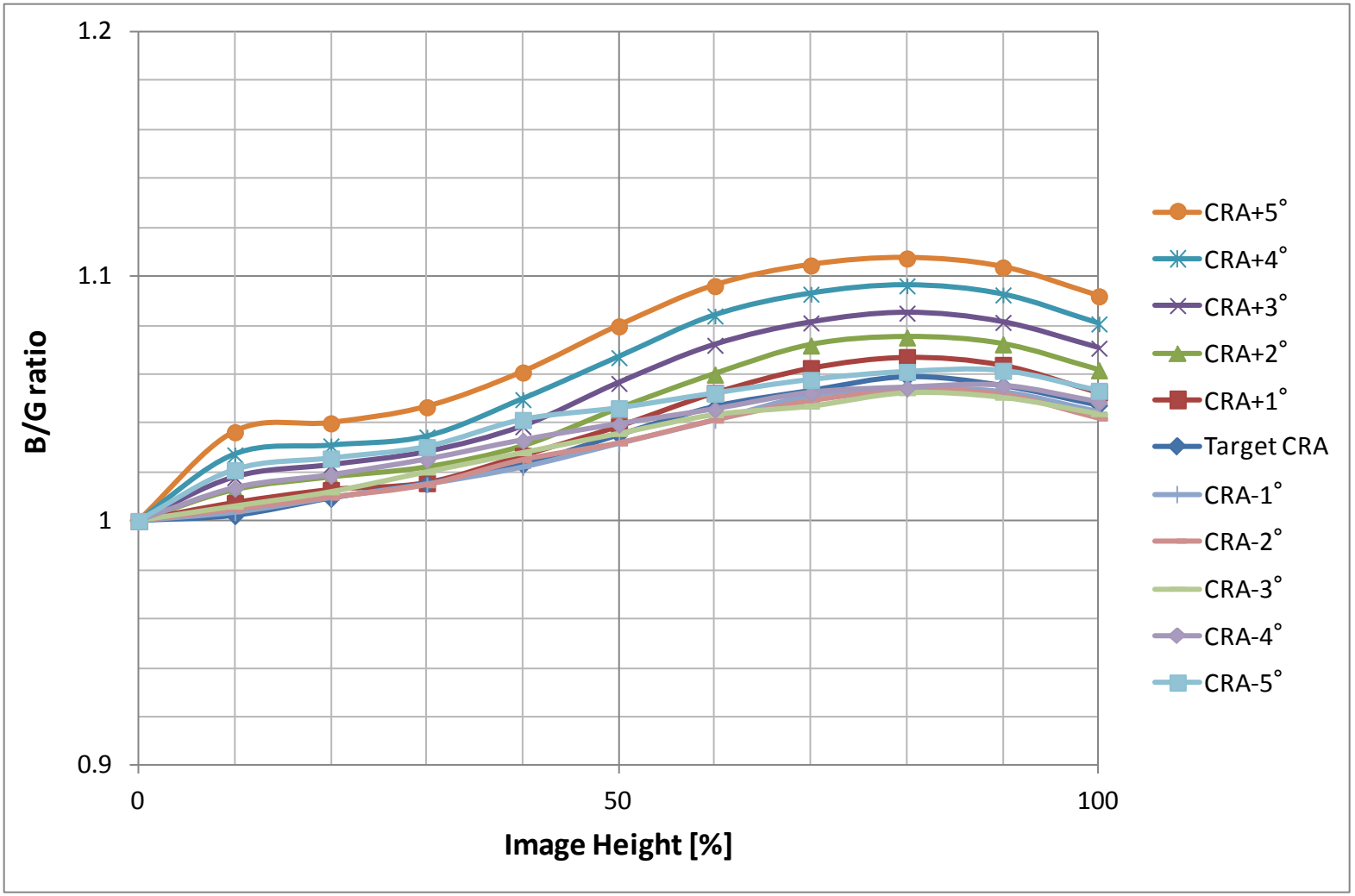
* Measurement with the white light source.



Note : In case of IMX219, minus(-) shift of ⊿CRA is much less risk than plus(+) side.

- IMX219 ΔCRA - Shading Characteristics of “R/G”

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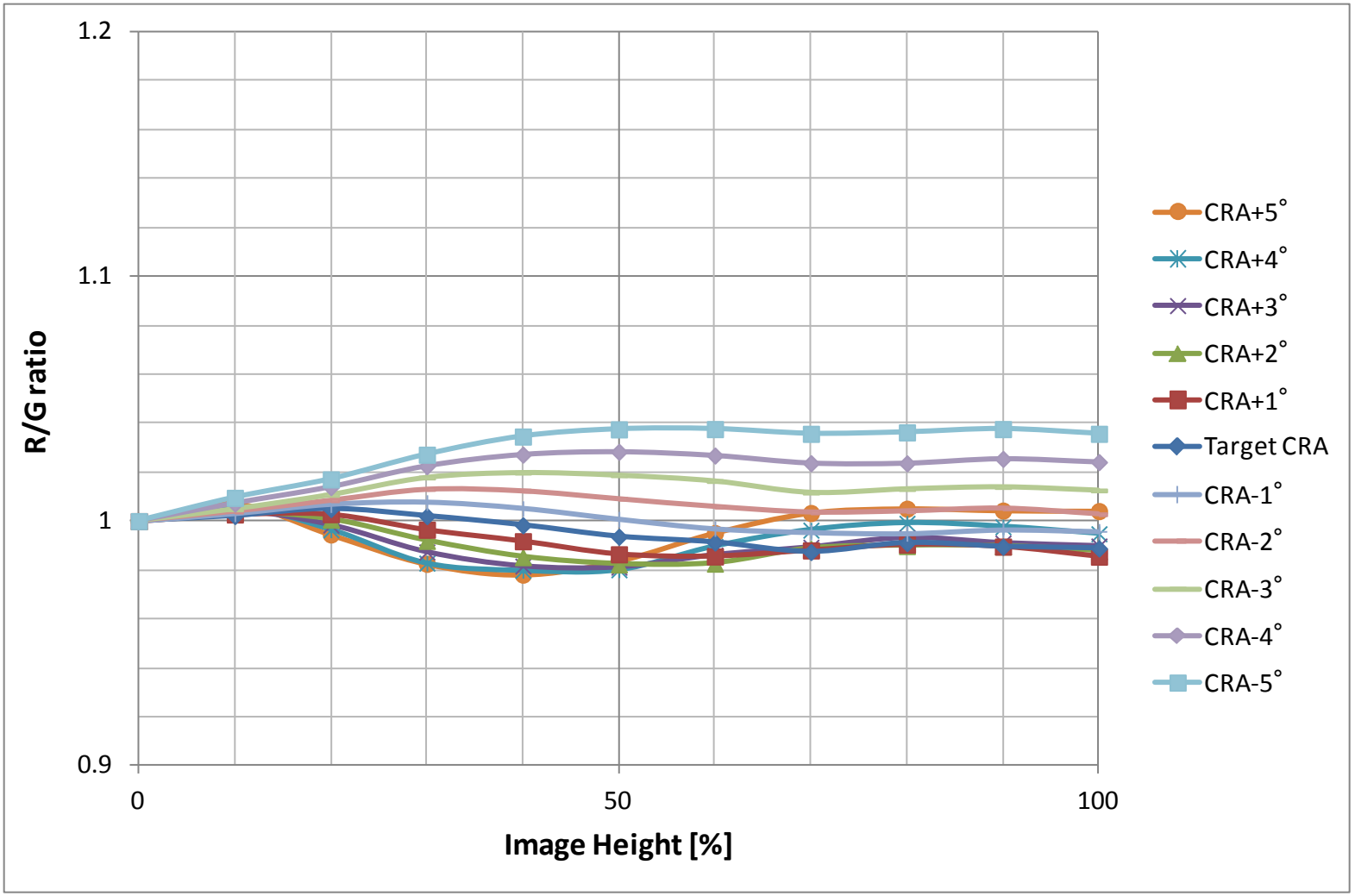
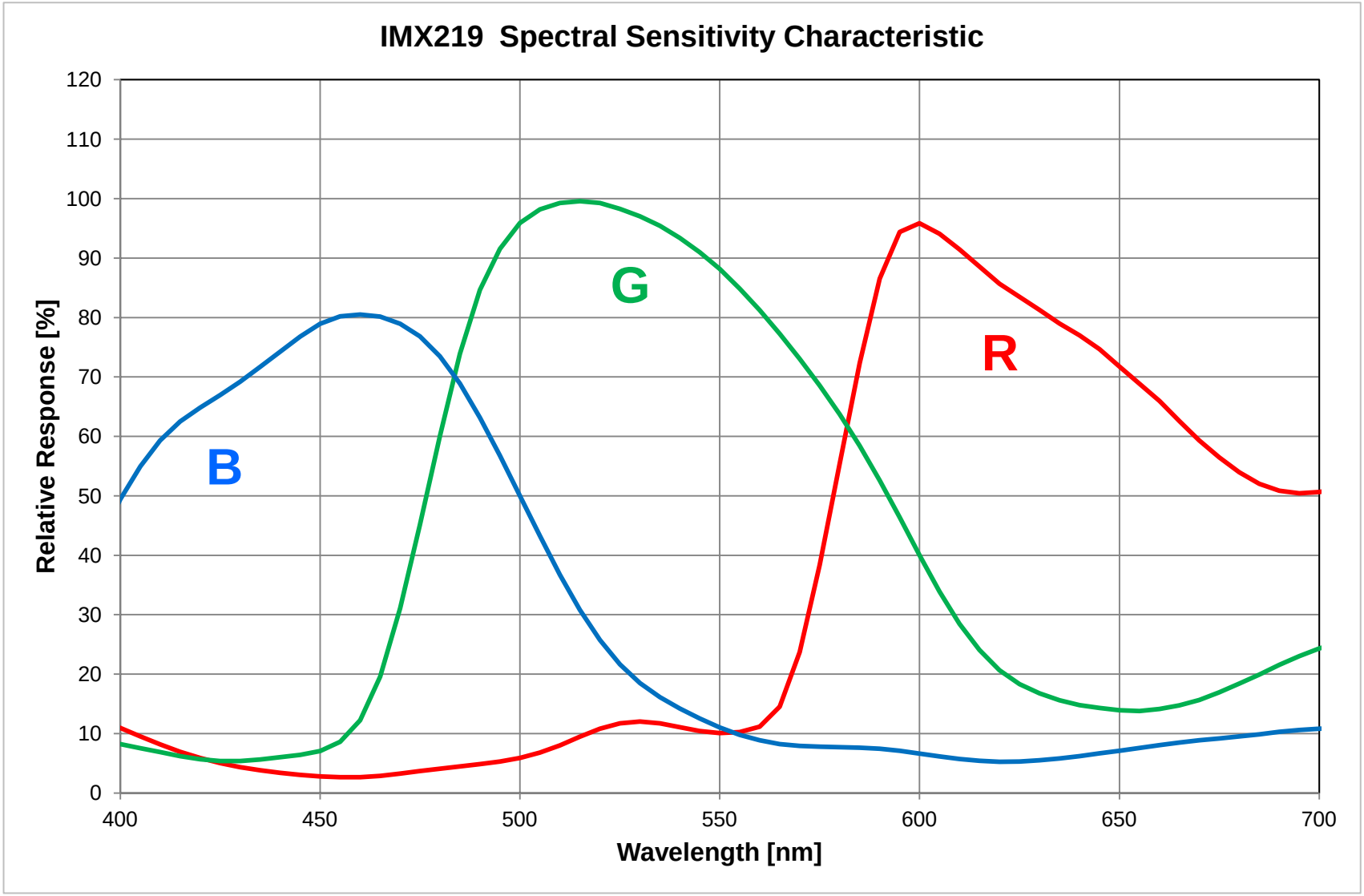
* Measurement with the white light source.



Note : In case of IMX219, minus(-) shift of ⊿CRA is much less risk than plus(+) side.


IMX219 Spectral Sensitivity Characteristic
Relative Response [%]
120
110
100
90
80
70
60
50
40
30
20
10
0
400
450
500
550
600
650
700
Wavelength [nm]
B
G
R

- Spectral Sensitivity Characteristic data

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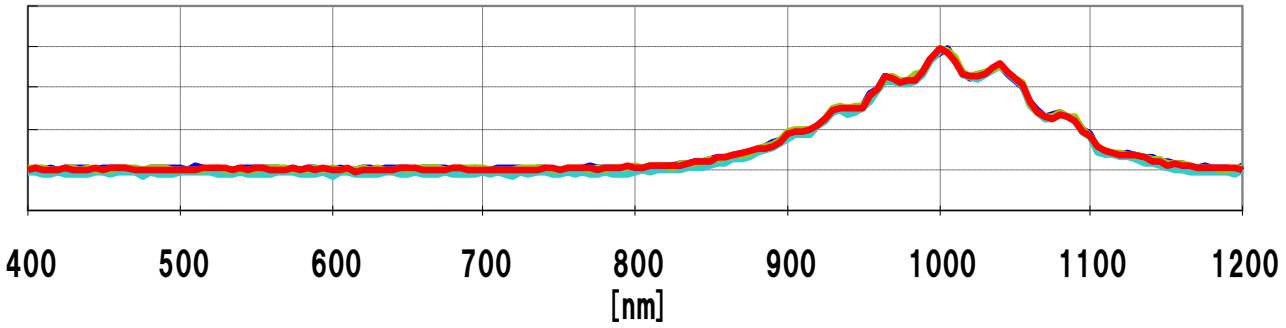
Wavelength	R	G	B
[nm]	[%]	[%]	[%]
400	10.96	8.23	49.45
405	9.51	7.56	54.98
410	8.17	6.87	59.29
415	6.94	6.20	62.49
420	5.90	5.67	64.86
425	5.04	5.37	66.93
430	4.35	5.38	69.20
435	3.81	5.64	71.70
440	3.38	6.01	74.24
445	3.04	6.41	76.80
450	2.79	7.06	78.93
455	2.65	8.63	80.21
460	2.67	12.25	80.51
465	2.89	19.56	80.13
470	3.27	31.08	78.95
475	3.69	45.10	76.83
480	4.10	60.04	73.47
485	4.49	73.88	68.90
490	4.87	84.64	63.16
495	5.29	91.57	56.77
500	5.90	95.91	50.01

Wavelength	R	G	B
[nm]	[%]	[%]	[%]
505	6.80	98.21	43.25
510	8.03	99.27	36.70
515	9.48	99.57	30.80
520	10.82	99.26	25.75
525	11.73	98.30	21.66
530	12.03	97.04	18.51
535	11.74	95.42	16.13
540	11.07	93.40	14.22
545	10.41	91.00	12.54
550	10.08	88.19	11.03
555	10.24	84.85	9.80
560	11.17	81.22	8.86
565	14.54	77.25	8.24
570	23.74	73.05	7.91
575	38.37	68.54	7.79
580	55.44	63.70	7.72
585	72.36	58.43	7.64
590	86.53	52.60	7.44
595	94.37	46.38	7.10
600	95.86	40.03	6.64

Wavelength	R	G	B
[nm]	[%]	[%]	[%]
605	94.09	33.91	6.16
610	91.46	28.47	5.72
615	88.55	24.07	5.41
620	85.69	20.66	5.26
625	83.49	18.32	5.30
630	81.30	16.75	5.50
635	78.97	15.59	5.81
640	76.98	14.81	6.20
645	74.69	14.31	6.66
650	71.75	13.91	7.13
655	68.86	13.80	7.59
660	65.95	14.13	8.04
665	62.61	14.74	8.48
670	59.32	15.67	8.86
675	56.45	16.95	9.19
680	53.98	18.40	9.52
685	52.02	19.94	9.88
690	50.86	21.55	10.30
695	50.44	23.02	10.61
700	50.63	24.33	10.81

- Notes on IR-Cut Selection

Image captured at 2300K(Low color temp.)

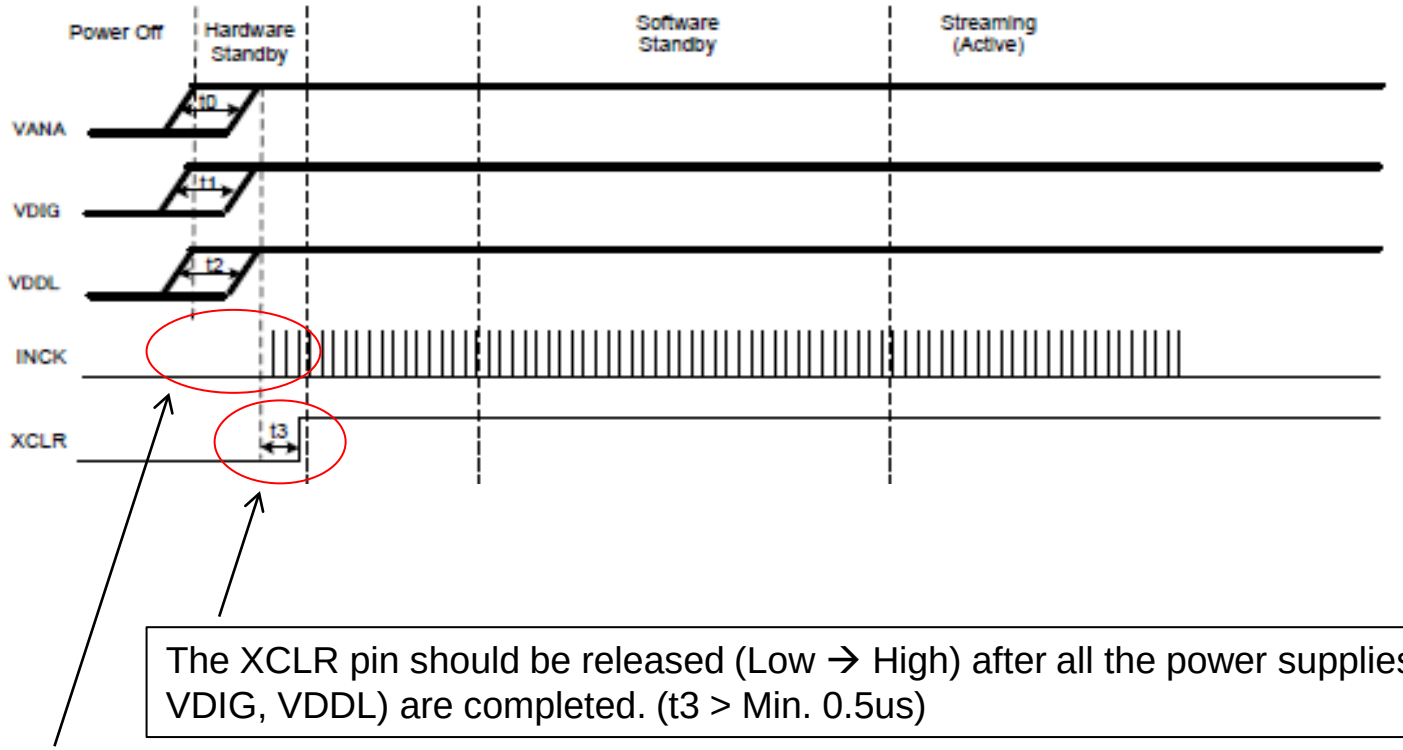


Proper selection of IR-Cut filter is critical for an overall image quality of camera system.

Optical Black output response at different wavelength is one of important factors when selecting IR Cut filter.

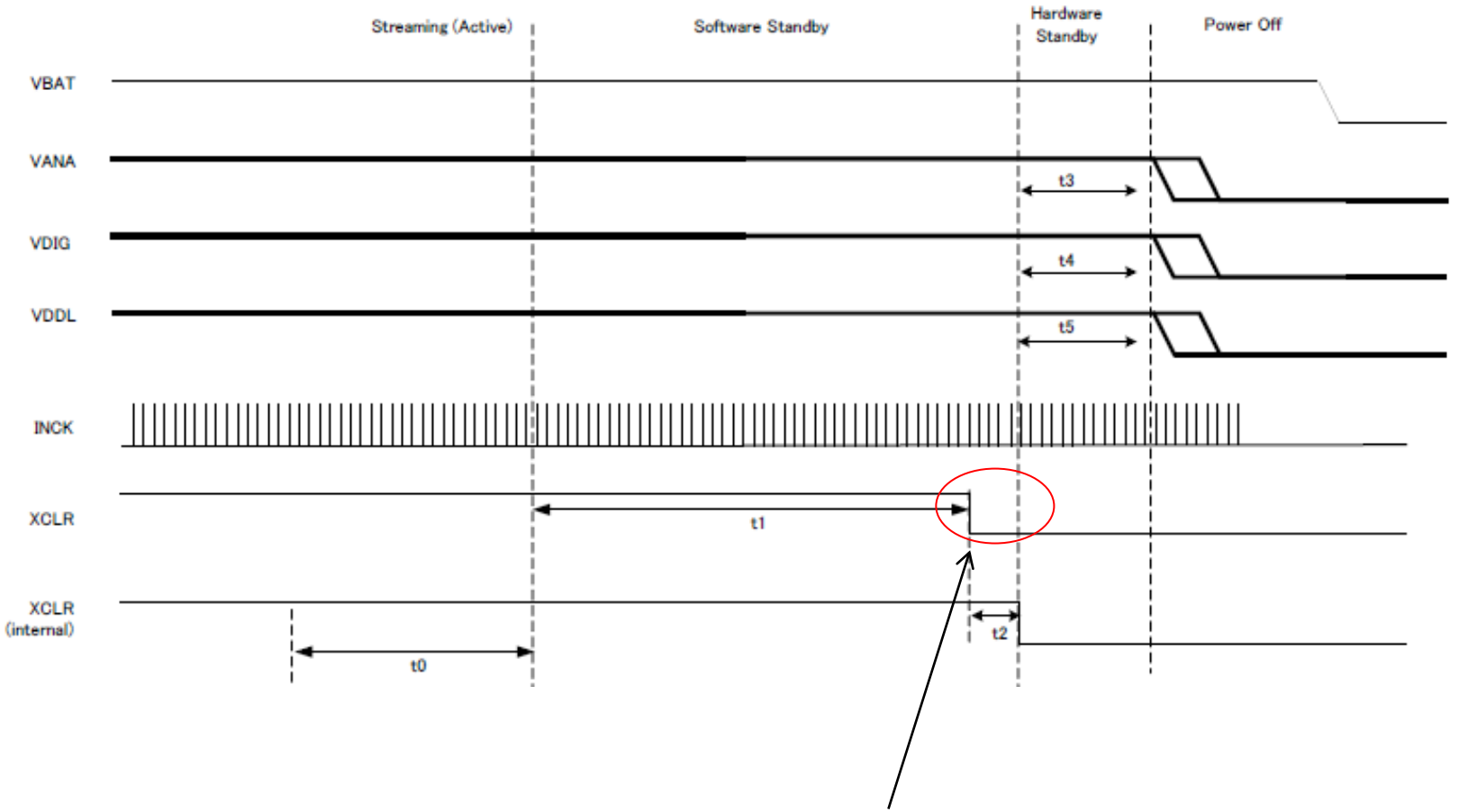
For IMX219,

SONY recommend IR cut filter with cut off from 650 to 1200nm.



The XCLR pin should be released (Low → High) after all the power supplies (VANA, VDIG, VDDL) are completed. (t3 > Min. 0.5us)

The INCK should be input after all the power supplies (VANA, VDIG, VDDL) are completed and need to input before XCLR (Low → High).



The XCLR should be set from High to Low before all the power supplies (VANA, VDIG, VDDL) are disabled. (t1 > min 0ns, t2 < max 10usec)

-History

Ver.	Date	Status	Note
1.0	2013.8.5	First version	P.8 INCK Power off Low -> HiZ , HWSTB Low/High -> HiZ P5,P9,P11 Optical Center (0,-93.83) -> (-0.025,-91.065) P8 GPO Type O->I/O , HWSTB HiZ->Low SCL SW STB Clock input->HiZ SDA SW STB Low->HiZ DVDD Power Off Low or High ->HiZ IOVDD Power Off Low or High ->HiZ AVDD Power Off Low or High ->HiZ Add -Assembly Guideline(P7) - Pin Information P6 TVMON Type I -> O Analog Output - Pin Status List P8 TVMON Type I -> O Analog Output
1.1	2013.8.22	Up Date	P7 Optical Center -> Chip Center
1.2	2013.9.19	Up Date	VDDH Typ. 2.7V-> 2.8V
1.3	2013.10.28	Up Date	PAD Structure(P.10～P.13)
1.4	2013.11.08	Up Date	Revise P.11（PAD Structure) IPQC PAD wide/height size and pin assign is “VDDHFIL1”
2.0	2014.1.8	Up Date	Change document name from : “IMX219_Module_Design_Reference_Manual” to : “IMX219PQH5_Module_Design_Reference_Manual” Minor corrections P15 remove “tentative” P16 remove “tentative”
2.1	2014.3.13	Up Date	P15, Add “PSRR” P17, Add “Power Consumption on each mode (Reference data)” P19-20, Add “Spectral Sensitivity Characteristic data” P22 Add the comment P23, Add “Power off sequence”

-History

Ver.	Date	Status	Note
2.2	2014.4.25	Up date	P18-21, Add ΔCRA-Shading characteristics data