

UNIVERSIDAD DE COSTA RICA  
Escuela de Ingeniería Eléctrica  
IE-0624 Laboratorio de Microcontroladores

## Laboratorio 4

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Grupo 01

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# 1. Introducción

En el siguiente reporte, se llevó a cabo el diseño y la implementación de un monitor de pendientes mediante el microcontrolador STM32F429 y la biblioteca libopencm3, con el fin de registrar y estudiar la inclinación de los terrenos. El diseño integra la lectura de los ejes (X, Y, Z) del giroscopio, lee la temperatura, además implementa un botón para habilitar/deshabilitar comunicaciones por USART/USB.

Además se tiene la capacidad de monitorear el nivel de la batería, cuyo rango va de 0 a 9 V. cuando el nivel de batería se aproxima al límite mínimo del microcontrolador para poder operar (7V), el sistema activa un LED. Con esta misma funcionalidad otro LED parpadea indicando que existe una deformación angular mayor a 5 grados en cualquier eje.

Esta misma implementación se prestó además para estudiar sobre el internet de las cosas mediante la plataforma de ThingsBoard, logrando así aprender sobre las aplicaciones de monitorio y análisis de datos en tiempo real.

Link del repositorio: <https://github.com/dagueroc/Laboratorio-de-Microcontroladores.git>

## 2. Nota teórica

### 2.1. Microcontrolador STM32F429

El STM32F429 es un microcontrolador de la familia STM32 de STMicroelectronics, basado en el núcleo ARM Cortex-M4. Es conocido por su alto rendimiento y sus características avanzadas, lo que lo hace ideal para aplicaciones que requieren una considerable capacidad de procesamiento y funciones avanzadas. MCU posee un DSP y también instrucciones de punto flotante, las características específicas son las siguientes:

1. Memoria: 2MB Memoria Flash, 256KB RAM.
2. Procesador: ARM Cortex M4 32-bits con FPU a 180MHz.
3. Pantalla: 2.4" QVGA TFT LCD.
4. Sensor de movimiento L3GD20.
5. Alimentación: USB o fuente externa de 3V o 5V.
6. Timers: 12 timers de 16bit, 2 de 32bit de hasta 180MHz, c/u con 4IC/OC/PWM.
7. Convertidor Analógico-Digital: 3x12bits.
8. Convertidor Digital-Analógico: 2x12bits.
9. Conectividad USB 2.0 Avanzada (Debug, COM virtual, almacenamiento, OTG).
10. Interfaces de comunicación (I2C, USART, SPI, SAI, CAN).

A continuación, se tienen las especificaciones técnicas del microcontrolador:

## 2.2. Diagrama de bloques

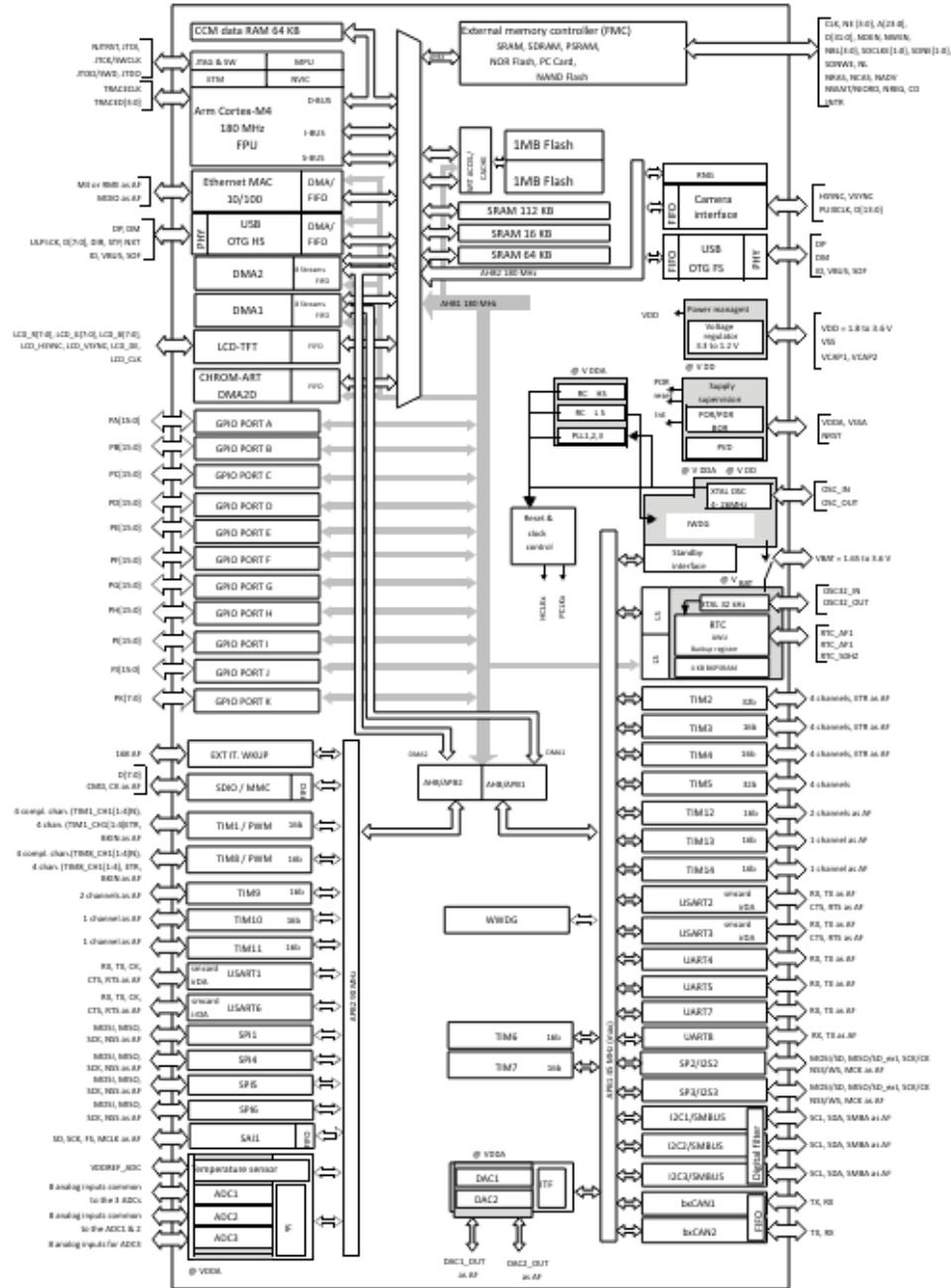


Figura 1: Diagrama de bloques

## 2.3. Diagrama de pines

Se muestra el diagrama de pines, en este caso el STM32F429 incluye el Cortex M4F - LQFP144

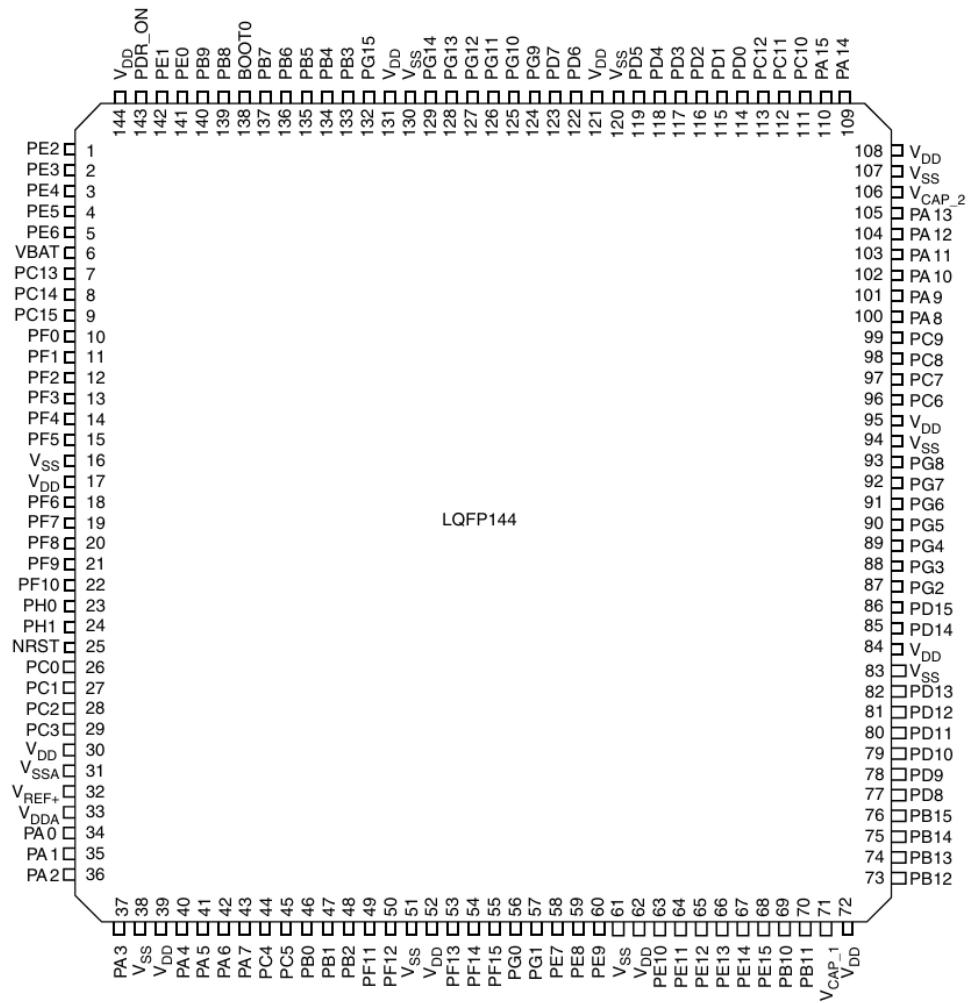


Figura 2: Pin Layout del STM32F429i

## 2.4. Registros

Tanto el microcontrolador, como el giroscopio, como el modulo de la pantalla, tienen registros independientes. Del microcontrolador se ingresaron específicamente los periféricos. Entre los utilizados mas importantes, los cuales se utilizaron para habilitar lecturas de otros registros, leer variables del giroscopio, ajustar variables físicas, entre otros:

- CTRL REG1
  - CTRL REG4
  - GYR OUT X L
  - GYR OUT X H
  - GYR OUT Y L

- GYR OUT Y H
- GYR OUT Z L
- GYR OUT Z H

Bus	Boundary address	Peripheral
	0x4008 0000- 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00- 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	DMA2D
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	ETHERNET MAC
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0X4002 5000 - 0X4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0X4002 3400 - 0X4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0X4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Figura 3: Pin Layout del STM32F429i

## 2.5. Componentes

Para el laboratorio se utilizaron los componentes integrados del STM32F429 Discovery kit, el switch, la pantalla, y los LEDs. Adicional a esto se conectó una batería externa para simular el comportamiento que tendría en el circuito y por lo mismo fue necesario utilizar resistores.

Componente	Cantidad	Precio (USD)
Resistores 100Ω	10	1.6
Batería 9V	1	2
STM32F429 Discovery kit	1	98.6
<b>Total</b>		<b>102.2</b>

Figura 4: Componentes y costos

### 3. Desarrollo/Análisis de resultados

#### 3.1. Análisis electrónico

El voltaje de máximo del I/O utilizado es de 5V, se diseña un divisor de tensión de modo que la tensión que lea el pin cuando la batería tenga 9V sea 5V.

$$V_{in} = \frac{5 \cdot 100\Omega}{4 \cdot 100\Omega + 5 \cdot 100\Omega} \cdot 9V = 5V \quad (1)$$

#### 3.2. Análisis del programa

Para la funcionalidad del software, se desarrolló un código en el lenguaje de programación C, cubriendo diversas funcionalidades relacionadas con la interacción de periféricos y sensores, como un giroscopio, utilizando la lógica implementada en la biblioteca de ejemplos del microcontrolador STM32: libopencm3-examples.

Es importante destacar que gran parte de la configuración se enfocó en el giroscopio, que es crucial para el funcionamiento de un sismógrafo, ya que permite interactuar con la posición del dispositivo en las coordenadas X, Y y Z. Entre las configuraciones del giroscopio se incluyen la identificación del dispositivo, registros de control, registros de datos, entre otros, con el objetivo de configurar y obtener datos del giroscopio. Se utilizó una estructura en C llamada "gyro" con tres enteros de 16 bits para almacenar los valores de los ejes X, Y y Z del giroscopio.

Además, se definieron funciones para realizar transacciones SPI con el giroscopio y configurar la interfaz SPI, un protocolo de comunicación que permite la interacción entre periféricos. También se implementó otro protocolo de comunicación, USART (Universal Synchronous Asynchronous Receiver Transmitter), para la transmisión de datos generados por el giroscopio, utilizando el pin GPIO9 del puerto A con una velocidad de transmisión de 115200 bps.

La pantalla requiere un proceso de inicialización y configuración, que incluye la activación de ciertos periféricos, configuración de pines y comunicación inicial con la pantalla para establecer parámetros operativos.

El sistema utiliza una biblioteca gráfica que ofrece funciones para varias operaciones gráficas, tales como:

- Limpiar la pantalla.
- Configurar el tamaño y color del texto.
- Dibujar y llenar rectángulos.

Para la configuración de los pines, se realizó la conexión de la siguiente manera:

- GPIOC, GPIO1: Utilizado para controlar el Chip Select (CS) del giroscopio durante las transacciones SPI.

- GPIOF, GPIO7 — GPIO8 — GPIO9: Configurados para el modo de función alternativa (AF), específicamente para la interfaz SPI con el giroscopio. Aunque no se detalla la función exacta de cada uno, generalmente en SPI estos pines corresponden a MISO (Master In, Slave Out), MOSI (Master Out, Slave In) y SCLK (Serial Clock).
- GPIOA, GPIO9: Configurado para transmitir datos desde USART1, por donde se transmiten los datos que son interpretados por un script de Python.
- GPIOA, GPIO0: Configurados como entradas.
- GPIOG, GPIO13 y GPIO14: Configurados como salidas.
- GPIOA, GPIO3: Utilizado para leer el nivel de batería mediante el ADC, siendo una entrada analógica que recoge los valores de voltaje de la batería.

### 3.2.1. Código Python

Este script es responsable de recibir la comunicación serial desde el MCU, decodificarla y postprocesarla para visualizarla en la terminal del ordenador. Además, este script toma el array de datos, que se actualiza constantemente cuando las comunicaciones USART/USB están habilitadas, y lo envía a la plataforma de IoT en internet: ThingsBoard.

El script se divide en dos secciones principales. Una se encarga de la conexión serial con el microcontrolador a través de comunicación USB, y la otra establece la conexión con ThingsBoard. Existen dos funciones para verificar la conexión y otra para notificar si la desconexión se ha realizado con éxito. La conexión con la plataforma de IoT se establece utilizando el protocolo de comunicación MQTT, un estándar en IoT. Los datos se deben enviar a la plataforma en formato JSON. En las siguientes figuras se muestra cómo funciona el software en la plataforma ThingsBoard.

### 3.3. Muestra del funcionamiento

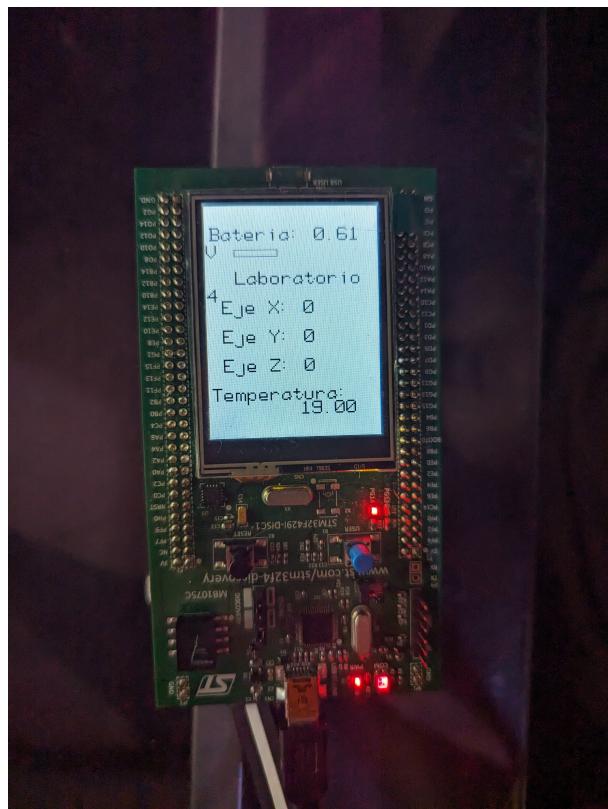


Figura 5: STM32F429

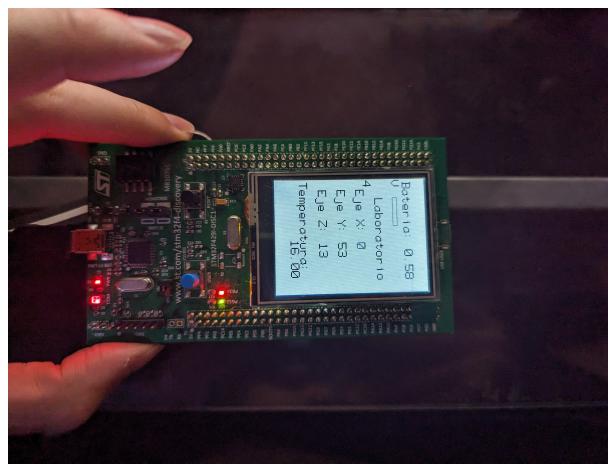


Figura 6: STM32F429



Figura 7: STM32F429

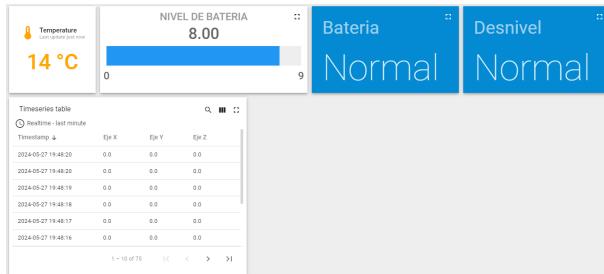


Figura 8: Thingsboard



Figura 9: Thingsboard

## 4. Conclusiones y recomendaciones

- El desarrollo y puesta en marcha del monitor de pendientes se completo de manera satisfactoria empleando el Microcontrolador STM32F429 Discovery kit y el apoyo de la biblioteca libopencm3.
- La conexión entre el monitor de pendientes y la plataforma de IoT Thingsboard se estableció exitosamente usando un script de Python.
- El uso de la plataforma de IoT Thingsboard permitió una visualización efectiva y en tiempo real de los datos recogidos, mostrando la importancia de las plataformas de IoT en la era digital.
- Para asegurar la correcta lectura de todas las bibliotecas requeridas, se sugiere trabajar con la biblioteca libopencm3. Además, es aconsejable implementar y ejecutar el código del monitor de pendientes dentro de las carpetas de libopencm3-examples.
- Para facilitar la implementación y acelerar el proceso de desarrollo, es beneficioso tomar como referencia los ejemplos previamente establecidos en libopencm3-examples

## Referencias

## 5. Anexos

### 5.1. Hoja de datos

En próximas páginas se adjuntan las hojas del fabricante cuya información fue necesaria para realizar el procedimiento

**a-Si TFT LCD Single Chip Driver  
240RGBx320 Resolution and 262K color**

**Specification**

Version: V1.11  
Document No.: ILI9341\_DS\_V1.11.pdf

**ILI TECHNOLOGY CORP.**

8F, No. 38, Taiyuan St., Jhubei City,  
Hsinchu Country 302 Taiwan R.O.C.  
Tel.886-3-5600099; Fax.886-3-5670585  
<http://www.ilitek.com>

*Table of Contents*

<i>Section</i>	<i>Page</i>
1. Introduction.....	7
2. Features .....	7
3. Block Diagram.....	9
4. Pin Descriptions .....	10
5. Pad Arrangement and Coordination.....	15
6. Block Function Description.....	24
7. Function Description .....	26
7.1. MCU interfaces .....	26
7.1.1. MCU interface selection .....	26
7.1.2. 8080- I Series Parallel Interface.....	27
7.1.3. Write Cycle Sequence .....	28
7.1.4. Read Cycle Sequence.....	29
7.1.5. 8080-II Series Parallel Interface.....	30
7.1.6. Write Cycle Sequence .....	31
7.1.7. Read Cycle Sequence.....	32
7.1.8. Serial Interface .....	33
7.1.9. Write Cycle Sequence .....	33
7.1.10. Read Cycle Sequence.....	36
7.1.11. Data Transfer Break and Recovery .....	40
7.1.12. Data Transfer Pause.....	42
7.1.13. Serial Interface Pause (3_wire) .....	43
7.1.14. Parallel Interface Pause .....	43
7.1.15. Data Transfer Mode .....	44
7.1.16. Data Transfer Method 1 .....	44
7.1.17. Data Transfer Method 2 .....	44
7.2. RGB Interface .....	45
7.2.1. RGB Interface Selection .....	45
7.2.2. RGB Interface Timing .....	49
7.3. VSYNC Interface.....	52
7.4. Color Depth Conversion Look Up Table.....	55
7.5. Display Data RAM (DDRAM) .....	59
7.6. Display Data Format .....	60
7.6.1. 3-line Serial Interface.....	60
7.6.2. 4-line Serial Interface.....	63
7.6.3. 8-bit Parallel MCU Interface .....	65
7.6.4. 9-bit Parallel MCU Interface .....	67
7.6.5. 16-bit Parallel MCU Interface .....	70

7.6.6.	18-bit Parallel MCU Interface .....	76
7.6.7.	6-bit Parallel RGB Interface.....	80
7.6.8.	16-bit Parallel RGB Interface.....	82
7.6.9.	18-bit Parallel RGB Interface.....	82
8.	Command.....	83
8.1.	Command List .....	83
8.2.	Description of Level 1 Command.....	89
8.2.1.	NOP (00h).....	89
8.2.2.	Software Reset (01h).....	90
8.2.3.	Read display identification information (04h) .....	91
8.2.4.	Read Display Status (09h).....	92
8.2.5.	Read Display Power Mode (0Ah) .....	94
8.2.6.	Read Display MADCTL (0Bh).....	95
8.2.7.	Read Display Pixel Format (0Ch).....	96
8.2.8.	Read Display Image Format (0Dh).....	97
8.2.9.	Read Display Signal Mode (0Eh) .....	98
8.2.10.	Read Display Self-Diagnostic Result (0Fh) .....	99
8.2.11.	Enter Sleep Mode (10h) .....	100
8.2.12.	Sleep Out (11h).....	101
8.2.13.	Partial Mode ON (12h).....	103
8.2.14.	Normal Display Mode ON (13h) .....	104
8.2.15.	Display Inversion OFF (20h).....	105
8.2.16.	Display Inversion ON (21h) .....	106
8.2.17.	Gamma Set (26h) .....	107
8.2.18.	Display OFF (28h) .....	108
8.2.19.	Display ON (29h) .....	109
8.2.20.	Column Address Set (2Ah) .....	110
8.2.21.	Page Address Set (2Bh) .....	112
8.2.22.	Memory Write (2Ch) .....	114
8.2.23.	Color Set (2Dh).....	115
8.2.24.	Memory Read (2Eh) .....	116
8.2.25.	Partial Area (30h).....	118
8.2.26.	Vertical Scrolling Definition (33h) .....	120
8.2.27.	Tearing Effect Line OFF (34h) .....	124
8.2.28.	Tearing Effect Line ON (35h) .....	125
8.2.29.	Memory Access Control (36h) .....	127
8.2.30.	Vertical Scrolling Start Address (37h) .....	129
8.2.31.	Idle Mode OFF (38h) .....	131
8.2.32.	Idle Mode ON (39h) .....	132

8.2.33. COLMOD: Pixel Format Set (3Ah) .....	134
8.2.34. Write_Memory_Continue (3Ch).....	135
8.2.35. Read_Memory_Continue (3Eh).....	137
8.2.36. Set_Tear_Scanline (44h) .....	139
8.2.37. Get_Scanline (45h).....	140
8.2.38. Write Display Brightness (51h) .....	141
8.2.39. Read Display Brightness (52h).....	142
8.2.40. Write CTRL Display (53h).....	143
8.2.41. Read CTRL Display (54h) .....	145
8.2.42. Write Content Adaptive Brightness Control (55h).....	147
8.2.43. Read Content Adaptive Brightness Control (56h) .....	148
8.2.44. Write CABC Minimum Brightness (5Eh).....	149
8.2.45. Read CABC Minimum Brightness (5Fh).....	150
8.2.46. Read ID1 (DAh) .....	151
8.2.47. Read ID2 (DBh) .....	152
8.2.48. Read ID3 (DCh) .....	153
8.3. Description of Level 2 Command.....	154
8.3.1. RGB Interface Signal Control (B0h) .....	154
8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h).....	155
8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h) .....	157
8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h) .....	159
8.3.5. Display Inversion Control (B4h).....	161
8.3.6. Blanking Porch Control (B5h).....	162
8.3.7. Display Function Control (B6h).....	164
8.3.8. Entry Mode Set (B7h) .....	168
8.3.9. Backlight Control 1 (B8h).....	169
8.3.10. Backlight Control 2 (B9h).....	170
8.3.11. Backlight Control 3 (BAh) .....	172
8.3.12. Backlight Control 4 (BBh) .....	173
8.3.13. Backlight Control 5 (BCh) .....	175
8.3.14. Backlight Control 7 (BEh) .....	176
8.3.15. Backlight Control 8 (BFh) .....	177
8.3.16. Power Control 1 (C0h) .....	178
8.3.17. Power Control 2 (C1h) .....	179
8.3.18. VCOM Control 1(C5h) .....	180
8.3.19. VCOM Control 2(C7h) .....	182
8.3.20. NV Memory Write (D0h) .....	184
8.3.21. NV Memory Protection Key (D1h) .....	185
8.3.22. NV Memory Status Read (D2h) .....	186

8.3.23. Read ID4 (D3h) .....	187
8.3.24. Positive Gamma Correction (E0h).....	188
8.3.25. Negative Gamma Correction (E1h) .....	189
8.3.26. Digital Gamma Control 1 (E2h) .....	190
8.3.27. Digital Gamma Control 2(E3h) .....	191
8.3.28. Interface Control (F6h) .....	192
8.4 Description of Extend register command .....	195
8.4.1 Power control A (CBh).....	195
8.4.2 Power control B (CFh).....	196
8.4.3 Driver timing control A (E8h) .....	197
8.4.4 Driver timing control A (E9h) .....	198
8.4.5 Driver timing control B (EAh).....	199
8.4.6 Power on sequence control (EDh) .....	200
8.4.7 Enable 3G (F2h).....	201
8.4.8 Pump ratio control (F7h) .....	202
9. Display Data RAM .....	203
9.1. Configuration.....	203
9.2. Memory to Display Address Mapping .....	204
9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF.....	204
9.2.2. Vertical Scroll Mode .....	205
9.2.3. Vertical Scroll Example.....	206
9.2.4. Case1: TFA+VSA+BFA < 320 .....	206
9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling) .....	206
9.3. MCU to memory write/read direction .....	208
10. Tearing Effect Output.....	210
10.1. Tearing Effect Line Modes.....	210
10.2. Tearing Effect Line Timings .....	211
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module.....	212
11.1. Register loading Detection .....	212
11.2. Functionality Detection .....	213
12. Power ON/OFF Sequence .....	214
12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON .....	214
12.2. Case 2 – RESX line is held Low by Host at Power ON .....	215
12.3. Uncontrolled Power Off .....	216
13. Power Level Definition .....	217
13.1. Power Levels.....	217
13.2. Power Flow Chart.....	218
14. Gamma Curves Selection .....	223
14.1. Gamma Default Values (for NW type LC) .....	223

14.2. Gamma Curves .....	224
14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$ .....	224
14.3. Gamma Curves .....	225
14.3.1. Grayscale Voltage Generation.....	225
14.3.2. Positive Gamma Correction.....	226
14.3.3. Negative Gamma Correction.....	227
15. Reset .....	228
15.1. Registers .....	228
15.2. Output Pins, I/O Pins.....	229
15.3. Input Pins .....	229
15.4. Reset Timing .....	230
16. Configuration of Power Supply Circuit .....	231
17. NV Memory Programming Flow .....	234
18. Electrical Characteristics .....	235
18.1 Absolute Maximum Ratings .....	235
18.2 DC Characteristics .....	236
18.2.1 General DC Characteristics.....	236
18.3 AC Characteristics .....	238
18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system) .....	238
18.3.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080- II system) .....	240
18.3.3 Display Serial Interface Timing Characteristics (3-line SPI system) .....	242
18.3.4 Display Serial Interface Timing Characteristics (4-line SPI system) .....	243
18.3.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics .....	244
19 Revision History .....	245

## 1. Introduction

ILI9341 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9341 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

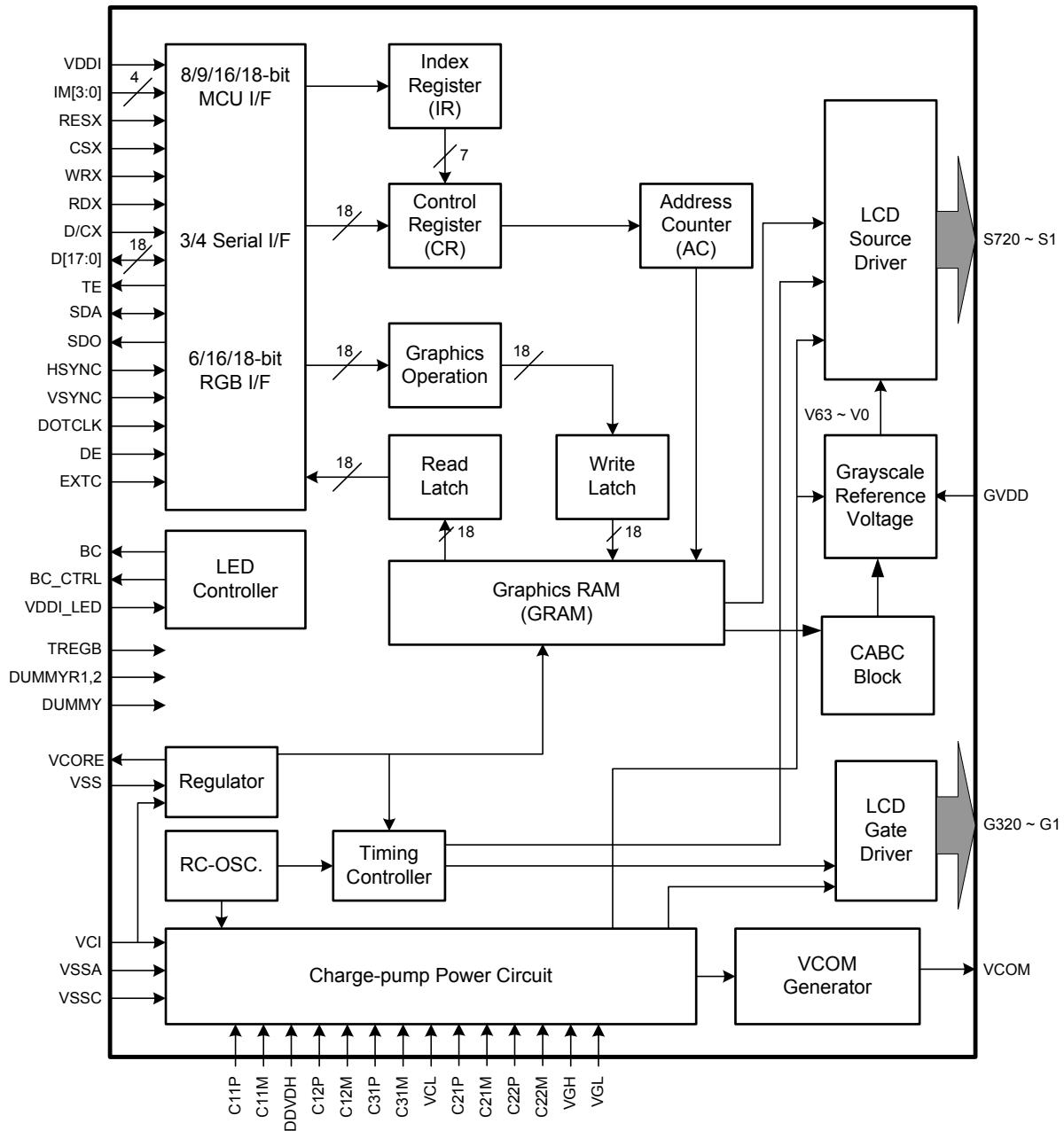
ILI9341 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9341 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9341 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

## 2. Features

- ◆ Display resolution: [240xRGB](H) x 320(V)
- ◆ Output:
  - 720 source outputs
  - 320 gate outputs
  - Common electrode output (VCOM)
- ◆ a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- ◆ System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080- I /8080- II series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface
- ◆ Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- ◆ Power saving mode:
  - Sleep mode
- ◆ On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
  - 1 preset Gamma curve with separate RGB Gamma correction
- ◆ Content Adaptive Brightness Control
- ◆ MTP (3 times):
  - 8-bits for ID1, ID2, ID3
  - 7-bits for VCOM adjustment

- ◆ Low -power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3V (logic)
    - **VCI = 2.5V ~ 3.3V** (analog)
  - LCD Voltage drive:
    - Source/VCOM power supply voltage
      - DDVDH - GND = 4.5V ~ 5.8V
      - VCL - GND = -1.5V ~ -2.5V
    - Gate driver output voltage
      - VGH - GND = 10.0V ~ 18.0V
      - VGL - GND = -5.0V ~ -10.0V
      - VGH - VGL  $\leq$  28V
    - VCOM driver output voltage
      - VCOMH = 3.0V ~ (DDVDH – 0.2)V
      - VCOML = (VCL+0.2)V ~ 0V
      - VCOMH - VCOML  $\leq$  6.0V
  - Operate temperature range: -40°C to 85°C
  - a-Si TFT LCD storage capacitor : Cst on Common structure only

### 3. Block Diagram



## 4. Pin Descriptions

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
VDDI	I	P	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VDDI_LED	I		Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VDDI.
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)
Vcore	O	Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad
VSS3	I	I/O Ground	System ground level for I/O circuits.
VSS	I	Digital Ground	System ground level for logic blocks
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.
VSSC	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise

Interface Logic Signals																																																																																																		
Pin Name	I/O	Type	Descriptions																																																																																															
IM[3:0]	I	(VDDI/VSS)	Select the MCU interface mode																																																																																															
			<table border="1"> <thead> <tr> <th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU-Interface Mode</th><th>DB Pin in use</th><th></th></tr> <tr> <th>Register/Content</th><th></th><th></th><th></th><th></th><th>Register/Content</th><th>GRAM</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr> </tbody> </table>	IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use		Register/Content					Register/Content	GRAM	0	0	0	0	80 MCU 8-bit bus interface I	D[7:0]	D[7:0]	0	0	0	1	80 MCU 16-bit bus interface I	D[7:0]	D[15:0]	0	0	1	0	80 MCU 9-bit bus interface I	D[7:0]	D[8:0]	0	0	1	1	80 MCU 18-bit bus interface I	D[7:0]	D[17:0]	0	1	0	1	3-wire 9-bit data serial interface I	SDA: In/OUT		0	1	1	0	4-wire 8-bit data serial interface I	SDA: In/OUT		1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]	1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]	1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]	1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]	1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Out		1	1	1	0
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MPU Parallel interface bus and serial interface select																																																																																																		
If use RGB Interface must select serial interface.																																																																																																		
* : Fix this pin at VDDI or VSS.																																																																																																		

RESX	I	MCU (VDDI/VSS)	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
EXTC	I	MCU (VDDI/VSS)	Extended command set enable. Low: extended command set is discarded. High: extended command set is accepted.  Please connect EXTC to VDDI to read/write extended registers (RB0h~RCFh, RE0h~RFFh)
CSX	I	MCU (VDDI/VSS)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. * note1,2
D/CX (SCL)	I	MCU (VDDI/VSS)	This pin is used to select "Data or Command" in the parallel interface or 4-wire 8-bit serial data interface. When DCX = '1', data is selected. When DCX = '0', command is selected.  This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. <b>If not used, this pin should be connected to VDDI or VSS.</b>
RDX	I	MCU (VDDI/VSS)	8080- I /8080- II system (RDX): Serves as a read signal and MCU read data at the rising edge. <b>Fix to VDDI level when not in use.</b>
WRX (D/CX)	I	MCU (VDDI/VSS)	- 8080- I /8080- II system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. <b>Fix to VDDI level when not in use.</b>
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode <b>Fix to VSS level when not in use</b>
SDI/SDA	I/O	MCU (VDDI/VSS)	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. <b>If not used, fix this pin at VDDI or VSS.</b>
SDO	O	MCU (VDDI/VSS)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/VSS)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation. <b>Fix to VDDI or VSS level when not in use.</b>
VSYNC	I	MCU (VDDI/VSS)	Frame synchronizing signal for RGB interface operation. <b>Fix to VDDI or VSS level when not in use.</b>
H SYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. <b>Fix to VDDI or VSS level when not in use.</b>
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. <b>Fix to VDDI or VSS level when not in use.</b>

**Note.**

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.
2. When CSX='1', there is no influence to the parallel and serial interface.

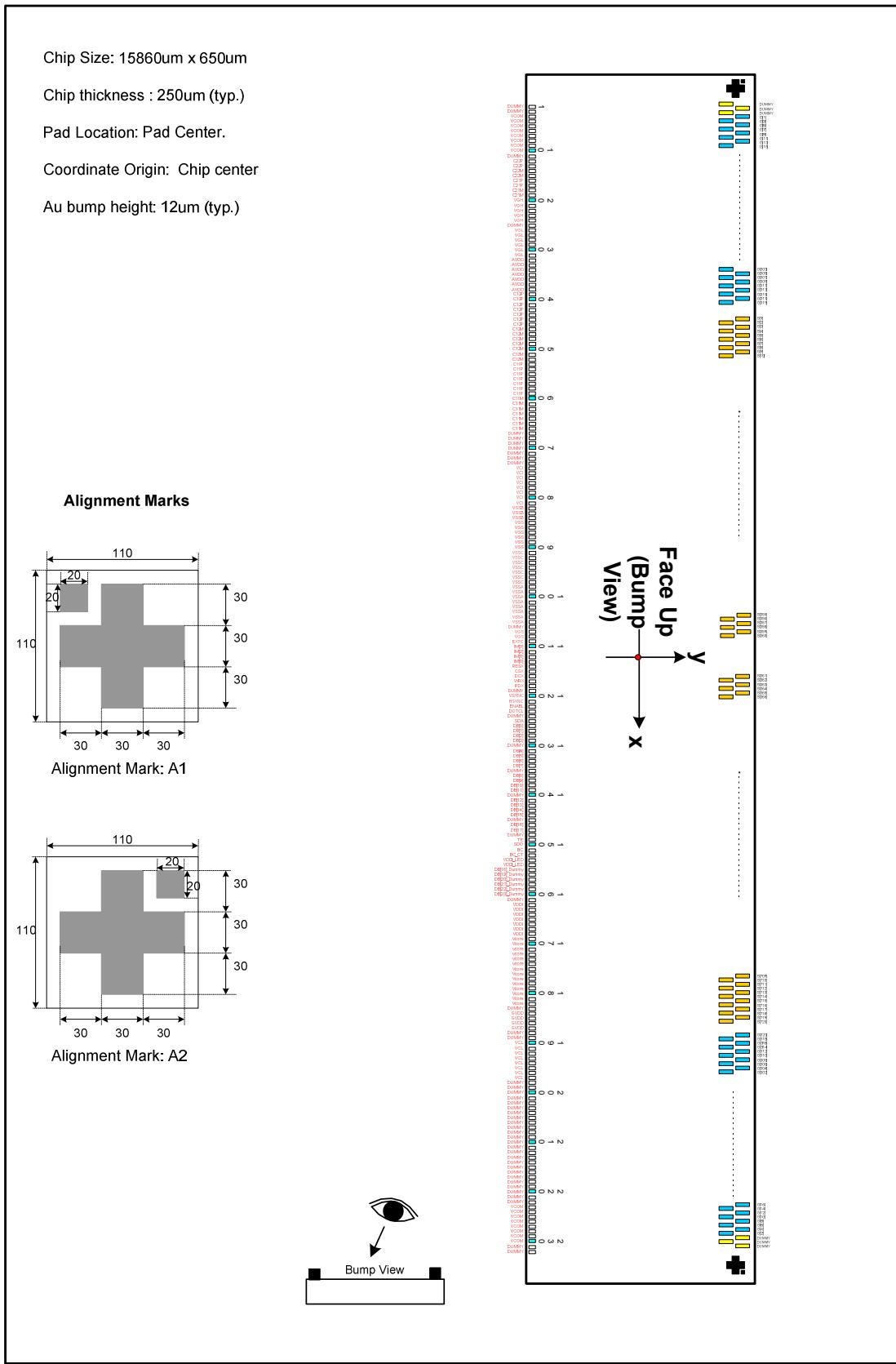
LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S720~S1	O	Source	Source output signals.. <i>Leave the pin to open when not in use.</i>
G320~G1	O	Gate	Gate output signals. <i>Leave the pin to open when not in use.</i>
DDVDH	O	Power Stabilizing capacitor	Output voltage of 1st step up circuit (2 x VCI). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.
VGH	O	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits. <b>Connect this pad with a stabilizing capacitor.</b>
VGL	O	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VCL	O	Power Stabilizing capacitor	Power supply for VCOML. VCL = 0~ - VCI Connect this pad with a stabilizing capacitor.
C11P, C11M C12P, C12M	P	Stabilizing capacitor	Connect the charge-pumping capacitor for generating DDVDH level.
C21P, C21M C22P, C22M	P	Stabilizing capacitor	Connect the charge-pumping capacitor for generating VGH, VGL level.
GVDD	O		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VCOM	O		Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.
LEDPWM	O		Output pin for PWM (Pulse Width Modulation) signal of LED driving. If not used, open this pad.
LEDON	O		Output pin for enabling LED driving. If not used, open this pad.

Test Pins			
Pin Name	I/O	Type	Descriptions
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
INT_TEST1 INT_TEST2	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.

**Liquid crystal power supply specifications Table**

No.	Item	Description	
1	TFT Source Driver	720 pins (240 x RGB)	
2	TFT Gate Driver	320 pins	
3	TFT Display's Capacitor Structure	Cst structure only (Cs on Common)	
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	VDDI	1.65V ~ 3.30V
		VCI	<b>2.50V ~ 3.30V</b>
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 5.8V
		VGH	10.0V ~ 18.0V
		VGL	-5.0V ~ -10.0V
		VCL	-1.5V ~ -2.5V
		VGH - VGL	Max. 28.0V
7	Internal Step-up Circuits	DDVDH	VCI x2,
		VGH	VCI x6, x7
		VGL	VCI x-3, x-4,
		VCL	VCI x-1

## 5. Pad Arrangement and Coordination



No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY	-7292.5	-248	51	C12M	-4292.5	-248	101	VSSA	-1292.5	-248	151	LEDPWM	2245	-248
2	DUMMY	-7232.5	-248	52	C12M	-4232.5	-248	102	VSSA	-1232.5	-248	152	LEDON	2330	-248
3	VCOM	-7172.5	-248	53	C11P	-4172.5	-248	103	VSSA	-1172.5	-248	153	VDDI_LED	2402.5	-248
4	VCOM	-7112.5	-248	54	C11P	-4112.5	-248	104	VSSA	-1112.5	-248	154	VDDI_LED	2462.5	-248
5	VCOM	-7052.5	-248	55	C11P	-4052.5	-248	105	VSSA	-1052.5	-248	155	DB[18]_Dummy	2535	-248
6	VCOM	-6992.5	-248	56	C11P	-3992.5	-248	106	DUMMY	-992.5	-248	156	DB[19]_Dummy	2620	-248
7	VCOM	-6932.5	-248	57	C11P	-3932.5	-248	107	VGS	-932.5	-248	157	DB[20]_Dummy	2705	-248
8	VCOM	-6872.5	-248	58	C11P	-3872.5	-248	108	VGS	-872.5	-248	158	DB[21]_Dummy	2790	-248
9	VCOM	-6812.5	-248	59	C11P	-3812.5	-248	109	EXTC	-812.5	-248	159	DB[22]_Dummy	2875	-248
10	VCOM	-6752.5	-248	60	C11M	-3752.5	-248	110	IM<3>	-752.5	-248	160	DB[23]_Dummy	2960	-248
11	DUMMY	-6692.5	-248	61	C11M	-3692.5	-248	111	IM<2>	-692.5	-248	161	DUMMY	3032.5	-248
12	C22P	-6632.5	-248	62	C11M	-3632.5	-248	112	IM<1>	-632.5	-248	162	VDDI	3092.5	-248
13	C22P	-6572.5	-248	63	C11M	-3572.5	-248	113	IM<0>	-572.5	-248	163	VDDI	3152.5	-248
14	C22M	-6512.5	-248	64	C11M	-3512.5	-248	114	RESX	-512.5	-248	164	VDDI	3212.5	-248
15	C22M	-6452.5	-248	65	C11M	-3452.5	-248	115	CSX	-452.5	-248	165	VDDI	3272.5	-248
16	C21P	-6392.5	-248	66	C11M	-3392.5	-248	116	DCX	-392.5	-248	166	VDDI	3332.5	-248
17	C21P	-6332.5	-248	67	(GND)	-3332.5	-248	117	WRX	-332.5	-248	167	VDDI	3392.5	-248
18	C21M	-6272.5	-248	68	(GND)	-3272.5	-248	118	RDX	-272.5	-248	168	VDDI	3452.5	-248
19	C21M	-6212.5	-248	69	(GND)	-3212.5	-248	119	DUMMY	-212.5	-248	169	Vcore	3512.5	-248
20	VGH	-6152.5	-248	70	(GND)	-3152.5	-248	120	VSYNC	-152.5	-248	170	Vcore	3572.5	-248
21	VGH	-6092.5	-248	71	(GND)	-3092.5	-248	121	HSYNC	-92.5	-248	171	Vcore	3632.5	-248
22	VGH	-6032.5	-248	72	(GND)	-3032.5	-248	122	ENABL	-32.5	-248	172	Vcore	3692.5	-248
23	VGH	-5972.5	-248	73	(GND)	-2972.5	-248	123	DOTCLK	27.5	-248	173	Vcore	3752.5	-248
24	VGH	-5912.5	-248	74	VCI	-2912.5	-248	124	DUMMY	87.5	-248	174	Vcore	3812.5	-248
25	DUMMY	-5852.5	-248	75	VCI	-2852.5	-248	125	SDA	160	-248	175	Vcore	3872.5	-248
26	VGL	-5792.5	-248	76	VCI	-2792.5	-248	126	DB[0]	245	-248	176	Vcore	3932.5	-248
27	VGL	-5732.5	-248	77	VCI	-2732.5	-248	127	DB[1]	330	-248	177	Vcore	3992.5	-248
28	VGL	-5672.5	-248	78	VCI	-2672.5	-248	128	DB[2]	415	-248	178	Vcore	4052.5	-248
29	VGL	-5612.5	-248	79	VCI	-2612.5	-248	129	DB[3]	500	-248	179	Vcore	4112.5	-248
30	VGL	-5552.5	-248	80	VCI	-2552.5	-248	130	DUMMY	572.5	-248	180	Vcore	4172.5	-248
31	VGL	-5492.5	-248	81	VCI	-2492.5	-248	131	DB[4]	645	-248	181	Vcore	4232.5	-248
32	DDVDH	-5432.5	-248	82	VSS3	-2432.5	-248	132	DB[5]	730	-248	182	Vcore	4292.5	-248
33	DDVDH	-5372.5	-248	83	VSS3	-2372.5	-248	133	DB[6]	815	-248	183	DUMMY	4352.5	-248
34	DDVDH	-5312.5	-248	84	VSS3	-2312.5	-248	134	DB[7]	900	-248	184	GVDD	4412.5	-248
35	DDVDH	-5252.5	-248	85	VSS	-2252.5	-248	135	DUMMY	972.5	-248	185	GVDD	4472.5	-248
36	DDVDH	-5192.5	-248	86	VSS	-2192.5	-248	136	DB[8]	1045	-248	186	GVDD	4532.5	-248
37	DDVDH	-5132.5	-248	87	VSS	-2132.5	-248	137	DB[9]	1130	-248	187	GVDD	4592.5	-248
38	DDVDH	-5072.5	-248	88	VSS	-2072.5	-248	138	DB[10]	1215	-248	188	DUMMY	4652.5	-248
39	C12P	-5012.5	-248	89	VSS	-2012.5	-248	139	DB[11]	1300	-248	189	DUMMY	4712.5	-248
40	C12P	-4952.5	-248	90	VSS	-1952.5	-248	140	DUMMY	1372.5	-248	190	VCL	4772.5	-248
41	C12P	-4892.5	-248	91	VSSC	-1892.5	-248	141	DB[12]	1445	-248	191	VCL	4832.5	-248
42	C12P	-4832.5	-248	92	VSSC	-1832.5	-248	142	DB[13]	1530	-248	192	VCL	4892.5	-248
43	C12P	-4772.5	-248	93	VSSC	-1772.5	-248	143	DB[14]	1615	-248	193	VCL	4952.5	-248
44	C12P	-4712.5	-248	94	VSSC	-1712.5	-248	144	DB[15]	1700	-248	194	VCL	5012.5	-248
45	C12P	-4652.5	-248	95	VSSC	-1652.5	-248	145	DUMMY	1772.5	-248	195	VCL	5072.5	-248
46	C12M	-4592.5	-248	96	VSSC	-1592.5	-248	146	DB[16]	1845	-248	196	VCL	5132.5	-248
47	C12M	-4532.5	-248	97	VSSC	-1532.5	-248	147	DB[17]	1930	-248	197	VCL	5192.5	-248
48	C12M	-4472.5	-248	98	VSSA	-1472.5	-248	148	DUMMY	2002.5	-248	198	DUMMY	5252.5	-248
49	C12M	-4412.5	-248	99	VSSA	-1412.5	-248	149	TE	2075	-248	199	DUMMY	5312.5	-248
50	C12M	-4352.5	-248	100	VSSA	-1352.5	-248	150	SDO	2160	-248	200	DUMMY	5372.5	-248

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
201	DUMMY	5432.5	-248	251	G32	7147	224	301	G132	6447	224	351	G232	5747	224
202	DUMMY	5492.5	-248	252	G34	7133	93	302	G134	6433	93	352	G234	5733	93
203	DUMMY	5552.5	-248	253	G36	7119	224	303	G136	6419	224	353	G236	5719	224
204	DUMMY	5612.5	-248	254	G38	7105	93	304	G138	6405	93	354	G238	5705	93
205	DUMMY	5672.5	-248	255	G40	7091	224	305	G140	6391	224	355	G240	5691	224
206	(GND)	5732.5	-248	256	G42	7077	93	306	G142	6377	93	356	G242	5677	93
207	(GND)	5792.5	-248	257	G44	7063	224	307	G144	6363	224	357	G244	5663	224
208	(GND)	5852.5	-248	258	G46	7049	93	308	G146	6349	93	358	G246	5649	93
209	(GND)	5912.5	-248	259	G48	7035	224	309	G148	6335	224	359	G248	5635	224
210	(GND)	5972.5	-248	260	G50	7021	93	310	G150	6321	93	360	G250	5621	93
211	(GND)	6032.5	-248	261	G52	7007	224	311	G152	6307	224	361	G252	5607	224
212	(GND)	6092.5	-248	262	G54	6993	93	312	G154	6293	93	362	G254	5593	93
213	(GND)	6152.5	-248	263	G56	6979	224	313	G156	6279	224	363	G256	5579	224
214	DUMMY	6212.5	-248	264	G58	6965	93	314	G158	6265	93	364	G258	5565	93
215	DUMMY	6272.5	-248	265	G60	6951	224	315	G160	6251	224	365	G260	5551	224
216	DUMMY	6332.5	-248	266	G62	6937	93	316	G162	6237	93	366	G262	5537	93
217	DUMMY	6392.5	-248	267	G64	6923	224	317	G164	6223	224	367	G264	5523	224
218	DUMMY	6452.5	-248	268	G66	6909	93	318	G166	6209	93	368	G266	5509	93
219	DUMMY	6512.5	-248	269	G68	6895	224	319	G168	6195	224	369	G268	5495	224
220	DUMMY	6572.5	-248	270	G70	6881	93	320	G170	6181	93	370	G270	5481	93
221	DUMMY	6632.5	-248	271	G72	6867	224	321	G172	6167	224	371	G272	5467	224
222	DUMMY	6692.5	-248	272	G74	6853	93	322	G174	6153	93	372	G274	5453	93
223	VCOM	6752.5	-248	273	G76	6839	224	323	G176	6139	224	373	G276	5439	224
224	VCOM	6812.5	-248	274	G78	6825	93	324	G178	6125	93	374	G278	5425	93
225	VCOM	6872.5	-248	275	G80	6811	224	325	G180	6111	224	375	G280	5411	224
226	VCOM	6932.5	-248	276	G82	6797	93	326	G182	6097	93	376	G282	5397	93
227	VCOM	6992.5	-248	277	G84	6783	224	327	G184	6083	224	377	G284	5383	224
228	VCOM	7052.5	-248	278	G86	6769	93	328	G186	6069	93	378	G286	5369	93
229	VCOM	7112.5	-248	279	G88	6755	224	329	G188	6055	224	379	G288	5355	224
230	VCOM	7172.5	-248	280	G90	6741	93	330	G190	6041	93	380	G290	5341	93
231	INT_TEST1	7232.5	-248	281	G92	6727	224	331	G192	6027	224	381	G292	5327	224
232	INT_TEST2	7292.5	-248	282	G94	6713	93	332	G194	6013	93	382	G294	5313	93
233	DUMMY	7399	224	283	G96	6699	224	333	G196	5999	224	383	G296	5299	224
234	DUMMY	7385	93	284	G98	6685	93	334	G198	5985	93	384	G298	5285	93
235	DUMMY	7371	224	285	G100	6671	224	335	G200	5971	224	385	G300	5271	224
236	G2	7357	93	286	G102	6657	93	336	G202	5957	93	386	G302	5257	93
237	G4	7343	224	287	G104	6643	224	337	G204	5943	224	387	G304	5243	224
238	G6	7329	93	288	G106	6629	93	338	G206	5929	93	388	G306	5229	93
239	G8	7315	224	289	G108	6615	224	339	G208	5915	224	389	G308	5215	224
240	G10	7301	93	290	G110	6601	93	340	G210	5901	93	390	G310	5201	93
241	G12	7287	224	291	G112	6587	224	341	G212	5887	224	391	G312	5187	224
242	G14	7273	93	292	G114	6573	93	342	G214	5873	93	392	G314	5173	93
243	G16	7259	224	293	G116	6559	224	343	G216	5859	224	393	G316	5159	224
244	G18	7245	93	294	G118	6545	93	344	G218	5845	93	394	G318	5145	93
245	G20	7231	224	295	G120	6531	224	345	G220	5831	224	395	G320	5131	224
246	G22	7217	93	296	G122	6517	93	346	G222	5817	93	396	S720	5075	93
247	G24	7203	224	297	G124	6503	224	347	G224	5803	224	397	S719	5061	224
248	G26	7189	93	298	G126	6489	93	348	G226	5789	93	398	S718	5047	93
249	G28	7175	224	299	G128	6475	224	349	G228	5775	224	399	S717	5033	224
250	G30	7161	93	300	G130	6461	93	350	G230	5761	93	400	S716	5019	93

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No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
401	S715	5005	224	451	S665	4305	224	501	S615	3605	224	551	S565	2905	224
402	S714	4991	93	452	S664	4291	93	502	S614	3591	93	552	S564	2891	93
403	S713	4977	224	453	S663	4277	224	503	S613	3577	224	553	S563	2877	224
404	S712	4963	93	454	S662	4263	93	504	S612	3563	93	554	S562	2863	93
405	S711	4949	224	455	S661	4249	224	505	S611	3549	224	555	S561	2849	224
406	S710	4935	93	456	S660	4235	93	506	S610	3535	93	556	S560	2835	93
407	S709	4921	224	457	S659	4221	224	507	S609	3521	224	557	S559	2821	224
408	S708	4907	93	458	S658	4207	93	508	S608	3507	93	558	S558	2807	93
409	S707	4893	224	459	S657	4193	224	509	S607	3493	224	559	S557	2793	224
410	S706	4879	93	460	S656	4179	93	510	S606	3479	93	560	S556	2779	93
411	S705	4865	224	461	S655	4165	224	511	S605	3465	224	561	S555	2765	224
412	S704	4851	93	462	S654	4151	93	512	S604	3451	93	562	S554	2751	93
413	S703	4837	224	463	S653	4137	224	513	S603	3437	224	563	S553	2737	224
414	S702	4823	93	464	S652	4123	93	514	S602	3423	93	564	S552	2723	93
415	S701	4809	224	465	S651	4109	224	515	S601	3409	224	565	S551	2709	224
416	S700	4795	93	466	S650	4095	93	516	S600	3395	93	566	S550	2695	93
417	S699	4781	224	467	S649	4081	224	517	S599	3381	224	567	S549	2681	224
418	S698	4767	93	468	S648	4067	93	518	S598	3367	93	568	S548	2667	93
419	S697	4753	224	469	S647	4053	224	519	S597	3353	224	569	S547	2653	224
420	S696	4739	93	470	S646	4039	93	520	S596	3339	93	570	S546	2639	93
421	S695	4725	224	471	S645	4025	224	521	S595	3325	224	571	S545	2625	224
422	S694	4711	93	472	S644	4011	93	522	S594	3311	93	572	S544	2611	93
423	S693	4697	224	473	S643	3997	224	523	S593	3297	224	573	S543	2597	224
424	S692	4683	93	474	S642	3983	93	524	S592	3283	93	574	S542	2583	93
425	S691	4669	224	475	S641	3969	224	525	S591	3269	224	575	S541	2569	224
426	S690	4655	93	476	S640	3955	93	526	S590	3255	93	576	S540	2555	93
427	S689	4641	224	477	S639	3941	224	527	S589	3241	224	577	S539	2541	224
428	S688	4627	93	478	S638	3927	93	528	S588	3227	93	578	S538	2527	93
429	S687	4613	224	479	S637	3913	224	529	S587	3213	224	579	S537	2513	224
430	S686	4599	93	480	S636	3899	93	530	S586	3199	93	580	S536	2499	93
431	S685	4585	224	481	S635	3885	224	531	S585	3185	224	581	S535	2485	224
432	S684	4571	93	482	S634	3871	93	532	S584	3171	93	582	S534	2471	93
433	S683	4557	224	483	S633	3857	224	533	S583	3157	224	583	S533	2457	224
434	S682	4543	93	484	S632	3843	93	534	S582	3143	93	584	S532	2443	93
435	S681	4529	224	485	S631	3829	224	535	S581	3129	224	585	S531	2429	224
436	S680	4515	93	486	S630	3815	93	536	S580	3115	93	586	S530	2415	93
437	S679	4501	224	487	S629	3801	224	537	S579	3101	224	587	S529	2401	224
438	S678	4487	93	488	S628	3787	93	538	S578	3087	93	588	S528	2387	93
439	S677	4473	224	489	S627	3773	224	539	S577	3073	224	589	S527	2373	224
440	S676	4459	93	490	S626	3759	93	540	S576	3059	93	590	S526	2359	93
441	S675	4445	224	491	S625	3745	224	541	S575	3045	224	591	S525	2345	224
442	S674	4431	93	492	S624	3731	93	542	S574	3031	93	592	S524	2331	93
443	S673	4417	224	493	S623	3717	224	543	S573	3017	224	593	S523	2317	224
444	S672	4403	93	494	S622	3703	93	544	S572	3003	93	594	S522	2303	93
445	S671	4389	224	495	S621	3689	224	545	S571	2989	224	595	S521	2289	224
446	S670	4375	93	496	S620	3675	93	546	S570	2975	93	596	S520	2275	93
447	S669	4361	224	497	S619	3661	224	547	S569	2961	224	597	S519	2261	224
448	S668	4347	93	498	S618	3647	93	548	S568	2947	93	598	S518	2247	93
449	S667	4333	224	499	S617	3633	224	549	S567	2933	224	599	S517	2233	224
450	S666	4319	93	500	S616	3619	93	550	S566	2919	93	600	S516	2219	93

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No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
601	S515	2205	224	651	S465	1505	224	701	S415	805	224	751	S365	105	224
602	S514	2191	93	652	S464	1491	93	702	S414	791	93	752	S364	91	93
603	S513	2177	224	653	S463	1477	224	703	S413	777	224	753	S363	77	224
604	S512	2163	93	654	S462	1463	93	704	S412	763	93	754	S362	63	93
605	S511	2149	224	655	S461	1449	224	705	S411	749	224	755	S361	49	224
606	S510	2135	93	656	S460	1435	93	706	S410	735	93	756	S360	-49	93
607	S509	2121	224	657	S459	1421	224	707	S409	721	224	757	S359	-63	224
608	S508	2107	93	658	S458	1407	93	708	S408	707	93	758	S358	-77	93
609	S507	2093	224	659	S457	1393	224	709	S407	693	224	759	S357	-91	224
610	S506	2079	93	660	S456	1379	93	710	S406	679	93	760	S356	-105	93
611	S505	2065	224	661	S455	1365	224	711	S405	665	224	761	S355	-119	224
612	S504	2051	93	662	S454	1351	93	712	S404	651	93	762	S354	-133	93
613	S503	2037	224	663	S453	1337	224	713	S403	637	224	763	S353	-147	224
614	S502	2023	93	664	S452	1323	93	714	S402	623	93	764	S352	-161	93
615	S501	2009	224	665	S451	1309	224	715	S401	609	224	765	S351	-175	224
616	S500	1995	93	666	S450	1295	93	716	S400	595	93	766	S350	-189	93
617	S499	1981	224	667	S449	1281	224	717	S399	581	224	767	S349	-203	224
618	S498	1967	93	668	S448	1267	93	718	S398	567	93	768	S348	-217	93
619	S497	1953	224	669	S447	1253	224	719	S397	553	224	769	S347	-231	224
620	S496	1939	93	670	S446	1239	93	720	S396	539	93	770	S346	-245	93
621	S495	1925	224	671	S445	1225	224	721	S395	525	224	771	S345	-259	224
622	S494	1911	93	672	S444	1211	93	722	S394	511	93	772	S344	-273	93
623	S493	1897	224	673	S443	1197	224	723	S393	497	224	773	S343	-287	224
624	S492	1883	93	674	S442	1183	93	724	S392	483	93	774	S342	-301	93
625	S491	1869	224	675	S441	1169	224	725	S391	469	224	775	S341	-315	224
626	S490	1855	93	676	S440	1155	93	726	S390	455	93	776	S340	-329	93
627	S489	1841	224	677	S439	1141	224	727	S389	441	224	777	S339	-343	224
628	S488	1827	93	678	S438	1127	93	728	S388	427	93	778	S338	-357	93
629	S487	1813	224	679	S437	1113	224	729	S387	413	224	779	S337	-371	224
630	S486	1799	93	680	S436	1099	93	730	S386	399	93	780	S336	-385	93
631	S485	1785	224	681	S435	1085	224	731	S385	385	224	781	S335	-399	224
632	S484	1771	93	682	S434	1071	93	732	S384	371	93	782	S334	-413	93
633	S483	1757	224	683	S433	1057	224	733	S383	357	224	783	S333	-427	224
634	S482	1743	93	684	S432	1043	93	734	S382	343	93	784	S332	-441	93
635	S481	1729	224	685	S431	1029	224	735	S381	329	224	785	S331	-455	224
636	S480	1715	93	686	S430	1015	93	736	S380	315	93	786	S330	-469	93
637	S479	1701	224	687	S429	1001	224	737	S379	301	224	787	S329	-483	224
638	S478	1687	93	688	S428	987	93	738	S378	287	93	788	S328	-497	93
639	S477	1673	224	689	S427	973	224	739	S377	273	224	789	S327	-511	224
640	S476	1659	93	690	S426	959	93	740	S376	259	93	790	S326	-525	93
641	S475	1645	224	691	S425	945	224	741	S375	245	224	791	S325	-539	224
642	S474	1631	93	692	S424	931	93	742	S374	231	93	792	S324	-553	93
643	S473	1617	224	693	S423	917	224	743	S373	217	224	793	S323	-567	224
644	S472	1603	93	694	S422	903	93	744	S372	203	93	794	S322	-581	93
645	S471	1589	224	695	S421	889	224	745	S371	189	224	795	S321	-595	224
646	S470	1575	93	696	S420	875	93	746	S370	175	93	796	S320	-609	93
647	S469	1561	224	697	S419	861	224	747	S369	161	224	797	S319	-623	224
648	S468	1547	93	698	S418	847	93	748	S368	147	93	798	S318	-637	93
649	S467	1533	224	699	S417	833	224	749	S367	133	224	799	S317	-651	224
650	S466	1519	93	700	S416	819	93	750	S366	119	93	800	S316	-665	93

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No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
801	S315	-679	224	851	S265	-1379	224	901	S215	-2079	224	951	S165	-2779	224
802	S314	-693	93	852	S264	-1393	93	902	S214	-2093	93	952	S164	-2793	93
803	S313	-707	224	853	S263	-1407	224	903	S213	-2107	224	953	S163	-2807	224
804	S312	-721	93	854	S262	-1421	93	904	S212	-2121	93	954	S162	-2821	93
805	S311	-735	224	855	S261	-1435	224	905	S211	-2135	224	955	S161	-2835	224
806	S310	-749	93	856	S260	-1449	93	906	S210	-2149	93	956	S160	-2849	93
807	S309	-763	224	857	S259	-1463	224	907	S209	-2163	224	957	S159	-2863	224
808	S308	-777	93	858	S258	-1477	93	908	S208	-2177	93	958	S158	-2877	93
809	S307	-791	224	859	S257	-1491	224	909	S207	-2191	224	959	S157	-2891	224
810	S306	-805	93	860	S256	-1505	93	910	S206	-2205	93	960	S156	-2905	93
811	S305	-819	224	861	S255	-1519	224	911	S205	-2219	224	961	S155	-2919	224
812	S304	-833	93	862	S254	-1533	93	912	S204	-2233	93	962	S154	-2933	93
813	S303	-847	224	863	S253	-1547	224	913	S203	-2247	224	963	S153	-2947	224
814	S302	-861	93	864	S252	-1561	93	914	S202	-2261	93	964	S152	-2961	93
815	S301	-875	224	865	S251	-1575	224	915	S201	-2275	224	965	S151	-2975	224
816	S300	-889	93	866	S250	-1589	93	916	S200	-2289	93	966	S150	-2989	93
817	S299	-903	224	867	S249	-1603	224	917	S199	-2303	224	967	S149	-3003	224
818	S298	-917	93	868	S248	-1617	93	918	S198	-2317	93	968	S148	-3017	93
819	S297	-931	224	869	S247	-1631	224	919	S197	-2331	224	969	S147	-3031	224
820	S296	-945	93	870	S246	-1645	93	920	S196	-2345	93	970	S146	-3045	93
821	S295	-959	224	871	S245	-1659	224	921	S195	-2359	224	971	S145	-3059	224
822	S294	-973	93	872	S244	-1673	93	922	S194	-2373	93	972	S144	-3073	93
823	S293	-987	224	873	S243	-1687	224	923	S193	-2387	224	973	S143	-3087	224
824	S292	-1001	93	874	S242	-1701	93	924	S192	-2401	93	974	S142	-3101	93
825	S291	-1015	224	875	S241	-1715	224	925	S191	-2415	224	975	S141	-3115	224
826	S290	-1029	93	876	S240	-1729	93	926	S190	-2429	93	976	S140	-3129	93
827	S289	-1043	224	877	S239	-1743	224	927	S189	-2443	224	977	S139	-3143	224
828	S288	-1057	93	878	S238	-1757	93	928	S188	-2457	93	978	S138	-3157	93
829	S287	-1071	224	879	S237	-1771	224	929	S187	-2471	224	979	S137	-3171	224
830	S286	-1085	93	880	S236	-1785	93	930	S186	-2485	93	980	S136	-3185	93
831	S285	-1099	224	881	S235	-1799	224	931	S185	-2499	224	981	S135	-3199	224
832	S284	-1113	93	882	S234	-1813	93	932	S184	-2513	93	982	S134	-3213	93
833	S283	-1127	224	883	S233	-1827	224	933	S183	-2527	224	983	S133	-3227	224
834	S282	-1141	93	884	S232	-1841	93	934	S182	-2541	93	984	S132	-3241	93
835	S281	-1155	224	885	S231	-1855	224	935	S181	-2555	224	985	S131	-3255	224
836	S280	-1169	93	886	S230	-1869	93	936	S180	-2569	93	986	S130	-3269	93
837	S279	-1183	224	887	S229	-1883	224	937	S179	-2583	224	987	S129	-3283	224
838	S278	-1197	93	888	S228	-1897	93	938	S178	-2597	93	988	S128	-3297	93
839	S277	-1211	224	889	S227	-1911	224	939	S177	-2611	224	989	S127	-3311	224
840	S276	-1225	93	890	S226	-1925	93	940	S176	-2625	93	990	S126	-3325	93
841	S275	-1239	224	891	S225	-1939	224	941	S175	-2639	224	991	S125	-3339	224
842	S274	-1253	93	892	S224	-1953	93	942	S174	-2653	93	992	S124	-3353	93
843	S273	-1267	224	893	S223	-1967	224	943	S173	-2667	224	993	S123	-3367	224
844	S272	-1281	93	894	S222	-1981	93	944	S172	-2681	93	994	S122	-3381	93
845	S271	-1295	224	895	S221	-1995	224	945	S171	-2695	224	995	S121	-3395	224
846	S270	-1309	93	896	S220	-2009	93	946	S170	-2709	93	996	S120	-3409	93
847	S269	-1323	224	897	S219	-2023	224	947	S169	-2723	224	997	S119	-3423	224
848	S268	-1337	93	898	S218	-2037	93	948	S168	-2737	93	998	S118	-3437	93
849	S267	-1351	224	899	S217	-2051	224	949	S167	-2751	224	999	S117	-3451	224
850	S266	-1365	93	900	S216	-2065	93	950	S166	-2765	93	1000	S116	-3465	93

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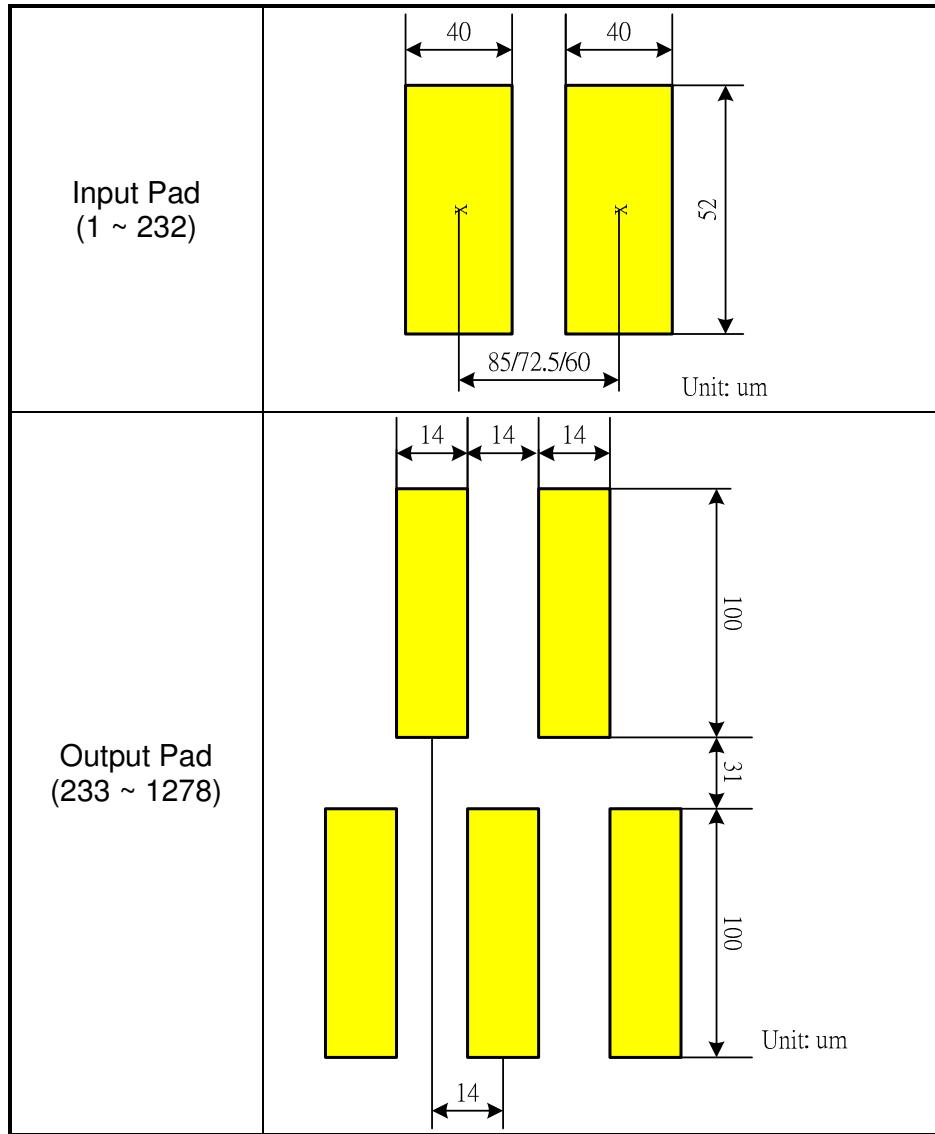
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1001	S115	-3479	224	1051	S65	-4179	224	1101	S15	-4879	224	1151	G249	-5621	224
1002	S114	-3493	93	1052	S64	-4193	93	1102	S14	-4893	93	1152	G247	-5635	93
1003	S113	-3507	224	1053	S63	-4207	224	1103	S13	-4907	224	1153	G245	-5649	224
1004	S112	-3521	93	1054	S62	-4221	93	1104	S12	-4921	93	1154	G243	-5663	93
1005	S111	-3535	224	1055	S61	-4235	224	1105	S11	-4935	224	1155	G241	-5677	224
1006	S110	-3549	93	1056	S60	-4249	93	1106	S10	-4949	93	1156	G239	-5691	93
1007	S109	-3563	224	1057	S59	-4263	224	1107	S9	-4963	224	1157	G237	-5705	224
1008	S108	-3577	93	1058	S58	-4277	93	1108	S8	-4977	93	1158	G235	-5719	93
1009	S107	-3591	224	1059	S57	-4291	224	1109	S7	-4991	224	1159	G233	-5733	224
1010	S106	-3605	93	1060	S56	-4305	93	1110	S6	-5005	93	1160	G231	-5747	93
1011	S105	-3619	224	1061	S55	-4319	224	1111	S5	-5019	224	1161	G229	-5761	224
1012	S104	-3633	93	1062	S54	-4333	93	1112	S4	-5033	93	1162	G227	-5775	93
1013	S103	-3647	224	1063	S53	-4347	224	1113	S3	-5047	224	1163	G225	-5789	224
1014	S102	-3661	93	1064	S52	-4361	93	1114	S2	-5061	93	1164	G223	-5803	93
1015	S101	-3675	224	1065	S51	-4375	224	1115	S1	-5075	224	1165	G221	-5817	224
1016	S100	-3689	93	1066	S50	-4389	93	1116	G319	-5131	93	1166	G219	-5831	93
1017	S99	-3703	224	1067	S49	-4403	224	1117	G317	-5145	224	1167	G217	-5845	224
1018	S98	-3717	93	1068	S48	-4417	93	1118	G315	-5159	93	1168	G215	-5859	93
1019	S97	-3731	224	1069	S47	-4431	224	1119	G313	-5173	224	1169	G213	-5873	224
1020	S96	-3745	93	1070	S46	-4445	93	1120	G311	-5187	93	1170	G211	-5887	93
1021	S95	-3759	224	1071	S45	-4459	224	1121	G309	-5201	224	1171	G209	-5901	224
1022	S94	-3773	93	1072	S44	-4473	93	1122	G307	-5215	93	1172	G207	-5915	93
1023	S93	-3787	224	1073	S43	-4487	224	1123	G305	-5229	224	1173	G205	-5929	224
1024	S92	-3801	93	1074	S42	-4501	93	1124	G303	-5243	93	1174	G203	-5943	93
1025	S91	-3815	224	1075	S41	-4515	224	1125	G301	-5257	224	1175	G201	-5957	224
1026	S90	-3829	93	1076	S40	-4529	93	1126	G299	-5271	93	1176	G199	-5971	93
1027	S89	-3843	224	1077	S39	-4543	224	1127	G297	-5285	224	1177	G197	-5985	224
1028	S88	-3857	93	1078	S38	-4557	93	1128	G295	-5299	93	1178	G195	-5999	93
1029	S87	-3871	224	1079	S37	-4571	224	1129	G293	-5313	224	1179	G193	-6013	224
1030	S86	-3885	93	1080	S36	-4585	93	1130	G291	-5327	93	1180	G191	-6027	93
1031	S85	-3899	224	1081	S35	-4599	224	1131	G289	-5341	224	1181	G189	-6041	224
1032	S84	-3913	93	1082	S34	-4613	93	1132	G287	-5355	93	1182	G187	-6055	93
1033	S83	-3927	224	1083	S33	-4627	224	1133	G285	-5369	224	1183	G185	-6069	224
1034	S82	-3941	93	1084	S32	-4641	93	1134	G283	-5383	93	1184	G183	-6083	93
1035	S81	-3955	224	1085	S31	-4655	224	1135	G281	-5397	224	1185	G181	-6097	224
1036	S80	-3969	93	1086	S30	-4669	93	1136	G279	-5411	93	1186	G179	-6111	93
1037	S79	-3983	224	1087	S29	-4683	224	1137	G277	-5425	224	1187	G177	-6125	224
1038	S78	-3997	93	1088	S28	-4697	93	1138	G275	-5439	93	1188	G175	-6139	93
1039	S77	-4011	224	1089	S27	-4711	224	1139	G273	-5453	224	1189	G173	-6153	224
1040	S76	-4025	93	1090	S26	-4725	93	1140	G271	-5467	93	1190	G171	-6167	93
1041	S75	-4039	224	1091	S25	-4739	224	1141	G269	-5481	224	1191	G169	-6181	224
1042	S74	-4053	93	1092	S24	-4753	93	1142	G267	-5495	93	1192	G167	-6195	93
1043	S73	-4067	224	1093	S23	-4767	224	1143	G265	-5509	224	1193	G165	-6209	224
1044	S72	-4081	93	1094	S22	-4781	93	1144	G263	-5523	93	1194	G163	-6223	93
1045	S71	-4095	224	1095	S21	-4795	224	1145	G261	-5537	224	1195	G161	-6237	224
1046	S70	-4109	93	1096	S20	-4809	93	1146	G259	-5551	93	1196	G159	-6251	93
1047	S69	-4123	224	1097	S19	-4823	224	1147	G257	-5565	224	1197	G157	-6265	224
1048	S68	-4137	93	1098	S18	-4837	93	1148	G255	-5579	93	1198	G155	-6279	93
1049	S67	-4151	224	1099	S17	-4851	224	1149	G253	-5593	224	1199	G153	-6293	224
1050	S66	-4165	93	1100	S16	-4865	93	1150	G251	-5607	93	1200	G151	-6307	93

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No.	Pad name	X	Y	No.	Pad name	X	Y
1201	G149	-6321	224	1251	G49	-7021	224
1202	G147	-6335	93	1252	G47	-7035	93
1203	G145	-6349	224	1253	G45	-7049	224
1204	G143	-6363	93	1254	G43	-7063	93
1205	G141	-6377	224	1255	G41	-7077	224
1206	G139	-6391	93	1256	G39	-7091	93
1207	G137	-6405	224	1257	G37	-7105	224
1208	G135	-6419	93	1258	G35	-7119	93
1209	G133	-6433	224	1259	G33	-7133	224
1210	G131	-6447	93	1260	G31	-7147	93
1211	G129	-6461	224	1261	G29	-7161	224
1212	G127	-6475	93	1262	G27	-7175	93
1213	G125	-6489	224	1263	G25	-7189	224
1214	G123	-6503	93	1264	G23	-7203	93
1215	G121	-6517	224	1265	G21	-7217	224
1216	G119	-6531	93	1266	G19	-7231	93
1217	G117	-6545	224	1267	G17	-7245	224
1218	G115	-6559	93	1268	G15	-7259	93
1219	G113	-6573	224	1269	G13	-7273	224
1220	G111	-6587	93	1270	G11	-7287	93
1221	G109	-6601	224	1271	G9	-7301	224
1222	G107	-6615	93	1272	G7	-7315	93
1223	G105	-6629	224	1273	G5	-7329	224
1224	G103	-6643	93	1274	G3	-7343	93
1225	G101	-6657	224	1275	G1	-7357	224
1226	G99	-6671	93	1276	DUMMY	-7371	93
1227	G97	-6685	224	1277	DUMMY	-7385	224
1228	G95	-6699	93	1278	DUMMY	-7399	93
1229	G93	-6713	224				
1230	G91	-6727	93				
1231	G89	-6741	224				
1232	G87	-6755	93				
1233	G85	-6769	224				
1234	G83	-6783	93				
1235	G81	-6797	224				
1236	G79	-6811	93				
1237	G77	-6825	224				
1238	G75	-6839	93				
1239	G73	-6853	224				
1240	G71	-6867	93				
1241	G69	-6881	224				
1242	G67	-6895	93				
1243	G65	-6909	224				
1244	G63	-6923	93				
1245	G61	-6937	224				
1246	G59	-6951	93				
1247	G57	-6965	224				
1248	G55	-6979	93				
1249	G53	-6993	224				
1250	G51	-7007	93				

Alignment mark	X	Y
Left COG Align	-7480	225
Right COG Align	7480	225

## BUMP Size



## 6. Block Function Description

### MCU System Interface

ILI9341 provides four kinds of MCU system interface with 8080- I /8080- II series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,D/CX,SDO, CSX	

In 8080- I /8080- II series parallel interface, the registers are accessed by the D[17:0] data pins.

8080- I Series				8080- II Series				Operation
CSX	D/CX	RDX	WRX	CSX	D/CX	RDX	WRX	
"L"	"L"	"H"	◻	"L"	"L"	"H"	◻	Write command
"L"	"H"	◻	"H"	"L"	"H"	◻	"H"	Read parameter
"L"	"H"	"H"	◻	"L"	"H"	"H"	◻	Write parameter

### Parallel RGB Interface

ILI9341 also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

### Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

### Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9341 can display maximum 262,144 colors.

**Power Supply Circuit**

The LCD drive power supply circuit generates the voltage levels as GVDD, VGH, VGL and VCOM for driving TFT LCD panel.

**Timing controller**

The timing controller generates all the timing signals for display and GRAM access.

**Oscillator**

ILI9341 incorporates RC oscillator circuit and output a stable output frequency for operation.

**Panel Driver Circuit**

Liquid crystal display driver circuit consists of 720-output source driver (S1~S720), 320-output gate driver (G1~G320), and VCOM signal.

## 7. Function Description

### 7.1. MCU interfaces

ILI9341 provides the 8-/9-/16-/18-bit parallel system interface for 8080- I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

#### 7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO,CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,D/CX,SDO,CSX	

### 7.1.2. 8080- I Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080- I series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080- I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080- I Interface selection is done when IM3 pin is low state (VSS level). Interface bus width can be selected by IM [2:0] bits.

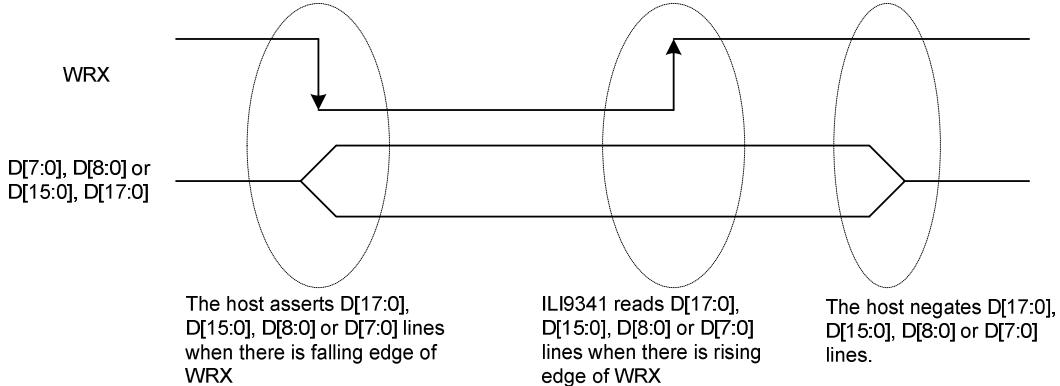
The selection of 8080- I series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
0	0	0	0	8080 MCU 8-bit bus interface I	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 16-bit bus interface I	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
0	0	1	0	8080 MCU 9-bit bus interface I	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface I	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.

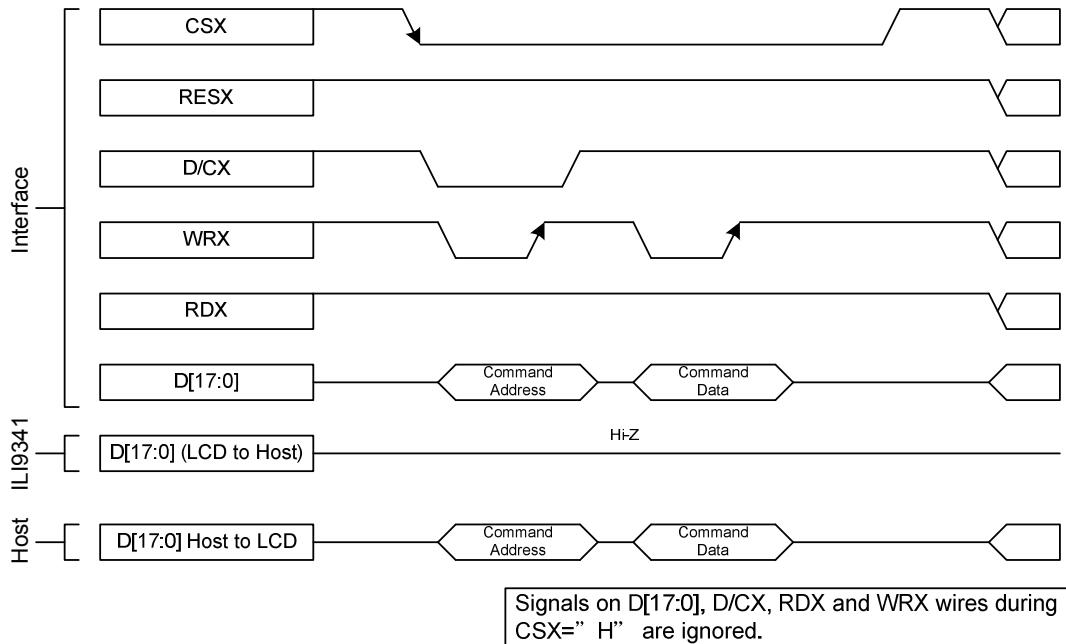
### 7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080- I<sub>2</sub>MCU interface.



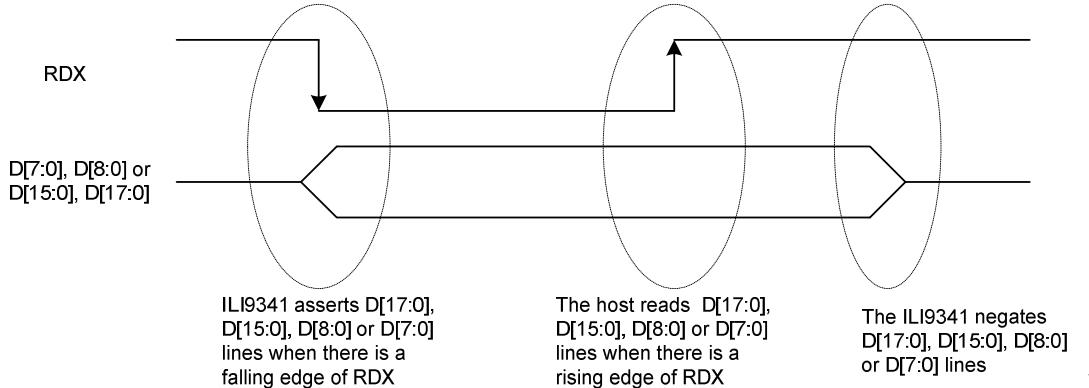
Note: WRX is an unsynchronized signal (It can be stopped)



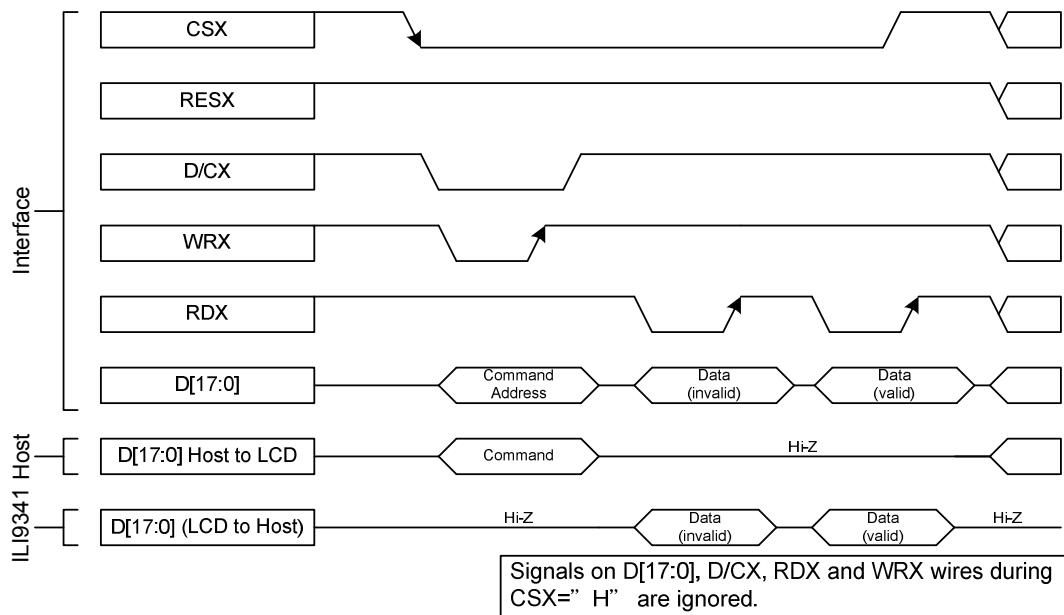
#### 7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- I<sub>M</sub> MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

### 7.1.5. 8080-II Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080-II series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-II Interface selection is done when IM3 pin is high state (VDDI level). Interface bus width can be selected by IM [2:0] bits.

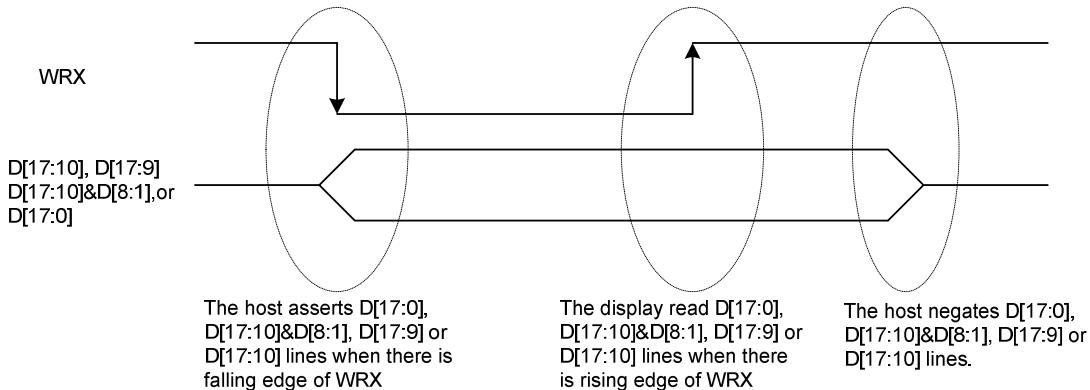
The selection of 8080-II series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
1	0	0	0	8080 MCU 16-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
1	0	0	1	8080 MCU 8-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
1	0	1	0	8080 MCU 18-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.

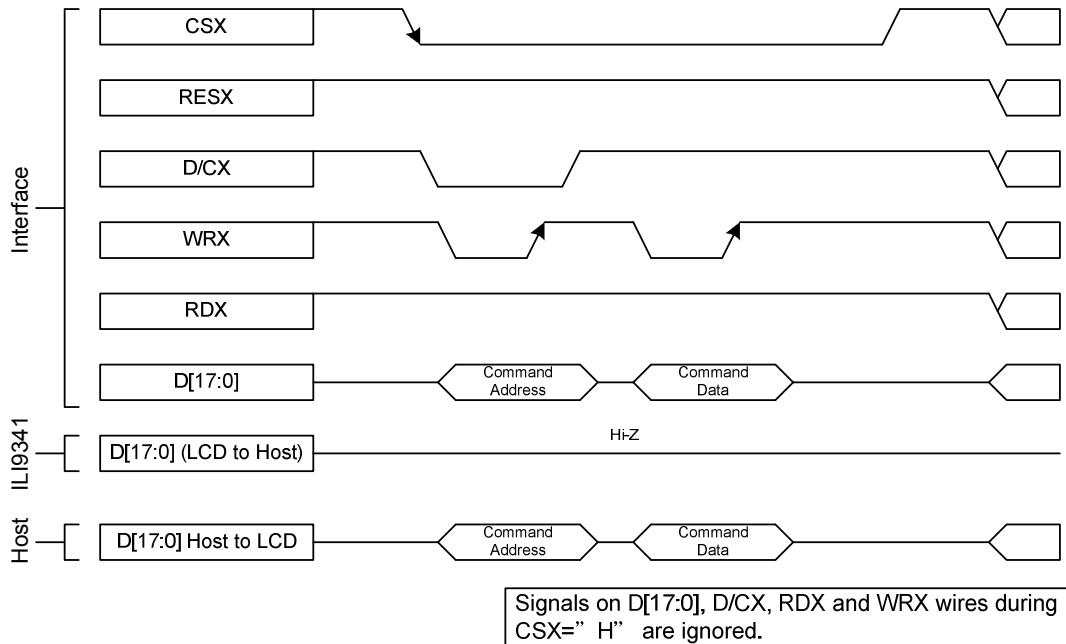
### 7.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-II MCU interface.



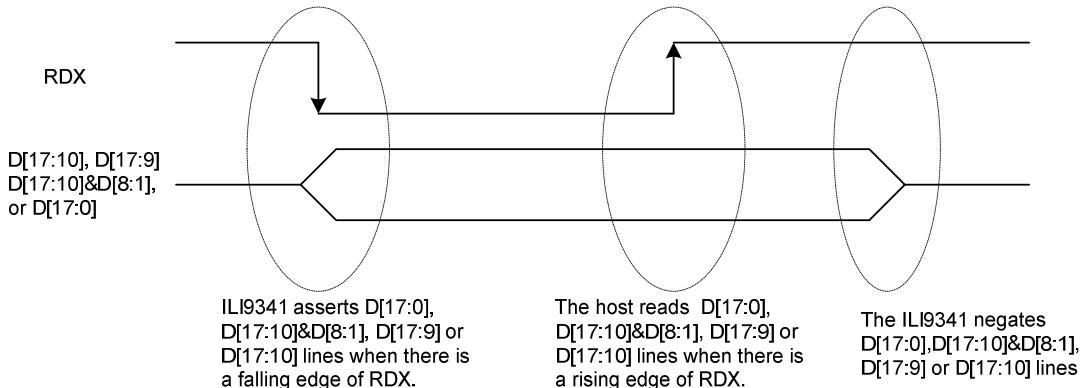
Note: WRX is an unsynchronized signal (It can be stopped)



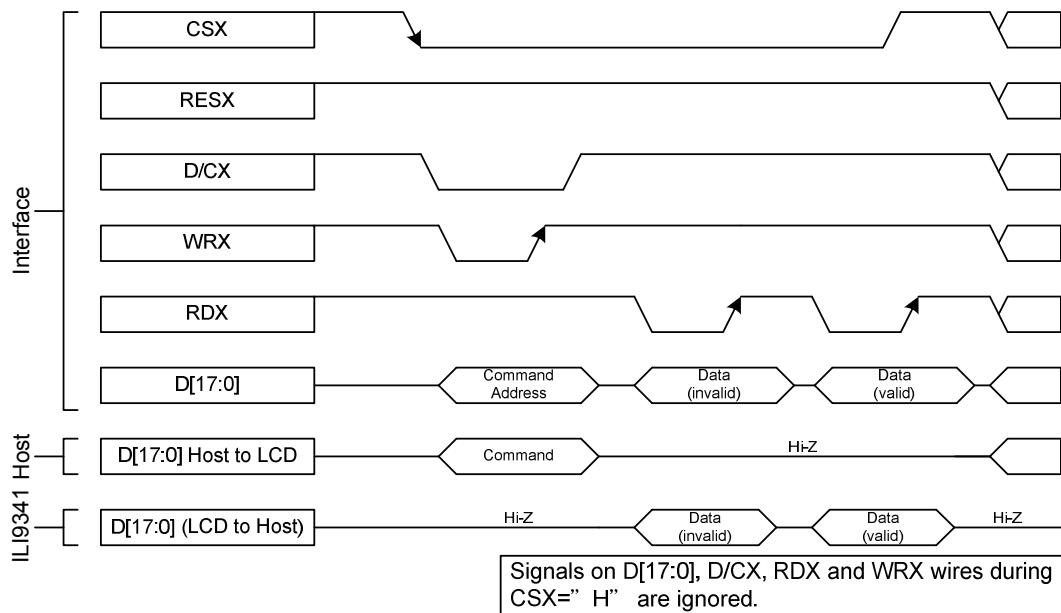
### 7.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-II MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

### 7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	"L"	-	↓	Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	"L"	'H/L"	↓	Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	"L"	-	↓	Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	"L"	'H/L"	↓	Read/Write command, parameter or display data.

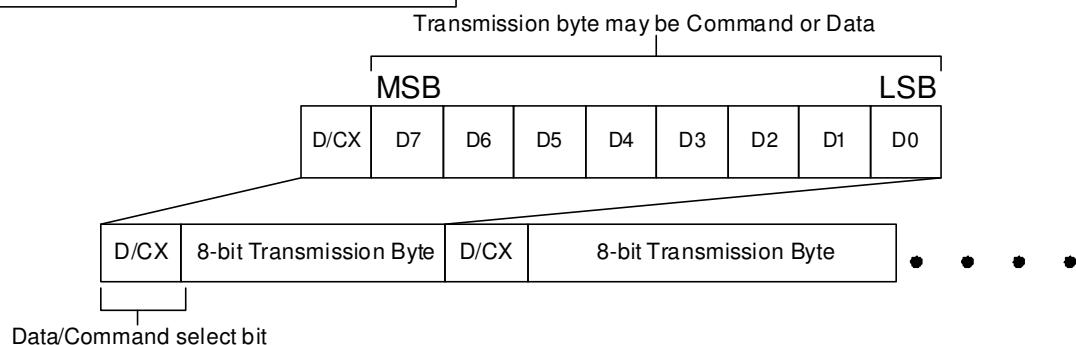
ILI9341 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9341. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

### 7.1.9. Write Cycle Sequence

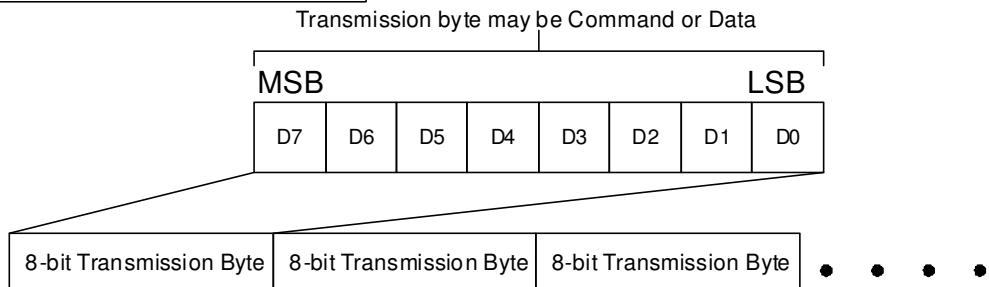
The write mode of the interface means that host writes commands or data to ILI9341. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to ILI9341 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

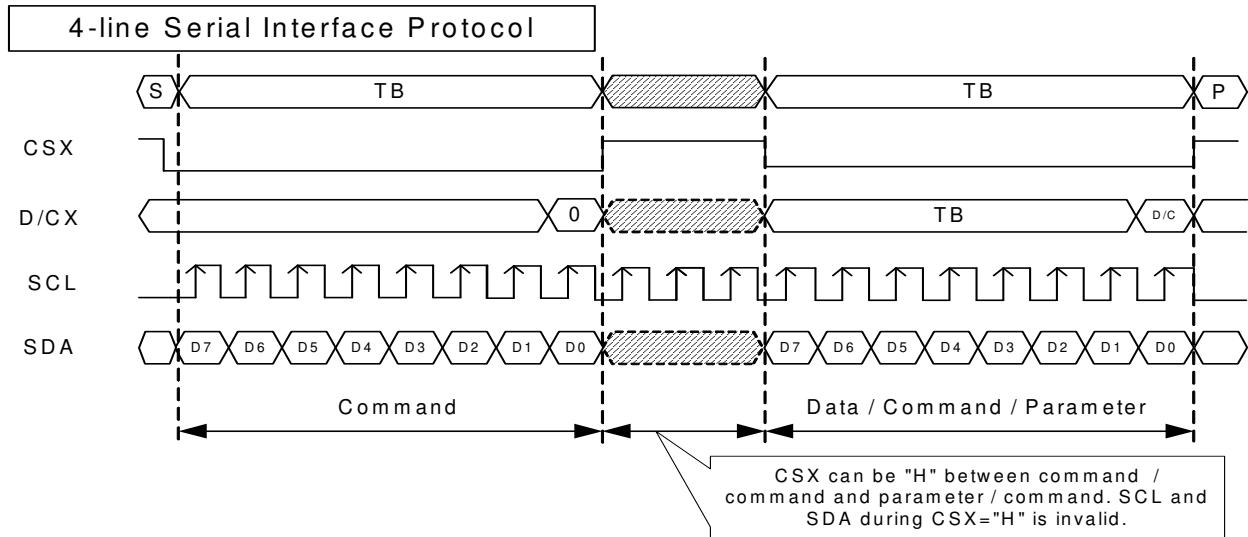
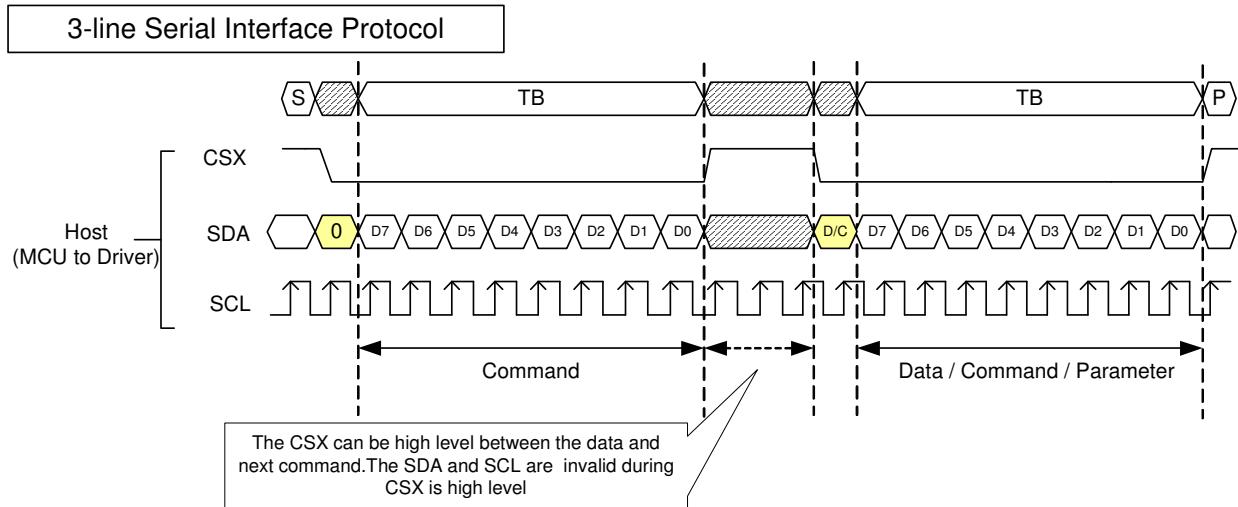
#### Data Format for 3-line Serial Interface



## Data Format for 4-line Serial Interface



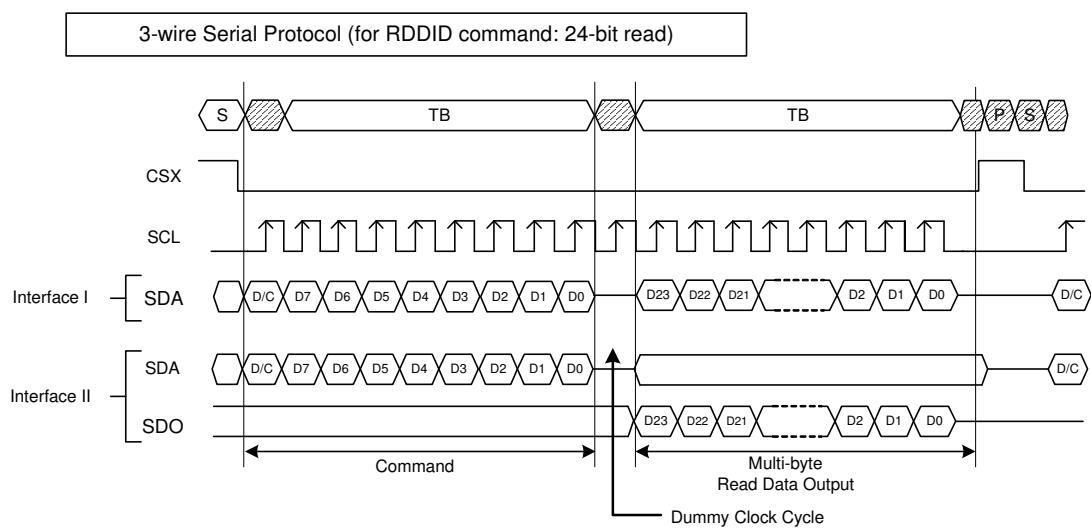
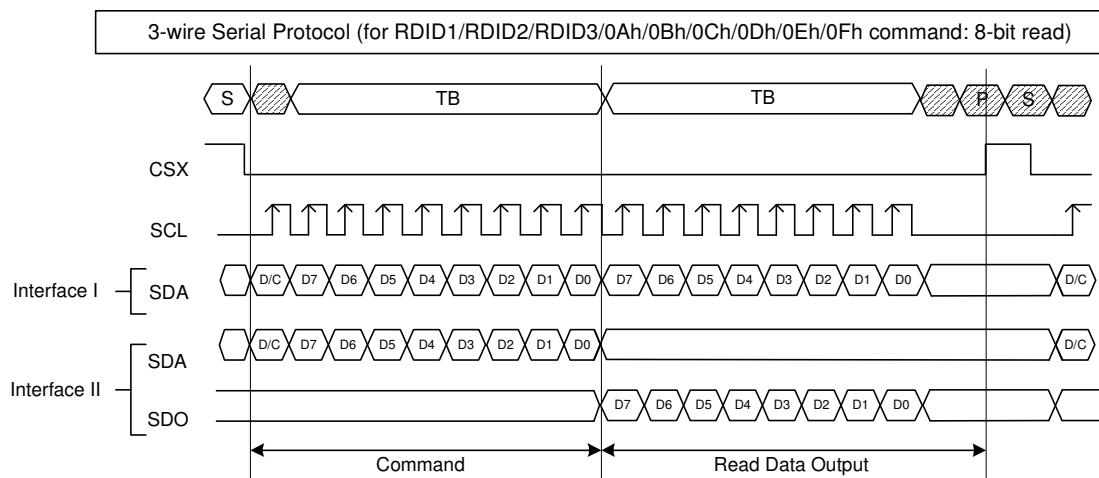
Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9341 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

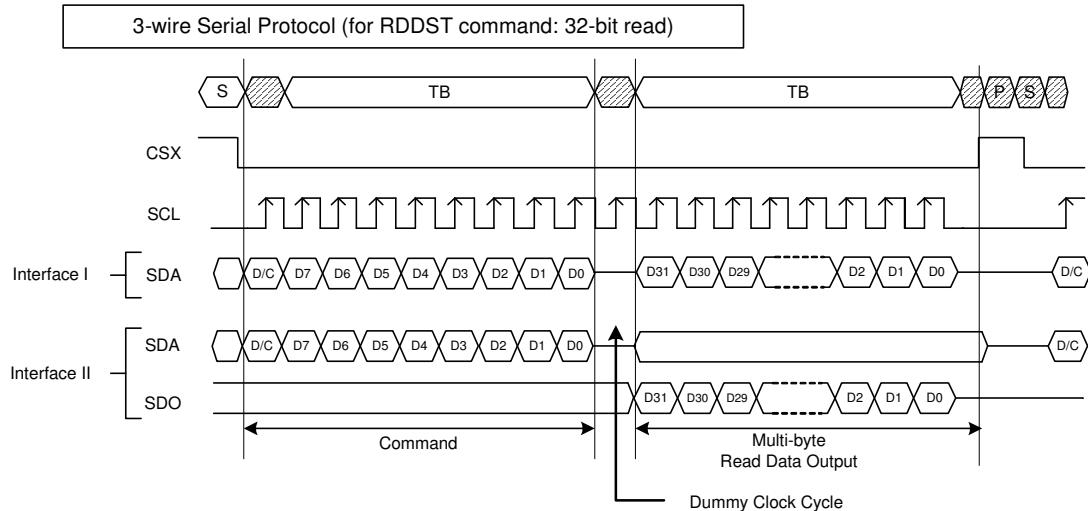


### 7.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter or display data from ILI9341. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9341 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

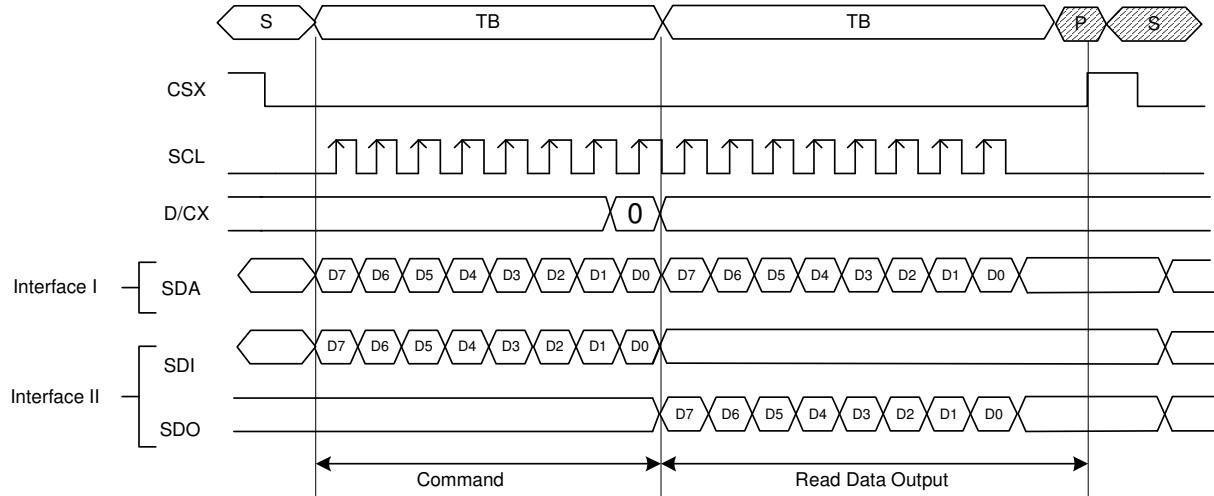
#### 3-wire Serial Interface Protocol



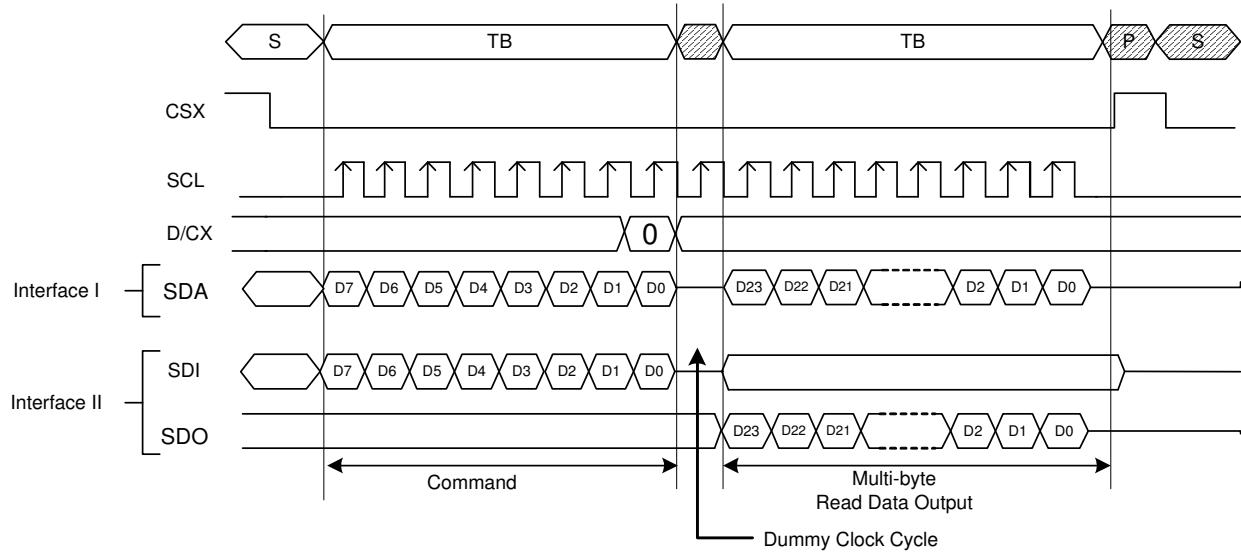


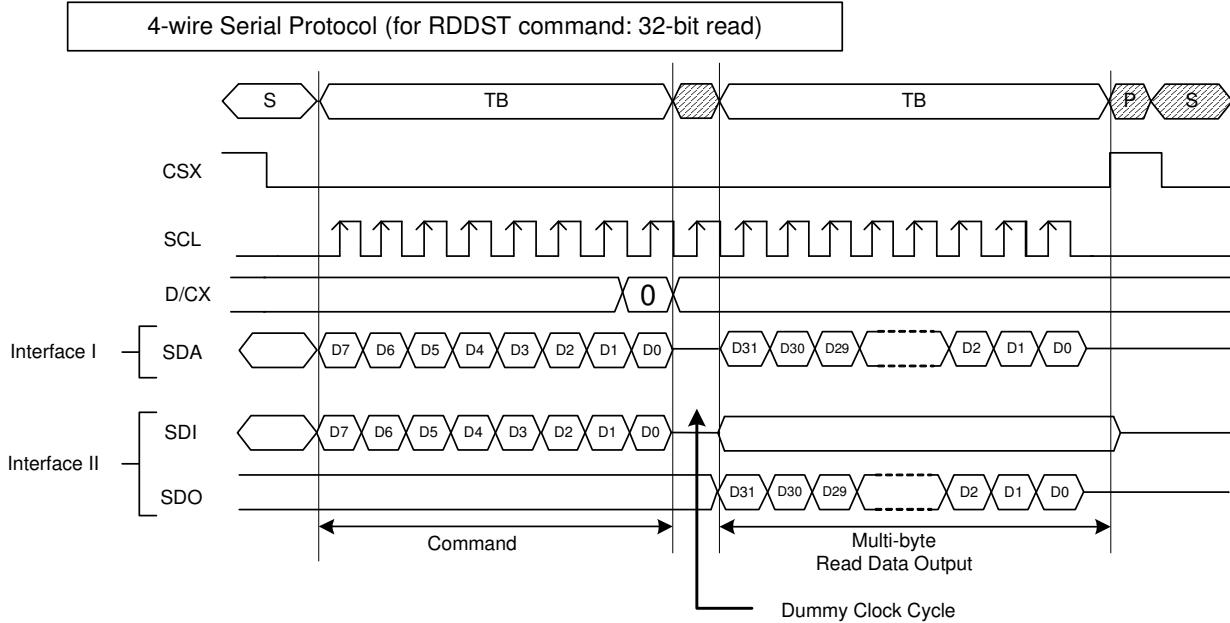
#### 4-wire Serial Interface Protocol

4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



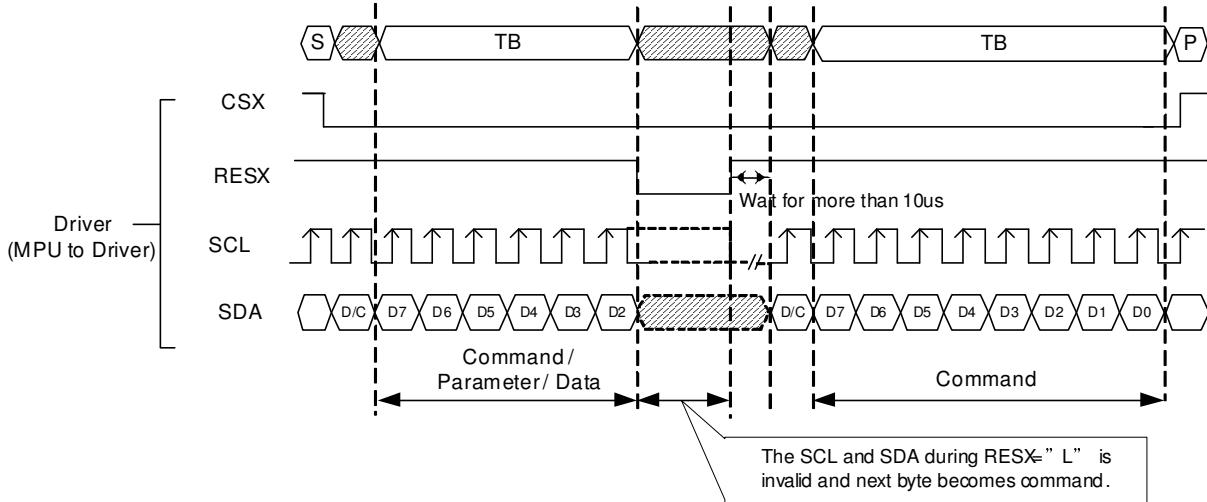
4-wire Serial Protocol (for RDDID command: 24-bit read)



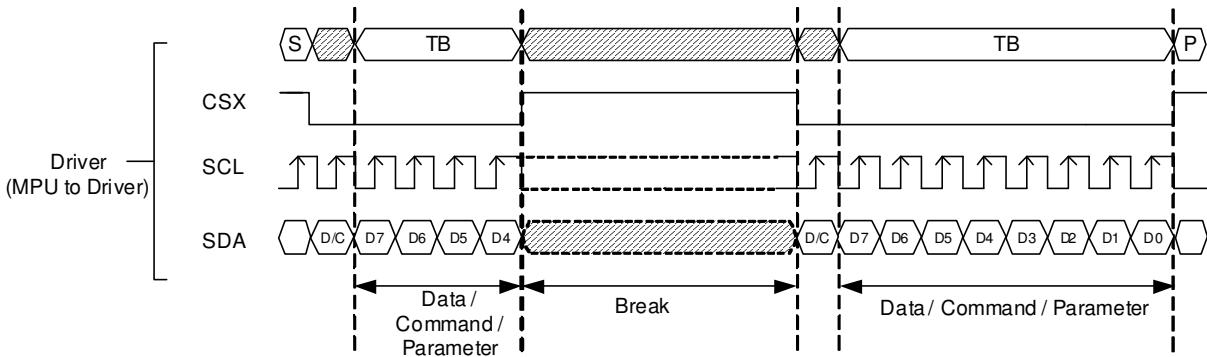


### 7.1.11. Data Transfer Break and Recovery

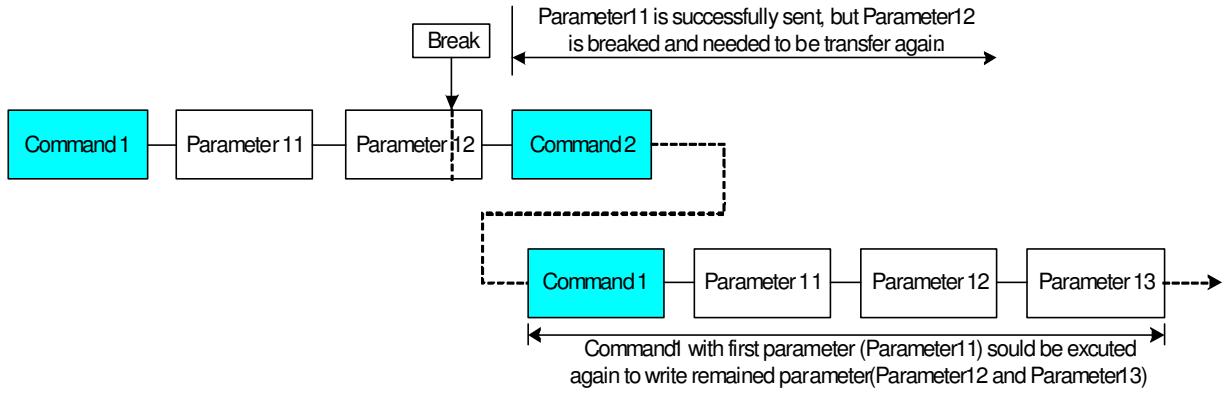
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



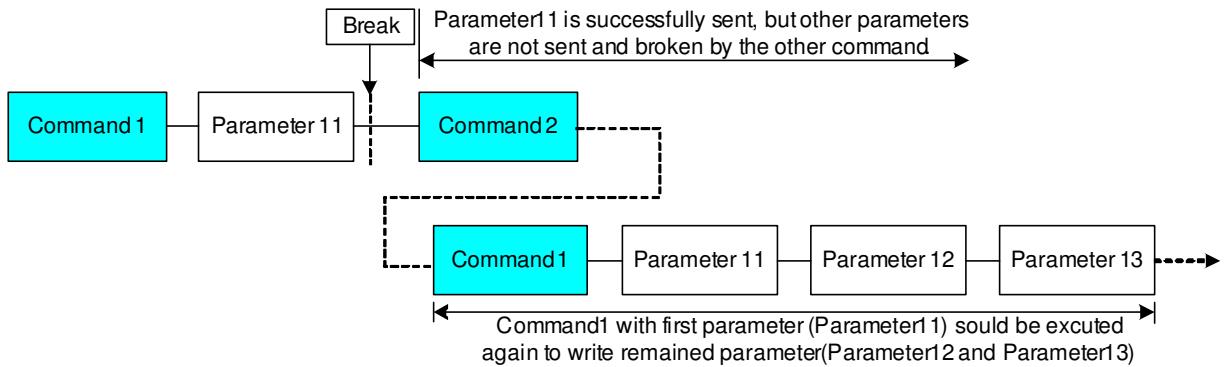
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

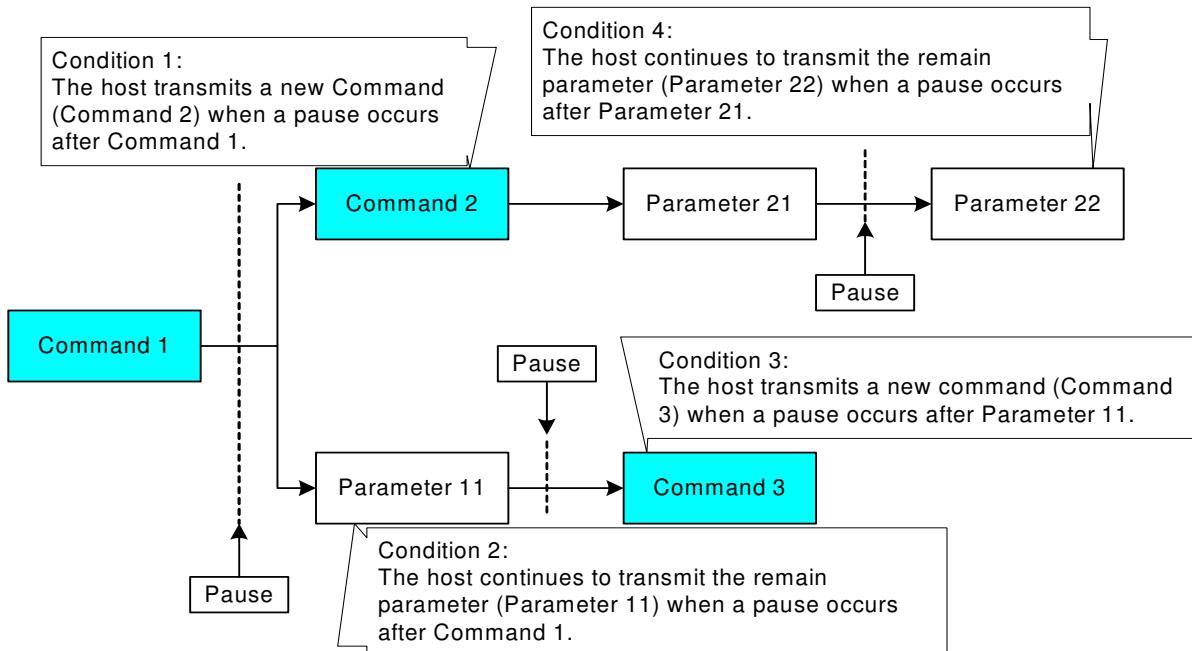


### 7.1.12. Data Transfer Pause

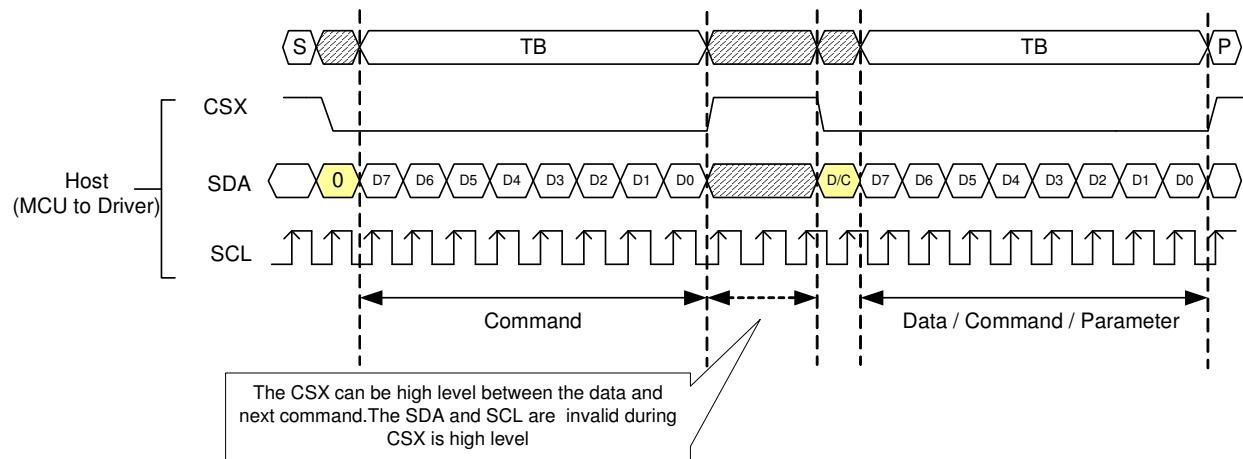
It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9341 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:

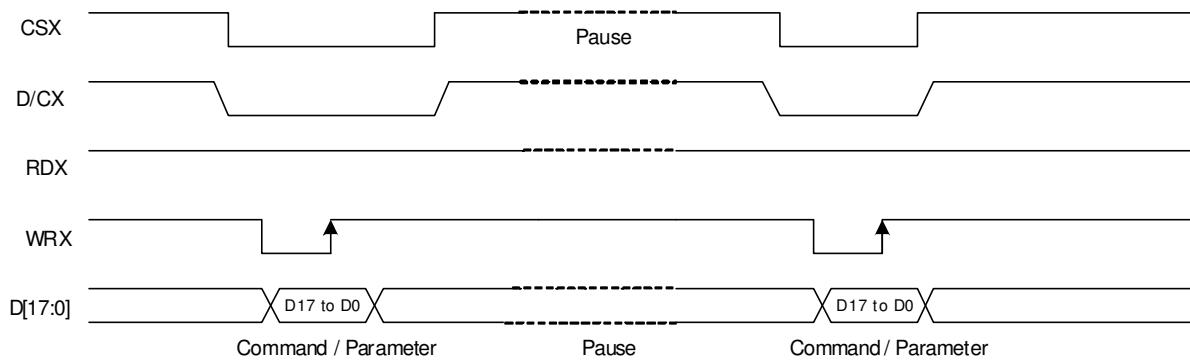
- 1) Command-Pause-Command
  - 2) Command-Pause-Parameter
  - 3) Parameter-Pause-Command
  - 4) Parameter-Pause-Parameter



### 7.1.13. Serial Interface Pause (3\_wire)



### 7.1.14. Parallel Interface Pause

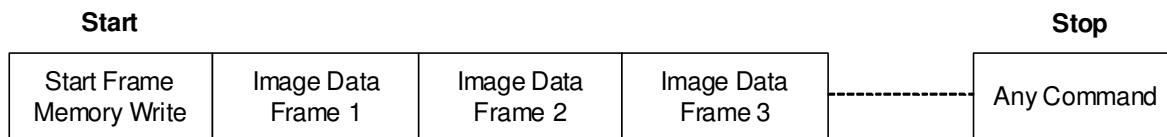


### 7.1.15. Data Transfer Mode

ILI9341 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

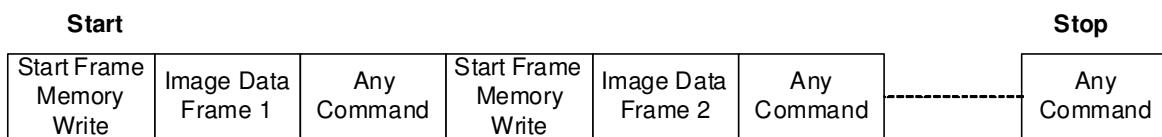
### 7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



### 7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



*Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.*

*Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.*

## 7.2. RGB Interface

### 7.2.1. RGB Interface Selection

ILI9341 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to "10", the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to "11", the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9341 supports several pixel formats that can be selected by DPI [2:0] bits of "Pixel Format Set (3Ah)" and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM[1:0]			RIM		DPI[2:0]		RGB Interface Mode				RGB Mode								Used Pins													
1	0	0	1	1	0	0	18-bit RGB interface (262K colors)				<b>DE Mode</b> Valid data is determined by the DE signal								VSYNC, HSYNC, DE, DOTCLK,D[17:0]													
1	0	0	1	0	1	1	16-bit RGB interface (65K colors)																VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1]									
1	0	1	1	1	0	0	6-bit RGB interface (262K colors)																VSYNC, HSYNC, DE, DOTCLK, D[5:0]									
1	0	1	1	0	1	1	6-bit RGB interface (65K colors)																VSYNC, HSYNC, DE, DOTCLK, D[5:0]									
1	1	0	1	1	0	0	18-bit RGB interface (262K colors)																VSYNC, HSYNC, DOTCLK, D[17:0]									
1	1	0	1	0	1	1	16-bit RGB interface (65K colors)																VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1]									
1	1	1	1	1	0	0	6-bit RGB interface (262K colors)																VSYNC, HSYNC, DOTCLK, D[5:0]									
1	1	1	1	0	1	1	6-bit RGB interface (65K colors)																VSYNC, HSYNC, DOTCLK, D[5:0]									

18-bit data bus interface (D[17:0] is used) , DPI[2:0] = 110, and RIM=0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 110, and RIM=1

D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 101, and RIM=1

D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

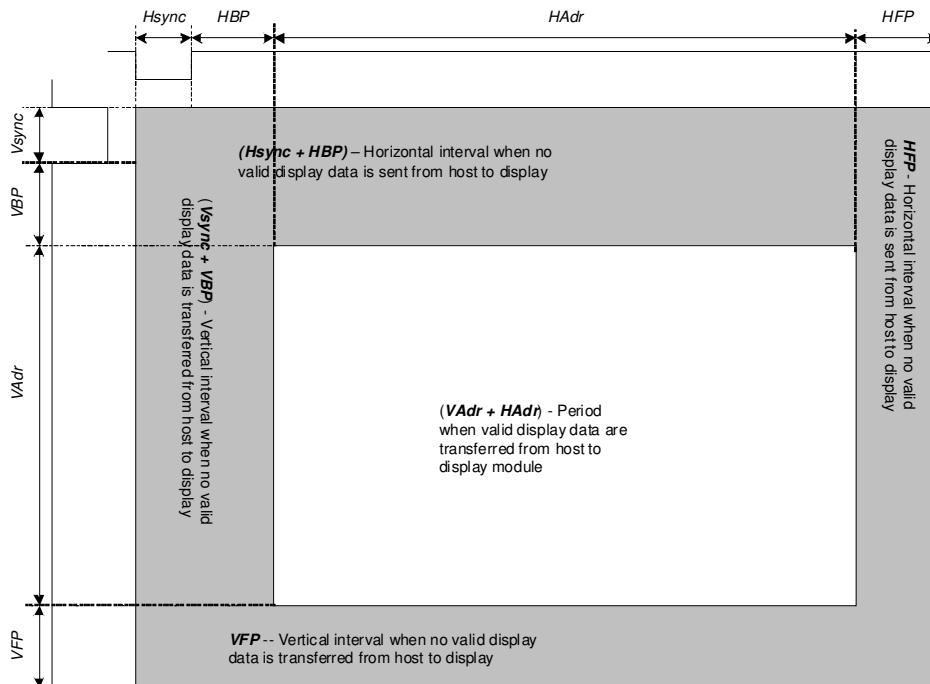
Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when

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there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (Hsync) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data is inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	Hadr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame

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frequency about 70Hz.

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

$$(\text{Number of PCLK per 1 line}) \geq (\text{Number of RTN clock}) \times \text{Division ratio (DIV)} \times \text{PCDIV}$$

#### Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

**PCDIV [5:0]:** Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction

$$(\text{Number of PCLK in 1H}) \geq (\text{Number of RTN clock}) \times \text{Division ratio (DIV)} \times \text{PCDIV}.$$

**Setting Example:** To set frame frequency to 70Hz:

#### Internal Clock

Internal Oscillation Clock: 615KHz

DIV[1:0] = 2'b0 (x 1/1)

RTN[4:0] = 5'h1b (27 clocks)

FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h27 (320 lines)

**Frame Rate → 70.30Hz**

#### DOTCLK

HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz x (2 + 320 + 2) lines x (10 + 20 + 240 + 10) clocks = 6.35MHz

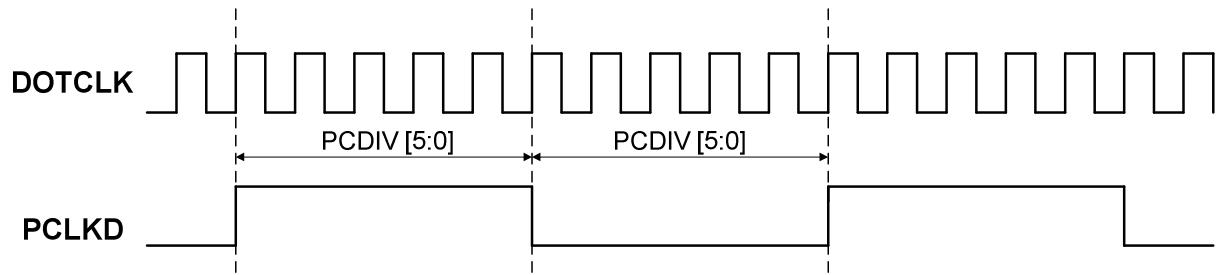
DOTCLK frequency = 6.35MHz

6.35 MHz / 615KHz = 10.32 □ Set PCDIV so that PCLK is divided by 10.

external fosc = 6.35 MHz / 10 = 635KHz

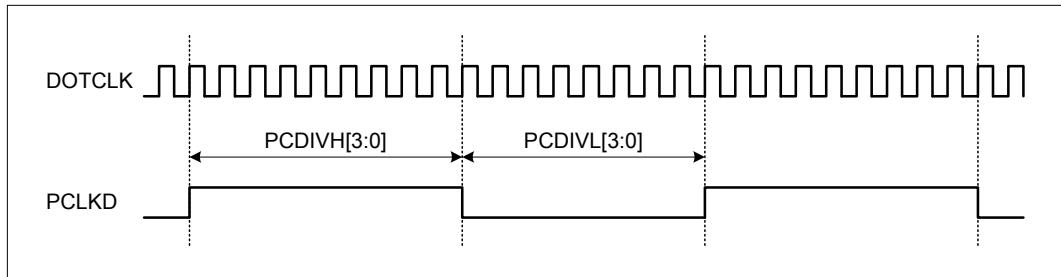
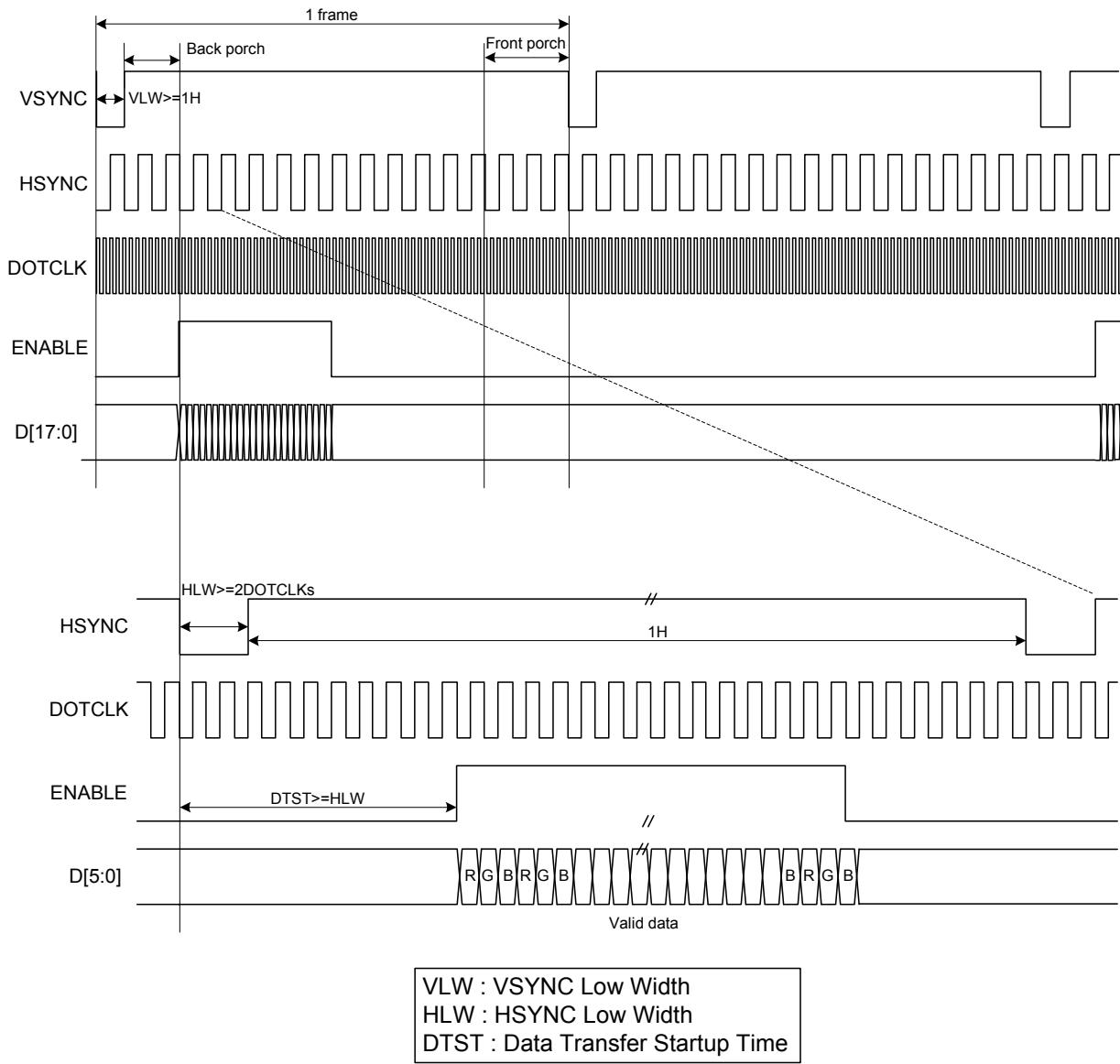
PCDIV = [ 6.35MHz / 635KHz ] / 2 ] - 1 = 4

PCDIV[5:0] = 6'h04 (10 DOTCLK)



### 7.2.2. RGB Interface Timing

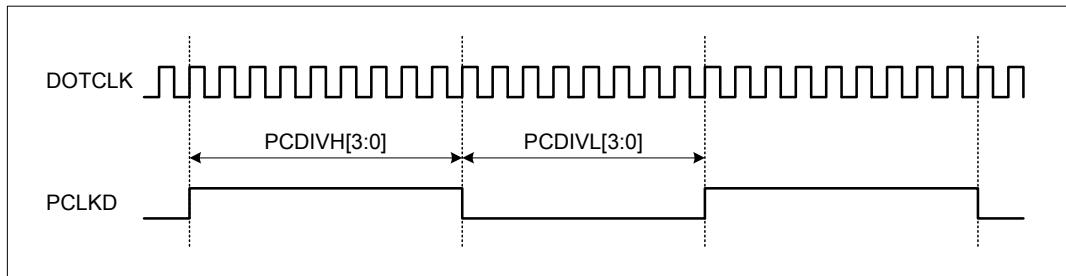
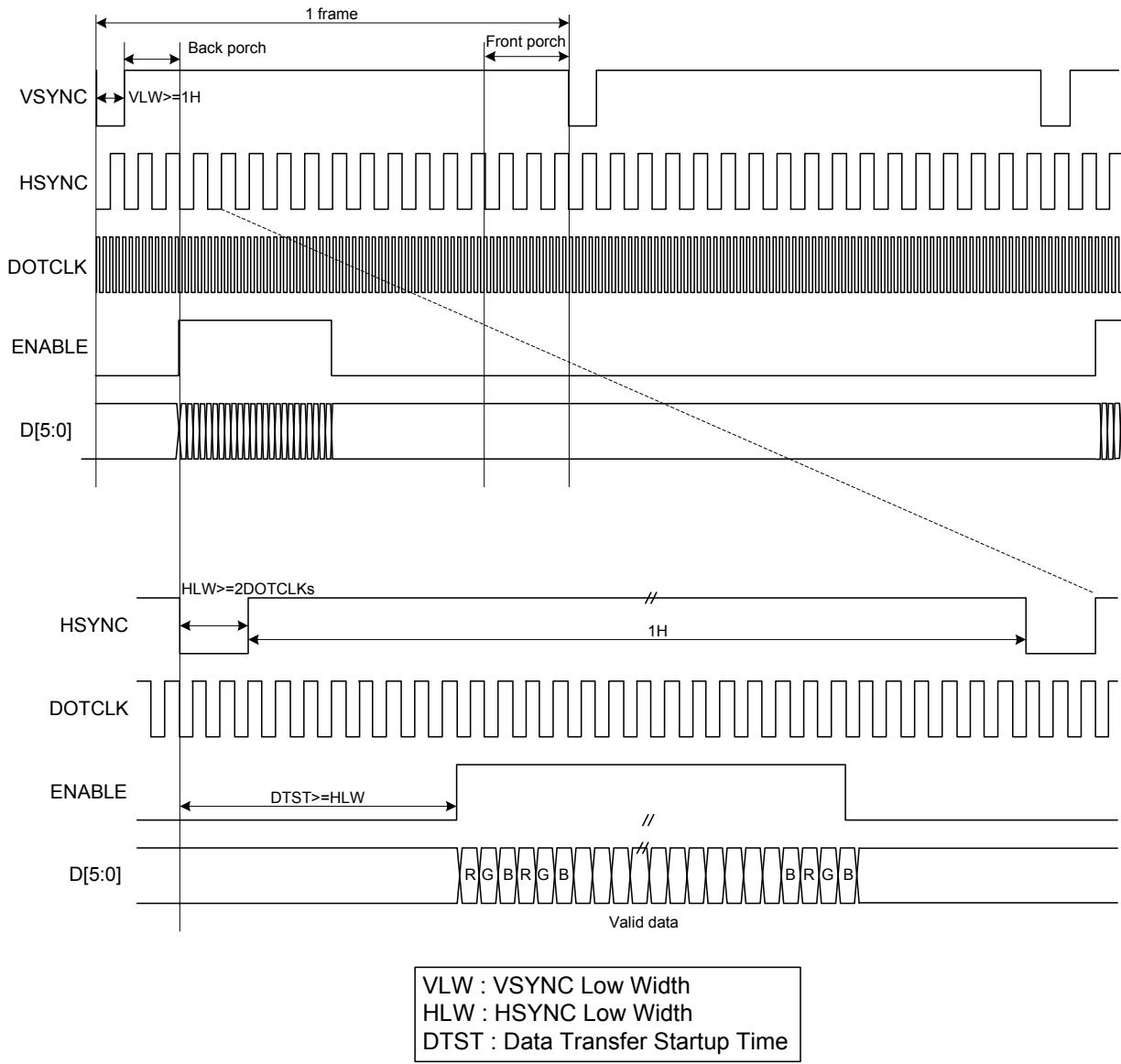
The timing chart of 18-/16-bit RGB interface mode is shown as below.



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



*Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.*

*Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.*

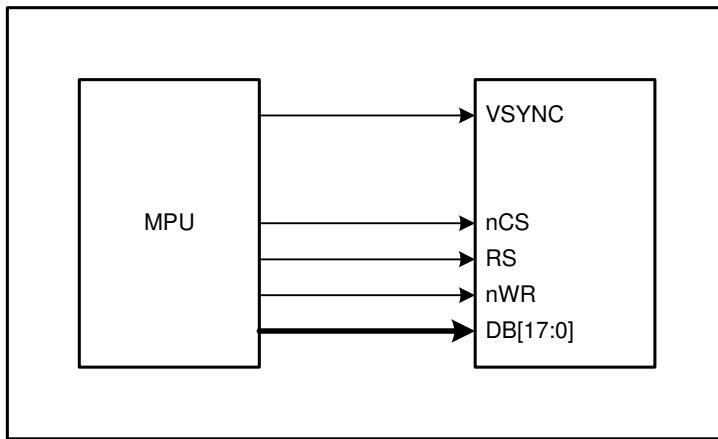
*Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.*

---

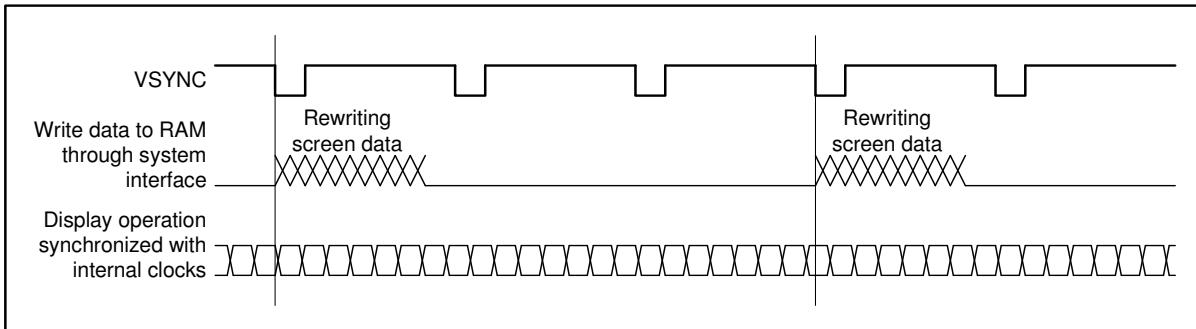
*Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.*

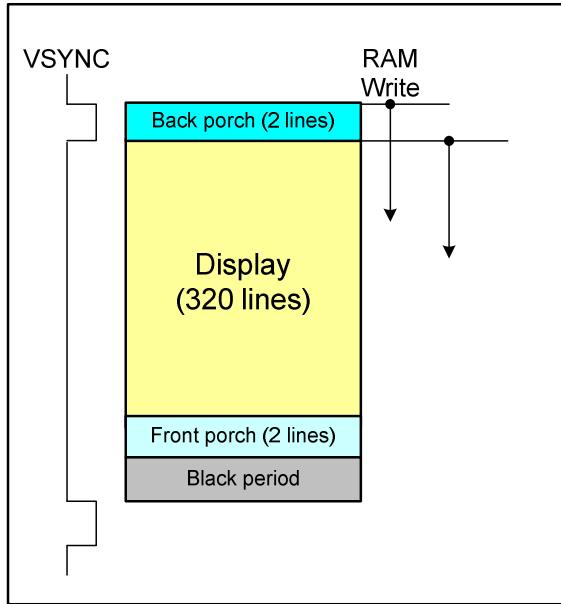
### 7.3. VSYNC Interface

ILI9341 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-I /8080-II system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".



In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

*Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.*

$$\text{Minimum RAM write speed [Hz]} > \frac{240 \times \text{DisplayLines}(NL)}{[\text{BackPorch}(VBP) + \text{DisplayLines}(NL) - \text{margins}] \times \text{Clocks per line} \times (1/fosc)}$$

*Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.*

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

#### [Example]

Display size: 240 RGB × 320 lines

Lines: 320 lines (NL = 100111)

Back porch: 2 lines (VBP = 00000010)

Front porch: 2 lines (VFP = 00000010)

Frame frequency: 70 Hz

Frequency fluctuation: 10%

$$\text{Internal oscillator clock (fosc.) [Hz]} = 70 \times [320 + 2 + 2] \times 27 \text{ clocks} \times (1.1/0.9) \doteq 748\text{KHz}$$

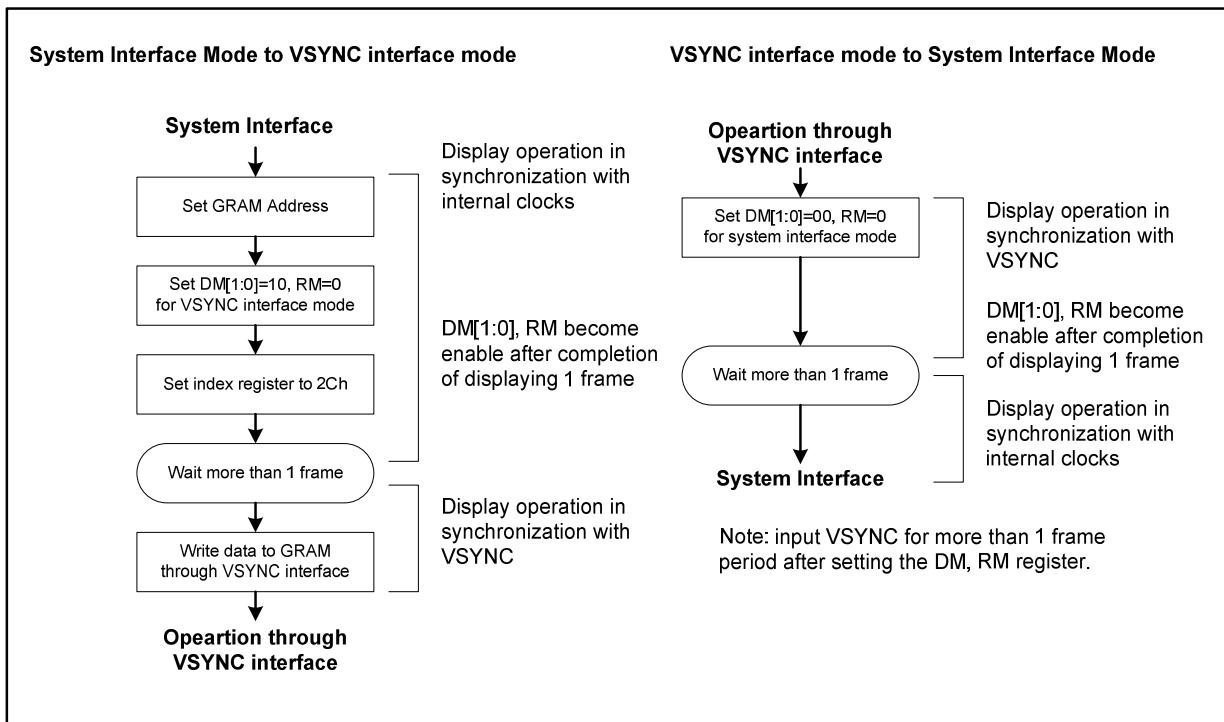
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with  $\pm 10\%$  margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

*Minimum speed for RAM writing [Hz] > 240 x 320 x 748K / [(2 + 320 - 2)lines x 27clocks] ≈ 6.65 MHz*

The above theoretical value is calculated based on the premise that the ILI9341 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9341 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

#### Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.



## 7.4. Color Depth Conversion Look Up Table

When ILI9341 operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel –mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R <sub>005</sub> R <sub>004</sub> R <sub>003</sub> R <sub>002</sub> R <sub>001</sub> R <sub>000</sub>	1
00001	R <sub>015</sub> R <sub>014</sub> R <sub>013</sub> R <sub>012</sub> R <sub>011</sub> R <sub>010</sub>	2
00010	R <sub>025</sub> R <sub>024</sub> R <sub>023</sub> R <sub>022</sub> R <sub>021</sub> R <sub>020</sub>	3
00011	R <sub>035</sub> R <sub>034</sub> R <sub>033</sub> R <sub>032</sub> R <sub>031</sub> R <sub>030</sub>	4
00100	R <sub>045</sub> R <sub>044</sub> R <sub>043</sub> R <sub>042</sub> R <sub>041</sub> R <sub>040</sub>	5
00101	R <sub>055</sub> R <sub>054</sub> R <sub>053</sub> R <sub>052</sub> R <sub>051</sub> R <sub>050</sub>	6
00110	R <sub>065</sub> R <sub>064</sub> R <sub>063</sub> R <sub>062</sub> R <sub>061</sub> R <sub>060</sub>	7
00111	R <sub>075</sub> R <sub>074</sub> R <sub>073</sub> R <sub>072</sub> R <sub>071</sub> R <sub>070</sub>	8
01000	R <sub>085</sub> R <sub>084</sub> R <sub>083</sub> R <sub>082</sub> R <sub>081</sub> R <sub>080</sub>	9
01001	R <sub>095</sub> R <sub>094</sub> R <sub>093</sub> R <sub>092</sub> R <sub>091</sub> R <sub>090</sub>	10
01010	R <sub>105</sub> R <sub>104</sub> R <sub>103</sub> R <sub>102</sub> R <sub>101</sub> R <sub>100</sub>	11
01011	R <sub>115</sub> R <sub>114</sub> R <sub>113</sub> R <sub>112</sub> R <sub>111</sub> R <sub>110</sub>	12
01100	R <sub>125</sub> R <sub>124</sub> R <sub>123</sub> R <sub>122</sub> R <sub>121</sub> R <sub>120</sub>	13
01101	R <sub>135</sub> R <sub>134</sub> R <sub>133</sub> R <sub>132</sub> R <sub>131</sub> R <sub>130</sub>	14
01110	R <sub>145</sub> R <sub>144</sub> R <sub>143</sub> R <sub>142</sub> R <sub>141</sub> R <sub>140</sub>	15
01111	R <sub>155</sub> R <sub>154</sub> R <sub>153</sub> R <sub>152</sub> R <sub>151</sub> R <sub>150</sub>	16
10000	R <sub>165</sub> R <sub>164</sub> R <sub>163</sub> R <sub>162</sub> R <sub>161</sub> R <sub>160</sub>	17
10001	R <sub>175</sub> R <sub>174</sub> R <sub>173</sub> R <sub>172</sub> R <sub>171</sub> R <sub>170</sub>	18
10010	R <sub>185</sub> R <sub>184</sub> R <sub>183</sub> R <sub>182</sub> R <sub>181</sub> R <sub>180</sub>	19
10011	R <sub>195</sub> R <sub>194</sub> R <sub>193</sub> R <sub>192</sub> R <sub>191</sub> R <sub>190</sub>	20
10100	R <sub>205</sub> R <sub>204</sub> R <sub>203</sub> R <sub>202</sub> R <sub>201</sub> R <sub>200</sub>	21
10101	R <sub>215</sub> R <sub>214</sub> R <sub>213</sub> R <sub>212</sub> R <sub>211</sub> R <sub>210</sub>	22
10110	R <sub>225</sub> R <sub>224</sub> R <sub>223</sub> R <sub>222</sub> R <sub>221</sub> R <sub>220</sub>	23
10111	R <sub>235</sub> R <sub>234</sub> R <sub>233</sub> R <sub>232</sub> R <sub>231</sub> R <sub>230</sub>	24
11000	R <sub>245</sub> R <sub>244</sub> R <sub>243</sub> R <sub>242</sub> R <sub>241</sub> R <sub>240</sub>	25
11001	R <sub>255</sub> R <sub>254</sub> R <sub>253</sub> R <sub>252</sub> R <sub>251</sub> R <sub>250</sub>	26
11010	R <sub>265</sub> R <sub>264</sub> R <sub>263</sub> R <sub>262</sub> R <sub>261</sub> R <sub>260</sub>	27
11011	R <sub>275</sub> R <sub>274</sub> R <sub>273</sub> R <sub>272</sub> R <sub>271</sub> R <sub>270</sub>	28
11100	R <sub>285</sub> R <sub>284</sub> R <sub>283</sub> R <sub>282</sub> R <sub>281</sub> R <sub>280</sub>	29
11101	R <sub>295</sub> R <sub>294</sub> R <sub>293</sub> R <sub>292</sub> R <sub>291</sub> R <sub>290</sub>	30
11110	R <sub>305</sub> R <sub>304</sub> R <sub>303</sub> R <sub>302</sub> R <sub>301</sub> R <sub>300</sub>	31
11111	R <sub>315</sub> R <sub>314</sub> R <sub>313</sub> R <sub>312</sub> R <sub>311</sub> R <sub>310</sub>	32

G input (6-bit) 16-bit/pixel –mode <b>65,536 colors</b>	G output (6-bit) 18-bit/pixel –mode <b>262,144 colors</b>	Command Code (0x2Dh) RGBSET Parameter
000000	G <sub>005</sub> G <sub>004</sub> G <sub>003</sub> G <sub>002</sub> G <sub>001</sub> G <sub>000</sub>	33
000001	G <sub>015</sub> G <sub>014</sub> G <sub>013</sub> G <sub>012</sub> G <sub>011</sub> G <sub>010</sub>	34
000010	G <sub>025</sub> G <sub>024</sub> G <sub>023</sub> G <sub>022</sub> G <sub>021</sub> G <sub>020</sub>	35
000011	G <sub>035</sub> G <sub>034</sub> G <sub>033</sub> G <sub>032</sub> G <sub>031</sub> G <sub>030</sub>	36
000100	G <sub>045</sub> G <sub>044</sub> G <sub>043</sub> G <sub>042</sub> G <sub>041</sub> G <sub>040</sub>	37
000101	G <sub>055</sub> G <sub>054</sub> G <sub>053</sub> G <sub>052</sub> G <sub>051</sub> G <sub>050</sub>	38
000110	G <sub>065</sub> G <sub>064</sub> G <sub>063</sub> G <sub>062</sub> G <sub>061</sub> G <sub>060</sub>	39
000111	G <sub>075</sub> G <sub>074</sub> G <sub>073</sub> G <sub>072</sub> G <sub>071</sub> G <sub>070</sub>	40
001000	G <sub>085</sub> G <sub>084</sub> G <sub>083</sub> G <sub>082</sub> G <sub>081</sub> G <sub>080</sub>	41
001001	G <sub>095</sub> G <sub>094</sub> G <sub>093</sub> G <sub>092</sub> G <sub>091</sub> G <sub>090</sub>	42
001010	G <sub>105</sub> G <sub>104</sub> G <sub>103</sub> G <sub>102</sub> G <sub>101</sub> G <sub>100</sub>	43
001011	G <sub>115</sub> G <sub>114</sub> G <sub>113</sub> G <sub>112</sub> G <sub>111</sub> G <sub>110</sub>	44
001100	G <sub>125</sub> G <sub>124</sub> G <sub>123</sub> G <sub>122</sub> G <sub>121</sub> G <sub>120</sub>	45
001101	G <sub>135</sub> G <sub>134</sub> G <sub>133</sub> G <sub>132</sub> G <sub>131</sub> G <sub>130</sub>	46
001110	G <sub>145</sub> G <sub>144</sub> G <sub>143</sub> G <sub>142</sub> G <sub>141</sub> G <sub>140</sub>	47
001111	G <sub>155</sub> G <sub>154</sub> G <sub>153</sub> G <sub>152</sub> G <sub>151</sub> G <sub>150</sub>	48
010000	G <sub>165</sub> G <sub>164</sub> G <sub>163</sub> G <sub>162</sub> G <sub>161</sub> G <sub>160</sub>	49
010001	G <sub>175</sub> G <sub>174</sub> G <sub>173</sub> G <sub>172</sub> G <sub>171</sub> G <sub>170</sub>	50
010010	G <sub>185</sub> G <sub>184</sub> G <sub>183</sub> G <sub>182</sub> G <sub>181</sub> G <sub>180</sub>	51
010011	G <sub>195</sub> G <sub>194</sub> G <sub>193</sub> G <sub>192</sub> G <sub>191</sub> G <sub>190</sub>	52
010100	G <sub>205</sub> G <sub>204</sub> G <sub>203</sub> G <sub>202</sub> G <sub>201</sub> G <sub>200</sub>	53
010101	G <sub>215</sub> G <sub>214</sub> G <sub>213</sub> G <sub>212</sub> G <sub>211</sub> G <sub>210</sub>	54
010110	G <sub>225</sub> G <sub>224</sub> G <sub>223</sub> G <sub>222</sub> G <sub>221</sub> G <sub>220</sub>	55
010111	G <sub>235</sub> G <sub>234</sub> G <sub>233</sub> G <sub>232</sub> G <sub>231</sub> G <sub>230</sub>	56
011000	G <sub>245</sub> G <sub>244</sub> G <sub>243</sub> G <sub>242</sub> G <sub>241</sub> G <sub>240</sub>	57
011001	G <sub>255</sub> G <sub>254</sub> G <sub>253</sub> G <sub>252</sub> G <sub>251</sub> G <sub>250</sub>	58
011010	G <sub>265</sub> G <sub>264</sub> G <sub>263</sub> G <sub>262</sub> G <sub>261</sub> G <sub>260</sub>	59
011011	G <sub>275</sub> G <sub>274</sub> G <sub>273</sub> G <sub>272</sub> G <sub>271</sub> G <sub>270</sub>	60
011100	G <sub>285</sub> G <sub>284</sub> G <sub>283</sub> G <sub>282</sub> G <sub>281</sub> G <sub>280</sub>	61
011101	G <sub>295</sub> G <sub>294</sub> G <sub>293</sub> G <sub>292</sub> G <sub>291</sub> G <sub>290</sub>	62
011110	G <sub>305</sub> G <sub>304</sub> G <sub>303</sub> G <sub>302</sub> G <sub>301</sub> G <sub>300</sub>	63
011111	G <sub>315</sub> G <sub>314</sub> G <sub>313</sub> G <sub>312</sub> G <sub>311</sub> G <sub>310</sub>	64
100000	G <sub>325</sub> G <sub>324</sub> G <sub>323</sub> G <sub>322</sub> G <sub>321</sub> G <sub>320</sub>	65
100001	G <sub>335</sub> G <sub>334</sub> G <sub>333</sub> G <sub>332</sub> G <sub>331</sub> G <sub>330</sub>	66

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G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G <sub>345</sub> G <sub>344</sub> G <sub>343</sub> G <sub>342</sub> G <sub>341</sub> G <sub>340</sub>	67
100011	G <sub>355</sub> G <sub>354</sub> G <sub>353</sub> G <sub>352</sub> G <sub>351</sub> G <sub>350</sub>	68
100100	G <sub>365</sub> G <sub>364</sub> G <sub>363</sub> G <sub>362</sub> G <sub>361</sub> G <sub>360</sub>	69
100101	G <sub>375</sub> G <sub>374</sub> G <sub>373</sub> G <sub>372</sub> G <sub>371</sub> G <sub>370</sub>	70
100110	G <sub>385</sub> G <sub>384</sub> G <sub>383</sub> G <sub>382</sub> G <sub>381</sub> G <sub>380</sub>	71
100111	G <sub>395</sub> G <sub>394</sub> G <sub>393</sub> G <sub>392</sub> G <sub>391</sub> G <sub>390</sub>	72
101000	G <sub>405</sub> G <sub>404</sub> G <sub>403</sub> G <sub>402</sub> G <sub>401</sub> G <sub>400</sub>	73
101001	G <sub>415</sub> G <sub>414</sub> G <sub>413</sub> G <sub>412</sub> G <sub>411</sub> G <sub>410</sub>	74
101010	G <sub>425</sub> G <sub>424</sub> G <sub>423</sub> G <sub>422</sub> G <sub>421</sub> G <sub>420</sub>	75
101011	G <sub>435</sub> G <sub>434</sub> G <sub>433</sub> G <sub>432</sub> G <sub>431</sub> G <sub>430</sub>	76
101100	G <sub>445</sub> G <sub>444</sub> G <sub>443</sub> G <sub>442</sub> G <sub>441</sub> G <sub>440</sub>	77
101101	G <sub>455</sub> G <sub>454</sub> G <sub>453</sub> G <sub>452</sub> G <sub>451</sub> G <sub>450</sub>	78
101110	G <sub>465</sub> G <sub>464</sub> G <sub>463</sub> G <sub>462</sub> G <sub>461</sub> G <sub>460</sub>	79
101111	G <sub>475</sub> G <sub>474</sub> G <sub>473</sub> G <sub>472</sub> G <sub>471</sub> G <sub>470</sub>	80
110000	G <sub>485</sub> G <sub>484</sub> G <sub>483</sub> G <sub>482</sub> G <sub>481</sub> G <sub>480</sub>	81
110001	G <sub>495</sub> G <sub>494</sub> G <sub>493</sub> G <sub>492</sub> G <sub>491</sub> G <sub>490</sub>	82
110010	G <sub>505</sub> G <sub>504</sub> G <sub>503</sub> G <sub>502</sub> G <sub>501</sub> G <sub>500</sub>	83
110011	G <sub>515</sub> G <sub>514</sub> G <sub>513</sub> G <sub>512</sub> G <sub>511</sub> G <sub>510</sub>	84
110100	G <sub>525</sub> G <sub>524</sub> G <sub>523</sub> G <sub>522</sub> G <sub>521</sub> G <sub>520</sub>	85
110101	G <sub>535</sub> G <sub>534</sub> G <sub>533</sub> G <sub>532</sub> G <sub>531</sub> G <sub>530</sub>	86
110110	G <sub>545</sub> G <sub>544</sub> G <sub>543</sub> G <sub>542</sub> G <sub>541</sub> G <sub>540</sub>	87
110111	G <sub>555</sub> G <sub>554</sub> G <sub>553</sub> G <sub>552</sub> G <sub>551</sub> G <sub>550</sub>	88
111000	G <sub>565</sub> G <sub>564</sub> G <sub>563</sub> G <sub>562</sub> G <sub>561</sub> G <sub>560</sub>	89
111001	G <sub>575</sub> G <sub>574</sub> G <sub>573</sub> G <sub>572</sub> G <sub>571</sub> G <sub>570</sub>	90
111010	G <sub>585</sub> G <sub>584</sub> G <sub>583</sub> G <sub>582</sub> G <sub>581</sub> G <sub>580</sub>	91
111011	G <sub>595</sub> G <sub>594</sub> G <sub>593</sub> G <sub>592</sub> G <sub>591</sub> G <sub>590</sub>	92
111100	G <sub>605</sub> G <sub>604</sub> G <sub>603</sub> G <sub>602</sub> G <sub>601</sub> G <sub>600</sub>	93
111101	G <sub>615</sub> G <sub>614</sub> G <sub>613</sub> G <sub>612</sub> G <sub>611</sub> G <sub>610</sub>	94
111110	G <sub>625</sub> G <sub>624</sub> G <sub>623</sub> G <sub>622</sub> G <sub>621</sub> G <sub>620</sub>	95
111111	G <sub>635</sub> G <sub>634</sub> G <sub>633</sub> G <sub>632</sub> G <sub>631</sub> G <sub>630</sub>	96

B input (5-bit) 16-bit/pixel –mode <b>65,536 colors</b>	B output (6-bit) 18-bit/pixel –mode <b>262,144 colors</b>	Command Code (0x2Dh) RGBSET Parameter
00000	B <sub>005</sub> B <sub>004</sub> B <sub>003</sub> B <sub>002</sub> B <sub>001</sub> B <sub>000</sub>	97
00001	B <sub>015</sub> B <sub>014</sub> B <sub>013</sub> B <sub>012</sub> B <sub>011</sub> B <sub>010</sub>	98
00010	B <sub>025</sub> B <sub>024</sub> B <sub>023</sub> B <sub>022</sub> B <sub>021</sub> B <sub>020</sub>	99
00011	B <sub>035</sub> B <sub>034</sub> B <sub>033</sub> B <sub>032</sub> B <sub>031</sub> B <sub>030</sub>	100
00100	B <sub>045</sub> B <sub>044</sub> B <sub>043</sub> B <sub>042</sub> B <sub>041</sub> B <sub>040</sub>	101
00101	B <sub>055</sub> B <sub>054</sub> B <sub>053</sub> B <sub>052</sub> B <sub>051</sub> B <sub>050</sub>	102
00110	B <sub>065</sub> B <sub>064</sub> B <sub>063</sub> B <sub>062</sub> B <sub>061</sub> B <sub>060</sub>	103
00111	B <sub>075</sub> B <sub>074</sub> B <sub>073</sub> B <sub>072</sub> B <sub>071</sub> B <sub>070</sub>	104
01000	B <sub>085</sub> B <sub>084</sub> B <sub>083</sub> B <sub>082</sub> B <sub>081</sub> B <sub>080</sub>	105
01001	B <sub>095</sub> B <sub>094</sub> B <sub>093</sub> B <sub>092</sub> B <sub>091</sub> B <sub>090</sub>	106
01010	B <sub>105</sub> B <sub>104</sub> B <sub>103</sub> B <sub>102</sub> B <sub>101</sub> B <sub>100</sub>	107
01011	B <sub>115</sub> B <sub>114</sub> B <sub>113</sub> B <sub>112</sub> B <sub>111</sub> B <sub>110</sub>	108
01100	B <sub>125</sub> B <sub>124</sub> B <sub>123</sub> B <sub>122</sub> B <sub>121</sub> B <sub>120</sub>	109
01101	B <sub>135</sub> B <sub>134</sub> B <sub>133</sub> B <sub>132</sub> B <sub>131</sub> B <sub>130</sub>	110
01110	B <sub>145</sub> B <sub>144</sub> B <sub>143</sub> B <sub>142</sub> B <sub>141</sub> B <sub>140</sub>	111
01111	B <sub>155</sub> B <sub>154</sub> B <sub>153</sub> B <sub>152</sub> B <sub>151</sub> B <sub>150</sub>	112
10000	B <sub>165</sub> B <sub>164</sub> B <sub>163</sub> B <sub>162</sub> B <sub>161</sub> B <sub>160</sub>	113
10001	B <sub>175</sub> B <sub>174</sub> B <sub>173</sub> B <sub>172</sub> B <sub>171</sub> B <sub>170</sub>	114
10010	B <sub>185</sub> B <sub>184</sub> B <sub>183</sub> B <sub>182</sub> B <sub>181</sub> B <sub>180</sub>	115
10011	B <sub>195</sub> B <sub>194</sub> B <sub>193</sub> B <sub>192</sub> B <sub>191</sub> B <sub>190</sub>	116
10100	B <sub>205</sub> B <sub>204</sub> B <sub>203</sub> B <sub>202</sub> B <sub>201</sub> B <sub>200</sub>	117
10101	B <sub>215</sub> B <sub>214</sub> B <sub>213</sub> B <sub>212</sub> B <sub>211</sub> B <sub>210</sub>	118
10110	B <sub>225</sub> B <sub>224</sub> B <sub>223</sub> B <sub>222</sub> B <sub>221</sub> B <sub>220</sub>	119
10111	B <sub>235</sub> B <sub>234</sub> B <sub>233</sub> B <sub>232</sub> B <sub>231</sub> B <sub>230</sub>	120
11000	B <sub>245</sub> B <sub>244</sub> B <sub>243</sub> B <sub>242</sub> B <sub>241</sub> B <sub>240</sub>	121
11001	B <sub>255</sub> B <sub>254</sub> B <sub>253</sub> B <sub>252</sub> B <sub>251</sub> B <sub>250</sub>	122
11010	B <sub>265</sub> B <sub>264</sub> B <sub>263</sub> B <sub>262</sub> B <sub>261</sub> B <sub>260</sub>	123
11011	B <sub>275</sub> B <sub>274</sub> B <sub>273</sub> B <sub>272</sub> B <sub>271</sub> B <sub>270</sub>	124
11100	B <sub>285</sub> B <sub>284</sub> B <sub>283</sub> B <sub>282</sub> B <sub>281</sub> B <sub>280</sub>	125
11101	B <sub>295</sub> B <sub>294</sub> B <sub>293</sub> B <sub>292</sub> B <sub>291</sub> B <sub>290</sub>	126
11110	B <sub>305</sub> B <sub>304</sub> B <sub>303</sub> B <sub>302</sub> B <sub>301</sub> B <sub>300</sub>	127
11111	B <sub>315</sub> B <sub>314</sub> B <sub>313</sub> B <sub>312</sub> B <sub>311</sub> B <sub>310</sub>	128

## 7.5. Display Data RAM (DDRAM)

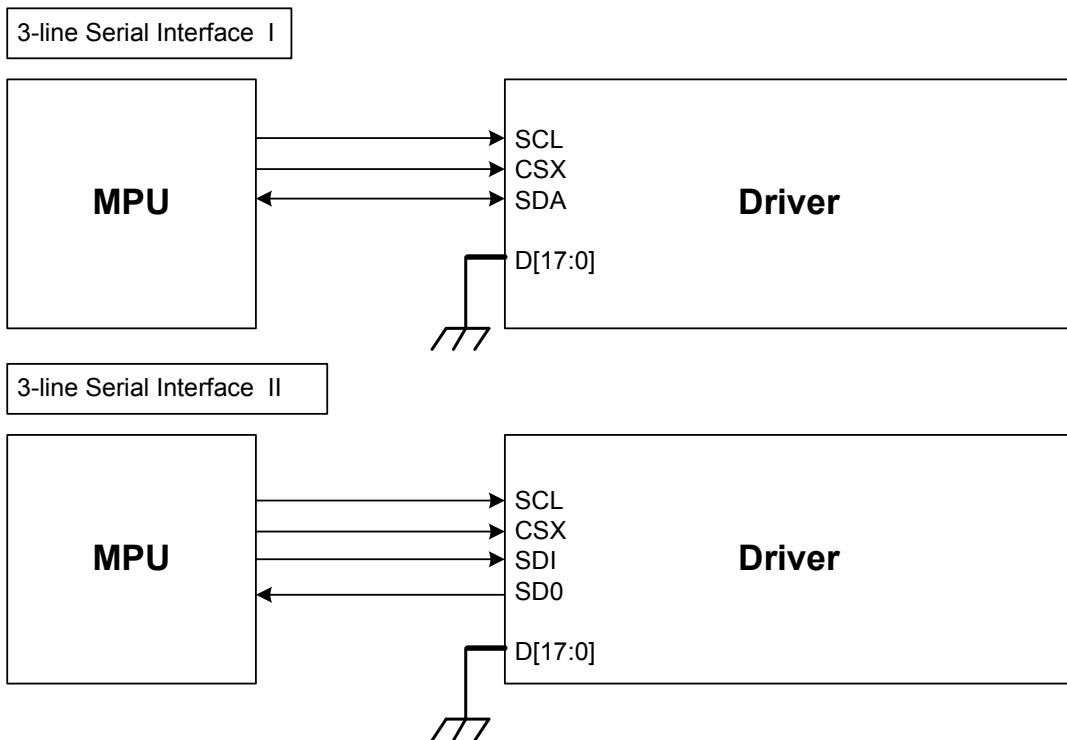
ILI9341 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

## 7.6. Display Data Format

ILI9341 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-I /8080-II series, 3-/4-line serial interface and 6-/16-/18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

### 7.6.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0101" for serial interface I or IM [3:0] to "1101" for serial interface II. The shown figure is the example of 3-line SPI interface.

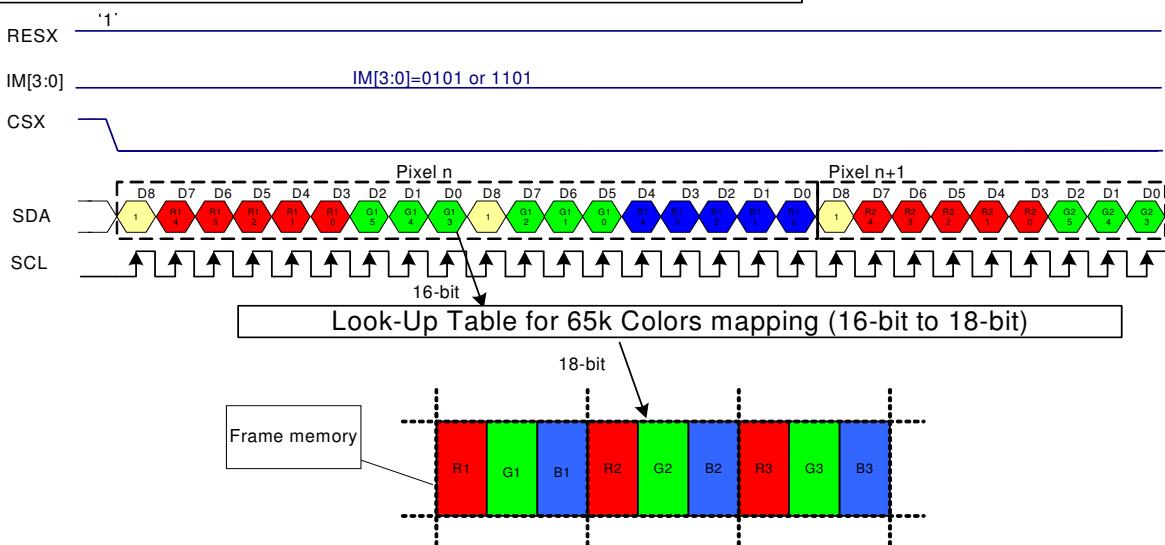


In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

**16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors**



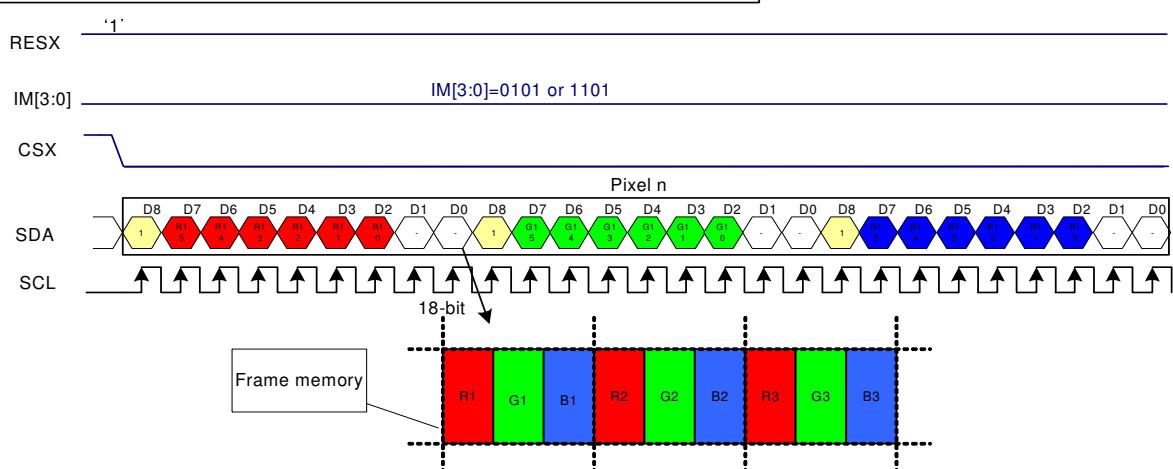
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '=' Don't care - Can be set "0" or "1".

**18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors**



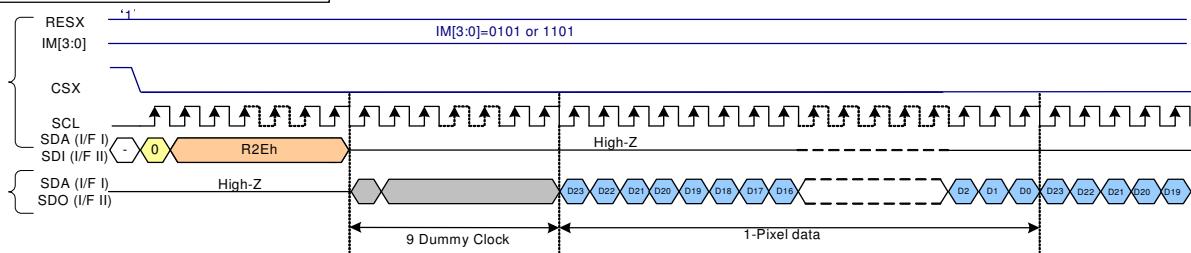
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '=' Don't care - Can be set "0" or "1".

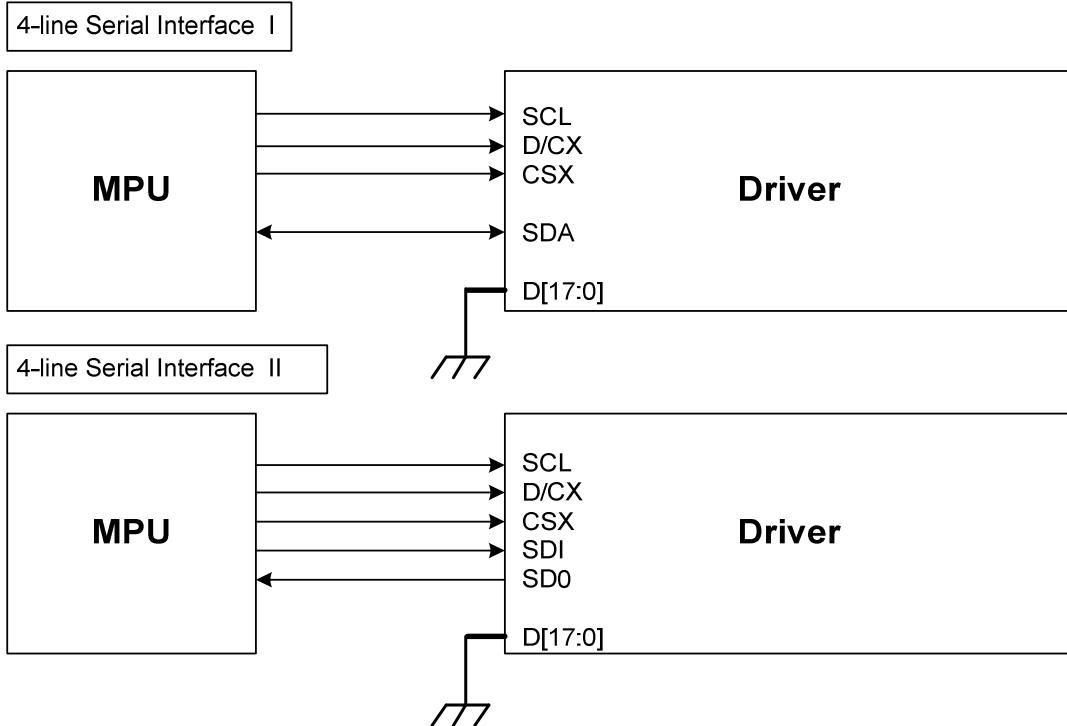
Read data through 3-line SPI mode



Note 1: '-' = Don't care –Can be set "0" or "1".

### 7.6.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0110" for serial interface I or IM [3:0] to "1110" for serial interface II. The shown figure is the example of 4-line SPI interface.

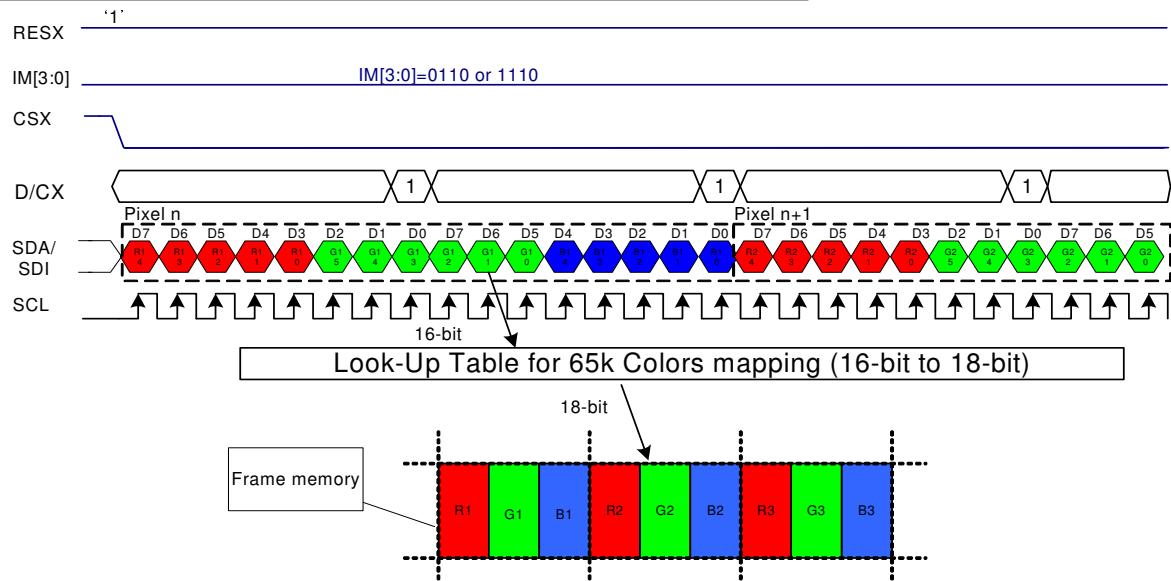


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

#### 16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors



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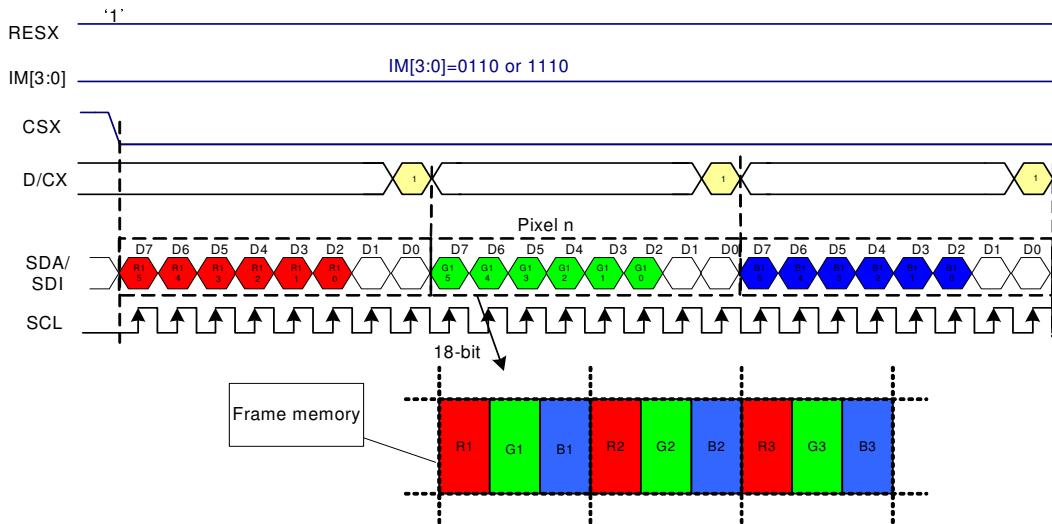
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

**18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors**



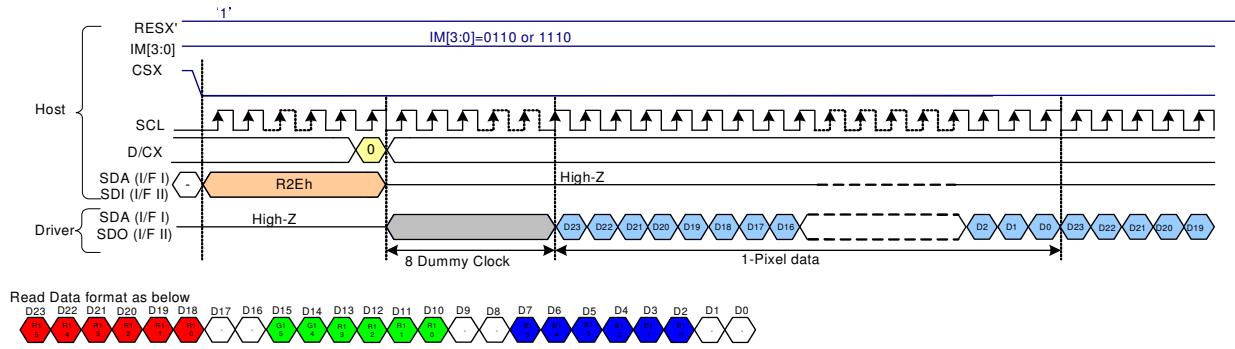
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

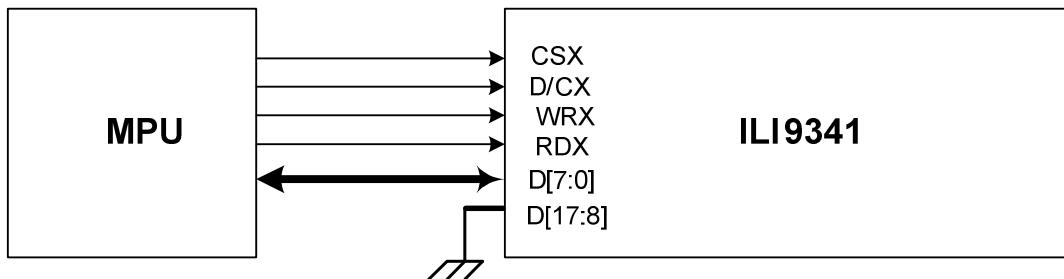
**Read data through 4-line SPI mode**



Note 1: '-'= Don't care – Can be set "0" or "1".

### 7.6.3. 8-bit Parallel MCU Interface

The 8080- I system 8-bit parallel bus interface of ILI9341 can be used by setting external pin as IM [3:0] to “0000”.The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

#### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

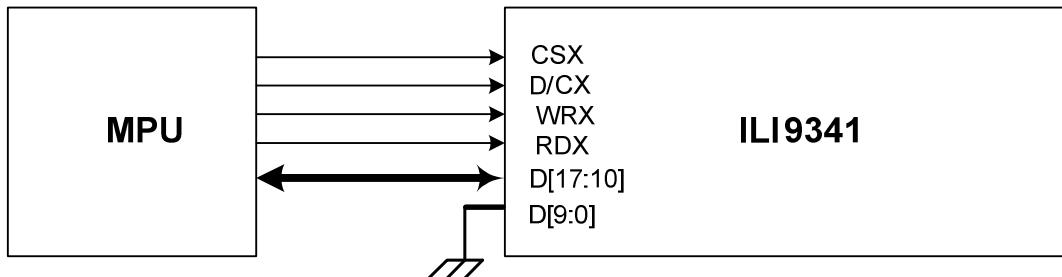
Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

#### 262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D7	C7	0R5	0G5	0B5	...	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	...	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	...	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	...	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	...	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	...	239R0	239G0	239B0
D1	C1				...			
D0	C0				...			

The 8080-II system 8-bit parallel bus interface of ILI9341 can be used by settings as IM [3:0] = "1001". The following shown figure is the example of interface with 8080-II MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

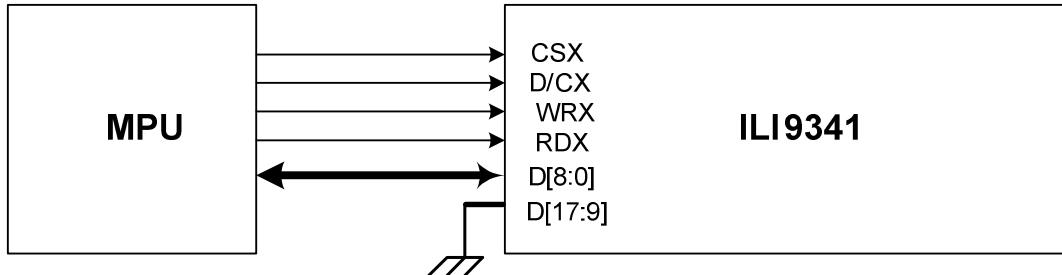
### 262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D17	C7	0R5	0G5	0B5	...	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	...	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	...	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	...	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	...	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	...	239R0	239G0	239B0
D11	C1				...			
D10	C0				...			

#### 7.6.4. 9-bit Parallel MCU Interface

The 8080- I system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "0010". The following shown figure is the example of interface with 8080- I MCU system interface.



#### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D8										
D7	C7	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

#### 262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

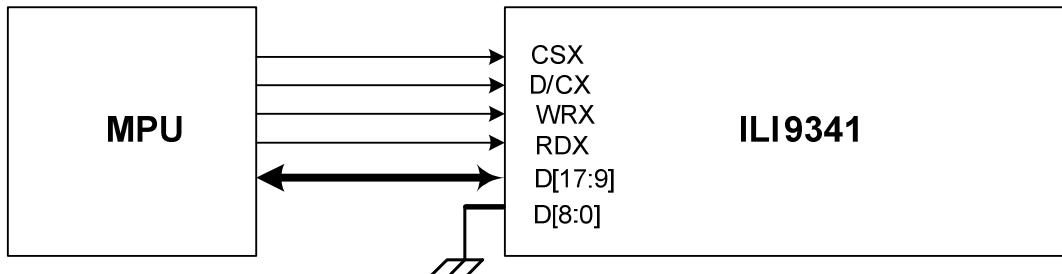
#### MDT[1:0] = "00"

Count	0	1	2	3	4	...	478	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D8		0R5	0G2	1R5	1G2	...	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	...	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	...	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	...	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

**MDT[1:0] = "01"**

Count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D8								
D7	C7	0R5	0G5	0B5	...	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	...	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	...	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	...	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	...	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	...	239R0	239G0	239B0
D1	C1				...			
D0	C0				...			

The 8080-II system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "1011". The following shown figure is the example of interface with 8080-II MCU system interface.



### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D17	C7									
D16	C6	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D15	C5	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D14	C4	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D13	C3	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

**262K color: 18-bit/pixel (RGB 6-6-6 bits input)**

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

**MDT[1:0] = "00"**

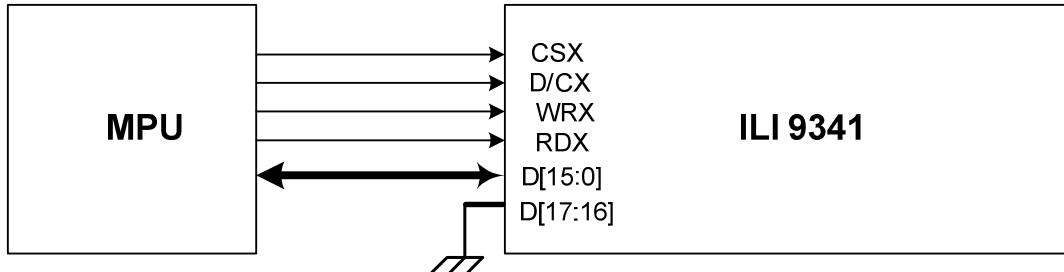
Count	0	1	2	3	4	...	478	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	...	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	...	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	...	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

**MDT[1:0] = "01"**

Count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D17	C7							
D16	C6	0R5	0G5	0B5	...	239R5	239G5	239B5
D15	C5	0R4	0G4	0B4	...	239R4	239G4	239B4
D14	C4	0R3	0G3	0B3	...	239R3	239G3	239B3
D13	C3	0R2	0G2	0B2	...	239R2	239G2	239B2
D12	C2	0R1	0G1	0B1	...	239R1	239G1	239B1
D11	C1	0R0	0G0	0B0	...	239R0	239G0	239B0
D10	C0				...			
D9					...			

### 7.6.5. 16-bit Parallel MCU Interface

The 8080- I system 16-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM[3:0] to “0001”.The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

#### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D15		0R4	1R4	2R4	...	237R4	238R4	239R4
D14		0R3	1R3	2R3	...	237R3	238R3	239R3
D13		0R2	1R2	2R2	...	237R2	238R2	239R2
D12		0R1	1R1	2R1	...	237R1	238R1	239R1
D11		0R0	1R0	2R0	...	237R0	238R0	239R0
D10		0G5	1G5	2G5	...	237G5	238G5	239G5
D9		0G4	1G4	2G4	...	237G4	238G4	239G4
D8		0G3	1G3	2G3	...	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

**262K color: 18-bit/pixel (RGB 6-6-6 bits input)**

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

**MDT[1:0] = "00"**

Count	0	1	2	3	...	358	359	360
D/CX	0	1	1	1	...	1	1	1
D15		0R5	0B5	1G5	...	238R5	238B5	239G5
D14		0R4	0B4	1G4	...	238R4	238B4	239G4
D13		0R3	0B3	1G3	...	238R3	238B3	239G3
D12		0R2	0B2	1G2	...	238R2	238B2	239G2
D11		0R1	0B1	1G1	...	238R1	238B1	239G1
D10		0R0	0B0	1G0	...	238R0	238B0	239G0
D9					...			
D8					...			
D7	C7	0G5	1R5	1B5	...	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	...	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	...	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	...	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	...	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	...	238G0	239R0	239B0
D1	C1				...			
D0	C0				...			

**MDT[1:0] = "01"**

Count	0	1	2	3	...	357	358	479	480
D/CX	0	1	1	1	...		1	1	1
D15		0R5	0B5	1R5	1B5	...	238R5	238B5	239R5
D14		0R4	0B4	1R4	1B4	...	238R4	238B4	239R4
D13		0R3	0B3	1R3	1B3	...	238R3	238B3	239R3
D12		0R2	0B2	1R2	1B2	...	238R2	238B2	239R2
D11		0R1	0B1	1R1	1B1	...	238R1	238B1	239R1
D10		0R0	0B0	1R0	1B0	...	238R0	238B0	239R0
D9					...				
D8					...				
D7	C7	0G5		1G5		...	238G5		239G5
D6	C6	0G4		1G4		...	238G4		239G4
D5	C5	0G3		1G3		...	238G3		239G3
D4	C4	0G2		1G2		...	238G2		239G2
D3	C3	0G1		1G1		...	238G1		239G1
D2	C2	0G0		1G0		...	238G0		239G0
D1	C1				...				
D0	C0				...				

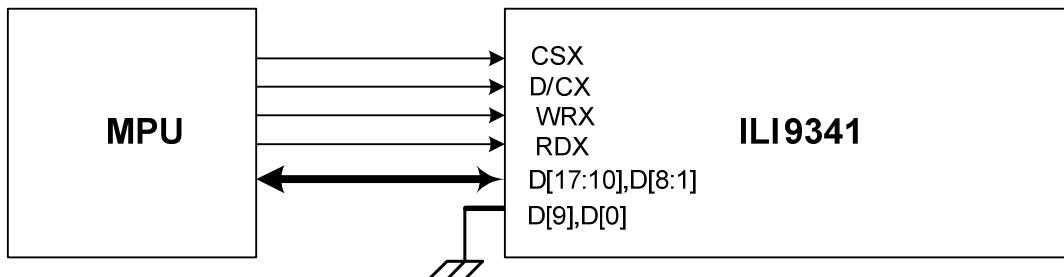
**MDT[1:0] = "10"**

Count	0	1	2	3		...	357	358	479	480
D/CX	0	1	1	1		...		1	1	1
D15		0R5	0B1	1R5	1B1	...	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	...	238R4	238B0	239R4	239B0
D13		0R3		1R3		...	238R3		239R3	
D12		0R2		1R2		...	238R2		239R2	
D11		0R1		1R1		...	238R1		239R1	
D10		0R0		1R0		...	238R0		239R0	
D9		0G5		1G5		...	238G5		239G5	
D8		0G4		1G4		...	238G4		239G4	
D7	C7	0G3		1G3		...	238G3		239G3	
D6	C6	0G2		1G2		...	238G2		239G2	
D5	C5	0G1		1G1		...	238G1		239G1	
D4	C4	0G0		1G0		...	238G0		239G0	
D3	C3	0B5		1B5		...	238B5		239B5	
D2	C2	0B4		1B4		...	238B4		239B4	
D1	C1	0B3		1B3		...	238B3		239B3	
D0	C0	0B2		1B2		...	238B2		239B2	

**MDT[1:0] = "11"**

Count	0	1	2	3		...	357	358	479	480
D/CX	0	1	1	1		...		1	1	1
D15			0R3		1R3	...	238R3		239R3	
D14			0R2		1R2	...	238R2		239R2	
D13			0R1		1R1	...	238R1		239R1	
D12			0R0		1R0	...	238R0		239R0	
D11			0G5		1G5	...	238G5		239G5	
D10			0G4		1G4	...	238G4		239G4	
D9			0G3		1G3	...	238G3		239G3	
D8			0G2		1G2	...	238G2		239G2	
D7	C7		0G1		1G1	...	238G1		239G1	
D6	C6		0G0		1G0	...	238G0		239G0	
D5	C5		0B5		1B5	...	238B5		239B5	
D4	C4		0B4		1B4	...	238B4		239B4	
D3	C3		0B3		1B3	...	238B3		239B3	
D2	C2		0B2		1B2	...	238B2		239B2	
D1	C1	0R5	0B1	1R5	1B1	...	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	...	238R4	238B0	239R4	239B0

The 8080-II system 16-bit parallel bus interface of ILI9341 can be selected by settings IM [3:0] = "1000". The following shown figure is the example of interface with 8080-II MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17	0R4	1R4	2R4	...	237R4	238R4	239R4	
D16	0R3	1R3	2R3	...	237R3	238R3	239R3	
D15	0R2	1R2	2R2	...	237R2	238R2	239R2	
D14	0R1	1R1	2R1	...	237R1	238R1	239R1	
D13	0R0	1R0	2R0	...	237R0	238R0	239R0	
D12	0G5	1G5	2G5	...	237G5	238G5	239G5	
D11	0G4	1G4	2G4	...	237G4	238G4	239G4	
D10	0G3	1G3	2G3	...	237G3	238G3	239G3	
D8	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

**262K color: 18-bit/pixel (RGB 6-6-6 bits input)**

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

**MDT[1:0] = "00"**

Count	0	1	2	3	...	358	359	360
D/CX	0	1	1	1	...	1	1	1
D17		0R5	0B5	1G5	...	238R5	238B5	239G5
D16		0R4	0B4	1G4	...	238R4	238B4	239G4
D15		0R3	0B3	1G3	...	238R3	238B3	239G3
D14		0R2	0B2	1G2	...	238R2	238B2	239G2
D13		0R1	0B1	1G1	...	238R1	238B1	239G1
D12		0R0	0B0	1G0	...	238R0	238B0	239G0
D11					...			
D10					...			
D8	C7	0G5	1R5	1B5	...	238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	...	238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	...	238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	...	238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	...	238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	...	238G0	239R0	239B0
D2	C1				...			
D1	C0				...			

**MDT[1:0] = "01"**

Count	0	1	2	3	...	357	358	479	480
D/CX	0	1	1	1	...		1	1	1
D17		0R5	0B5	1R5	1B5	...	238R5	238B5	239R5
D16		0R4	0B4	1R4	1B4	...	238R4	238B4	239R4
D15		0R3	0B3	1R3	1B3	...	238R3	238B3	239R3
D14		0R2	0B2	1R2	1B2	...	238R2	238B2	239R2
D13		0R1	0B1	1R1	1B1	...	238R1	238B1	239R1
D12		0R0	0B0	1R0	1B0	...	238R0	238B0	239R0
D11					...				
D10					...				
D8	C7	0G5		1G5		...	238G5		239G5
D7	C6	0G4		1G4		...	238G4		239G4
D6	C5	0G3		1G3		...	238G3		239G3
D5	C4	0G2		1G2		...	238G2		239G2
D4	C3	0G1		1G1		...	238G1		239G1
D3	C2	0G0		1G0		...	238G0		239G0
D2	C1				...				
D1	C0				...				

**MDT[1:0] = "10"**

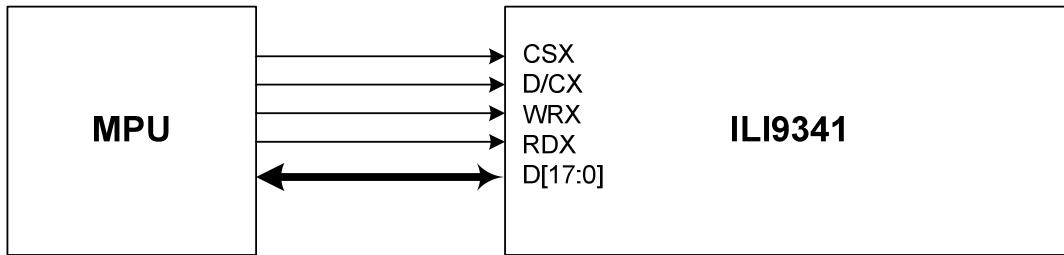
Count	0	1	2	3		...	357	358	479	480
D/CX	0	1	1	1		...		1	1	1
D17		0R5	0B1	1R5	1B1	...	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	...	238R4	238B0	239R4	239B0
D15		0R3		1R3		...	238R3		239R3	
D14		0R2		1R2		...	238R2		239R2	
D13		0R1		1R1		...	238R1		239R1	
D12		0R0		1R0		...	238R0		239R0	
D11		0G5		1G5		...	238G5		239G5	
D10		0G4		1G4		...	238G4		239G4	
D8	C7	0G3		1G3		...	238G3		239G3	
D7	C6	0G2		1G2		...	238G2		239G2	
D6	C5	0G1		1G1		...	238G1		239G1	
D5	C4	0G0		1G0		...	238G0		239G0	
D4	C3	0B5		1B5		...	238B5		239B5	
D3	C2	0B4		1B4		...	238B4		239B4	
D2	C1	0B3		1B3		...	238B3		239B3	
D1	C0	0B2		1B2		...	238B2		239B2	

**MDT[1:0] = "11"**

Count	0	1	2	3		...	357	358	479	480
D/CX	0	1	1	1		...		1	1	1
D17			0R3		1R3	...	238R3		239R3	
D16			0R2		1R2	...	238R2		239R2	
D15			0R1		1R1	...	238R1		239R1	
D14			0R0		1R0	...	238R0		239R0	
D13			0G5		1G5	...	238G5		239G5	
D12			0G4		1G4	...	238G4		239G4	
D11			0G3		1G3	...	238G3		239G3	
D10			0G2		1G2	...	238G2		239G2	
D8	C7		0G1		1G1	...	238G1		239G1	
D7	C6		0G0		1G0	...	238G0		239G0	
D6	C5		0B5		1B5	...	238B5		239B5	
D5	C4		0B4		1B4	...	238B4		239B4	
D4	C3		0B3		1B3	...	238B3		239B3	
D3	C2		0B2		1B2	...	238B2		239B2	
D2	C1	0R5	0B1	1R5	1B1	...	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	...	238R4	238B0	239R4	239B0

### 7.6.6. 18-bit Parallel MCU Interface

The 8080- I system 18-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM[3:0] to “0011”.The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

#### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

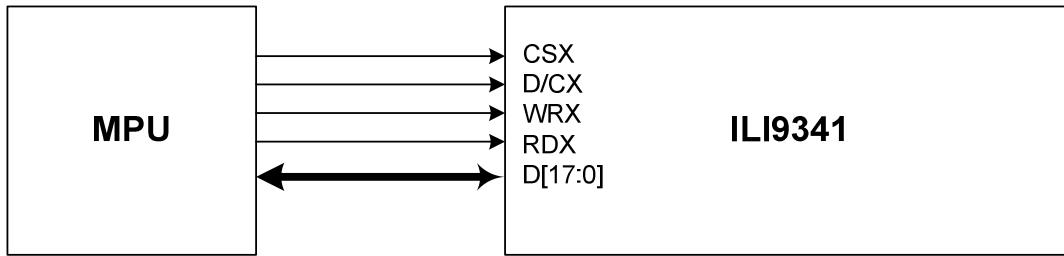
Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	...	237R4	238R4	239R4
D14		0R3	1R3	2R3	...	237R3	238R3	239R3
D13		0R2	1R2	2R2	...	237R2	238R2	239R2
D12		0R1	1R1	2R1	...	237R1	238R1	239R1
D11		0R0	1R0	2R0	...	237R0	238R0	239R0
D10		0G5	1G5	2G5	...	237G5	238G5	239G5
D9		0G4	1G4	2G4	...	237G4	238G4	239G4
D8		0G3	1G3	2G3	...	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

**262K color: 18-bit/pixel (RGB 6-6-6 bits input)**

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17		0R5	1R5	2R5	...	237R5	238R5	239R5
D16		0R4	1R4	2R4	...	237R4	238R4	239R4
D15		0R3	1R3	2R3	...	237R3	238R3	239R3
D14		0R2	1R2	2R2	...	237R2	238R2	239R2
D13		0R1	1R1	2R1	...	237R1	238R1	239R1
D12		0R0	1R0	2R0	...	237R0	238R0	239R0
D11		0G5	1G5	2G5	...	237G5	238G5	239G5
D10		0G4	1G4	2G4	...	237G4	238G4	239G4
D9		0G3	1G3	2G3	...	237G3	238G3	239G3
D8		0G2	1G2	2G2	...	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	...	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	...	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	...	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

The 8080-II system 18-bit parallel bus interface mode can be selected by settings IM [3:0] = "1010". The following shown figure is the example of interface with 8080-II MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17								
D16								
D15	0R4	1R4	2R4	...	237R4	238R4	239R4	
D14	0R3	1R3	2R3	...	237R3	238R3	239R3	
D13	0R2	1R2	2R2	...	237R2	238R2	239R2	
D12	0R1	1R1	2R1	...	237R1	238R1	239R1	
D11	0R0	1R0	2R0	...	237R0	238R0	239R0	
D10	0G5	1G5	2G5	...	237G5	238G5	239G5	
D9	0G4	1G4	2G4	...	237G4	238G4	239G4	
D8	C7	0G3	1G3	2G3	...	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	...	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	...	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	...	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	...	237B1	238B1	239B1
D0		0B0	1B0	2B0	...	237B0	238B0	239B0

**262K color: 18-bit/pixel (RGB 6-6-6 bits input)**

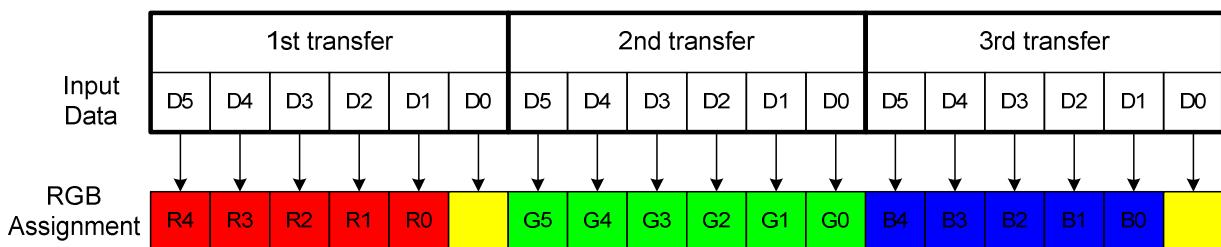
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17		0R5	1R5	2R5	...	237R5	238R5	239R5
D16		0R4	1R4	2R4	...	237R4	238R4	239R4
D15		0R3	1R3	2R3	...	237R3	238R3	239R3
D14		0R2	1R2	2R2	...	237R2	238R2	239R2
D13		0R1	1R1	2R1	...	237R1	238R1	239R1
D12		0R0	1R0	2R0	...	237R0	238R0	239R0
D11		0G5	1G5	2G5	...	237G5	238G5	239G5
D10		0G4	1G4	2G4	...	237G4	238G4	239G4
D9		0G3	1G3	2G3	...	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	...	237B5	238B5	239B5
D4	C3	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	...	237B1	238B1	239B1
D0		0B0	1B0	2B0	...	237B0	238B0	239B0

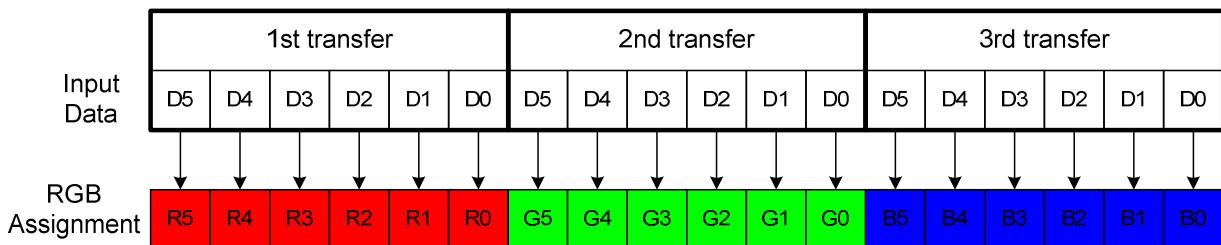
### 7.6.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

#### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)



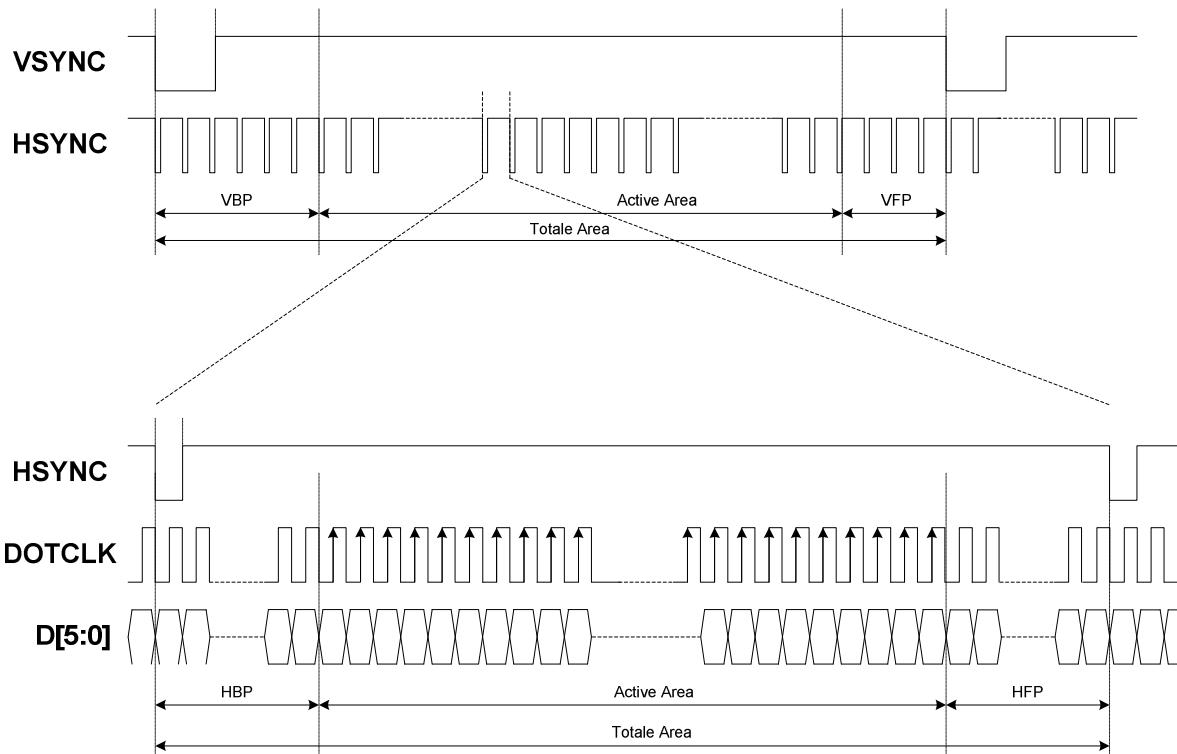
#### 262K color: 18-bit/pixel (RGB 6-6-6 bits input)



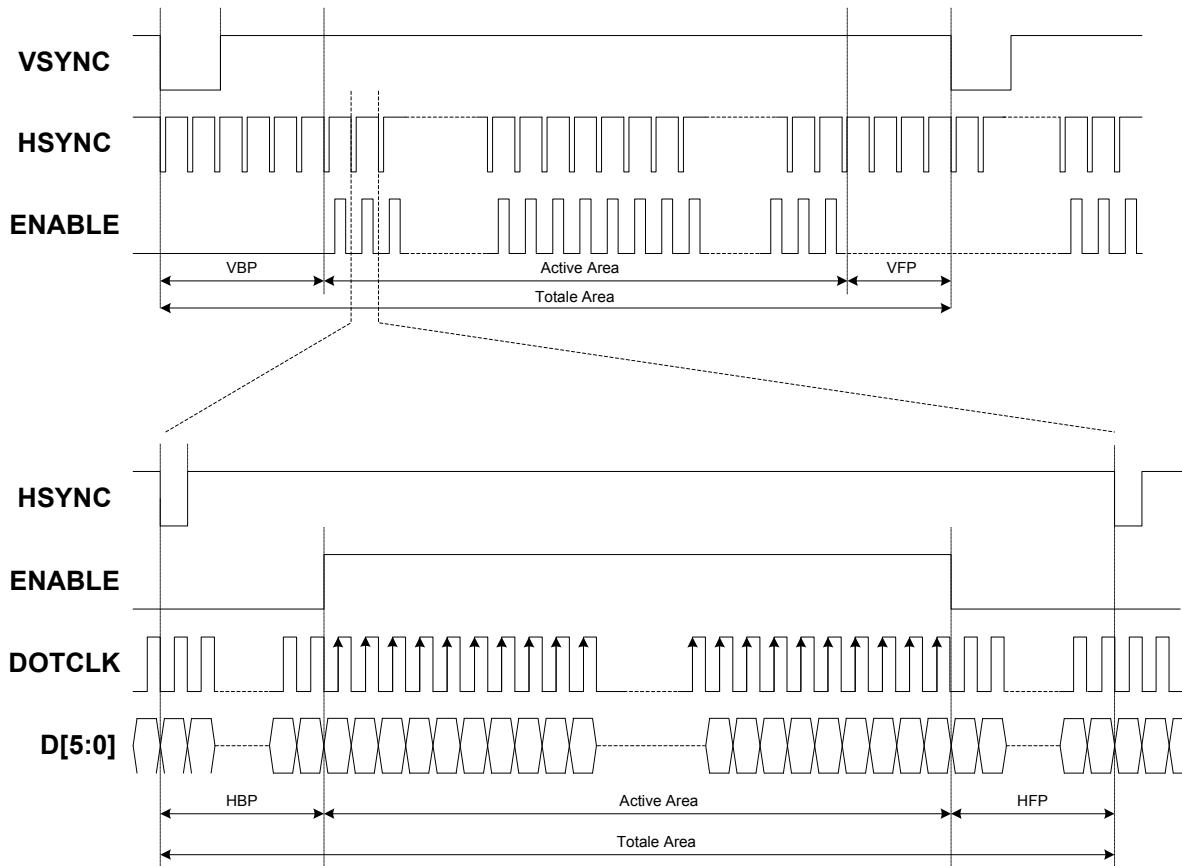
ILI9341 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

**SYNC Mode, RCM[1:0] = "11"**

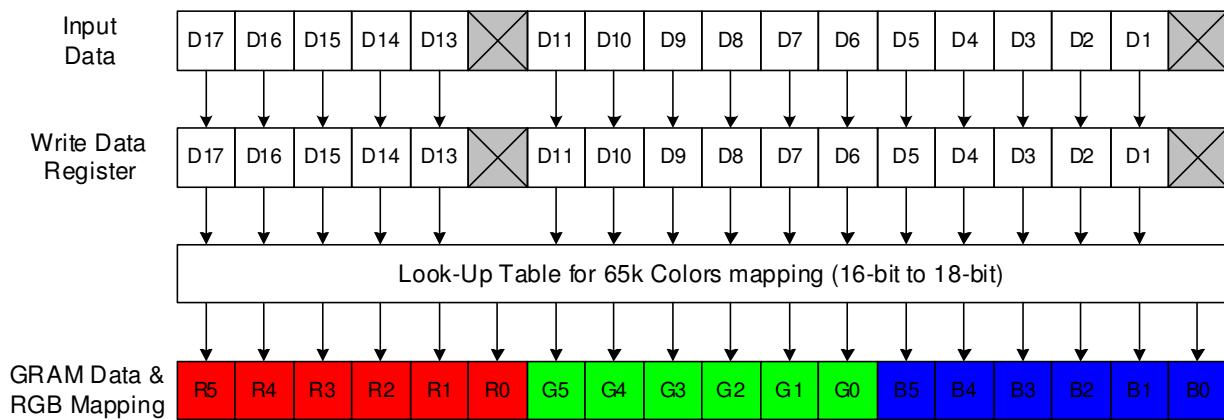


**DE Mode, RCM[1:0] = "10"**



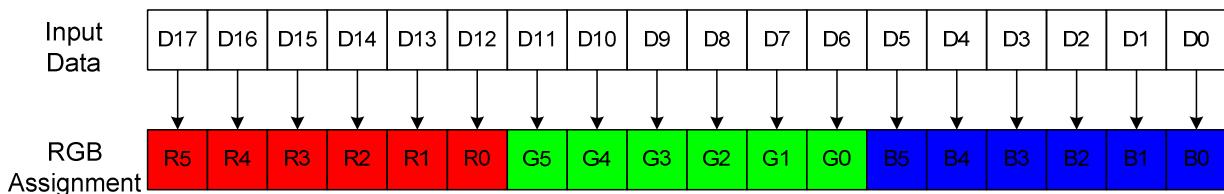
### 7.6.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [17:13] & D [11:1]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:13] and D [11:1] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



### 7.6.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.



## 8. Command

### 8.1. Command List

Regulative Command Set															
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex		
No Operation	0	1	↑	XX	0	0	0	0	0	0	0	0	0	00h	
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	0	1	01h	
Read Display Identification Information	0	1	↑	XX	0	0	0	0	0	1	0	0	0	04h	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
	1	↑	1	XX	ID1 [7:0]								XX		
	1	↑	1	XX	ID2 [7:0]								XX		
	1	↑	1	XX	ID3 [7:0]								XX		
	0	1	↑	XX	0	0	0	0	1	0	0	1	09h		
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
Read Display Status	1	↑	1	XX	D [31:25]								X	00	
	1	↑	1	XX	X	D [22:20]			D [19:16]					61	
	1	↑	1	XX	X	X	X	X	X	D [10:8]			00		
	1	↑	1	XX	D [7:5]			X	X	X	X	X	X	00	
	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah		
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
Read Display Power Mode	1	↑	1	XX	D [7:2]								0	0	08
	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh		
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
Read Display MADCTL	1	↑	1	XX	D [7:2]								0	0	00
	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch		
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
Read Display Pixel Format	1	↑	1	XX	RIM	DPI [2:0]			X	DBI [2:0]				06	
	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh		
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
Read Display Image Format	1	↑	1	XX	X	X	X	X	X	D [2:0]				00	
	0	1	↑	XX	0	0	0	0	1	1	1	1	0Eh		
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
Read Display Signal Mode	1	↑	1	XX	D [7:2]								0	0	00
	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh		
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
Read Display Self-Diagnostic Result	1	↑	1	XX	D [7:6]								00		
	0	1	↑	XX	0	0	0	0	1	0	0	0	0	10h	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX		
Enter Sleep Mode	0	1	↑	XX	0	0	0	0	1	0	0	0	0	11h	
Sleep OUT	0	1	↑	XX	0	0	0	0	1	0	0	0	1	12h	
Partial Mode ON	0	1	↑	XX	0	0	0	0	1	0	0	0	1	13h	
Normal Display Mode ON	0	1	↑	XX	0	0	0	0	1	0	0	0	1	14h	
Display Inversion OFF	0	1	↑	XX	0	0	0	1	0	0	0	0	0	20h	
Display Inversion ON	0	1	↑	XX	0	0	0	1	0	0	0	0	0	21h	
Gamma Set	0	1	↑	XX	0	0	1	0	0	0	1	1	0	26h	
	1	1	↑	XX	GC [7:0]								01		
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	0	28h	
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	0	1	29h	
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC [15:8]								XX		
	1	1	↑	XX	SC [7:0]								XX		
	1	1	↑	XX	EC [15:8]								XX		
	1	1	↑	XX	EC [7:0]								XX		
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	1	2Bh	
	1	1	↑	XX	SP [15:8]								XX		
	1	1	↑	XX	SP [7:0]								XX		
	1	1	↑	XX	EP [15:8]								XX		
	1	1	↑	XX	EP [7:0]								XX		

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Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch	
	1	1	↑										XX	
Color SET	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh	
	1	↑	1	XX									R00 [5:0]	
	1	↑	1	XX									Rnn [5:0]	
	1	↑	1	XX									R31 [5:0]	
	1	↑	1	XX									G00 [5:0]	
	1	↑	1	XX									Gnn [5:0]	
	1	↑	1	XX									G64 [5:0]	
	1	↑	1	XX									B00 [5:0]	
	1	↑	1	XX									Bnn [5:0]	
	1	↑	1	XX									B31 [5:0]	
Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
	1	↑	1										D [17:0]	
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h	
	1	1	↑	XX									SR [15:8]	
	1	1	↑	XX									SR [7:0]	
	1	1	↑	XX									ER [15:8]	
	1	1	↑	XX									ER [7:0]	
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h	
	1	1	↑	XX									TFA [15:8]	
	1	1	↑	XX									TFA [7:0]	
	1	1	↑	XX									VSA [15:8]	
	1	1	↑	XX									VSA [7:0]	
	1	1	↑	XX									BFA [15:8]	
	1	1	↑	XX									BFA [7:0]	
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h	
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h	
	1	1	↑	XX	X	X	X	X	X	X	X	M	00	
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h	
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00	
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h	
	1	1	↑	XX									VSP [15:8]	
	1	1	↑	XX									VSP [7:0]	
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h	
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h	
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah	
	1	1	↑	XX	X		DPI [2:0]		X			DBI [2:0]	66	
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch	
	1	1	↑				D [17:0]						XX	
Read Memory Continue	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
	1	↑	1				D [17:0]						XX	
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h	
	1	1	↑	XX	X	X	X	X	X	X	X	STS [8]	00	
	1	1	↑	XX									STS [7:0]	00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	X	X	X	X	X	X	X	X	GTS [9:8]	00
	1	↑	1	XX									GTS [7:0]	00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h	
	1	1	↑	XX									DBV [7:0]	00

Read Display Brightness	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
	1	↑	1	XX	X	X	X	X	X	X	X	XX	
	1	↑	1	XX									00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read CTRL Display	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	X	X	BCTRL	X	DD	BL	X	X	00
Write Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XX	X	X	X	X	X	X	C [1:0]	00	
Read Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XX	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	X	X	X	X	X	X	C [1:0]	00	
Write CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	XX									00
Read CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	0	1	1	1	5Fh
	1	↑	1	XX	X	X	X	X	X	X	X	XX	
	1	↑	1	XX									00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	XX	
	1	↑	1	XX									XX
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	XX	
	1	↑	1	XX									XX
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	XX	
	1	↑	1	XX									XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	ByPass MODE	RCM [1:0]	X	VSP	HSPL	DPL	EPL		40
Frame Control (In Normal Mode)	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XX	X	X	X	X	X	X	X		00
	1	1	↑	XX	X	X	X						1B
Frame Control (In Idle Mode)	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XX	X	X	X	X	X	X	X		00
	1	1	↑	XX	X	X	X						1B
Frame Control (In Partial Mode)	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XX	X	X	X	X	X	X	X		00
	1	1	↑	XX	X	X	X						1B
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	0	1	0	B4h
	1	1	↑	XX	X	X	X	X	X	NLA	NLB	NLC	02
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0								02
	1	1	↑	XX	0								02
	1	1	↑	XX	0	0	0						0A
	1	1	↑	XX	0	0	0						14

Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	X	X	X	X	PTG [1:0]		PT [1:0]		0A
	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				82
	1	1	↑	XX	X	X	NL [5:0]				PCDIV [5:0]		27
	1	1	↑	XX	X	X	PCDIV [5:0]				XX		XX
Entry Mode Set	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XX	X	X	X	X	0	GON	DTE	GAS	07
Backlight Control 1	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	X	X	X	X	TH UI [3:0]				04
Backlight Control 2	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	TH MV [3:0]				TH ST [3:0]				B8
Backlight Control 3	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	X	X	X	X	DTH UI [3:0]				04
Backlight Control 4	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	DTH MV [3:0]				DTH ST [3:0]				C9
Backlight Control 5	0	1	↑	XX	1	0	1	1	1	1	1	0	BCh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	DIM2 [3:0]				X	DIM1 [2:0]			44
Backlight Control 7	0	1	↑	XX	1	0	1	1	1	1	1	1	BEh
	1	1	↑	XX	PWM DIV [7:0]				0F				
Backlight Control 8	0	1	↑	XX	1	0	1	1	1	1	1	1	BFh
	1	1	↑	XX	X	X	X	X	X	LEDONR	LEDONPOL	LEDPWMOPL	00
Power Control 1	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XX	X	X	VRH [5:0]				26		
Power Control 2	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	X	X	X	X	X	BT [2:0]			00
VCOM Control 1	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XX	X	VMH [6:0]				31			
	1	1	↑	XX	X	VML [6:0]				3C			
VCOM Control 2	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
	1	1	↑	XX	nVM	VMF [6:0]				C0			
NV Memory Write	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
	1	1	↑	XX	X	X	X	X	X	PGM ADR [2:0]			00
	1	1	↑	XX	PGM DATA [7:0]				XX				
NV Memory Protection Key	0	1	↑	XX	1	1	0	1	0	0	0	0	D1h
	1	1	↑	XX	KEY [23:16]				55				
	1	1	↑	XX	KEY [15:8]				AA				
	1	1	↑	XX	KEY [7:0]				66				
NV Memory Status Read	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	ID2_CNT [2:0]		X	ID1_CNT [2:0]			XX	
	1	↑	1	XX	BUSY	VMF_CNT [2:0]		X	ID3_CNT [2:0]			XX	

Read ID4	0	↑	1	XX	1	1	0	1	0	0	1	1	D3h	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	0	0	0	0	0	0	0	0	00	
	1	↑	1	XX	1	0	0	1	0	0	1	1	93	
	1	↑	1	XX	0	1	0	0	0	0	0	1	41	
Positive Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h	
	1	1	↑	XX	X	X	X	X	VP0 [3:0]				08	
	1	1	↑	XX	X	X	VP1 [5:0]				0E			
	1	1	↑	XX	X	X	VP2 [5:0]				12			
	1	1	↑	XX	X	X	X	X	VP4 [3:0]				05	
	1	1	↑	XX	X	X	X	X	VP6 [4:0]				03	
	1	1	↑	XX	X	X	X	X	VP13 [3:0]				09	
	1	1	↑	XX	X	VP20 [6:0]				47				
	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]				86	
	1	1	↑	XX	X	VP43 [6:0]				2B				
	1	1	↑	XX	X	X	X	X	VP50 [3:0]				0B	
	1	1	↑	XX	X	X	X	X	VP57 [4:0]				04	
	1	1	↑	XX	X	X	X	X	VP59 [3:0]				00	
	1	1	↑	XX	X	X	VP61 [5:0]				00			
	1	1	↑	XX	X	X	VP62 [5:0]				00			
	1	1	↑	XX	X	X	X	X	VP63 [3:0]				00	
Negative Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	0	E1h	
	1	1	↑	XX	X	X	X	X	VN0 [3:0]				08	
	1	1	↑	XX	X	X	VN1 [5:0]				1A			
	1	1	↑	XX	X	X	VN2 [5:0]				20			
	1	1	↑	XX	X	X	X	X	VN4 [3:0]				07	
	1	1	↑	XX	X	X	X	X	VN6 [4:0]				0E	
	1	1	↑	XX	X	X	X	X	VN13 [3:0]				05	
	1	1	↑	XX	X	VN20 [6:0]				3A				
	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]				8A	
	1	1	↑	XX	X	VN43 [6:0]				40				
	1	1	↑	XX	X	X	X	X	VN50 [3:0]				04	
	1	1	↑	XX	X	X	X	X	VN57 [4:0]				18	
	1	1	↑	XX	X	X	X	X	VN59 [3:0]				0F	
	1	1	↑	XX	X	X	VN61 [5:0]				3F			
	1	1	↑	XX	X	X	VN62 [5:0]				3F			
	1	1	↑	XX	X	X	X	X	VN63 [3:0]				0F	
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	0	1	0	E2h
1 <sup>st</sup> Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				XX	
:	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				XX	
16 <sup>th</sup> Parameter	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]				XX	
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	0	1	1	E3h
1 <sup>st</sup> Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				XX	
:	1	1	↑	XX	RFAX [3:0]				BFAX [3:0]				XX	
64 <sup>th</sup> Parameter	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]				XX	
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	1	0	F6h
	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	X	BGR_EOR	X	X	WEMODE	01	
	1	1	↑	XX	X	X	EPF [1:0]		X	X	MDT [1:0]		00	
	1	1	↑	XX	X	X	ENDIAN	X	DM [1:0]	RM	RIM	00		

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP

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(00h).

*Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9341 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.*

## 8.2. Description of Level 1 Command

### 8.2.1. NOP (00h)

00h														NOP (No Operation)																					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																						
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h																						
Parameter	No Parameter.																																		
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.																																		
Restriction	None																																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>															Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																																		
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																		
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Status	Default Value																																		
Power On Sequence	N/A																																		
SW Reset	N/A																																		
HW Reset	N/A																																		
Flow Chart	None																																		

### 8.2.2. Software Reset (01h)

SWRESET																									
01h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h												
Parameter	No Parameter.																								
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command X = Don't care.																								
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	<pre> graph TD     SWRESET[SWRESET(01h)] --&gt; Blank[Display whole blank screen]     Blank --&gt; Default[Set Commands to S/W Default Values]     Default --&gt; SleepIn[Sleep In Mode]     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

### 8.2.3. Read display identification information (04h)

04h		RDDIDIF (Read Display Identification Information)																								
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command		0	1	↑	XX	0	0	0	0	0	1	0	0	04h												
1 <sup>st</sup> Parameter		1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 <sup>nd</sup> Parameter		1	↑	1	XX	ID1 [7:0]							XX													
3 <sup>rd</sup> Parameter		1	↑	1	XX	ID2 [7:0]							XX													
4 <sup>th</sup> Parameter		1	↑	1	XX	ID3 [7:0]							XX													
Description	This read byte returns 24 bits display identification information. The 1 <sup>st</sup> parameter is dummy data. The 2 <sup>nd</sup> parameter (ID1 [7:0]): LCD module's manufacturer ID. The 3 <sup>rd</sup> parameter (ID2 [7:0]): LCD module/driver version ID. The 4 <sup>th</sup> parameter (ID3 [7:0]): LCD module/driver ID.																									
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
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Sleep In	Yes																									
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Status	Default Value																									
Power On Sequence	See description																									
SW Reset	See description																									
HW Reset	See description																									
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																									

### 8.2.4. Read Display Status (09h)

09h		RDDST (Read Display Status)												
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑		XX	0	0	0	0	1	0	0	1	09h
1 <sup>st</sup> Parameter	1	↑	1		XX	X	X	X	X	X	X	X	X	X
2 <sup>nd</sup> Parameter	1	↑	1		XX	D [31:25]					0			
3 <sup>rd</sup> Parameter	1	↑	1		XX	0	D [22:20]			D [19:16]				61
4 <sup>th</sup> Parameter	1	↑	1		XX	0	0	0	0	0	D [10:8]			00
5 <sup>th</sup> Parameter	1	↑	1		XX	D [7:5]			0	0	0	0	0	00
Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description			Value	Status								
	D31	Booster voltage status			0	Booster OFF								
					1	Booster ON								
	D30	Row address order			0	Top to Bottom (When MADCTL B7='0')								
					1	Bottom to Top (When MADCTL B7='1')								
	D29	Column address order			0	Left to Right (When MADCTL B6='0').								
					1	Right to Left (When MADCTL B6='1').								
	D28	Row/column exchange			0	Normal Mode (When MADCTL B5='0').								
					1	Reverse Mode (When MADCTL B5='1').								
	D27	Vertical refresh			0	LCD Refresh Top to Bottom (When MADCTL B4='0')								
					1	LCD Refresh Bottom to Top (When MADCTL B4='1').								
	D26	RGB/BGR order			0	RGB (When MADCTL B3='0')								
					1	BGR (When MADCTL B3='1')								
	D25	Horizontal refresh order			0	LCD Refresh Left to Right (When MADCTL B2='0')								
					1	LCD Refresh Right to Left (When MADCTL B2='1')								
	D24	Not used			0	---								
	D23	Not used			0	---								
	D22	Interface color pixel format definition			101	16-bit/pixel								
	D21				110	18-bit/pixel								
	D20	Idle mode ON/OFF			0	Idle Mode OFF								
					1	Idle Mode ON								
	D19	Partial mode ON/OFF			0	Partial Mode OFF								
					1	Partial Mode ON.								
	D18	Sleep IN/OUT			0	Sleep IN Mode								
					1	Sleep OUT Mode.								
	D17	Display normal mode ON/OFF			0	Display Normal Mode OFF.								
					1	Display Normal Mode ON.								
	D16	Vertical scrolling status			0	Scroll OFF								
	D15	Not used			0	---								
	D14	Inversion status			0	Not defined								
	D13	All pixel ON			0	Not defined								
	D12	All pixel OFF			0	Not defined								
	D11	Display ON/OFF			0	Display is OFF								
					1	Display is ON								
	D10	Tearing effect line ON/OFF			0	Tearing Effect Line OFF								
					1	Tearing Effect ON								
	D9	Gamma curve selection			000	GC0								
					001	---								
					010	---								
					011	---								
					other	Not defined								

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		D5	Tearing effect line mode	0	Mode 1, V-Blanking only													
				1	Mode 2, both H-Blanking and V-Blanking.													
		D4	Not used	0	---													
		D3	Not used	0	---													
		D2	Not used	0	---													
		D1	Not used	0	---													
		D0	Not used	0	---													
		X = Don't care																
Restriction																		
Register Availability					<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
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Flow Chart				<p>RDDST(09h)</p> <p>Host</p> <p>Driver</p> <p>Legend</p> <p>Command</p> <p>Parameter</p> <p>Display</p> <p>Action</p> <p>Mode</p> <p>Sequential transfer</p>														

### 8.2.5. Read Display Power Mode (0Ah)

0Ah		RDDPM (Read Display Power Mode)																																																																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																											
Command		0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah																																																											
1 <sup>st</sup> Parameter		1	↑	1	XX	X	X	X	X	X	X	X	X	X																																																											
2 <sup>nd</sup> Parameter		1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	08																																																											
Description	This command indicates the current status of the display as described in the table below::																																																																								
	<table border="1"> <thead> <tr> <th>Bit</th><th>Value</th><th>Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>D7</td><td>0</td><td>Booster Off or has a fault.</td><td>---</td></tr> <tr> <td>D7</td><td>1</td><td>Booster On and working OK</td><td>---</td></tr> <tr> <td>D6</td><td>0</td><td>Idle Mode Off.</td><td>---</td></tr> <tr> <td>D6</td><td>1</td><td>Idle Mode On.</td><td>---</td></tr> <tr> <td>D5</td><td>0</td><td>Partial Mode Off.</td><td>---</td></tr> <tr> <td>D5</td><td>1</td><td>Partial Mode On.</td><td>---</td></tr> <tr> <td>D4</td><td>0</td><td>Sleep In Mode</td><td>---</td></tr> <tr> <td>D4</td><td>1</td><td>Sleep Out Mode</td><td>---</td></tr> <tr> <td>D3</td><td>0</td><td>Display Normal Mode Off.</td><td>---</td></tr> <tr> <td>D3</td><td>1</td><td>Display Normal Mode On</td><td>---</td></tr> <tr> <td>D2</td><td>0</td><td>Display is Off.</td><td>---</td></tr> <tr> <td>D2</td><td>1</td><td>Display is On</td><td>---</td></tr> <tr> <td>D1</td><td>--</td><td>Not Defined</td><td>Set to '0'</td></tr> <tr> <td>D0</td><td>--</td><td>Not Defined</td><td>Set to '0'</td></tr> </tbody> </table>														Bit	Value	Description	Comment	D7	0	Booster Off or has a fault.	---	D7	1	Booster On and working OK	---	D6	0	Idle Mode Off.	---	D6	1	Idle Mode On.	---	D5	0	Partial Mode Off.	---	D5	1	Partial Mode On.	---	D4	0	Sleep In Mode	---	D4	1	Sleep Out Mode	---	D3	0	Display Normal Mode Off.	---	D3	1	Display Normal Mode On	---	D2	0	Display is Off.	---	D2	1	Display is On	---	D1	--	Not Defined	Set to '0'	D0	--	Not Defined
Bit	Value	Description	Comment																																																																						
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Flow Chart	<p>The flowchart illustrates the communication between the Host and the Driver. The Host sends the RDDPM(0Ah) command to the Driver. The Driver responds with two parameters: the 1st Parameter is a dummy read, and the 2nd Parameter is the send of the D[7:2] display power mode status.</p> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command (triangular box)</li> <li>Parameter (horizontal bar)</li> <li>Display (oval)</li> <li>Action (diamond)</li> <li>Mode (horizontal bar)</li> <li>Sequential transfer (oval)</li> </ul>																																																																								

### 8.2.6. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh													
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X													
2 <sup>nd</sup> Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00													
Description	This command indicates the current status of the display as described in the table below:																									
	Bit	Value	Description										Comment													
	D7	0	Top to Bottom (When MADCTL B7='0').										---													
		1	Bottom to Top (When MADCTL B7='1').										---													
	D6	0	Left to Right (When MADCTL B6='0')										---													
		1	Right to Left (When MADCTL B6='1')										---													
	D5	0	Normal Mode (When MADCTL B5='0').										---													
		1	Reverse Mode (When MADCTL B5='1')										---													
	D4	0	LCD Refresh Top to Bottom (When MADCTL B4='0')										---													
		1	LCD Refresh Bottom to Top (When MADCTL B4='1').										---													
	D3	0	RGB (When MADCTL B3='0')										---													
		1	BGR (When MADCTL B3='1').										---													
	D2	0	LCD Refresh Left to Right (When MADCTL B2='0').										---													
		1	LCD Refresh Right to Left (When MADCTL B2='1').										---													
	D1	--	Switching between Segment outputs and RAM										Set to '0'													
	D0	--	Switching between Segment outputs and RAM										Set to '0'													
X = Don't care																										
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																									
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Status	Default Value																									
Power On Sequence	8'h00h																									
SW Reset	No Change																									
HW Reset	8'h00h																									
Flow Chart	<p>The flowchart illustrates the communication sequence. A box labeled "RDDMADCTL(0Bh)" is at the top, connected by a vertical line to a dashed horizontal line representing the interface. This line then splits into two paths: one leading to a trapezoid labeled "Host" and another leading to a trapezoid labeled "Driver". The "Driver" trapezoid contains the text "1st Parameter: Dummy Read" and "2nd Parameter: Send D[7:2] display power mode status". To the right of the interface, a legend is enclosed in a dashed box, defining symbols for Command (triangle), Parameter (rectangle), Display (parallelogram), Action (diamond), Mode (oval), and Sequential transfer (horizontal bar).</p>																									

### 8.2.7. Read Display Pixel Format (0Ch)

0Ch		RDDCOLMOD (Read Display Pixel Format)																																													
	D/CX	RDX	WRX	D17-8			D7	D6	D5	D4	D3	D2	D1	D0	HEX																																
Command	0	1	↑	XX			0	0	0	0	1	1	0	0	0Ch																																
1 <sup>st</sup> Parameter	1	↑	1	XX			X	X	X	X	X	X	X	X	X																																
2 <sup>nd</sup> Parameter	1	↑	1	XX			RIM	DPI [2:0]			0	DBI [2:0]			06																																
Description	This command indicates the current status of the display as described in the table below:																																														
	<table border="1"> <thead> <tr> <th>RIM</th> <th>DPI [2:0]</th> <th colspan="2">RGB Interface Format</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0 0 0</td> <td colspan="2">Reserved</td> </tr> <tr> <td>0</td> <td>0 0 1</td> <td colspan="2">Reserved</td> </tr> <tr> <td>0</td> <td>0 1 0</td> <td colspan="2">Reserved</td> </tr> <tr> <td>0</td> <td>0 1 1</td> <td colspan="2">Reserved</td> </tr> <tr> <td>0</td> <td>1 0 0</td> <td colspan="2">Reserved</td> </tr> <tr> <td>0</td> <td>1 0 1</td> <td colspan="2">16 bits / pixel</td> </tr> <tr> <td>0</td> <td>1 1 0</td> <td colspan="2">18 bits / pixel</td> </tr> <tr> <td>0</td> <td>1 1 1</td> <td colspan="2">Reserved</td> </tr> <tr> <td>1</td> <td>1 0 1</td> <td colspan="2">16 bits / pixel (6-bit 3 times data transfer)</td> </tr> <tr> <td>1</td> <td>1 1 0</td> <td colspan="2">18 bits / pixel (6-bit 3 times data transfer)</td> </tr> </tbody> </table>				RIM	DPI [2:0]	RGB Interface Format		0	0 0 0	Reserved		0	0 0 1	Reserved		0	0 1 0	Reserved		0	0 1 1	Reserved		0	1 0 0	Reserved		0	1 0 1	16 bits / pixel		0	1 1 0	18 bits / pixel		0	1 1 1	Reserved		1	1 0 1	16 bits / pixel (6-bit 3 times data transfer)		1	1 1 0	18 bits / pixel (6-bit 3 times data transfer)
RIM	DPI [2:0]	RGB Interface Format																																													
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Flow Chart	<p>The flowchart illustrates the communication between the Host and the Driver. A box labeled "RDDCOLMOD(0Ch)" has an arrow pointing down to a dashed horizontal line separating the Host and Driver. Below the line, the text "1st Parameter: Dummy Read" and "2nd Parameter: Send D[7:2] display pixel format status" is shown. To the right of the line is a legend box containing six items: "Command" (upward arrow), "Parameter" (downward arrow), "Display" (rightward arrow), "Action" (leftward arrow), "Mode" (oval), and "Sequential transfer" (elliptical arrow).</p>																																														

### 8.2.8. Read Display Image Format (0Dh)

RDDIM (Read Display Image Mode)																									
0Dh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	XX	0	0	0	0	0	0	D [2:0]		00												
Description	This command indicates the current status of the display as described in the table below:																								
	<table border="1"> <thead> <tr> <th>D [2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Gamma curve 1 (G2.2)</td> </tr> <tr> <td>001</td> <td>---</td> </tr> <tr> <td>010</td> <td>---</td> </tr> <tr> <td>011</td> <td>---</td> </tr> <tr> <td>Other</td> <td>Not defined</td> </tr> </tbody> </table>													D [2:0]	Description	000	Gamma curve 1 (G2.2)	001	---	010	---	011	---	Other	Not defined
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000	Gamma curve 1 (G2.2)																								
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Status	Default Value																								
Power On Sequence	3'b000																								
SW Reset	3'b000																								
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Flow Chart	<p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> <p>1st Parameter: Dummy Read 2nd Parameter: Send D[7:0] display image mode status</p>																								

### 8.2.9. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)																																																										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																														
Command	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh																																														
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X																																														
2 <sup>nd</sup> Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00																																														
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>0</td> <td>Tearing effect line OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Tearing effect line ON</td> </tr> <tr> <td>D6</td> <td>0</td> <td>Tearing effect line mode 1</td> </tr> <tr> <td></td> <td>1</td> <td>Tearing effect line mode 2</td> </tr> <tr> <td>D5</td> <td>0</td> <td>Horizontal sync. (RGB interface) OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Horizontal sync. (RGB interface) ON</td> </tr> <tr> <td>D4</td> <td>0</td> <td>Vertical sync. (RGB interface) OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Vertical sync. (RGB interface) ON</td> </tr> <tr> <td>D3</td> <td>0</td> <td>Pixel clock (DOTCLK, RGB interface) OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Pixel clock (DOTCLK, RGB interface) ON</td> </tr> <tr> <td>D2</td> <td>0</td> <td>Data enable (DE, RGB interface) OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Data enable (DE, RGB interface) ON</td> </tr> <tr> <td>D1</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>D0</td> <td>0</td> <td>Reserved</td> </tr> </tbody> </table> X = Don't care														Bit	Value	Description	D7	0	Tearing effect line OFF		1	Tearing effect line ON	D6	0	Tearing effect line mode 1		1	Tearing effect line mode 2	D5	0	Horizontal sync. (RGB interface) OFF		1	Horizontal sync. (RGB interface) ON	D4	0	Vertical sync. (RGB interface) OFF		1	Vertical sync. (RGB interface) ON	D3	0	Pixel clock (DOTCLK, RGB interface) OFF		1	Pixel clock (DOTCLK, RGB interface) ON	D2	0	Data enable (DE, RGB interface) OFF		1	Data enable (DE, RGB interface) ON	D1	0	Reserved	D0	0	Reserved
Bit	Value	Description																																																									
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D6	0	Tearing effect line mode 1																																																									
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D5	0	Horizontal sync. (RGB interface) OFF																																																									
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D3	0	Pixel clock (DOTCLK, RGB interface) OFF																																																									
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Flow Chart	<p>The flowchart illustrates the communication between the Host and the Driver. A box labeled "RDDSM(0Eh)" is at the top. An arrow points down to a dashed horizontal line separating the Host from the Driver. Below the line, a trapezoid represents the Driver's response. Inside the trapezoid, the text "1st Parameter: Dummy Read" and "2nd Parameter: Send D[7:0] display signal mode status" is written. To the right of the trapezoid is a legend enclosed in a dashed box:</p> <ul style="list-style-type: none"> <li>Legend</li> <li>Command (arrow pointing up)</li> <li>Parameter (arrow pointing right)</li> <li>Display (oval)</li> <li>Action (arrow pointing left)</li> <li>Mode (arrow pointing down)</li> <li>Sequential transfer (oval)</li> </ul>																																																										

### 8.2.10. Read Display Self-Diagnostic Result (0Fh)

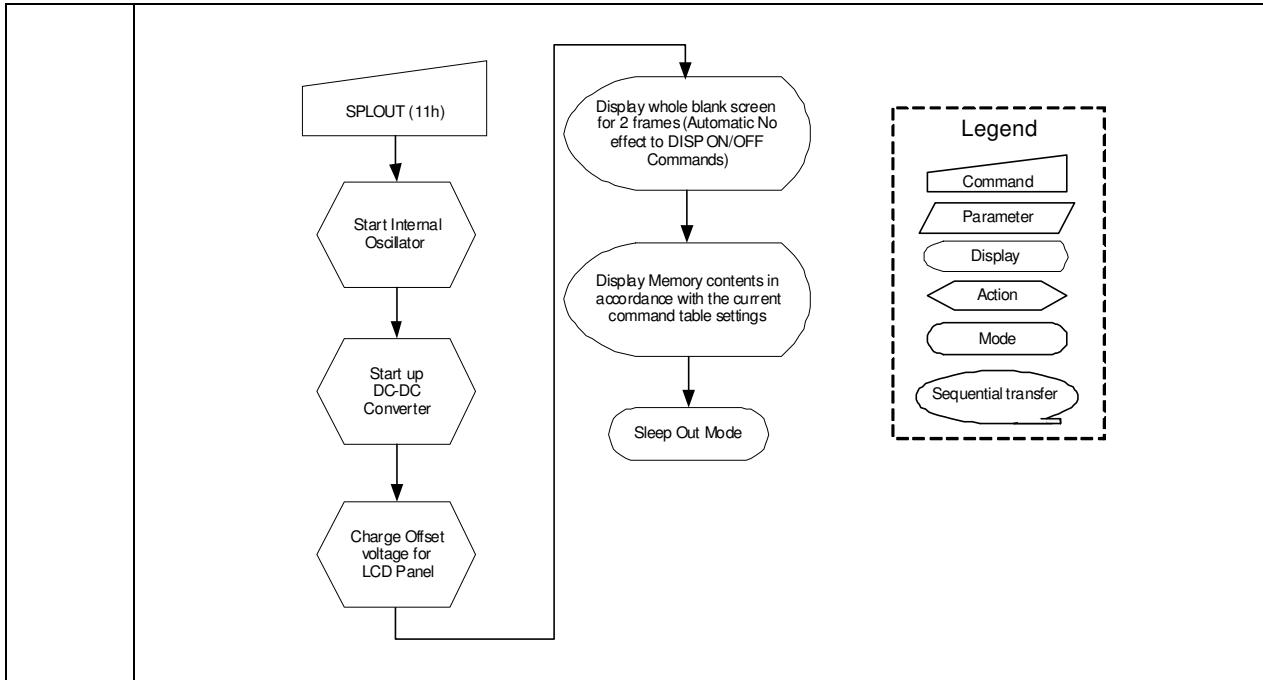
0Fh	RDDSDR (Read Display Self-Diagnostic Result)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00												
Description	Bit	Description		Action																					
	D7	Register Loading Detection		Invert the D7 bit if register values loading work properly.																					
	D6	Functionality Detection		Invert the D6 bit if the display is functionality																					
	D5	Not Used		'0'																					
	D4	Not Used		'0'																					
	D3	Not Used		'0'																					
	D2	Not Used		'0'																					
	D1	Not Used		'0'																					
	D0	Not Used		'0'																					
Restriction																									
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Power On Sequence	8'h00h																								
SW Reset	8'h00h																								
HW Reset	8'h00h																								
Flow Chart	<p>The flowchart illustrates the communication sequence. A box labeled "RDDSDR(0Fh)" is connected by a vertical line to a dashed horizontal line separating the "Host" and "Driver". Below the line, a trapezoid represents the "Driver" performing a "1st Parameter: Dummy Read" and sending "2nd Parameter: Send D[7:6] display self-diagnostic status". To the right, a legend defines symbols: a triangle for "Command", a rectangle for "Parameter", an oval for "Display", a parallelogram for "Action", a rounded rectangle for "Mode", and an ellipse for "Sequential transfer".</p>																								

### 8.2.11. Enter Sleep Mode (10h)

10h		SPLIN (Enter Sleep Mode)																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	XX	0	0	0	1	0	0	0	0	10h											
Parameter		No Parameter																							
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents.  X = Don't care																								
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Sleep IN Mode																								
SW Reset	Sleep IN Mode																								
HW Reset	Sleep IN Mode																								
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SPLIN command issued.</p> <pre> graph TD     SPLIN[SPLIN (10h)] --&gt; Blank[Display whole blank screen Automatic No effect to DISP ON/OFF commands]     Blank --&gt; Drain[Drain charge from LCD panel]     Drain --&gt; StopDC[Stop DC/DC Converter]     StopDC --&gt; StopIO[Stop Internal Oscillator]     StopIO --&gt; SleepIn[Sleep In Mode]     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

### 8.2.12. Sleep Out (11h)

SLPOUT (Sleep Out)																								
11h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h											
Parameter	No Parameter																							
Description	This command turns off sleep mode.  In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  X = Don't care																							
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait <b>5msec</b> before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this <b>5msec</b> and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out -mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep IN Mode</td> </tr> <tr> <td>SW Reset</td> <td>Sleep IN Mode</td> </tr> <tr> <td>HW Reset</td> <td>Sleep IN Mode</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Sleep IN Mode	SW Reset	Sleep IN Mode	HW Reset	Sleep IN Mode				
Status	Default Value																							
Power On Sequence	Sleep IN Mode																							
SW Reset	Sleep IN Mode																							
HW Reset	Sleep IN Mode																							
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued.																							



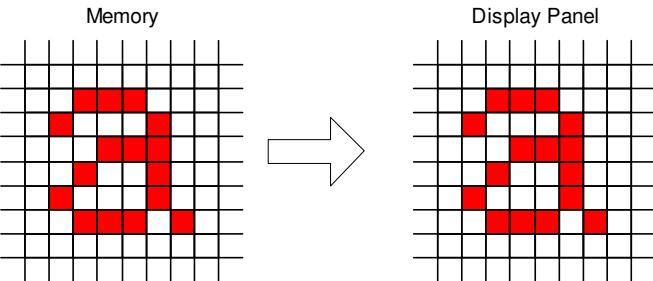
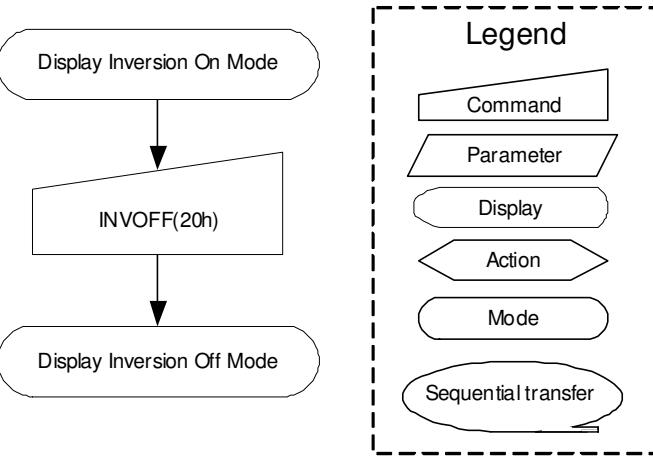
**8.2.13. Partial Mode ON (12h)**

12h	PTLON (Partial Mode On)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h											
Parameter	No Parameter																							
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. X = Don't care																							
Restriction	This command has no effect when Partial mode is active.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Normal Display Mode ON</td></tr> <tr> <td>SW Reset</td><td>Normal Display Mode ON</td></tr> <tr> <td>HW Reset</td><td>Normal Display Mode ON</td></tr> </tbody> </table>												Status	Default Value	Power On Sequence	Normal Display Mode ON	SW Reset	Normal Display Mode ON	HW Reset	Normal Display Mode ON				
Status	Default Value																							
Power On Sequence	Normal Display Mode ON																							
SW Reset	Normal Display Mode ON																							
HW Reset	Normal Display Mode ON																							
Flow Chart	See Partial Area (30h)																							

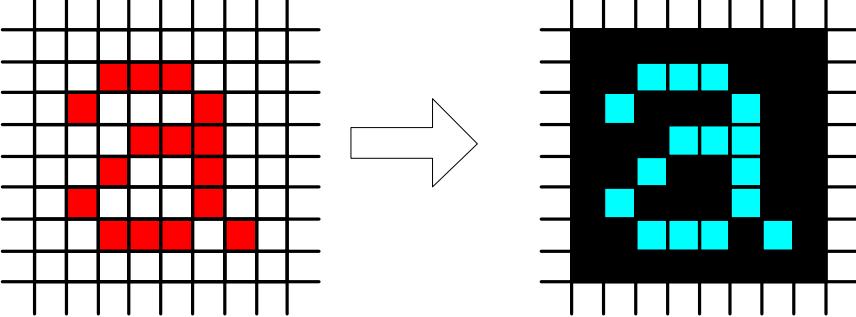
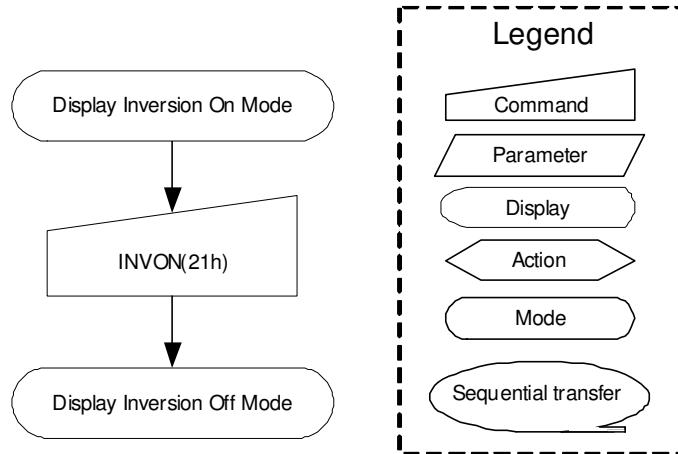
### 8.2.14. Normal Display Mode ON (13h)

NORON (Normal Display Mode On)																									
13h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13h												
Parameter	No Parameter																								
Description	This command returns the display to normal mode.  Normal display mode on means Partial mode off.  Exit from NORON by the Partial mode On command (12h)  X = Don't care																								
Restriction	This command has no effect when Normal Display mode is active.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode ON</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display Mode ON</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display Mode ON</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Normal Display Mode ON	SW Reset	Normal Display Mode ON	HW Reset	Normal Display Mode ON				
Status	Default Value																								
Power On Sequence	Normal Display Mode ON																								
SW Reset	Normal Display Mode ON																								
HW Reset	Normal Display Mode ON																								
Flow Chart	See Partial Area (30h)																								

### 8.2.15. Display Inversion OFF (20h)

DINVOFF (Display Inversion OFF)																									
20h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h												
Parameter	No Parameter																								
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status.																								
	 <p>X = Don't care</p>																								
Restriction	This command has no effect when module already is inversion OFF mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display Inversion OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display Inversion OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Inversion OFF	SW Reset	Display Inversion OFF	HW Reset	Display Inversion OFF				
Status	Default Value																								
Power On Sequence	Display Inversion OFF																								
SW Reset	Display Inversion OFF																								
HW Reset	Display Inversion OFF																								
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

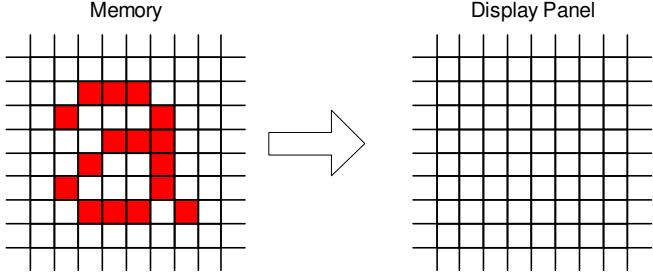
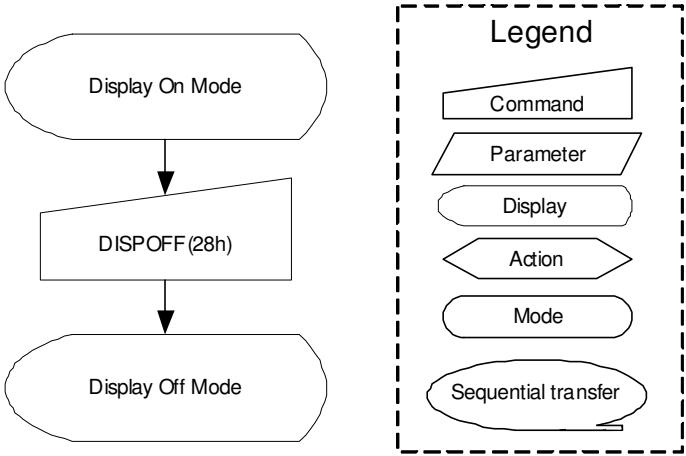
### 8.2.16. Display Inversion ON (21h)

DINVON (Display Inversion ON)																									
21h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h												
Parameter	No Parameter																								
Description	This command is used to enter into display inversion mode.  This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.  This command doesn't change any other status.  To exit Display inversion mode, the Display inversion OFF command (20h) should be written.																								
	 <p>X = Don't care</p>																								
Restriction	This command has no effect when module already is inversion ON mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display Inversion OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display Inversion OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Inversion OFF	SW Reset	Display Inversion OFF	HW Reset	Display Inversion OFF				
Status	Default Value																								
Power On Sequence	Display Inversion OFF																								
SW Reset	Display Inversion OFF																								
HW Reset	Display Inversion OFF																								
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> <pre> graph TD     A([Display Inversion On Mode]) --&gt; B[INVON(21h)]     B --&gt; C([Display Inversion Off Mode])     </pre>																								

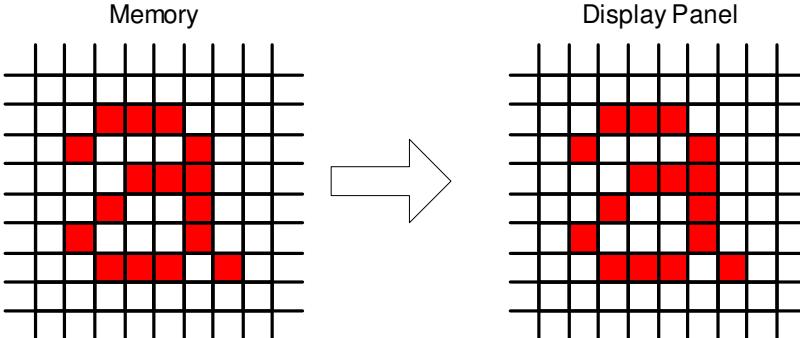
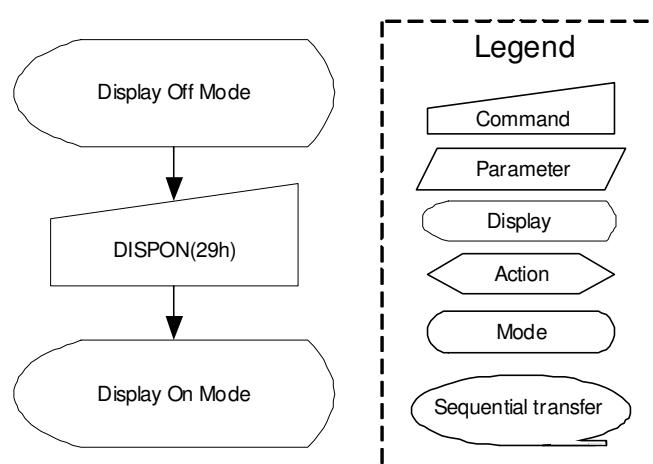
### 8.2.17. Gamma Set (26h)

26h		GAMSET (Gamma Set)																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	XX	0	0	1	0	0	1	1	0	26h											
Parameter		1	1	↑	XX	GC [7:0]							01												
Description	This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table: <table border="1" style="margin-left: 20px;"> <tr> <th>GC [7:0]</th> <th>Curve Selected</th> </tr> <tr> <td>01h</td> <td>Gamma curve 1 (G2.2)</td> </tr> <tr> <td>02h</td> <td>---</td> </tr> <tr> <td>04h</td> <td>---</td> </tr> <tr> <td>08h</td> <td>---</td> </tr> </table> Note: All other values are undefined. X = Don't care													GC [7:0]	Curve Selected	01h	Gamma curve 1 (G2.2)	02h	---	04h	---	08h	---		
GC [7:0]	Curve Selected																								
01h	Gamma curve 1 (G2.2)																								
02h	---																								
04h	---																								
08h	---																								
Restriction	Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.																								
Register Availability	<table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h01h</td> </tr> <tr> <td>SW Reset</td> <td>8'h01h</td> </tr> <tr> <td>HW Reset</td> <td>8'h01h</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	8'h01h	SW Reset	8'h01h	HW Reset	8'h01h				
Status	Default Value																								
Power On Sequence	8'h01h																								
SW Reset	8'h01h																								
HW Reset	8'h01h																								
Flow Chart	<pre> graph TD     A[GAMSET (26h)] --&gt; B{1st Parameter: GC[7:0]}     B --&gt; C{New Gamma Curve Loaded}     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

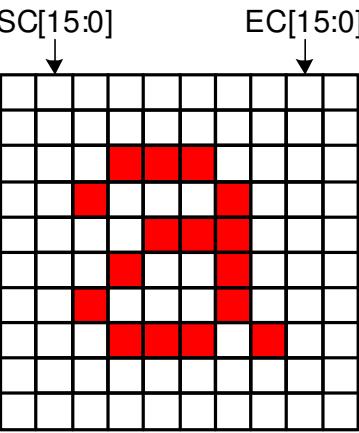
### 8.2.18. Display OFF (28h)

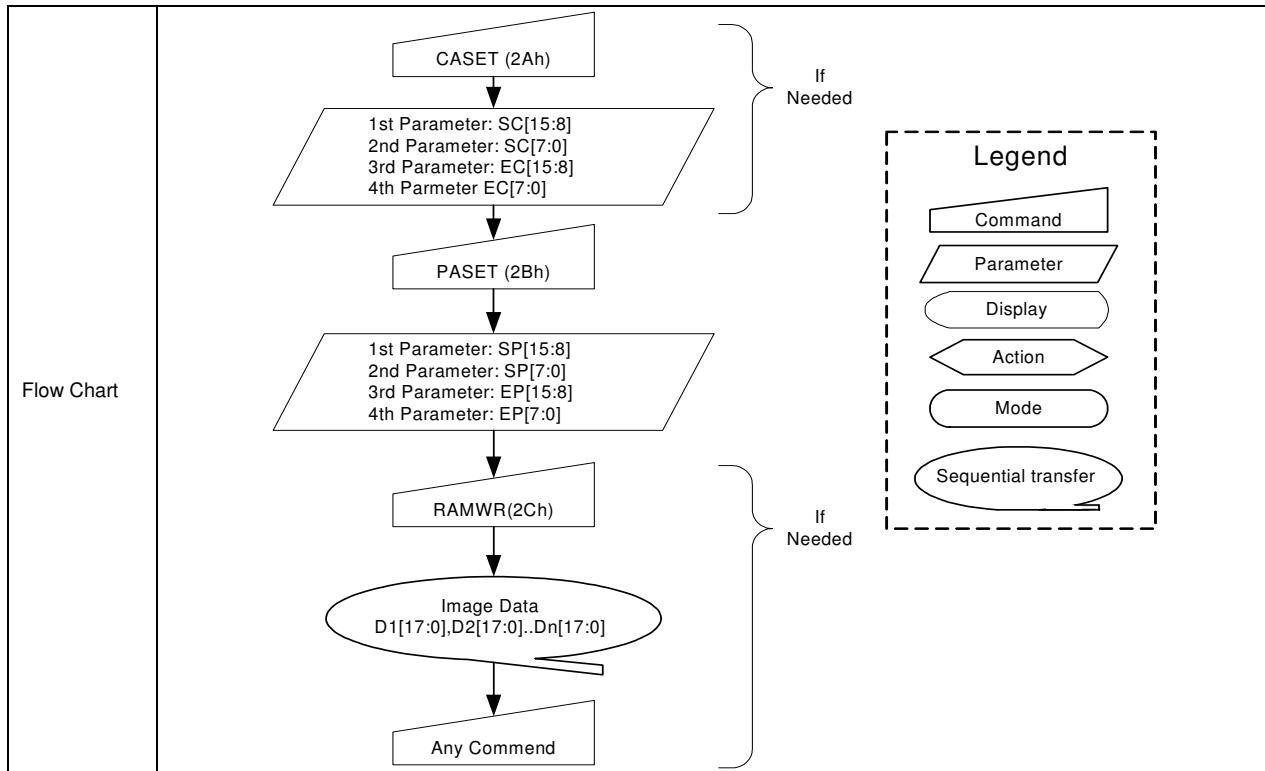
DISPOFF (Display OFF)																									
28h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h												
Parameter	No Parameter																								
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p>  <p>X = Don't care.</p>																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display OFF	SW Reset	Display OFF	HW Reset	Display OFF				
Status	Default Value																								
Power On Sequence	Display OFF																								
SW Reset	Display OFF																								
HW Reset	Display OFF																								
Flow Chart	 <pre> graph TD     A([Display On Mode]) --&gt; B[DISPOFF (28h)]     B --&gt; C([Display Off Mode])     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

### 8.2.19. Display ON (29h)

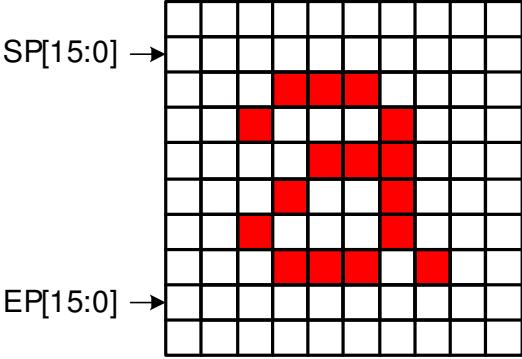
DISPON (Display ON)																									
29h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h												
Parameter	No Parameter																								
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status																								
	 <p>X = Don't care.</p>																								
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display OFF	SW Reset	Display OFF	HW Reset	Display OFF				
Status	Default Value																								
Power On Sequence	Display OFF																								
SW Reset	Display OFF																								
HW Reset	Display OFF																								
Flow Chart	 <p><b>Legend</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

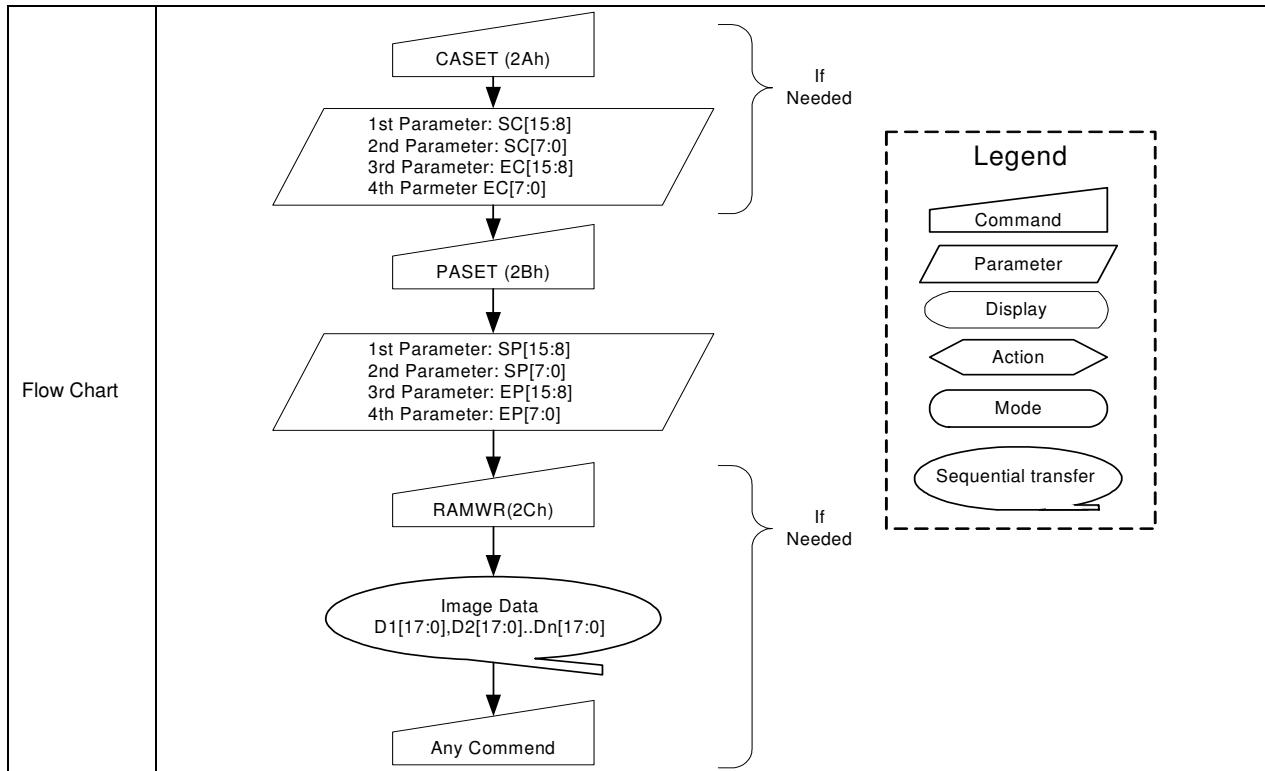
### 8.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah												
1 <sup>st</sup> Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1												
2 <sup>nd</sup> Parameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0													
3 <sup>rd</sup> Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1												
4 <sup>th</sup> Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0													
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.  X = Don't care																								
Restriction	SC [15:0] always must be equal to or less than EC [15:0]. Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SC [15:0]=0000h</td> <td>EC [15:0]=00EFh</td> </tr> <tr> <td>SW Reset</td> <td>SC [15:0]=0000h</td> <td>If MADCTL's B5 = 0: EC [15:0]=00EFh If MADCTL's B5 = 1: EC [15:0]=013Fh</td> </tr> <tr> <td>HW Reset</td> <td>SC [15:0]=0000h</td> <td>EC [15:0]=00EFh</td> </tr> </tbody> </table>													Status	Default Value		Power On Sequence	SC [15:0]=0000h	EC [15:0]=00EFh	SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=00EFh If MADCTL's B5 = 1: EC [15:0]=013Fh	HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh
Status	Default Value																								
Power On Sequence	SC [15:0]=0000h	EC [15:0]=00EFh																							
SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=00EFh If MADCTL's B5 = 1: EC [15:0]=013Fh																							
HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh																							



### 8.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh												
1 <sup>st</sup> Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1												
2 <sup>nd</sup> Parameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0													
3 <sup>rd</sup> Parameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1												
4 <sup>th</sup> Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0													
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.   → SP[15:0] → EP[15:0] X = Don't care																								
Restriction	SP [15:0] always must be equal to or less than EP [15:0] Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 = 1), data of out of range will be ignored.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SP [15:0]=0000h</td> <td>EP [15:0]=013Fh</td> </tr> <tr> <td>SW Reset</td> <td>SP [15:0]=0000h</td> <td>If MADCTL's B5 = 0: EP [15:0]=013Fh If MADCTL's B5 = 1: EP [15:0]=00EFh</td> </tr> <tr> <td>HW Reset</td> <td>SP [15:0]=0000h</td> <td>EP [15:0]=013Fh</td> </tr> </tbody> </table>													Status	Default Value		Power On Sequence	SP [15:0]=0000h	EP [15:0]=013Fh	SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=013Fh If MADCTL's B5 = 1: EP [15:0]=00EFh	HW Reset	SP [15:0]=0000h	EP [15:0]=013Fh
Status	Default Value																								
Power On Sequence	SP [15:0]=0000h	EP [15:0]=013Fh																							
SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=013Fh If MADCTL's B5 = 1: EP [15:0]=00EFh																							
HW Reset	SP [15:0]=0000h	EP [15:0]=013Fh																							



### 8.2.22. Memory Write (2Ch)

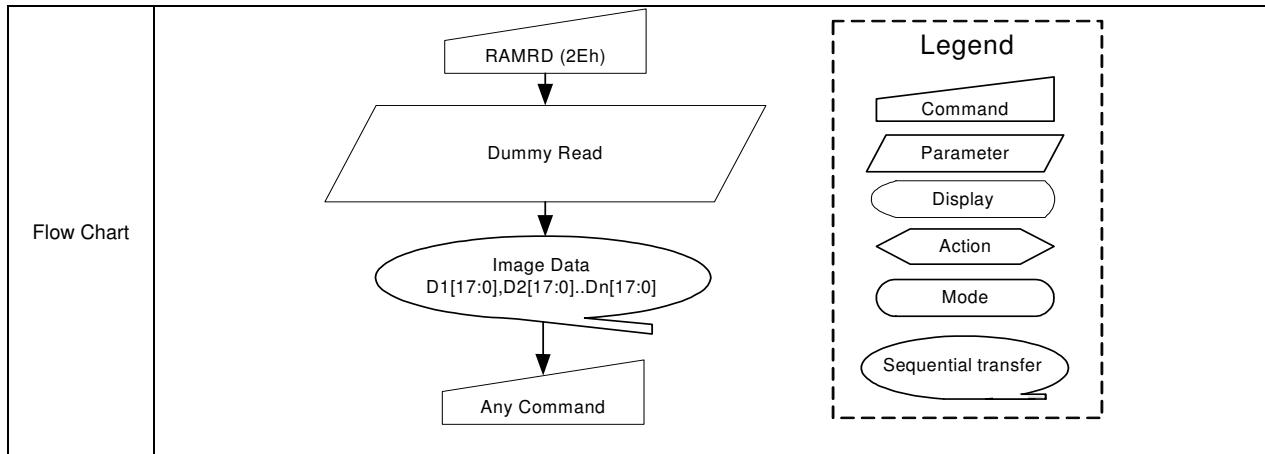
2Ch	RAMWR (Memory Write)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch											
1 <sup>st</sup> Parameter	1	1	↑						D1 [17:0]				XX											
:	1	1	↑						Dx [17:0]				XX											
N <sup>th</sup> Parameter	1	1	↑						Dn [17:0]				XX											
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.																							
Restriction	In all color modes, there is no restriction on length of parameters.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>SW Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>HW Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared				
Status	Default Value																							
Power On Sequence	Contents of memory is set randomly																							
SW Reset	Contents of memory is not cleared																							
HW Reset	Contents of memory is not cleared																							
Flow Chart	<pre> graph TD     CASET[CASET (2Ah)] --&gt; PASET[PASET (2Bh)]     PASET --&gt; RAMWR[RAMWR(2Ch)]     RAMWR --&gt; ImageData([Image Data D1[17:0], D2[17:0]..Dn[17:0]])     ImageData --&gt; AnyCommand[Any Command]     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																							

### 8.2.23. Color Set (2Dh)

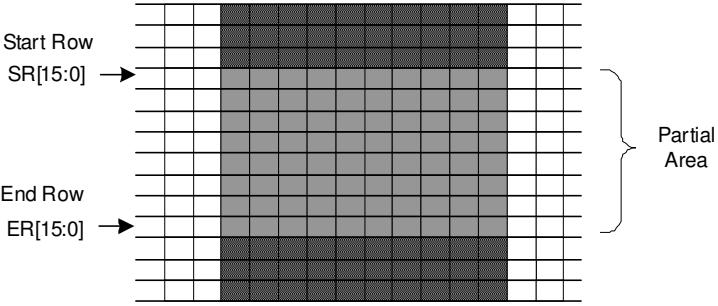
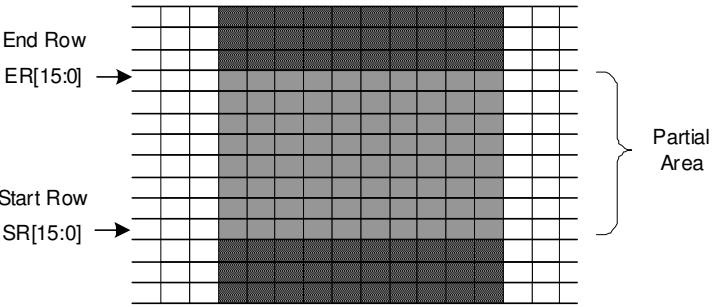
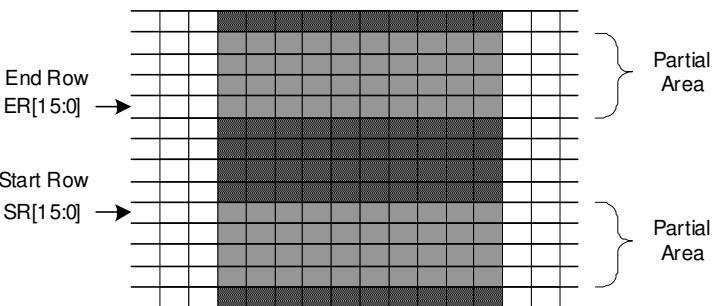
2Dh		RGBSET (Color Set)																								
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑		XX	0	0	1	0	1	1	0	1	2Dh												
1 <sup>st</sup> Parameter	1	1	↑		XX	0	0			R00 [5:0]				XX												
n <sup>th</sup> Parameter	1	1	↑		XX	0	0			Rnn [5:0]				XX												
32 <sup>nd</sup> Parameter	1	1	↑		XX	0	0			R31 [5:0]				XX												
33 <sup>rd</sup> Parameter	1	1	↑		XX	0	0			G00 [5:0]				XX												
n <sup>th</sup> Parameter	1	1	↑		XX	0	0			Gnn [5:0]				XX												
96 <sup>th</sup> Parameter	1	1	↑		XX	0	0			G64 [5:0]				XX												
97 <sup>th</sup> Parameter	1	1	↑		XX	0	0			B00 [5:0]				XX												
n <sup>th</sup> Parameter	1	1	↑		XX	0	0			Bnn [5:0]				XX												
128 <sup>th</sup> Parameter	1	1	↑		XX	0	0			B31 [5:0]				XX												
Description	This command is used to define the LUT for 16-bit to 18-bit color depth conversion.  128 bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.4 are referred.  This command has no effect on other commands, parameter and contents of frame memory. Visible change takes effect next time the frame memory is written to.																									
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Random values</td> </tr> <tr> <td>SW Reset</td> <td>Contents of LUT protected</td> </tr> <tr> <td>HW Reset</td> <td>Random values</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Random values	SW Reset	Contents of LUT protected	HW Reset	Random values					
Status	Default Value																									
Power On Sequence	Random values																									
SW Reset	Contents of LUT protected																									
HW Reset	Random values																									
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																									

### 8.2.24. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh											
1 <sup>st</sup> Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	X											
2 <sup>nd</sup> Parameter	1	1	↑					D1 [17:0]					XX											
:	1	1	↑					Dx [17:0]					XX											
(N+1) <sup>th</sup> Parameter	1	1	↑					Dn [17:0]					XX											
Description	This command transfers image data from ILI9341's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.  <b>If Memory Access control B5 = 0:</b> The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.  <b>If Memory Access Control B5 = 1:</b> The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.																							
Restriction	There is no restriction on length of parameters.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr> <tr> <td>SW Reset</td><td>Contents of memory is set randomly</td></tr> <tr> <td>HW Reset</td><td>Contents of memory is set randomly</td></tr> </tbody> </table>												Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is set randomly	HW Reset	Contents of memory is set randomly				
Status	Default Value																							
Power On Sequence	Contents of memory is set randomly																							
SW Reset	Contents of memory is set randomly																							
HW Reset	Contents of memory is set randomly																							

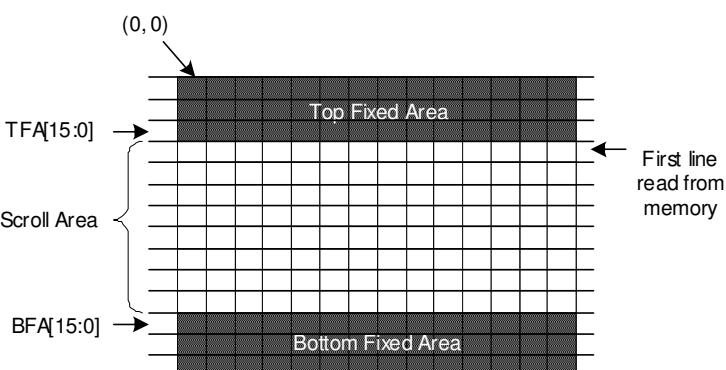


### 8.2.25. Partial Area (30h)

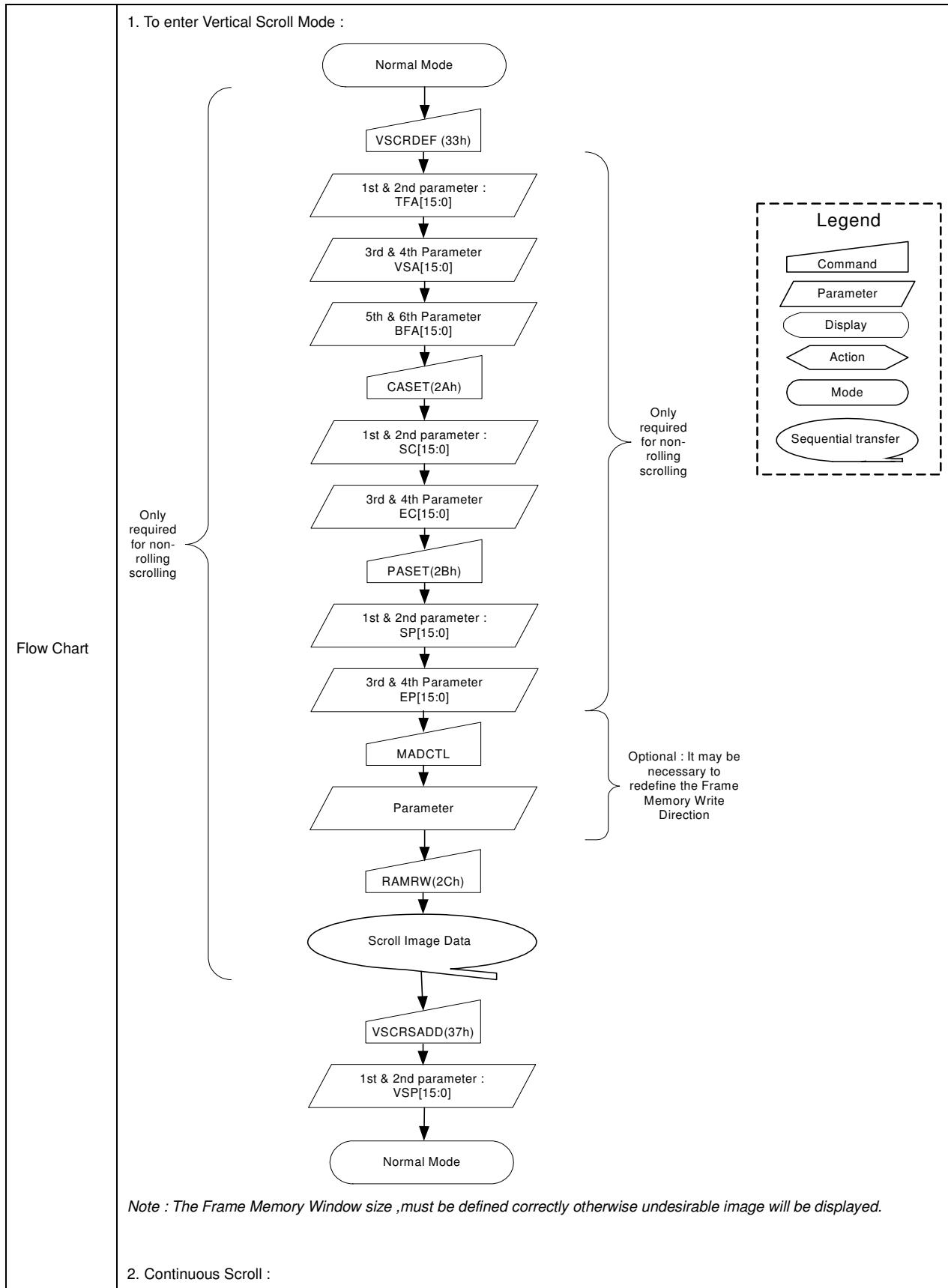
30h	PLTAR (Partial Area)													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h	
1 <sup>st</sup> Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00	
2 <sup>nd</sup> Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00	
3 <sup>rd</sup> Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01	
4 <sup>th</sup> Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	3F	
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.  If End Row>Start Row when MADCTL B4=0:-    If End Row>Start Row when MADCTL B4=1:-    If End Row<Start Row when MADCTL B4=0:-    If End Row = Start Row then the Partial Area will be one row deep.  X = Don't care.													
Restriction	SR [15...0] and ER [15...0] cannot be 0000h nor exceed 013Fh.													

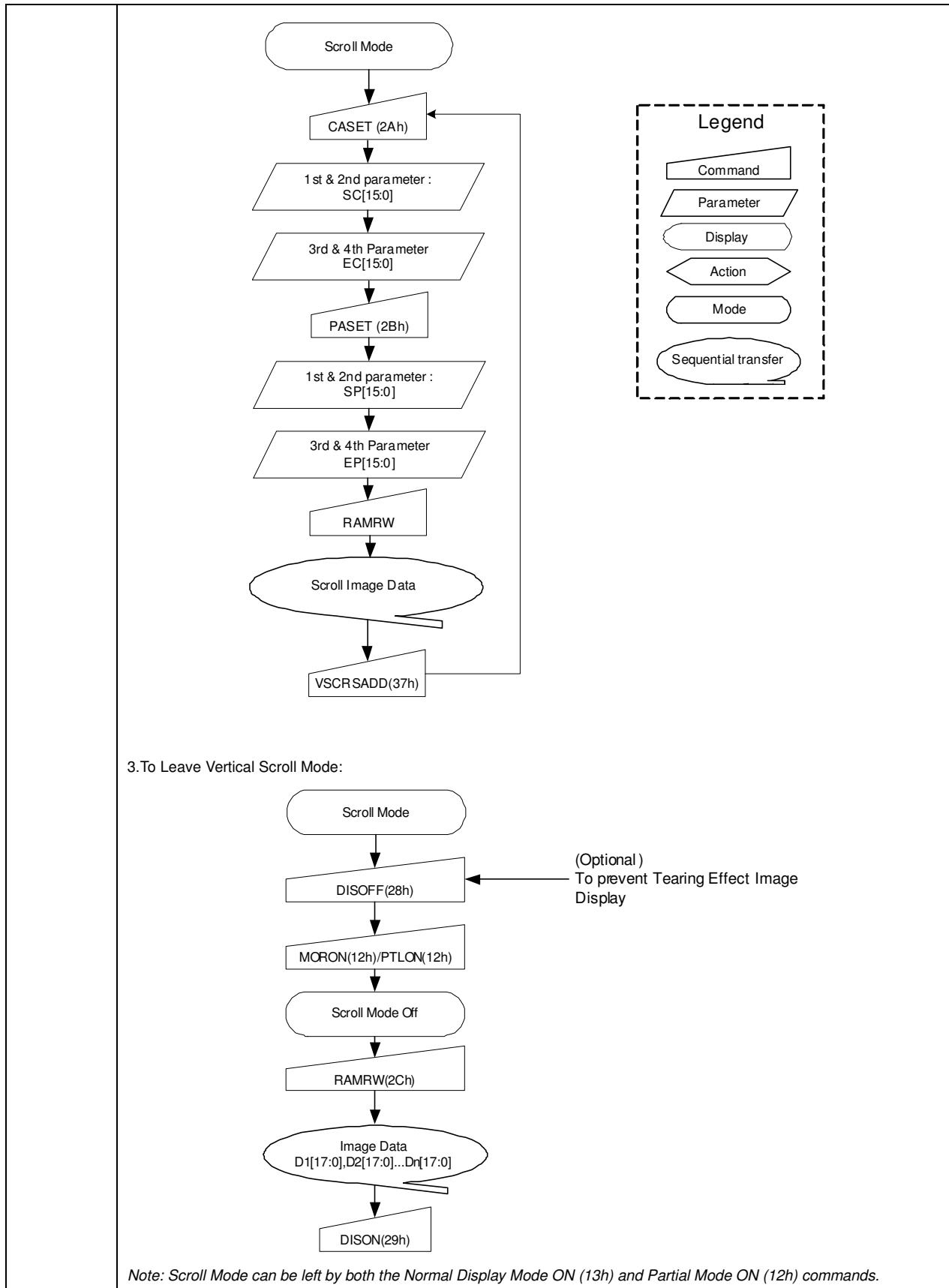
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: #cccccc;">Status</th><th style="text-align: center; background-color: #cccccc;">Availability</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td style="text-align: center;">Sleep In</td><td style="text-align: center;">Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2" style="text-align: center; background-color: #cccccc;">Status</th><th colspan="2" style="text-align: center; background-color: #cccccc;">Default Value</th></tr> <tr> <th style="text-align: center;">SR [15:0]</th><th style="text-align: center;">ER [15:0]</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td><td style="text-align: center;">16'h0000h</td><td style="text-align: center;">16'h013Fh</td></tr> <tr> <td style="text-align: center;">SW Reset</td><td style="text-align: center;">16'h 0000h</td><td style="text-align: center;">16'h 013Fh</td></tr> <tr> <td style="text-align: center;">HW Reset</td><td style="text-align: center;">16'h 0000h</td><td style="text-align: center;">16'h 013Fh</td></tr> </tbody> </table>	Status	Default Value		SR [15:0]	ER [15:0]	Power On Sequence	16'h0000h	16'h013Fh	SW Reset	16'h 0000h	16'h 013Fh	HW Reset	16'h 0000h	16'h 013Fh
Status	Default Value														
	SR [15:0]	ER [15:0]													
Power On Sequence	16'h0000h	16'h013Fh													
SW Reset	16'h 0000h	16'h 013Fh													
HW Reset	16'h 0000h	16'h 013Fh													
Flow Chart	<p>1. To Enter Partial Mode</p> <pre> graph TD     PLTAR[PLTAR(30h)] --&gt; P1[1st Parameter: SR[15:8] 2nd Parameter: SR[7:0]]     P1 --&gt; P2[3rd Parameter: ER[15:8] 4th Parameter: ER[7:0]]     P2 --&gt; PTION[PTION(12h)]     PTION --&gt; PM[Partial Mode]   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> <p>2. To Leave Partial Mode</p> <pre> graph TD     PM[Partial Mode] --&gt; PMOFF[Partial Mode OFF]     PMOFF --&gt; DISPOFF[DISPOFF(28h)]     DISPOFF --&gt; NORON[NORON(13h)]     NORON --&gt; RAMRW[RAMRW(2Ch)]     RAMRW --&gt; ID[Image Data D1[17:0], D2[17:0]..Dn[17:0]]     ID --&gt; DISPON[DISPON(29h)]   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>														

### 8.2.26. Vertical Scrolling Definition (33h)

VSCRDEF (Vertical Scrolling Definition)													
33h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1 <sup>st</sup> Parameter	1	↑	1	XX					TFA [15:8]				00
2 <sup>nd</sup> Parameter	1	↑	1	XX					TFA [7:0]				00
3 <sup>rd</sup> Parameter	1	↑	1	XX					VSA [15:8]				01
4 <sup>th</sup> Parameter	1	↑	1	XX					VSA [7:0]				40
5 <sup>th</sup> Parameter	1	↑	1	XX					BFA [15:8]				00
6 <sup>th</sup> Parameter	1	↑	1	XX					BFA [7:0]				00
Description	This command defines the Vertical Scrolling Area of the display.  When MADCTL B4=0  The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).  The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.  The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.												
													
	When MADCTL B4=1  The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).  The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.  The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).												

	<p>The diagram illustrates the LCD panel structure. It features a central 'Scroll Area' flanked by 'Bottom Fixed Area' at the top and 'Top Fixed Area' at the bottom. The top fixed area is labeled with 'BFA[15:0]' and the bottom fixed area with 'TFA[15:0]'. A coordinate point '(0, 0)' is marked at the top-left corner of the scroll area. An arrow points from the text 'First line read from memory' to the left edge of the scroll area.</p> <p>X = Don't care</p>																			
Restriction																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
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Normal Mode On, Idle Mode On, Sleep Out	Yes																			
Partial Mode On, Idle Mode Off, Sleep Out	Yes																			
Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																			
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>TFA [15:0]</th><th>VSA [15:0]</th><th>BFA [15:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>16'h0000h</td><td>16'h0140h</td><td>16'h0000h</td></tr> <tr> <td>SW Reset</td><td>16'h0000h</td><td>16'h0140h</td><td>16'h0000h</td></tr> <tr> <td>HW Reset</td><td>16'h0000h</td><td>16'h0140h</td><td>16'h0000h</td></tr> </tbody> </table>	Status	Default Value			TFA [15:0]	VSA [15:0]	BFA [15:0]	Power On Sequence	16'h0000h	16'h0140h	16'h0000h	SW Reset	16'h0000h	16'h0140h	16'h0000h	HW Reset	16'h0000h	16'h0140h	16'h0000h
Status	Default Value																			
	TFA [15:0]	VSA [15:0]	BFA [15:0]																	
Power On Sequence	16'h0000h	16'h0140h	16'h0000h																	
SW Reset	16'h0000h	16'h0140h	16'h0000h																	
HW Reset	16'h0000h	16'h0140h	16'h0000h																	

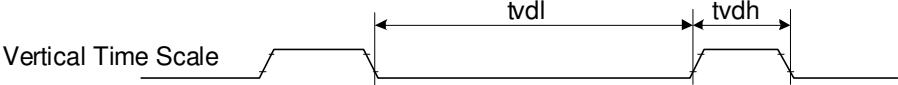
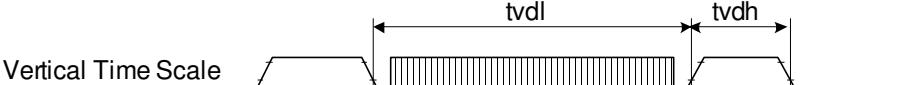


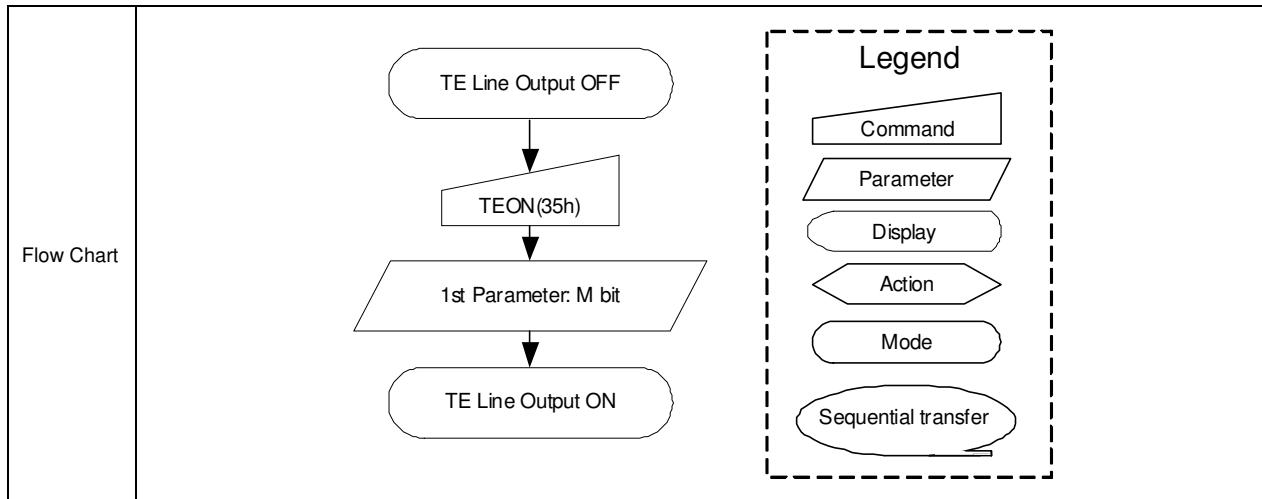


### 8.2.27. Tearing Effect Line OFF (34h)

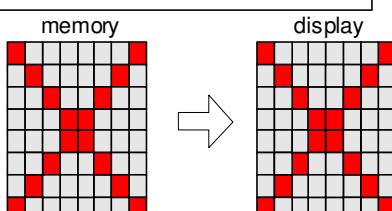
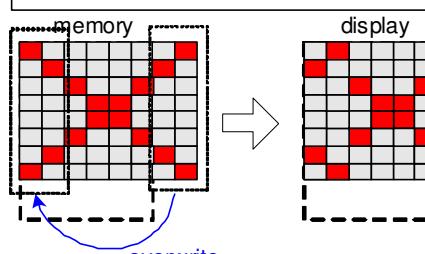
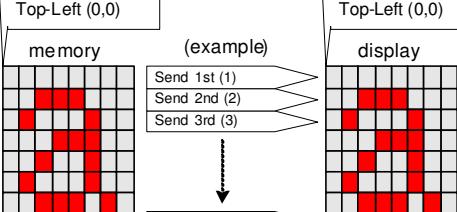
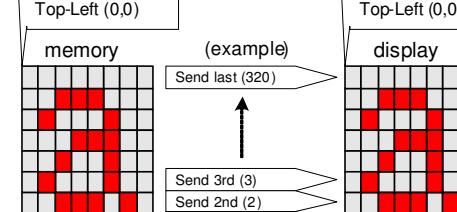
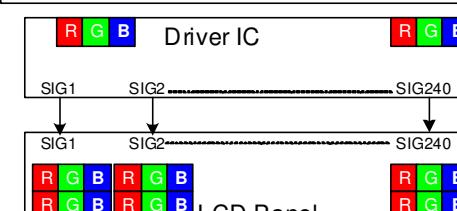
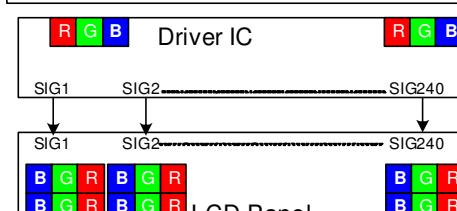
TEOFF (Tearing Effect Line OFF)																									
34h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h												
Parameter	No Parameter																								
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. X = Don't care.																								
Restriction	This command has no effect when Tearing Effect output is already OFF.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	OFF																								
SW Reset	OFF																								
HW Reset	OFF																								
Flow Chart	<pre> graph TD     A([TE Line Output ON]) --&gt; B[TEOFF(34h)]     B --&gt; C([TE Line Output OFF])     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

### 8.2.28. Tearing Effect Line ON (35h)

TEON (Tearing Effect Line ON)																									
35h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h												
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	M	00												
Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.  When <b>M=0</b> : The Tearing Effect Output line consists of V-Blanking information only:  When <b>M=1</b> : The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low. X = Don't care.																								
Restriction	This command has no effect when Tearing Effect output is already ON																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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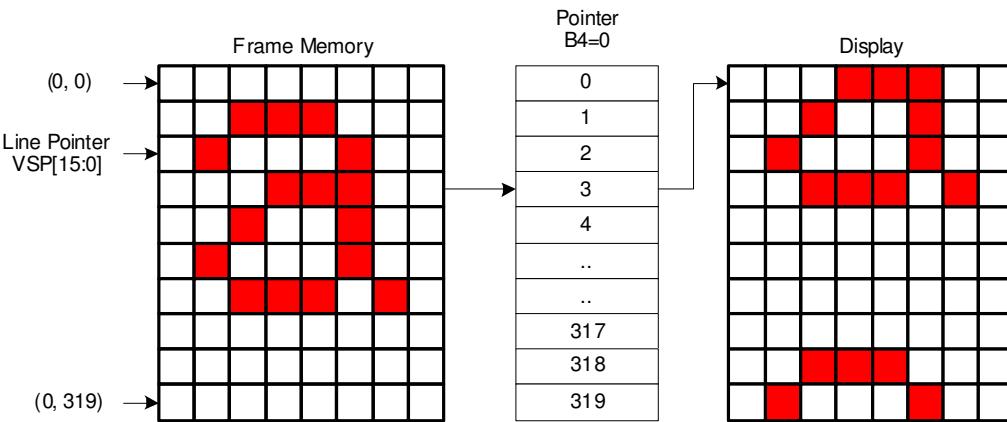
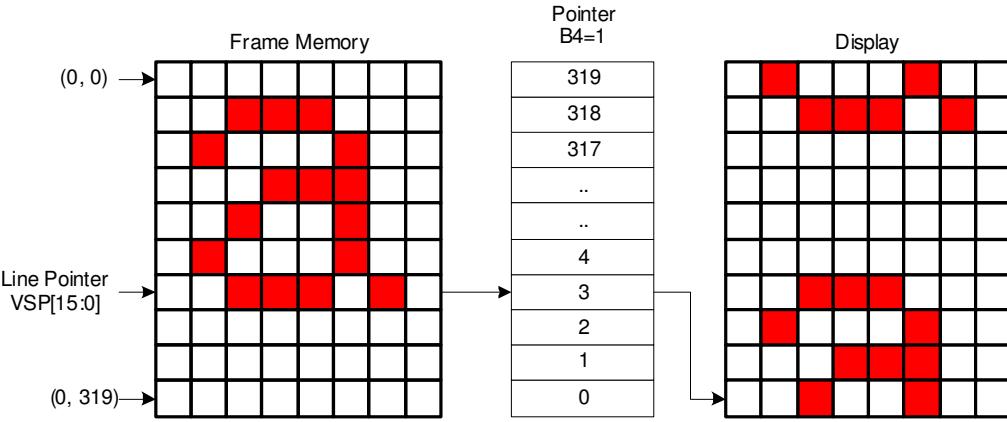


### 8.2.29. Memory Access Control (36h)

MADCTL (Memory Access Control)																																		
36h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h																					
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00																					
This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.																																		
<table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>MY</td> <td>Row Address Order</td> <td>These 3 bits control MCU to memory write/read direction.</td> </tr> <tr> <td>MX</td> <td>Column Address Order</td> <td>LCD vertical refresh direction control.</td> </tr> <tr> <td>MV</td> <td>Row / Column Exchange</td> <td>Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)</td> </tr> <tr> <td>ML</td> <td>Vertical Refresh Order</td> <td>LCD horizontal refreshing direction control.</td> </tr> <tr> <td>BGR</td> <td>RGB-BGR Order</td> <td></td> </tr> <tr> <td>MH</td> <td>Horizontal Refresh ORDER</td> <td></td> </tr> </tbody> </table> <p>Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.</p> <p>X = Don't care.</p>														Bit	Name	Description	MY	Row Address Order	These 3 bits control MCU to memory write/read direction.	MX	Column Address Order	LCD vertical refresh direction control.	MV	Row / Column Exchange	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)	ML	Vertical Refresh Order	LCD horizontal refreshing direction control.	BGR	RGB-BGR Order		MH	Horizontal Refresh ORDER	
Bit	Name	Description																																
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MX	Column Address Order	LCD vertical refresh direction control.																																
MV	Row / Column Exchange	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)																																
ML	Vertical Refresh Order	LCD horizontal refreshing direction control.																																
BGR	RGB-BGR Order																																	
MH	Horizontal Refresh ORDER																																	
Description	<b>MV(Vertical refresh order bit)="0"</b> 							<b>MV(Vertical refresh order bit)="1"</b> 																										
	<b>ML(Vertical refresh order bit)="0"</b> 							<b>ML(Vertical refresh order bit)="1"</b> 																										
	<b>BGR(RGB-BGR Order control bit)="0"</b> 							<b>BGR(RGB-BGR Order control bit)="1"</b> 																										

	MH(Horizontal refresh order control bit)="0"	MH(Horizontal refresh order control bit)="1"												
Note: Top-Left (0,0) means a physical memory location.														
Restriction														
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Status</th><th style="text-align: center; padding: 2px;">Availability</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center; padding: 2px;">Yes</td></tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center; padding: 2px;">Yes</td></tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center; padding: 2px;">Yes</td></tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center; padding: 2px;">Yes</td></tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td><td style="text-align: center; padding: 2px;">Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	8'h00h													
SW Reset	No change													
HW Reset	8'h00h													
Flow Chart	<p><b>Legend</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>													

### 8.2.30. Vertical Scrolling Start Address (37h)

37h		VSCRSADD (Vertical Scrolling Start Address)												
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command		0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1 <sup>st</sup> Parameter		1	↑	1	XX					VSP [15:8]				00
2 <sup>nd</sup> Parameter		1	↑	1	XX					VSP [7:0]				00
Description	This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-  When MADCTL B4=0  Example:  When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.    When MADCTL B4=1  Example:  When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.  													

Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9341 enters Partial mode.

X = Don't care

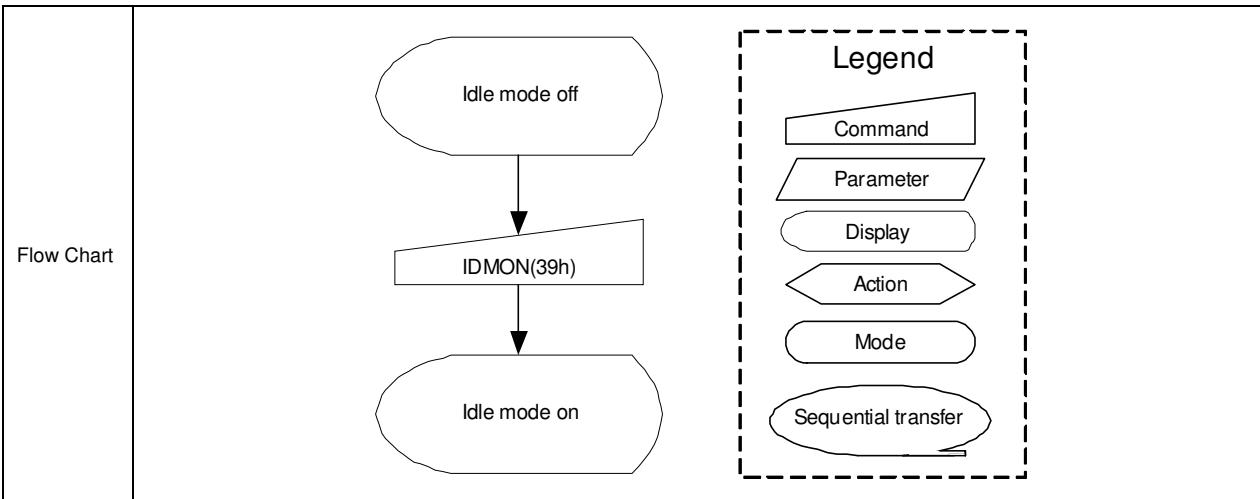
Restriction														
Register Availability		<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	No													
Partial Mode On, Idle Mode On, Sleep Out	No													
Sleep In	Yes													
Default		<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>VSP [15:0]</td><td></td></tr> <tr> <td>Power On Sequence</td><td>16'h0000h</td></tr> <tr> <td>SW Reset</td><td>16'h0000h</td></tr> <tr> <td>HW Reset</td><td>16'h0000h</td></tr> </tbody> </table>	Status	Default Value	VSP [15:0]		Power On Sequence	16'h0000h	SW Reset	16'h0000h	HW Reset	16'h0000h		
Status	Default Value													
	VSP [15:0]													
Power On Sequence	16'h0000h													
SW Reset	16'h0000h													
HW Reset	16'h0000h													
Flow Chart	See Vertical Scrolling Definition (33h) description.													

### 8.2.31. Idle Mode OFF (38h)

IDMOFF (Idle Mode OFF)																									
38h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h												
Parameter	No Parameter																								
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors. X = Don't care.																								
Restriction	This command has no effect when module is already in idle off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Idle mode OFF																								
SW Reset	Idle mode OFF																								
HW Reset	Idle mode OFF																								
Flow Chart	<pre> graph TD     A([Idle mode on]) --&gt; B[IDMOFF(38h)]     B --&gt; C([Idle mode off])     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

### 8.2.32. Idle Mode ON (39h)

39h		IDMON (Idle Mode ON)																																																
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command		0	1	↑	XX	0	0	1	1	1	0	0	1	39h																																				
Parameter	No Parameter																																																	
Description	<p>This command is used to enter into Idle mode on.</p> <p>In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.</p> <table border="1"> <caption>Memory Contents vs. Display Color</caption> <thead> <tr> <th></th> <th>R<sub>5</sub> R<sub>4</sub> R<sub>3</sub> R<sub>2</sub> R<sub>1</sub> R<sub>0</sub></th> <th>G<sub>5</sub> G<sub>4</sub> G<sub>3</sub> G<sub>2</sub> G<sub>1</sub> G<sub>0</sub></th> <th>B<sub>5</sub> B<sub>4</sub> B<sub>3</sub> B<sub>2</sub> B<sub>1</sub> B<sub>0</sub></th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> </tbody> </table> <p>X = Don't care.</p>															R <sub>5</sub> R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub>	G <sub>5</sub> G <sub>4</sub> G <sub>3</sub> G <sub>2</sub> G <sub>1</sub> G <sub>0</sub>	B <sub>5</sub> B <sub>4</sub> B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX
	R <sub>5</sub> R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub>	G <sub>5</sub> G <sub>4</sub> G <sub>3</sub> G <sub>2</sub> G <sub>1</sub> G <sub>0</sub>	B <sub>5</sub> B <sub>4</sub> B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>																																															
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Blue	0XXXXX	0XXXXX	1XXXXX																																															
Red	1XXXXX	0XXXXX	0XXXXX																																															
Magenta	1XXXXX	0XXXXX	1XXXXX																																															
Green	0XXXXX	1XXXXX	0XXXXX																																															
Cyan	0XXXXX	1XXXXX	1XXXXX																																															
Yellow	1XXXXX	1XXXXX	0XXXXX																																															
White	1XXXXX	1XXXXX	1XXXXX																																															
Restriction	This command has no effect when module is already in idle off mode.																																																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
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Status	Default Value																																																	
Power On Sequence	Idle mode OFF																																																	
SW Reset	Idle mode OFF																																																	
HW Reset	Idle mode OFF																																																	



### 8.2.33. COLMOD: Pixel Format Set (3Ah)

PIXSET (Pixel Format Set)																																																	
3Ah	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah																																				
Parameter	1	1	↑	XX	0	DPI [2:0]			0	DBI [2:0]			66																																				
Description	This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.																																																
	<table border="1"> <thead> <tr> <th>DPI [2:0]</th> <th>RGB Interface Format</th> <th>DBI [2:0]</th> <th>MCU Interface Format</th> </tr> </thead> <tbody> <tr> <td>0 0 0</td> <td>Reserved</td> <td>0 0 0</td> <td>Reserved</td> </tr> <tr> <td>0 0 1</td> <td>Reserved</td> <td>0 0 1</td> <td>Reserved</td> </tr> <tr> <td>0 1 0</td> <td>Reserved</td> <td>0 1 0</td> <td>Reserved</td> </tr> <tr> <td>0 1 1</td> <td>Reserved</td> <td>0 1 1</td> <td>Reserved</td> </tr> <tr> <td>1 0 0</td> <td>Reserved</td> <td>1 0 0</td> <td>Reserved</td> </tr> <tr> <td>1 0 1</td> <td>16 bits / pixel</td> <td>1 0 1</td> <td>16 bits / pixel</td> </tr> <tr> <td>1 1 0</td> <td>18 bits / pixel</td> <td>1 1 0</td> <td>18 bits / pixel</td> </tr> <tr> <td>1 1 1</td> <td>Reserved</td> <td>1 1 1</td> <td>Reserved</td> </tr> </tbody> </table> If using RGB Interface must selection serial interface. X = Don't care													DPI [2:0]	RGB Interface Format	DBI [2:0]	MCU Interface Format	0 0 0	Reserved	0 0 0	Reserved	0 0 1	Reserved	0 0 1	Reserved	0 1 0	Reserved	0 1 0	Reserved	0 1 1	Reserved	0 1 1	Reserved	1 0 0	Reserved	1 0 0	Reserved	1 0 1	16 bits / pixel	1 0 1	16 bits / pixel	1 1 0	18 bits / pixel	1 1 0	18 bits / pixel	1 1 1	Reserved	1 1 1	Reserved
DPI [2:0]	RGB Interface Format	DBI [2:0]	MCU Interface Format																																														
0 0 0	Reserved	0 0 0	Reserved																																														
0 0 1	Reserved	0 0 1	Reserved																																														
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0 1 1	Reserved	0 1 1	Reserved																																														
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1 0 1	16 bits / pixel	1 0 1	16 bits / pixel																																														
1 1 0	18 bits / pixel	1 1 0	18 bits / pixel																																														
1 1 1	Reserved	1 1 1	Reserved																																														
Restriction																																																	
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Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>DPI [2:0]</th> <th>DBI [2:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3'b110</td> <td>3'b110</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> <td>No Change</td> </tr> <tr> <td>HW Reset</td> <td>3'b110</td> <td>3'b110</td> </tr> </tbody> </table>													Status	Default Value		DPI [2:0]	DBI [2:0]	Power On Sequence	3'b110	3'b110	SW Reset	No Change	No Change	HW Reset	3'b110	3'b110																						
Status	Default Value																																																
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Power On Sequence	3'b110	3'b110																																															
SW Reset	No Change	No Change																																															
HW Reset	3'b110	3'b110																																															
Flow Chart	<p>The flowchart illustrates the sequence of commands. It begins with a rectangle labeled "COLMOD (3Ah)". An arrow points down to a trapezoid labeled "DPI[2:0] RGB pixel format DBI[2:0] MCU pixel format". Another arrow points down to a rectangle labeled "Any Command". To the right of the flowchart is a legend enclosed in a dashed box, defining six symbols: Command (triangle), Parameter (rectangle), Display (oval), Action (diamond), Mode (trapezoid), and Sequential transfer (elliptical arrow).</p>																																																

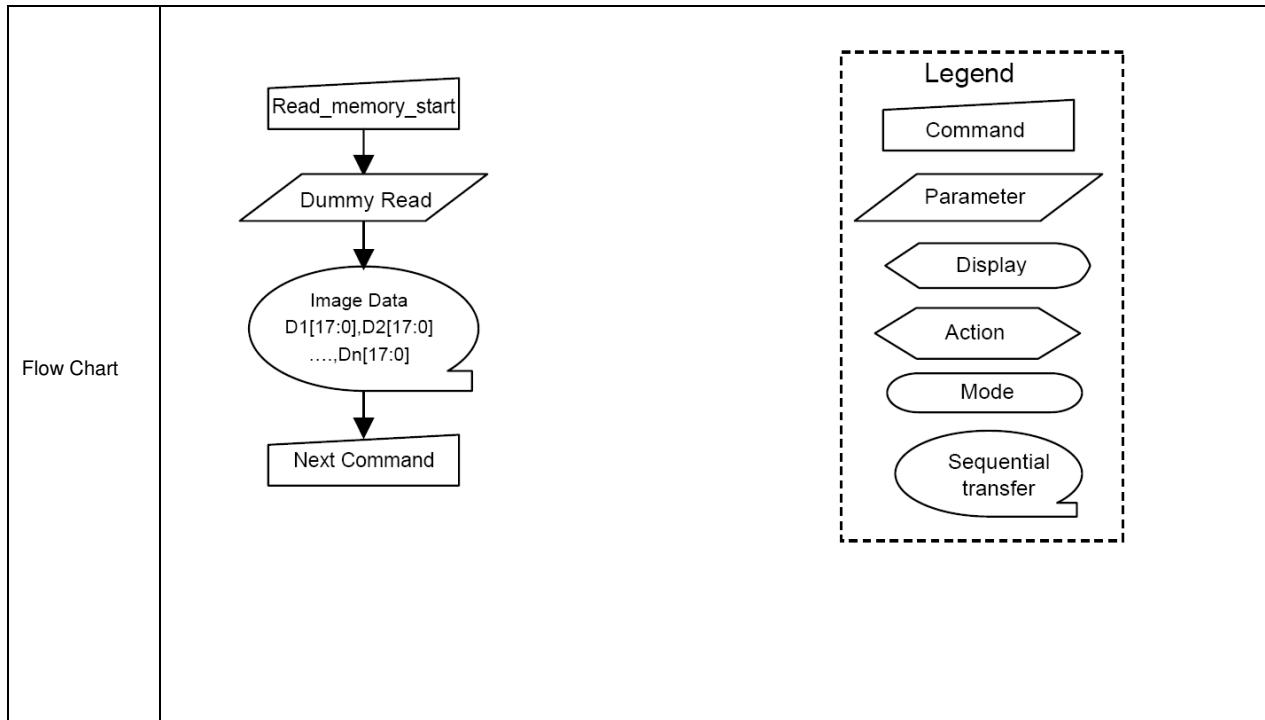
### 8.2.34. Write\_Memory\_Continue (3Ch)

Write_Memory_Continue													
3Ch	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
1 <sup>st</sup> Parameter	1	1	↑	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
X <sup>th</sup> Parameter	1	1	↑	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
N <sup>th</sup> Parameter	1	1	↑	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.  <b>If set_address_mode B5 = 0:</b> Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.  <b>If set_address_mode B5 = 1:</b> Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.  Sending any other command can stop frame Write.  Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.  Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.												
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.												

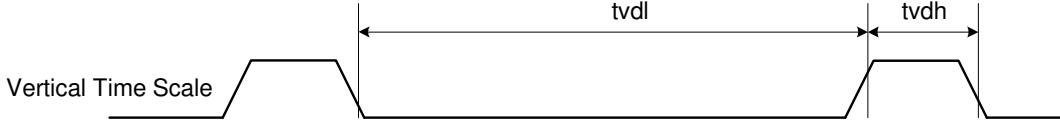
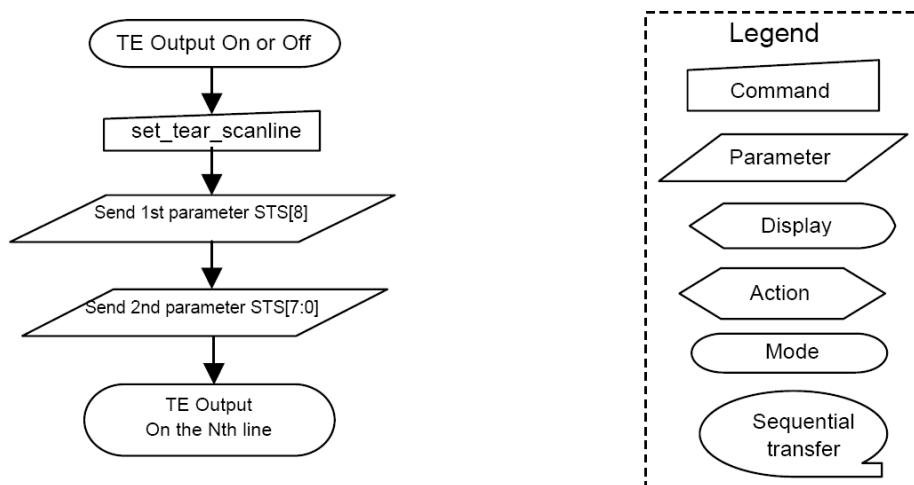
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>No</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Status	Default Value												
Power On Sequence	Random value												
SW Reset	No change												
HW Reset	No change												
Default													
Flow Chart	<pre> graph TD     A[Write_memory_continue] --&gt; B((Image Data D1[17:0], D2[17:0] ..., Dn[17:0]))     B --&gt; C[Next Command]     </pre> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p><b>Legend</b></p> <ul style="list-style-type: none"> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px;"></span> Command</li> <li><span style="width: 15px; height: 15px; display: inline-block; border-left: 1px solid black; border-bottom: 1px solid black; transform: rotate(-45deg);"></span> Parameter</li> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px; border-left: 1px solid black;"></span> Display</li> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px; border-right: 1px solid black;"></span> Action</li> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px; border-radius: 50%;"></span> Mode</li> <li><span style="border: 1px solid black; display: inline-block; width: 15px; height: 15px; border-radius: 50%; border: 1px solid black; border-left: none; border-bottom: none; border-right: none; border-top: none; border-top-left-radius: 50%; border-top-right-radius: 50%;"></span> Sequential transfer</li> </ul> </div>												

### 8.2.35. Read\_Memory\_Continue (3Eh)

Read_Memory_Continue																									
3Eh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF												
x <sup>st</sup> Parameter	1	↑	1	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF												
N <sup>st</sup> Parameter	1	↑	1	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF												
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue (3Eh) or read_memory_start (2Eh) command.  <b>If set_address_mode B5 = 0:</b> Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.																								
Restriction	A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Random data</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>No change</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Random data	SW Reset	No change	HW Reset	No change				
Status	Default Value																								
Power On Sequence	Random data																								
SW Reset	No change																								
HW Reset	No change																								



### 8.2.36. Set\_Tear\_Scanline (44h)

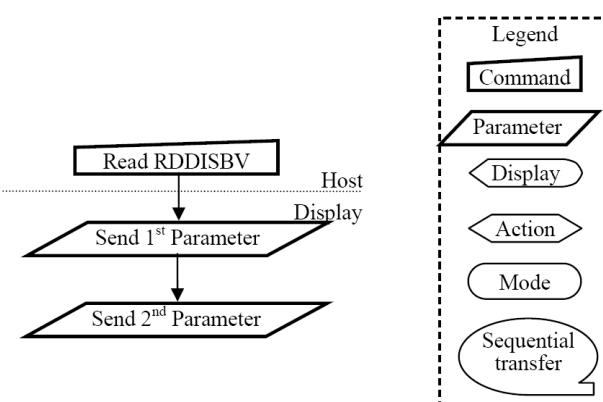
Set_Tear_Scanline																									
44h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h												
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	0	0	0	STS [8]	00												
2 <sup>nd</sup> Parameter	1	1	↑	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00												
Description	This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.  Note that set_tear_scanline with STS=0 is equivalent to set_tear_on with M=0. The Tearing Effect Output line shall be active low when the display module is in Sleep mode.																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>STS [8:0]=0000h</td> </tr> <tr> <td>SW Reset</td> <td>STS [8:0]=0000h</td> </tr> <tr> <td>HW Reset</td> <td>STS [8:0]=0000h</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	STS [8:0]=0000h	SW Reset	STS [8:0]=0000h	HW Reset	STS [8:0]=0000h				
Status	Default Value																								
Power On Sequence	STS [8:0]=0000h																								
SW Reset	STS [8:0]=0000h																								
HW Reset	STS [8:0]=0000h																								
Flow Chart	 <pre> graph TD     A([TE Output On or Off]) --&gt; B[set_tear_scanline]     B --&gt; C[/Send 1st parameter STS[8]/]     C --&gt; D[/Send 2nd parameter STS[7:0]/]     D --&gt; E([TE Output On the Nth line])     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

### 8.2.37. Get\_Scanline (45h)

Get_Scanline																									
45h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	XX	0	0	0	0	0	0	GTS [9]	GTS [8]	00												
3 <sup>rd</sup> Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00												
Description	The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.  When in Sleep Mode, the value returned by get_scanline is undefined.																								
Restriction	None																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>GTS [9:0]</td> <td></td> </tr> <tr> <td>Power On Sequence</td> <td>GTS [9:0]=0000h</td> </tr> <tr> <td>SW Reset</td> <td>GTS [9:0]=0000h</td> </tr> <tr> <td>HW Reset</td> <td>GTS [9:0]=0000h</td> </tr> </tbody> </table>													Status	Default Value	GTS [9:0]		Power On Sequence	GTS [9:0]=0000h	SW Reset	GTS [9:0]=0000h	HW Reset	GTS [9:0]=0000h		
Status	Default Value																								
GTS [9:0]																									
Power On Sequence	GTS [9:0]=0000h																								
SW Reset	GTS [9:0]=0000h																								
HW Reset	GTS [9:0]=0000h																								
Flow Chart	<pre> graph TD     Start[get_scanline] --&gt; Wait{Wait 3us}     Wait --&gt; Dummy[/Dummy Read/]     Dummy --&gt; Send1[/Send 1st parameter GTS[9:8]/]     Send1 --&gt; Send2[/Send 2nd parameter GTS[7:0]/]      subgraph Legend [Legend]         Command[Command]         Parameter[Parameter]         Display[Display]         Action[Action]         Mode[Mode]         Sequential[Sequential transfer]     end </pre>																								

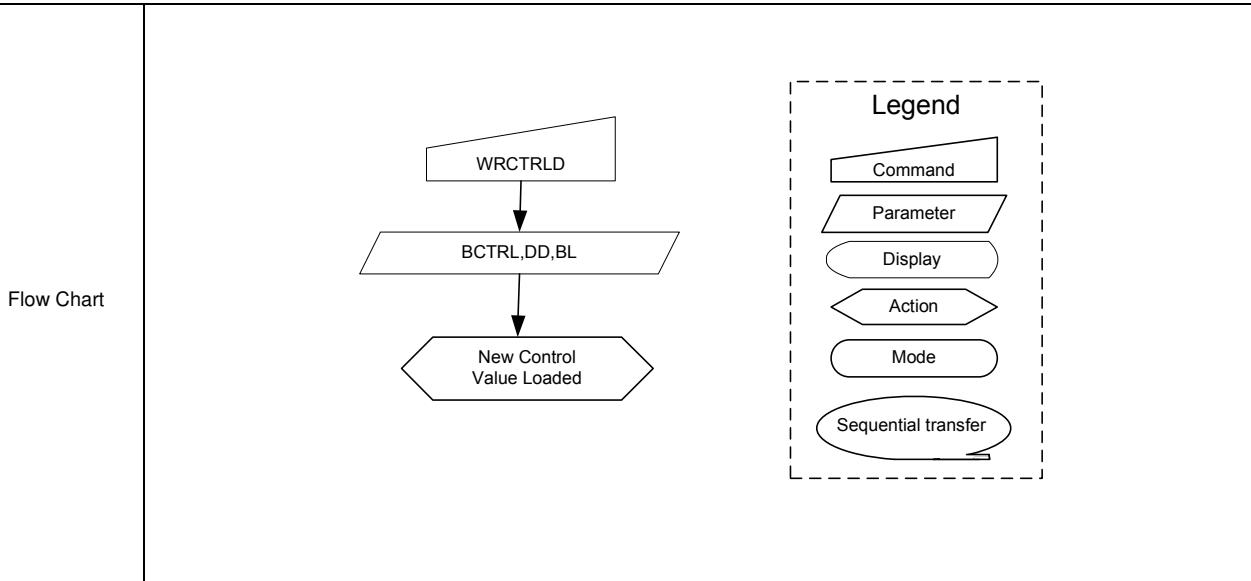
### **8.2.38. Write Display Brightness (51h)**

### 8.2.39. Read Display Brightness (52h)

52h		RDDISBV (Read Display Brightness Value)																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	XX	0	1	0	1	0	0	1	0	52h											
1 <sup>st</sup> Parameter		1	↑	1	XX	X	X	X	X	X	X	X	X	X											
2 <sup>nd</sup> Parameter		1	↑	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00											
Description	<p>This command returns the brightness value of the display.</p> <p>It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p>																								
Restriction	<p>The display module is sending 2<sup>nd</sup> parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode.</p> <p>Only 2<sup>nd</sup> parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th>Default Value</th> </tr> <tr> <th>DBV [7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00h</td> </tr> <tr> <td>SW Reset</td> <td>8'h00h</td> </tr> <tr> <td>HW Reset</td> <td>8'h00h</td> </tr> </tbody> </table>													Status	Default Value	DBV [7:0]	Power On Sequence	8'h00h	SW Reset	8'h00h	HW Reset	8'h00h			
Status	Default Value																								
	DBV [7:0]																								
Power On Sequence	8'h00h																								
SW Reset	8'h00h																								
HW Reset	8'h00h																								
Flow Chart	 <pre> graph TD     Start[Read RDDISBV] --&gt; Send1[/Send 1<sup>st</sup> Parameter/]     Send1 --&gt; Send2[/Send 2<sup>nd</sup> Parameter/]     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

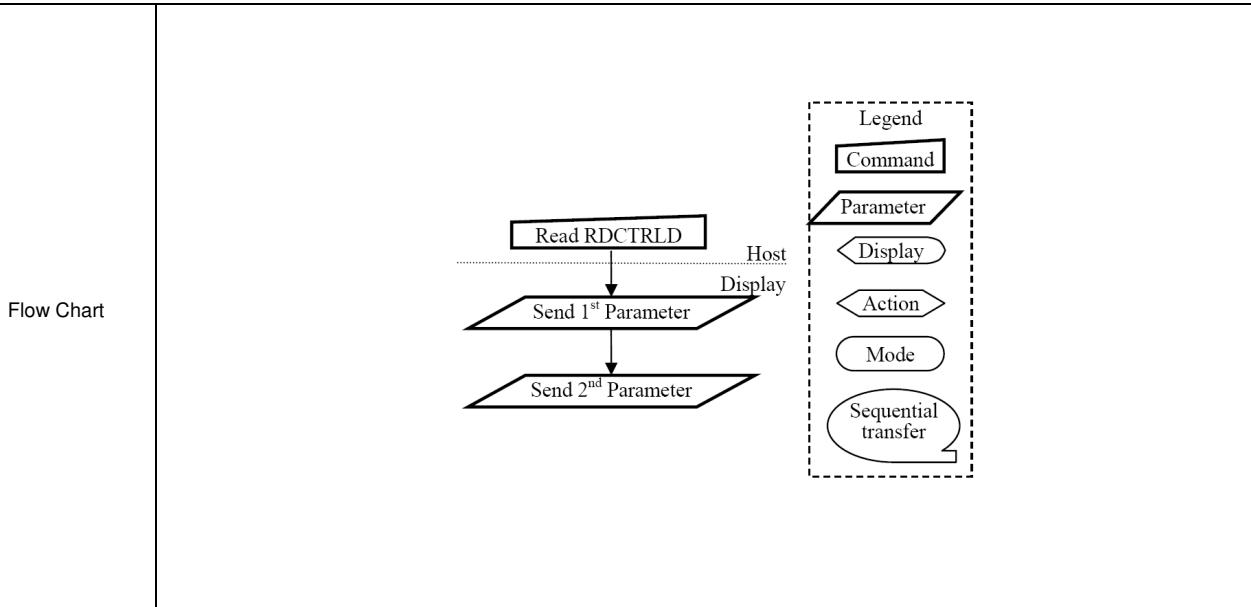
### 8.2.40. Write CTRL Display (53h)

53h		WRCTRLD (Write Control Display)																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h																			
Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00																			
This command is used to control display brightness.																																
<b>BCTRL:</b> Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.)																																
<b>DD:</b> Display Dimming, only for manual brightness setting DD = 0: Display Dimming is off DD = 1: Display Dimming is on																																
<b>BL:</b> Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low. ) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1 → 0.																																
When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.																																
Restriction	None																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In	Yes																															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>BCTRL</th> <th>DD</th> <th>BL</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> </tr> <tr> <td>SW Reset</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> </tr> <tr> <td>HW Reset</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> </tr> </tbody> </table>													Status	Default Value			BCTRL	DD	BL	Power On Sequence	1'b0	1'b0	1'b0	SW Reset	1'b0	1'b0	1'b0	HW Reset	1'b0	1'b0	1'b0
Status	Default Value																															
	BCTRL	DD	BL																													
Power On Sequence	1'b0	1'b0	1'b0																													
SW Reset	1'b0	1'b0	1'b0																													
HW Reset	1'b0	1'b0	1'b0																													



### 8.2.41. Read CTRL Display (54h)

RDCTRLD (Read Control Display)																																
54h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h																			
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX																			
2 <sup>nd</sup> Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00																			
Description	This command is used to return brightness setting.  <b>BCTRL:</b> Brightness Control Block On/Off, '0' = Off (Brightness registers are 00h) '1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)  <b>DD:</b> Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on  <b>BL:</b> Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low. ) '1' = On																															
Restriction	The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.  Only 2nd parameter is sent on DSI (The 1st parameter is not sent).																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In	Yes																															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>BCTRL</th> <th>DD</th> <th>BL</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> </tr> <tr> <td>SW Reset</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> </tr> <tr> <td>HW Reset</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> </tr> </tbody> </table>													Status	Default Value			BCTRL	DD	BL	Power On Sequence	1'b0	1'b0	1'b0	SW Reset	1'b0	1'b0	1'b0	HW Reset	1'b0	1'b0	1'b0
Status	Default Value																															
	BCTRL	DD	BL																													
Power On Sequence	1'b0	1'b0	1'b0																													
SW Reset	1'b0	1'b0	1'b0																													
HW Reset	1'b0	1'b0	1'b0																													



#### **8.2.42. Write Content Adaptive Brightness Control (55h)**

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### 8.2.43. Read Content Adaptive Brightness Control (56h)

RDCABC (Read Content Adaptive Brightness Control)																									
56h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	1	1	0	56h												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 <sup>nd</sup> Parameter	1	↑	1	XX	0	0	0	0	0	0	C [1]	C [0]	00												
Description	This command is used to read the settings for image content based adaptive brightness control functionality. It is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>C [1:0]</td> <td>Default Value</td> </tr> <tr> <td>2'b00</td> <td>Off</td> </tr> <tr> <td>2'b01</td> <td>User Interface Image</td> </tr> <tr> <td>2'b10</td> <td>Still Picture</td> </tr> <tr> <td>2'b11</td> <td>Moving Image</td> </tr> </table>													C [1:0]	Default Value	2'b00	Off	2'b01	User Interface Image	2'b10	Still Picture	2'b11	Moving Image		
C [1:0]	Default Value																								
2'b00	Off																								
2'b01	User Interface Image																								
2'b10	Still Picture																								
2'b11	Moving Image																								
Restriction	The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).																								
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>C [1:0]=00h</td> </tr> <tr> <td>SW Reset</td> <td>C [1:0]=00h</td> </tr> <tr> <td>HW Reset</td> <td>C [1:0]=00h</td> </tr> </table>													Status	Default Value	Power On Sequence	C [1:0]=00h	SW Reset	C [1:0]=00h	HW Reset	C [1:0]=00h				
Status	Default Value																								
Power On Sequence	C [1:0]=00h																								
SW Reset	C [1:0]=00h																								
HW Reset	C [1:0]=00h																								
Flow Chart	<p>The flowchart illustrates the communication sequence between the Host and the Display. The Host initiates the "Read RDCABC" command. In response, the Display sends the "1<sup>st</sup> Parameter" and then the "2<sup>nd</sup> Parameter".</p> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

### 8.2.44. Write CABC Minimum Brightness (5Eh)

5Eh		Backlight Control 1																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh											
Parameter		1	1	↑	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00											
Description	This command is used to set the minimum brightness value of the display for CABC function.  CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.  When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness cannot be changed.  This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.  When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)", CABC minimum brightness setting is ignored.  In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>CMB [7:0]</td> <td></td> </tr> <tr> <td>Power On Sequence</td> <td>8'h00h</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>HW Reset</td> <td>8'h00h</td> </tr> </tbody> </table>													Status	Default Value	CMB [7:0]		Power On Sequence	8'h00h	SW Reset	No Change	HW Reset	8'h00h		
Status	Default Value																								
CMB [7:0]																									
Power On Sequence	8'h00h																								
SW Reset	No Change																								
HW Reset	8'h00h																								

### 8.2.45. Read CABC Minimum Brightness (5Fh)

Backlight Control 1																									
5Fh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00												
Description	This command returns the minimum brightness value of CABC function.  In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.  CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th>Default Value</th> </tr> <tr> <th>CMB [7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00h</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>HW Reset</td> <td>8'h00h</td> </tr> </tbody> </table>													Status	Default Value	CMB [7:0]	Power On Sequence	8'h00h	SW Reset	No Change	HW Reset	8'h00h			
Status	Default Value																								
	CMB [7:0]																								
Power On Sequence	8'h00h																								
SW Reset	No Change																								
HW Reset	8'h00h																								

**8.2.46. Read ID1 (DAh)**

DAh	RDID1 (Read ID1)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	XX	ID1 [7:0]								00												
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1 <sup>st</sup> parameter is dummy data. The 2 <sup>nd</sup> parameter is LCD module's manufacturer ID. X = Don't care																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
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Status	Default Value (Before MTP program)	Default Value (After MTP program)																							
Power On Sequence	8'h00h	MTP value																							
SW Reset	8'h00h	MTP value																							
HW Reset	8'h00h	MTP value																							
Flow Chart	<p>The flowchart illustrates the communication sequence. A box labeled "RDID1(DAh)" is at the top. An arrow points down to a dashed horizontal line separating the "Host" from the "Driver". Below the line, a trapezoid represents the driver's response. Inside the trapezoid, the text "1st Parameter: Dummy Read" and "2nd Parameter: Send ID1[7:0]" is centered. To the right of the trapezoid is a legend box titled "Legend" containing six items: "Command" (triangular arrow), "Parameter" (horizontal arrow), "Display" (vertical rectangle), "Action" (right-pointing arrow), "Mode" (oval), and "Sequential transfer" (oval).</p>																								

### 8.2.47. Read ID2 (DBh)

DBh	RDID2 (Read ID2)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	XX	ID2 [7:0]								00												
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1 <sup>st</sup> parameter is dummy data. The 2 <sup>nd</sup> parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID2 can be programmed by MTP function. X = Don't care																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value (Before MTP program)</th><th>Default Value (After MTP program)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>8'h80h</td><td>MTP value</td></tr> <tr> <td>SW Reset</td><td>8'h80h</td><td>MTP value</td></tr> <tr> <td>HW Reset</td><td>8'h80h</td><td>MTP value</td></tr> </tbody> </table>													Status	Default Value (Before MTP program)	Default Value (After MTP program)	Power On Sequence	8'h80h	MTP value	SW Reset	8'h80h	MTP value	HW Reset	8'h80h	MTP value
Status	Default Value (Before MTP program)	Default Value (After MTP program)																							
Power On Sequence	8'h80h	MTP value																							
SW Reset	8'h80h	MTP value																							
HW Reset	8'h80h	MTP value																							
Flow Chart	<p>The flowchart illustrates the communication between the Host and the Driver. A box labeled "RDID2(DBh)" is connected by an arrow pointing down to a dashed horizontal line separating the Host and Driver. Below the line, a trapezoid represents the Driver. Inside the trapezoid, the text "1st Parameter: Dummy Read" and "2nd Parameter: Send ID2[7:0]" is shown. To the right of the trapezoid is a legend box titled "Legend" containing six items: "Command" (upward arrow), "Parameter" (downward arrow), "Display" (horizontal arrow), "Action" (right-pointing arrow), "Mode" (oval), and "Sequential transfer" (oval with a curved arrow).</p>																								

**8.2.48. Read ID3 (DCh)**

DCh	RDID3 (Read ID3)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	XX	ID3 [7:0]								00												
Description	This read byte identifies the LCD module/driver and It is specified by User. The 1 <sup>st</sup> parameter is dummy data. The 2 <sup>nd</sup> parameter is LCD module/driver ID. The ID3 can be programmed by MTP function. X = Don't care																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
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Status	Default Value (Before MTP program)	Default Value (After MTP program)																							
Power On Sequence	8'h00h	MTP value																							
SW Reset	8'h00h	MTP value																							
HW Reset	8'h00h	MTP value																							
Flow Chart	<p>The flowchart illustrates the RDID3(DCh) sequence. It starts with a 'Command' (triangle) from the 'Host' to the 'Driver'. The driver then responds with a 'Display' (parallelogram) containing the text: '1st Parameter: Dummy Read' and '2nd Parameter: Send ID3[7:0]'. To the right of the flowchart is a legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																								

## 8.3. Description of Level 2 Command

### 8.3.1. RGB Interface Signal Control (B0h)

IFMODE (Interface Mode Control)																																															
B0h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																		
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h																																		
Parameter	1	1	↑	XX	ByPass_MODE	RCM [1]	RCM [0]	0	VSPL	HSPL	DPL	EPL	40																																		
Description	Sets the operation status of the display interface. The setting becomes effective as soon as the command is received. <b>EPL:</b> DE polarity ("0"= High enable for RGB interface, "1"= Low enable for RGB interface) <b>DPL:</b> DOTCLK polarity set ("0"= data fetched at the rising time, "1"= data fetched at the falling time) <b>HSPL:</b> HSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock) <b>VSPL:</b> VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock) <b>RCM [1:0]:</b> RGB interface selection (refer to the RGB interface section).  <b>ByPass_MODE:</b> Select display data path whether Memory or Direct to Shift register when RGB Interface is used.																																														
Restriction	EXTC should be high to enable this command																																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																						
Status	Availability																																														
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Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="6">Default Value</th> </tr> <tr> <th>ByPass_MODE</th> <th>RCM [1:0]</th> <th>VSPL</th> <th>HSPL</th> <th>DPL</th> <th>EPL</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>1'b0</td> <td>2'b10</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> <td>1'b1</td> </tr> <tr> <td>SW Reset</td> <td>1'b0</td> <td>2'b10</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> <td>1'b1</td> </tr> <tr> <td>HW Reset</td> <td>1'b0</td> <td>2'b10</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> <td>1'b1</td> </tr> </tbody> </table>													Status	Default Value						ByPass_MODE	RCM [1:0]	VSPL	HSPL	DPL	EPL	Power ON Sequence	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1	SW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1	HW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1
Status	Default Value																																														
	ByPass_MODE	RCM [1:0]	VSPL	HSPL	DPL	EPL																																									
Power ON Sequence	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1																																									
SW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1																																									
HW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1																																									

### 8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))																																																																																																																																																																																																																																																																																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																																																																																																																																												
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h																																																																																																																																																																																																																																																																												
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVA [1:0]	00																																																																																																																																																																																																																																																																													
2 <sup>nd</sup> Parameter	1	1	↑	XX	0	0	0				RTNA [4:0]	1B																																																																																																																																																																																																																																																																													
Description	Formula to calculate frame frequency:  Frame Rate = $\frac{fosc}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$																																																																																																																																																																																																																																																																																								
	Sets the division ratio for internal clocks of Normal mode at MCU interface.																																																																																																																																																																																																																																																																																								
	fosc : internal oscillator frequency																																																																																																																																																																																																																																																																																								
	Clocks per line : RTNA setting																																																																																																																																																																																																																																																																																								
	Division ratio : DIVA setting																																																																																																																																																																																																																																																																																								
	Lines : total driving line number																																																																																																																																																																																																																																																																																								
	VBP : back porch line number																																																																																																																																																																																																																																																																																								
	VFP : front porch line number																																																																																																																																																																																																																																																																																								
	<table border="1"> <thead> <tr> <th colspan="5">RTNA [4:0]</th> <th>Frame Rate (Hz)</th> </tr> </thead> <tbody> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>119</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>112</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>106</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>100</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>95</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>90</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>86</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>83</td></tr> </tbody> </table>					RTNA [4:0]					Frame Rate (Hz)	1	0	0	0	0	119	1	0	0	0	1	112	1	0	0	1	0	106	1	0	0	1	1	100	1	0	1	0	0	95	1	0	1	0	1	90	1	0	1	1	0	86	1	0	1	1	1	83	<table border="1"> <thead> <tr> <th colspan="5">RTNA [4:0]</th> <th>Frame Rate (Hz)</th> </tr> </thead> <tbody> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>79</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>76</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>73</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>70(default)</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>68</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>65</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>63</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>61</td></tr> </tbody> </table>													RTNA [4:0]					Frame Rate (Hz)	1	1	0	0	0	79	1	1	0	0	1	76	1	1	0	1	0	73	1	1	0	1	1	70(default)	1	1	1	0	0	68	1	1	1	0	1	65	1	1	1	0	1	63	1	1	1	1	1	61																																																																																																																																																											
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Restriction	EXTC should be high to enable this command														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes	
Status	Availability														
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes														
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes														
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes														
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes														
Sleep IN	Yes														
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Status	Default Value														
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Power ON Sequence	2'b00	5'h1Bh													
SW Reset	2'b00	5'h1Bh													
HW Reset	2'b00	5'h1Bh													

### 8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control (In Idle Mode / 8I colors))																																																																																																																		
	D/CX	RDX	WRX	D17-8		D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																					
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2 <sup>nd</sup> Parameter	1	1	↑	XX		0	0	0		RTNB [4:0]				1B																																																																																																					
Description	Formula to calculate frame frequency																																																																																																																		
	$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$																																																																																																																		
	Sets the division ratio for internal clocks of Idle mode at MCU interface.																																																																																																																		
	fosc : internal oscillator frequency																																																																																																																		
	Clocks per line : RTNB setting																																																																																																																		
	Division ratio : DIVB setting																																																																																																																		
	Lines : total driving line number																																																																																																																		
	VBP : back porch line number																																																																																																																		
	VFP : front porch line number																																																																																																																		
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Restriction	EXTC should be high to enable this command														
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Status	Default Value														
	DIVB [1:0]	RTNB [4:0]													
Power ON Sequence	2'b00	5'h1Bh													
SW Reset	2'b00	5'h1Bh													
HW Reset	2'b00	5'h1Bh													

#### **8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)**

B3h	FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC [1:0]	00	
2 <sup>nd</sup> Parameter	1	1	↑	XX	0	0	0	RTNC [4:0]					1B

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VPF})}$$

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.

`fosc` : internal oscillator frequency

Clocks per line : RTNC setting

Division ratio : DIVC setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNC [4:0]					Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

RTNC [4:0]					Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

**DIVC [1:0]**: division ratio for internal clocks when Partial mode.

DIVC [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

Note: 1clock unit=1.625μ sec

**BTNC [4:0]:** BTNC [4:0] is used to set 1H (line) period of Partial mode at MClI interface

RTNC [4:0]					Clock per Line
RTNC [4:0]					Clock per Line
RTNC [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited
0	1	0	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	1	0	1	1	22 clocks
1	1	0	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction	EXTC should be high to enable this command														
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Status	Default Value														
	DIVC [1:0]	RTNC [4:0]													
Power ON Sequence	2'b00	5'h1Bh													
SW Reset	2'b00	5'h1Bh													
HW Reset	2'b00	5'h1Bh													

### 8.3.5. Display Inversion Control (B4h)

INVTR (Display Inversion Control)																																
B4h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h																			
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	0	NLA	NLB	NLC	02																			
Description	Display inversion mode set  <b>NLA:</b> Inversion setting in full colors normal mode (Normal mode on) <b>NLB:</b> Inversion setting in Idle mode (Idle mode on) <b>NLC:</b> Inversion setting in full colors partial mode (Partial mode on / Idle mode off) <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>NLA / NLB / NLC</th> <th>Inversion</th> </tr> <tr> <td>0</td> <td>Line inversion</td> </tr> <tr> <td>1</td> <td>Frame inversion</td> </tr> </table>													NLA / NLB / NLC	Inversion	0	Line inversion	1	Frame inversion													
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1	Frame inversion																															
Restriction	EXTC should be high to enable this command																															
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Status	Availability																															
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Status	Default Value																															
	NLA	NLB	NLC																													
Power ON Sequence	1'b0	1'b1	1'b0																													
SW Reset	1'b0	1'b1	1'b0																													
H/W Reset	1'b0	1'b1	1'b0																													

### 8.3.6. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)																			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h							
1 <sup>st</sup> Parameter	1	1	↑	XX	0				VFP [6:0]				02							
2 <sup>nd</sup> Parameter	1	1	↑	XX	0				VBP [6:0]				02							
3 <sup>rd</sup> Parameter	1	1	↑	XX	0	0	0		HFP [4:0]				0A							
4 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0		HBP [4:0]				14							
Description	<b>VFP [6:0] / VBP [6:0]:</b> The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.																			
	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch				VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch													
	0000000	Setting inhibited				1000000	64													
	0000001	Setting inhibited				1000001	65													
	0000010	2				1000010	66													
	0000011	3				1000011	67													
	0000100	4				1000100	68													
	0000101	5				1000101	69													
	0000110	6				1000110	70													
	0000111	7				1000111	71													
	0001000	8				1001000	72													
	0001001	9				1001001	73													
	0001010	10				1001010	74													
	0001011	11				1001011	75													
	0001100	12				1001100	76													
	0001101	13				1001101	77													
	:	:				:	:													
	0111101	61				1111101	125													
	0111110	62				1111110	126													
	0111111	63				1111111	127													
<i>Note: VFP + VBP ≤ 254 HSYNC signals</i>																				
Description	<b>HFP [4:0] / HBP [4:0]:</b> The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.																			
	HFP [4:0] HBP [4:0]	Number of DOTCLK of the front/back porch				HFP [4:0] HBP [4:0]	Number of DOTCLK of front/back porch													
	00000	Setting prohibited				10000	16													
	00001	Setting prohibited				10001	17													
	00010	2				10010	18													
	00011	3				10011	19													
	00100	4				10100	20													
	00101	5				10101	21													
	00110	6				10110	22													
	00111	7				10111	23													
	01000	8				11000	24													
	01001	9				11001	25													
	01010	10				11010	26													
	01011	11				11011	27													
	01100	12				11100	28													
	01101	13				11101	29													
	01110	14				11110	30													
	01111	15				11111	31													

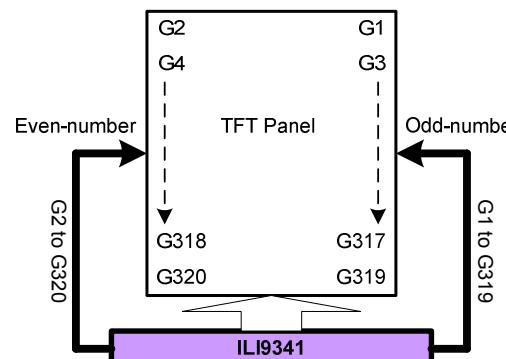
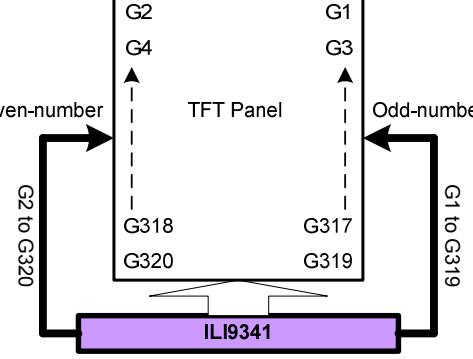
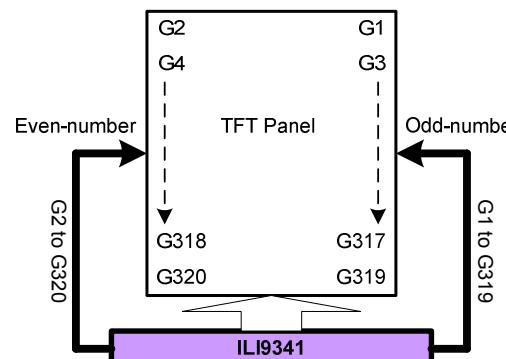
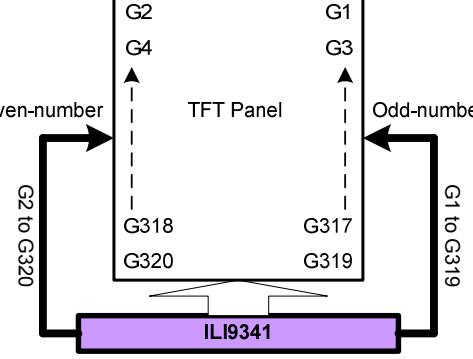
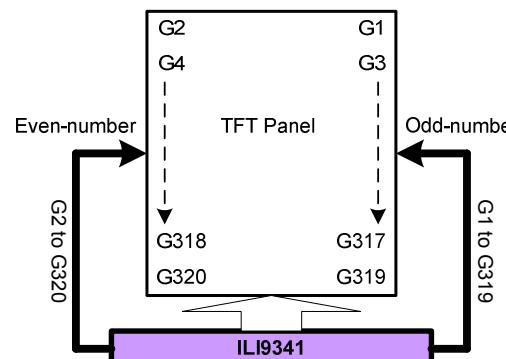
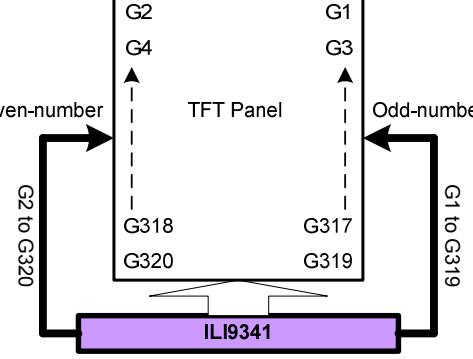
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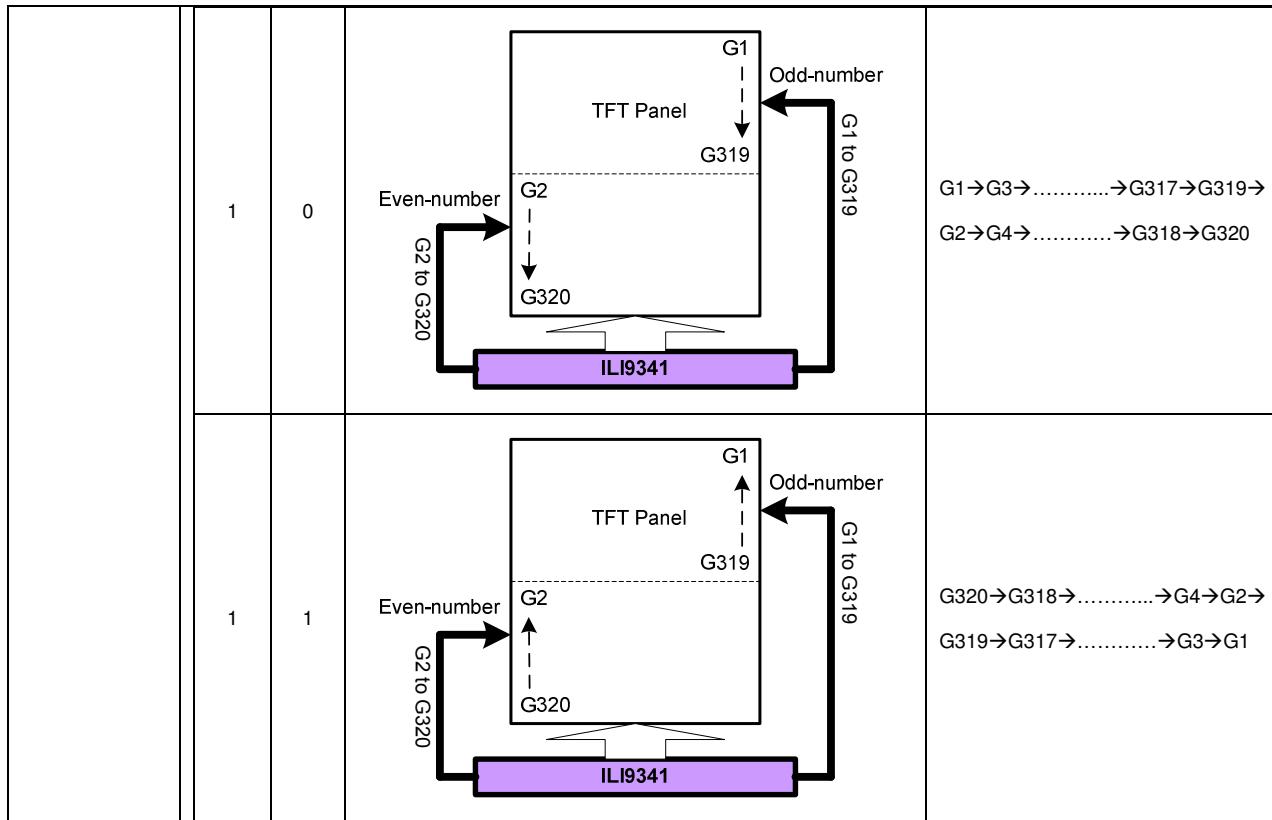
Restriction	EXTC should be high to enable this command																												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table>					Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes												
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Status	Default Value																												
	VFP [6:0]	VBP [6:0]	HFP [4:0]	HBP [4:0]																									
Power ON Sequence	7'h02h	7'h02h	5'h0Ah	5'h14h																									
SW Reset	7'h02h	7'h02h	5'h0Ah	5'h14h																									
HW Reset	7'h02h	7'h02h	5'h0Ah	5'h14h																									

### 8.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)																					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h									
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	PTG [1:0]	PT [1:0]			0A									
2 <sup>nd</sup> Parameter	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				82									
3 <sup>rd</sup> Parameter	1	1	↑	XX	0	0			NL [5:0]				27									
4 <sup>th</sup> Parameter	1	1	↑	XX	0	0			PCDIV [5:0]				XX									
Description	<b>PTG [1:0]:</b> Set the scan mode in non-display area.																					
	PTG1	PTG0	Gate outputs in non-display area			Source outputs in non-display area			VCOM output													
	0	0	Normal scan			Set with the PT [2:0] bits			VCOMH/VCOML													
	0	1	Setting prohibited			---			---													
	1	0	Interval scan			Set with the PT [2:0] bits																
	1	1	Setting prohibited			---			---													
	<b>PT [1:0]:</b> Determine source/VCOM output in a non-display area in the partial display mode.																					
	PT [1:0]		Source output on non-display area			VCOM output on non-display area																
			Positive polarity	Negative polarity	Positive polarity	Negative polarity	Positive polarity	Negative polarity														
	0	0	V63	V0	VCOML	VCOMH																
	0	1	V0	V63	VCOML	VCOMH																
	1	0	AGND	AGND	AGND	AGND	AGND	AGND														
	1	1	Hi-Z	Hi-Z	AGND	AGND	AGND	AGND														
	<b>SS:</b> Select the shift direction of outputs from the source driver.																					
	SS		Source Output Scan Direction																			
			0	S1 → S720																		
			1	S720 → S1																		
	In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.																					
	To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.																					
	To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.																					
	<b>REV:</b> Select whether the liquid crystal type is normally white type or normally black type.																					
	REV		Liquid crystal type																			
			0	Normally black																		
			1	Normally white																		
	<b>ISC [3:0]:</b> Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] = "10" to select interval scan.																					
	Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.																					
	ISC [3:0]		Scan Cycle		f <sub>FLM</sub> = 60Hz																	
			0000	1 frame			17ms															
			0001	3 frames			51ms															
			0010	5 frames			85ms															
			0011	7 frames			119ms															
			0100	9 frames			153ms															
			0101	11 frames			187ms															
			0110	13 frames			221ms															
			0111	15 frames			255ms															

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			<table border="1"> <tr><td>1000</td><td>17 frames</td><td>289ms</td></tr> <tr><td>1001</td><td>19 frames</td><td>323ms</td></tr> <tr><td>1010</td><td>21 frames</td><td>357ms</td></tr> <tr><td>1011</td><td>23 frames</td><td>391ms</td></tr> <tr><td>1100</td><td>25 frames</td><td>425ms</td></tr> <tr><td>1101</td><td>27 frames</td><td>459ms</td></tr> <tr><td>1110</td><td>29 frames</td><td>493ms</td></tr> <tr><td>1111</td><td>31 frames</td><td>527ms</td></tr> </table>	1000	17 frames	289ms	1001	19 frames	323ms	1010	21 frames	357ms	1011	23 frames	391ms	1100	25 frames	425ms	1101	27 frames	459ms	1110	29 frames	493ms	1111	31 frames	527ms	
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1100	25 frames	425ms																										
1101	27 frames	459ms																										
1110	29 frames	493ms																										
1111	31 frames	527ms																										
		<b>GS:</b> Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.																										
			<table border="1"> <tr><td>GS</td><td>Gate Output Scan Direction</td></tr> <tr><td>0</td><td>G1 → G320</td></tr> <tr><td>1</td><td>G320 → G1</td></tr> </table>	GS	Gate Output Scan Direction	0	G1 → G320	1	G320 → G1																			
GS	Gate Output Scan Direction																											
0	G1 → G320																											
1	G320 → G1																											
		<b>SM:</b> Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.																										
		<table border="1"> <thead> <tr> <th>SM</th><th>GS</th><th>Scan Direction</th><th>Gate Output Sequence</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>   TFT Panel           </td><td>           G1 → G2 → G3 → G4 → .....            .... → G317 → G318 → G319 → G320         </td></tr> <tr> <td>0</td><td>1</td><td>   TFT Panel           </td><td>           G320 → G319 → G318 → G317 → .....            .... → G4 → G3 → G2 → G1         </td></tr> </tbody> </table>	SM	GS	Scan Direction	Gate Output Sequence	0	0	 TFT Panel	G1 → G2 → G3 → G4 → ..... .... → G317 → G318 → G319 → G320	0	1	 TFT Panel	G320 → G319 → G318 → G317 → ..... .... → G4 → G3 → G2 → G1														
SM	GS	Scan Direction	Gate Output Sequence																									
0	0	 TFT Panel	G1 → G2 → G3 → G4 → ..... .... → G317 → G318 → G319 → G320																									
0	1	 TFT Panel	G320 → G319 → G318 → G317 → ..... .... → G4 → G3 → G2 → G1																									



**NL [5:0]:** Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	0	1	0	0	1	80 lines
0	0	1	0	1	0	88 lines
0	0	1	0	1	1	96 lines
0	0	1	1	0	0	104 lines
0	0	1	1	0	1	112 lines
0	0	1	1	1	0	120 lines
0	0	1	1	1	1	128 lines
0	1	0	0	0	0	136 lines
0	1	0	0	0	1	144 lines
0	1	0	0	1	0	152 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

NL [5:0]						LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
0	1	1	1	1	0	248 lines
0	1	1	1	1	1	256 lines
1	0	0	0	0	0	264 lines
1	0	0	0	0	1	272 lines
1	0	0	0	1	0	280 lines
1	0	0	0	1	1	288 lines
1	0	0	1	0	0	296 lines
1	0	0	1	0	1	304 lines
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
Others						Setting inhibited

**PCDIV [5:0]:**

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	$\text{external fosc} = \frac{\text{DOTCLK}}{2 \times (\text{PCDIV} + 1)}$																																												
Restriction	EXTC should be high to enable this command																																												
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SW Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h																																					
HW Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h																																					

### 8.3.8. Entry Mode Set (B7h)

B7h		ETMOD (Entry Mode Set)																																																																																																																																
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																				
Command		0	1	↑	XX	1	0	1	1	0	1	1	1	B7h																																																																																																																				
Parameter		1	1	↑	XX	0	0	0	0	0	GON	DTE	GAS	06																																																																																																																				
<b>GAS:</b> Low voltage detection control.																																																																																																																																		
Description	<table border="1"> <tr> <td>GAS</td><td colspan="14">Low voltage detection</td></tr> <tr> <td>0</td><td colspan="14">Enable</td></tr> <tr> <td>1</td><td colspan="14">Disable</td></tr> </table>														GAS	Low voltage detection														0	Enable														1	Disable																																																																																				
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0	Enable																																																																																																																																	
1	Disable																																																																																																																																	
<b>GON/DTE:</b> Set the output level of gate driver G1 ~ G320 as follows																																																																																																																																		
<table border="1"> <tr> <td>GON</td><td>DTE</td><td colspan="13">G1~G320 Gate Output</td></tr> <tr> <td>0</td><td>0</td><td colspan="13">VGH</td></tr> <tr> <td>0</td><td>1</td><td colspan="13">VGH</td></tr> <tr> <td>1</td><td>0</td><td colspan="13">VGL</td></tr> <tr> <td>1</td><td>1</td><td colspan="13" rowspan="12">Normal display</td></tr> </table>														GON	DTE	G1~G320 Gate Output													0	0	VGH													0	1	VGH													1	0	VGL													1	1	Normal display																																																						
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### 8.3.9. Backlight Control 1 (B8h)

<b>B8h</b>	<b>Backlight Control 1</b>																																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																															
Command	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h																															
Parameter		1	↑	XX	0	0	0	0	TH_UI [3]	TH_UI [2]	TH_UI [1]	TH_UI [0]	0C																															
<b>TH_UI [3:0]:</b> These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.																																												
Description	<table border="1"> <thead> <tr> <th>TH_UI [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'0h</td><td>99%</td></tr> <tr><td>4'1h</td><td>98%</td></tr> <tr><td>4'2h</td><td>96%</td></tr> <tr><td>4'3h</td><td>94%</td></tr> <tr><td>4'4h</td><td>92%</td></tr> <tr><td>4'5h</td><td>90%</td></tr> <tr><td>4'6h</td><td>88%</td></tr> <tr><td>4'7h</td><td>86%</td></tr> </tbody> </table>				TH_UI [3:0]	Description	4'0h	99%	4'1h	98%	4'2h	96%	4'3h	94%	4'4h	92%	4'5h	90%	4'6h	88%	4'7h	86%	<table border="1"> <thead> <tr> <th>TH_UI [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'8h</td><td>84%</td></tr> <tr><td>4'9h</td><td>82%</td></tr> <tr><td>4'Ah</td><td>80%</td></tr> <tr><td>4'Bh</td><td>78%</td></tr> <tr><td>4'Ch</td><td>76%</td></tr> <tr><td>4'Dh</td><td>74%</td></tr> <tr><td>4'Eh</td><td>72%</td></tr> <tr><td>4'Fh</td><td>70%</td></tr> </tbody> </table>				TH_UI [3:0]	Description	4'8h	84%	4'9h	82%	4'Ah	80%	4'Bh	78%	4'Ch	76%	4'Dh	74%	4'Eh	72%	4'Fh	70%
TH_UI [3:0]	Description																																											
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Status	Default Value																																											
TH_UI [3:0]																																												
Power On Sequence	4'b0110																																											
SW Reset	No change																																											
HW Reset	4'b0110																																											

### 8.3.10. Backlight Control 2 (B9h)

B9h		Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h	
Parameter	1	1	↑	XX	TH_MV [3]	TH_MV [2]	TH_MV [1]	TH_MV [0]	TH_ST [3]	TH_ST [2]	TH_ST [1]	TH_ST [0]	CC	

**TH\_ST [3:0]:** These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_ST [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_ST [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

**TH\_MV [3:0]:** These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_MV [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_MV [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

**Description**

The graph illustrates the cumulative distribution of grayscale values. The x-axis represents 'Gray Scales' with markers at  $D_{th}$  and 255. The y-axis represents the 'Histogram' with a marker at 100%. A smooth curve starts near 0% for low gray scales, remains flat until  $D_{th}$ , and then rises sharply towards 100% as it approaches 255. A vertical red arrow originates from the text 'TH\_MV[3:0], TH\_ST[3:0], TH\_UI[3:0]' and points to the point on the curve where the histogram reaches 100%, which is also aligned with the  $D_{th}$  mark on the x-axis.

Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
		TH_MV [3:0]	TH_ST [3:0]
	Power On Sequence	4'b1100	4'b1100
	SW Reset	No change	No change
	HW Reset	4'b1100	4'b1100

### 8.3.11. Backlight Control 3 (BAh)

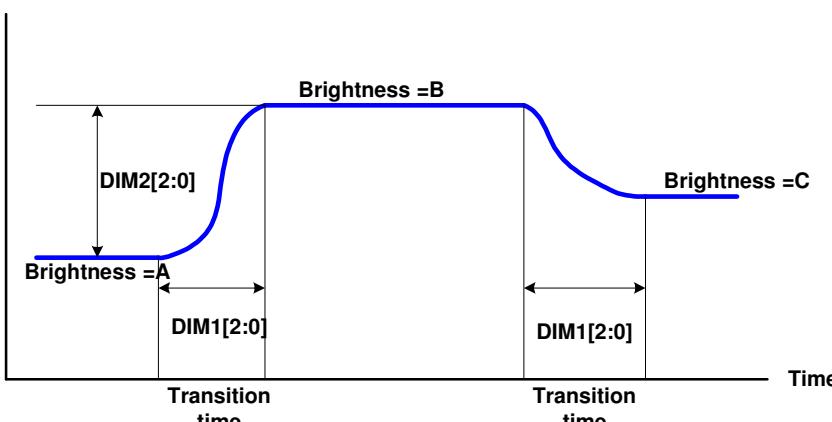
BAh	Backlight Control 3																																											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																															
Command	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh																															
Parameter	1	1	↑	XX	0	0	0	0	DTH_UI [3]	DTH_UI [2]	DTH_UI [1]	DTH_UI [0]	04																															
<b>DTH_UI [3:0]:</b> This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.																																												
Description	<table border="1"> <thead> <tr> <th>DTH_UI [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'0h</td><td>252</td></tr> <tr><td>4'1h</td><td>248</td></tr> <tr><td>4'2h</td><td>244</td></tr> <tr><td>4'3h</td><td>240</td></tr> <tr><td>4'4h</td><td>236</td></tr> <tr><td>4'5h</td><td>232</td></tr> <tr><td>4'6h</td><td>228</td></tr> <tr><td>4'7h</td><td>224</td></tr> </tbody> </table>				DTH_UI [3:0]	Description	4'0h	252	4'1h	248	4'2h	244	4'3h	240	4'4h	236	4'5h	232	4'6h	228	4'7h	224	<table border="1"> <thead> <tr> <th>DTH_UI [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'8h</td><td>220</td></tr> <tr><td>4'9h</td><td>216</td></tr> <tr><td>4'Ah</td><td>212</td></tr> <tr><td>4'Bh</td><td>208</td></tr> <tr><td>4'Ch</td><td>204</td></tr> <tr><td>4'Dh</td><td>200</td></tr> <tr><td>4'Eh</td><td>196</td></tr> <tr><td>4'Fh</td><td>192</td></tr> </tbody> </table>				DTH_UI [3:0]	Description	4'8h	220	4'9h	216	4'Ah	212	4'Bh	208	4'Ch	204	4'Dh	200	4'Eh	196	4'Fh	192
DTH_UI [3:0]	Description																																											
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Power On Sequence	4'b0100																																											
SW Reset	No change																																											
HW Reset	4'b0100																																											

### 8.3.12. Backlight Control 4 (BBh)

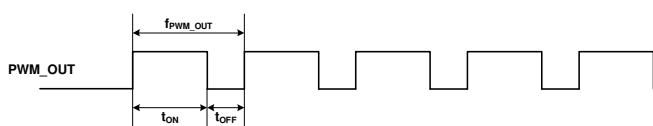
BBh	Backlight Control 4																																																			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																							
Command	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh																																							
Parameter	1	1	↑	XX	DTH_MV [3]	DTH_MV [2]	DTH_MV [1]	DTH_MV [0]	DTH_ST [3]	DTH_ST [2]	DTH_ST [1]	DTH_ST [0]	65																																							
<b>DTH_ST [3:0]/DTH_MV [3:0]:</b> This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.																																																				
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DTH_MV [3:0]	Description																																																			
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Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																			
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																																			
Sleep In	Yes																																																			

Default	Status	Default Value	
		DTH_MV [3:0]	DTH_ST [3:0]
	Power On Sequence	4'b0110	4'b0101
	SW Reset	No change	No change
	HW Reset	4'b0110	4'b0101

### 8.3.13. Backlight Control 5 (BCh)

BCh	Backlight Control 5																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	XX	1	0	1	1	1	1	0	0	BCh																		
Parameter	1	1	↑	XX	DIM2 [3]	DIM2 [2]	DIM2 [1]	DIM2 [0]	0	DIM1 [2]	DIM1 [1]	DIM1 [0]	44																		
<b>DIM1 [2:0]:</b> This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.																															
	<table border="1"> <thead> <tr> <th>DIM1 [2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3'0h</td> <td>1 frame</td> </tr> <tr> <td>3'1h</td> <td>1 frame</td> </tr> <tr> <td>3'2h</td> <td>2 frames</td> </tr> <tr> <td>3'3h</td> <td>4 frames</td> </tr> <tr> <td>3'4h</td> <td>8 frames</td> </tr> <tr> <td>3'5h</td> <td>16 frames</td> </tr> <tr> <td>3'6h</td> <td>32 frames</td> </tr> <tr> <td>3'7h</td> <td>64 frames</td> </tr> </tbody> </table>													DIM1 [2:0]	Description	3'0h	1 frame	3'1h	1 frame	3'2h	2 frames	3'3h	4 frames	3'4h	8 frames	3'5h	16 frames	3'6h	32 frames	3'7h	64 frames
DIM1 [2:0]	Description																														
3'0h	1 frame																														
3'1h	1 frame																														
3'2h	2 frames																														
3'3h	4 frames																														
3'4h	8 frames																														
3'5h	16 frames																														
3'6h	32 frames																														
3'7h	64 frames																														
																															
<b>DIM2 [3:0]:</b> This parameter is used to set the threshold of brightness change.																															
When the brightness transition difference is smaller than DIM2 [3:0], the brightness transition will be ignored.																															
For example:																															
If $  \text{brightness B} - \text{brightness A}   < \text{DIM2 [2:0]}$ , the brightness transition will be ignored and keep the brightness A.																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
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Partial Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In	Yes																														
<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>DIM2 [3:0]</th> <th>DIM1 [2:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>4'b0100</td> <td>4'b0100</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>4'b0100</td> <td>4'b0100</td> </tr> </tbody> </table>													Status	Default Value		DIM2 [3:0]	DIM1 [2:0]	Power On Sequence	4'b0100	4'b0100	SW Reset	No change	No change	HW Reset	4'b0100	4'b0100					
Status	Default Value																														
	DIM2 [3:0]	DIM1 [2:0]																													
Power On Sequence	4'b0100	4'b0100																													
SW Reset	No change	No change																													
HW Reset	4'b0100	4'b0100																													

### 8.3.14. Backlight Control 7 (BEh)

BEh	Backlight Control 7																																				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
Command	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh																								
Parameter	1	1	↑	XX	PWM_DIV[7]	PWM_DIV[6]	PWM_DIV[5]	PWM_DIV[4]	PWM_DIV[3]	PWM_DIV[2]	PWM_DIV[1]	PWM_DIV[0]	0F																								
<b>PWM_DIV [7:0]:</b> PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of PWM_OUT. The PWM frequency can be calculated by using the following equation.																																					
Description	$f_{\text{PWM\_OUT}} = \frac{16\text{MHz}}{( \text{PWM\_DIV}[7:0] + 1 ) \times 255}$ <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PWM_DIV [7:0]</th> <th><math>f_{\text{PWM\_OUT}}</math></th> </tr> </thead> <tbody> <tr><td>8'h0</td><td>62.74 KHz</td></tr> <tr><td>8'h1</td><td>31.38 KHz</td></tr> <tr><td>8'h2</td><td>20.915 KHz</td></tr> <tr><td>8'h3</td><td>15.686 KHz</td></tr> <tr><td>8'h4</td><td>12.549 KHz</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>8'hFB</td><td>249Hz</td></tr> <tr><td>8'hFC</td><td>248Hz</td></tr> <tr><td>8'hFD</td><td>247Hz</td></tr> <tr><td>8'hFE</td><td>246Hz</td></tr> <tr><td>8'hFF</td><td>245Hz</td></tr> </tbody> </table>  <p>Note: The output frequency tolerance of internal frequency divider in CABC is ±10%</p>													PWM_DIV [7:0]	$f_{\text{PWM\_OUT}}$	8'h0	62.74 KHz	8'h1	31.38 KHz	8'h2	20.915 KHz	8'h3	15.686 KHz	8'h4	12.549 KHz	...	...	8'hFB	249Hz	8'hFC	248Hz	8'hFD	247Hz	8'hFE	246Hz	8'hFF	245Hz
PWM_DIV [7:0]	$f_{\text{PWM\_OUT}}$																																				
8'h0	62.74 KHz																																				
8'h1	31.38 KHz																																				
8'h2	20.915 KHz																																				
8'h3	15.686 KHz																																				
8'h4	12.549 KHz																																				
...	...																																				
8'hFB	249Hz																																				
8'hFC	248Hz																																				
8'hFD	247Hz																																				
8'hFE	246Hz																																				
8'hFF	245Hz																																				
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																				
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																				
Partial Mode On, Idle Mode On, Sleep Out	Yes																																				
Sleep In	Yes																																				
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>PWM_DIV [7:0]=0Fh</td></tr> <tr><td>SW Reset</td><td>No change</td></tr> <tr><td>HW Reset</td><td>PWM_DIV [7:0]=0Fh</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	PWM_DIV [7:0]=0Fh	SW Reset	No change	HW Reset	PWM_DIV [7:0]=0Fh																
Status	Default Value																																				
Power On Sequence	PWM_DIV [7:0]=0Fh																																				
SW Reset	No change																																				
HW Reset	PWM_DIV [7:0]=0Fh																																				

### 8.3.15. Backlight Control 8 (BFh)

Backlight Control 2																															
BFh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	XX	1	0	1	1	1	1	1	1	BFh																		
Parameter	1	1	↑	XX	0	0	0	0	0	LEDONR	LEDONPOL	LEDPWMMPOL	00																		
Description	<b>LEDPWMMPOL:</b> The bit is used to define polarity of LEDPWM signal.																														
	<table border="1"> <thead> <tr> <th>BL</th> <th>LEDPWMMPOL</th> <th>LEDPWM pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Original polarity of PWM signal</td> </tr> <tr> <td>1</td> <td>1</td> <td>Inversed polarity of PWM signal</td> </tr> </tbody> </table>													BL	LEDPWMMPOL	LEDPWM pin	0	0	0	0	1	1	1	0	Original polarity of PWM signal	1	1	Inversed polarity of PWM signal			
BL	LEDPWMMPOL	LEDPWM pin																													
0	0	0																													
0	1	1																													
1	0	Original polarity of PWM signal																													
1	1	Inversed polarity of PWM signal																													
<b>LEDONPOL:</b> This bit is used to control LEDON pin.																															
<table border="1"> <thead> <tr> <th>BL</th> <th>LEDONPOL</th> <th>LEDON pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>LEDONR</td> </tr> <tr> <td>1</td> <td>1</td> <td>Inversed LEDONR</td> </tr> </tbody> </table>													BL	LEDONPOL	LEDON pin	0	0	0	0	1	1	1	0	LEDONR	1	1	Inversed LEDONR				
BL	LEDONPOL	LEDON pin																													
0	0	0																													
0	1	1																													
1	0	LEDONR																													
1	1	Inversed LEDONR																													
Register Availability	<b>LEDONR:</b> This bit is used to control LEDON pin.																														
	<table border="1"> <thead> <tr> <th>LEDONR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Low</td> </tr> <tr> <td>1</td> <td>High</td> </tr> </tbody> </table>													LEDONR	Description	0	Low	1	High												
LEDONR	Description																														
0	Low																														
1	High																														
<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
Partial Mode On, Idle Mode Off, Sleep Out	Yes																														
Partial Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In	Yes																														
<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>LEDONR</th> <th>LEDONPOL</th> <th>LEDPWMMPOL</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> <td>No change</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>1'b0</td> <td>1'b0</td> <td>1'b0</td> </tr> </tbody> </table>													Status	Default Value			LEDONR	LEDONPOL	LEDPWMMPOL	Power On Sequence	1'b0	1'b0	1'b0	SW Reset	No change	No change	No change	HW Reset	1'b0	1'b0	1'b0
Status	Default Value																														
	LEDONR	LEDONPOL	LEDPWMMPOL																												
Power On Sequence	1'b0	1'b0	1'b0																												
SW Reset	No change	No change	No change																												
HW Reset	1'b0	1'b0	1'b0																												

### 8.3.16. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h												
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0			VRH [5:0]				21												
<b>VRH [5:0]:</b> Set the GVDD level, which is a reference level for the VCOM level and the grayscale voltage level.																									
Description	VRH [5:0]				GVDD				VRH [5:0]				GVDD												
	0	0	0	0	0	0	Setting prohibited	1	0	0	0	0	4.45 V												
	0	0	0	0	0	1	Setting prohibited	1	0	0	0	1	4.50 V												
	0	0	0	0	1	0	Setting prohibited	1	0	0	0	1	4.55 V												
	0	0	0	0	1	1	3.00 V	1	0	0	0	1	4.60 V												
	0	0	0	1	0	0	3.05 V	1	0	0	1	0	4.65 V												
	0	0	0	1	0	1	3.10 V	1	0	0	1	0	4.70 V												
	0	0	0	1	1	0	3.15 V	1	0	0	1	1	4.75 V												
	0	0	0	1	1	1	3.20 V	1	0	0	1	1	4.80 V												
	0	0	1	0	0	0	3.25 V	1	0	1	0	0	4.85 V												
	0	0	1	0	0	1	3.30 V	1	0	1	0	1	4.90 V												
	0	0	1	0	1	0	3.35 V	1	0	1	0	1	4.95 V												
	0	0	1	0	1	1	3.40 V	1	0	1	0	1	5.00 V												
	0	0	1	1	0	0	3.45 V	1	0	1	1	0	5.05 V												
	0	0	1	1	0	1	3.50 V	1	0	1	1	0	5.10 V												
	0	0	1	1	1	0	3.55 V	1	0	1	1	1	5.15 V												
	0	0	1	1	1	1	3.60 V	1	0	1	1	1	5.20 V												
	0	1	0	0	0	0	3.65 V	1	1	0	0	0	5.25 V												
	0	1	0	0	0	1	3.70 V	1	1	0	0	1	5.30 V												
	0	1	0	0	1	0	3.75 V	1	1	0	0	1	5.35 V												
	0	1	0	0	1	1	3.80 V	1	1	0	0	1	5.40 V												
	0	1	0	1	0	0	3.85 V	1	1	0	1	0	5.45 V												
	0	1	0	1	0	1	3.90 V	1	1	0	1	0	5.50 V												
	0	1	0	1	1	0	3.95 V	1	1	0	1	1	5.55 V												
	0	1	0	1	1	1	4.00 V	1	1	0	1	1	5.60 V												
	0	1	1	0	0	0	4.05 V	1	1	1	0	0	5.65 V												
	0	1	1	0	0	1	4.10 V	1	1	1	0	0	5.70 V												
	0	1	1	0	1	0	4.15 V	1	1	1	0	1	5.75 V												
	0	1	1	0	1	1	4.20 V	1	1	1	0	1	5.80 V												
	0	1	1	1	0	0	4.25 V	1	1	1	1	0	5.85 V												
	0	1	1	1	0	1	4.30 V	1	1	1	1	0	5.90 V												
	0	1	1	1	1	0	4.35 V	1	1	1	1	1	5.95 V												
	0	1	1	1	1	1	4.40 V	1	1	1	1	1	6.00 V												
Note1: Make sure that VC and VRH setting restriction: $GVDD \leq (DDVDH - 0.2) V$ .																									
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
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Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th>Default Value</th> </tr> <tr> <th>VRH [5:0]</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>6'h21h</td> </tr> <tr> <td>SW Reset</td> <td>6'h21h</td> </tr> <tr> <td>HW Reset</td> <td>6'h21h</td> </tr> </tbody> </table>													Status	Default Value	VRH [5:0]	Power ON Sequence	6'h21h	SW Reset	6'h21h	HW Reset	6'h21h			
Status	Default Value																								
	VRH [5:0]																								
Power ON Sequence	6'h21h																								
SW Reset	6'h21h																								
HW Reset	6'h21h																								

**8.3.17. Power Control 2 (C1h)**

PWCTRL 2 (Power Control 2)																											
C1h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h														
Parameter	1	1	↑	XX	0	0	0	0	0	BT [2:0]			10														
<b>BT [2:0]:</b> Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>BT [2:0]</th> <th>DDVDH</th> <th>VGH</th> <th>VGL</th> </tr> <tr> <td>0 0 0</td> <td rowspan="4" style="text-align: center;">VCI x 2</td> <td rowspan="2" style="text-align: center;">VCI x 7</td> <td>-VCI x 4</td> </tr> <tr> <td>0 0 1</td> <td>-VCI x 3</td> </tr> <tr> <td>0 1 0</td> <td rowspan="2" style="text-align: center;">VCI x 6</td> <td>-VCI x 4</td> </tr> <tr> <td>0 1 1</td> <td>-VCI x 3</td> </tr> </table> <p><i>Note 1:</i> Make sure that DDVDH setting restriction: DDVDH <math>\leq</math> 5.8 V.  <i>2:</i> Make sure that VGH and VGL setting restriction: VGH -VGL <math>\leq</math> 28 V.</p>													BT [2:0]	DDVDH	VGH	VGL	0 0 0	VCI x 2	VCI x 7	-VCI x 4	0 0 1	-VCI x 3	0 1 0	VCI x 6	-VCI x 4	0 1 1	-VCI x 3
BT [2:0]	DDVDH	VGH	VGL																								
0 0 0	VCI x 2	VCI x 7	-VCI x 4																								
0 0 1			-VCI x 3																								
0 1 0		VCI x 6	-VCI x 4																								
0 1 1			-VCI x 3																								
Restriction	EXTC should be high to enable this command																										
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																										
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																										
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																										
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																										
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																										
Sleep IN	Yes																										
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>3'b000</td> </tr> <tr> <td>SW Reset</td> <td>3'b000</td> </tr> <tr> <td>HW Reset</td> <td>3'b000</td> </tr> </tbody> </table>													Status	Default Value	Power ON Sequence	3'b000	SW Reset	3'b000	HW Reset	3'b000						
Status	Default Value																										
Power ON Sequence	3'b000																										
SW Reset	3'b000																										
HW Reset	3'b000																										

**8.3.18. VCOM Control 1(C5h)**

C5h	VMCTRL1 (VCOM Control 1)													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h	
1 <sup>st</sup> Parameter	1	1	↑	XX	0				VMH [6:0]				31	
2 <sup>nd</sup> Parameter	1	1	↑	XX	0				VML [6:0]				3C	
VMH [6:0] : Set the VCOMH voltage.														
Description	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)
	0000000	2.700	0100000	3.500	1000000	4.300	1100000	5.100	1000001	4.325	1100001	5.125	1000010	5.150
	0000001	2.725	0100001	3.525	1000011	4.375	1100011	5.175	1000100	4.400	1100100	5.200	1100101	5.225
	0000010	2.750	0100010	3.550	1000101	4.425	1100110	5.250	1000110	4.450	1100111	5.275	1101000	5.300
	0000011	2.775	0100011	3.575	1000111	4.475	1101001	5.325	1001001	4.500	1101010	5.350	1101011	5.375
	0000100	2.800	0100100	3.600	1001010	4.550	1101100	5.400	1001011	4.575	1101110	5.450	1101111	5.475
	0000101	2.825	0100101	3.625	1001100	4.600	1101111	5.500	1010000	4.700	1110000	5.525	1110001	5.550
	0000110	2.850	0100110	3.650	1010001	4.725	1110001	5.550	1010010	4.750	1110011	5.575	1110100	5.600
	0000111	2.875	0100111	3.675	1010010	4.775	1110100	5.625	1010011	4.800	1110110	5.650	1110111	5.675
	0001000	2.900	0101000	3.700	1010100	4.825	1010110	4.850	1010111	4.875	1110111	5.700	1111000	5.725
	0001001	2.925	0101001	3.725	1011000	4.900	1011001	4.925	1011010	4.950	1111001	5.750	1111010	5.775
	0001010	2.950	0101010	3.750	1011010	4.975	1011011	5.000	1011100	5.025	1111100	5.800	1111101	5.825
	0001011	2.975	0101011	3.775	1011100	5.050	1011110	5.075	1011111		1111110	5.850	1111111	5.875
	0001100	3.000	0101100	3.800										
	0001101	3.025	0101101	3.825										
	0001110	3.050	0101110	3.850										
	0001111	3.075	0101111	3.875										
	0010000	3.100	0110000	3.900										
	0010001	3.125	0110001	3.925										
	0010010	3.150	0110010	3.950										
	0010011	3.175	0110011	3.975										
	0010100	3.200	0110100	4.000										
	0010101	3.225	0110101	4.025										
	0010110	3.250	0110110	4.050										
	0010111	3.275	0110111	4.075										
	0011000	3.300	0111000	4.100										
	0011001	3.325	0111001	4.125										
	0011010	3.350	0111010	4.150										
	0011011	3.375	0111011	4.175										
	0011100	3.400	0111100	4.200										
	0011101	3.425	0111101	4.225										
	0011110	3.450	0111110	4.250										
	0011111	3.475	0111111	4.275										
VML [6:0] : Set the VCOML voltage														
Description	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)
	0000000	-2.500	0100000	-1.700	1000000	-0.900	1100000	-0.100	1000001	-0.875	1100001	-0.075	1000010	-0.850
	0000001	-2.475	0100001	-1.675	1000011	-0.825	1100011	-0.025	1000100	-0.800	1100100	0	1000101	Reserved
	0000010	-2.450	0100010	-1.650	1000110	-0.775	1100110	Reserved	1000111	-0.750	1100111	Reserved	1010000	Reserved
	0000011	-2.425	0100011	-1.625	1001000	-0.725	1101000	Reserved	1001001	-0.700	1101001	Reserved	1001010	-0.675
	0000100	-2.400	0100100	-1.600	1001011	-0.650	1101011	Reserved	1001100	-0.625	1101100	Reserved	1001110	-0.600
	0000101	-2.375	0100101	-1.575	1001111	-0.575	1101111	Reserved	1010000	-0.550	1101110	Reserved	1010001	-0.525
	0000110	-2.350	0100110	-1.550	1010001	-0.475	1101101	Reserved	1010010	-0.450	1101111	Reserved	1010011	-0.425
	0000111	-2.325	0100111	-1.525	1010100	-0.425	1110000	Reserved	1010110	-0.400	1110001	Reserved	1010111	-0.375
	0001000	-2.300	0101000	-1.500	1010111	-0.375	1110100	Reserved	1011000	-0.350	1110101	Reserved	1011010	-0.325
	0001001	-2.275	0101001	-1.475	1011000	-0.325	1111000	Reserved	1011011	-0.300	1111001	Reserved	1011012	-0.275
	0001010	-2.250	0101010	-1.450	1011011	-0.275	1111100	Reserved	1011100	-0.250	1111101	Reserved	1011110	-0.225
	0001011	-2.225	0101011	-1.425	1011100	-0.225	1111110	Reserved	1011111	-0.200	1111111	Reserved		
	0001100	-2.200	0101100	-1.400	1011111	-0.200								
	0001101	-2.175	0101101	-1.375										
	0001110	-2.150	0101110	-1.350										
	0001111	-2.125	0101111	-1.325										
	0010000	-2.100	0110000	-1.300										
	0010001	-2.075	0110001	-1.275										
	0010010	-2.050	0110010	-1.250										
	0010011	-2.025	0110011	-1.225										

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	0010100	-2.000	0110100	-1.200	1010100	-0.400	1110100	Reserved															
	0010101	-1.975	0110101	-1.175	1010101	-0.375	1110101	Reserved															
	0010110	-1.950	0110110	-1.150	1010110	-0.350	1110110	Reserved															
	0010111	-1.925	0110111	-1.125	1010111	-0.325	1110111	Reserved															
	0011000	-1.900	0111000	-1.100	1011000	-0.300	1111000	Reserved															
	0011001	-1.875	0111001	-1.075	1011001	-0.275	1111001	Reserved															
	0011010	-1.850	0111010	-1.050	1011010	-0.250	1111010	Reserved															
	0011011	-1.825	0111011	-1.025	1011011	-0.225	1111011	Reserved															
	0011100	-1.800	0111100	-1.000	1011100	-0.200	1111100	Reserved															
	0011101	-1.775	0111101	-0.975	1011101	-0.175	1111101	Reserved															
	0011110	-1.750	0111110	-0.950	1011110	-0.150	1111110	Reserved															
	0011111	-1.725	0111111	-0.925	1011111	-0.125	1111111	Reserved															
Restriction	EXTC should be high to enable this command																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>									Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																						
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																						
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																						
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																						
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																						
Sleep IN	Yes																						
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>VMH [6:0]</th> <th>VML [6:0]</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>7'h31</td> <td>7'h3C</td> </tr> <tr> <td>SW Reset</td> <td>7'h31</td> <td>7'h3C</td> </tr> <tr> <td>HW Rest</td> <td>7'h31</td> <td>7'h3C</td> </tr> </tbody> </table>									Status	Default Value		VMH [6:0]	VML [6:0]	Power ON Sequence	7'h31	7'h3C	SW Reset	7'h31	7'h3C	HW Rest	7'h31	7'h3C
Status	Default Value																						
	VMH [6:0]	VML [6:0]																					
Power ON Sequence	7'h31	7'h3C																					
SW Reset	7'h31	7'h3C																					
HW Rest	7'h31	7'h3C																					

### 8.3.19. VCOM Control 2(C7h)

C7h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
Parameter	1	1	↑	XX	nVM				VMF [6:0]				C0
<b>nVM:</b> nVM equals to "0" after power on reset and VCOM offset equals to program MTP value. When nVM set to "1", setting of VMF [6:0] becomes valid and VCOMH/VCOML can be adjusted.													
<b>VMF [6:0]:</b> Set the VCOM offset voltage.													
Description	VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML	VMF[6:0]
	0000000	VMH	VML	1000000	VMH	VML	1000000	VMH	VML	1000000	VMH	VML	1000000
	0000001	VMH - 63	VML - 63	1000001	VMH + 1	VML + 1	1000001	VMH + 1	VML + 1	1000001	VMH + 1	VML + 1	1000001
	0000010	VMH - 62	VML - 62	1000010	VMH + 2	VML + 2	1000010	VMH + 2	VML + 2	1000010	VMH + 2	VML + 2	1000010
	0000011	VMH - 61	VML - 61	1000011	VMH + 3	VML + 3	1000011	VMH + 3	VML + 3	1000011	VMH + 3	VML + 3	1000011
	0000100	VMH - 60	VML - 60	1000100	VMH + 4	VML + 4	1000100	VMH + 4	VML + 4	1000100	VMH + 4	VML + 4	1000100
	0000101	VMH - 58	VML - 58	1000101	VMH + 5	VML + 5	1000101	VMH + 5	VML + 5	1000101	VMH + 5	VML + 5	1000101
	0000110	VMH - 58	VML - 58	1000110	VMH + 6	VML + 6	1000110	VMH + 6	VML + 6	1000110	VMH + 6	VML + 6	1000110
	0000111	VMH - 57	VML - 57	1000111	VMH + 7	VML + 7	1000111	VMH + 7	VML + 7	1000111	VMH + 7	VML + 7	1000111
	0001000	VMH - 56	VML - 56	1001000	VMH + 8	VML + 8	1001000	VMH + 8	VML + 8	1001000	VMH + 8	VML + 8	1001000
	0001001	VMH - 55	VML - 55	1001001	VMH + 9	VML + 9	1001001	VMH + 9	VML + 9	1001001	VMH + 9	VML + 9	1001001
	0001010	VMH - 54	VML - 54	1001010	VMH + 10	VML + 10	1001010	VMH + 10	VML + 10	1001010	VMH + 10	VML + 10	1001010
	0001011	VMH - 53	VML - 53	1001011	VMH + 11	VML + 11	1001011	VMH + 11	VML + 11	1001011	VMH + 11	VML + 11	1001011
	0001100	VMH - 52	VML - 52	1001100	VMH + 12	VML + 12	1001100	VMH + 12	VML + 12	1001100	VMH + 12	VML + 12	1001100
	0001101	VMH - 51	VML - 51	1001101	VMH + 13	VML + 13	1001101	VMH + 13	VML + 13	1001101	VMH + 13	VML + 13	1001101
	0001110	VMH - 50	VML - 50	1001110	VMH + 14	VML + 14	1001110	VMH + 14	VML + 14	1001110	VMH + 14	VML + 14	1001110
	0001111	VMH - 49	VML - 49	1001111	VMH + 15	VML + 15	1001111	VMH + 15	VML + 15	1001111	VMH + 15	VML + 15	1001111
	0010000	VMH - 48	VML - 48	1010000	VMH + 16	VML + 16	1010000	VMH + 16	VML + 16	1010000	VMH + 16	VML + 16	1010000
	0010001	VMH - 47	VML - 47	1010001	VMH + 17	VML + 17	1010001	VMH + 17	VML + 17	1010001	VMH + 17	VML + 17	1010001
	0010010	VMH - 46	VML - 46	1010010	VMH + 18	VML + 18	1010010	VMH + 18	VML + 18	1010010	VMH + 18	VML + 18	1010010
	0010011	VMH - 45	VML - 45	1010011	VMH + 19	VML + 19	1010011	VMH + 19	VML + 19	1010011	VMH + 19	VML + 19	1010011
	0010100	VMH - 44	VML - 44	1010100	VMH + 20	VML + 20	1010100	VMH + 20	VML + 20	1010100	VMH + 20	VML + 20	1010100
	0010101	VMH - 43	VML - 43	1010101	VMH + 21	VML + 21	1010101	VMH + 21	VML + 21	1010101	VMH + 21	VML + 21	1010101
	0010110	VMH - 42	VML - 42	1010110	VMH + 22	VML + 22	1010110	VMH + 22	VML + 22	1010110	VMH + 22	VML + 22	1010110
	0010111	VMH - 41	VML - 41	1010111	VMH + 23	VML + 23	1010111	VMH + 23	VML + 23	1010111	VMH + 23	VML + 23	1010111
	0011000	VMH - 40	VML - 40	1011000	VMH + 24	VML + 24	1011000	VMH + 24	VML + 24	1011000	VMH + 24	VML + 24	1011000
	0011001	VMH - 39	VML - 39	1011001	VMH + 25	VML + 25	1011001	VMH + 25	VML + 25	1011001	VMH + 25	VML + 25	1011001
	0011010	VMH - 38	VML - 38	1011010	VMH + 26	VML + 26	1011010	VMH + 26	VML + 26	1011010	VMH + 26	VML + 26	1011010
	0011011	VMH - 37	VML - 37	1011011	VMH + 27	VML + 27	1011011	VMH + 27	VML + 27	1011011	VMH + 27	VML + 27	1011011
	0011100	VMH - 36	VML - 36	1011100	VMH + 28	VML + 28	1011100	VMH + 28	VML + 28	1011100	VMH + 28	VML + 28	1011100
	0011101	VMH - 35	VML - 35	1011101	VMH + 29	VML + 29	1011101	VMH + 29	VML + 29	1011101	VMH + 29	VML + 29	1011101
	0011110	VMH - 34	VML - 34	1011110	VMH + 30	VML + 30	1011110	VMH + 30	VML + 30	1011110	VMH + 30	VML + 30	1011110
	0011111	VMH - 33	VML - 33	1011111	VMH + 31	VML + 31	1011111	VMH + 31	VML + 31	1011111	VMH + 31	VML + 31	1011111
	0100000	VMH - 32	VML - 32	1100000	VMH + 32	VML + 32	1100000	VMH + 32	VML + 32	1100000	VMH + 32	VML + 32	1100000
	0100001	VMH - 31	VML - 31	1100001	VMH + 33	VML + 33	1100001	VMH + 33	VML + 33	1100001	VMH + 33	VML + 33	1100001
	0100010	VMH - 30	VML - 30	1100010	VMH + 34	VML + 34	1100010	VMH + 34	VML + 34	1100010	VMH + 34	VML + 34	1100010
	0100011	VMH - 29	VML - 29	1100011	VMH + 35	VML + 35	1100011	VMH + 35	VML + 35	1100011	VMH + 35	VML + 35	1100011
	0100100	VMH - 28	VML - 28	1100100	VMH + 36	VML + 36	1100100	VMH + 36	VML + 36	1100100	VMH + 36	VML + 36	1100100
	0100101	VMH - 27	VML - 27	1100101	VMH + 37	VML + 37	1100101	VMH + 37	VML + 37	1100101	VMH + 37	VML + 37	1100101
	0100110	VMH - 26	VML - 26	1100110	VMH + 38	VML + 38	1100110	VMH + 38	VML + 38	1100110	VMH + 38	VML + 38	1100110
	0100111	VMH - 25	VML - 25	1100111	VMH + 39	VML + 39	1100111	VMH + 39	VML + 39	1100111	VMH + 39	VML + 39	1100111
	0101000	VMH - 24	VML - 24	1101000	VMH + 40	VML + 40	1101000	VMH + 40	VML + 40	1101000	VMH + 40	VML + 40	1101000
	0101001	VMH - 23	VML - 23	1101001	VMH + 41	VML + 41	1101001	VMH + 41	VML + 41	1101001	VMH + 41	VML + 41	1101001
	0101010	VMH - 22	VML - 22	1101010	VMH + 42	VML + 42	1101010	VMH + 42	VML + 42	1101010	VMH + 42	VML + 42	1101010
	0101011	VMH - 21	VML - 21	1101011	VMH + 43	VML + 43	1101011	VMH + 43	VML + 43	1101011	VMH + 43	VML + 43	1101011
	0101100	VMH - 20	VML - 20	1101100	VMH + 44	VML + 44	1101100	VMH + 44	VML + 44	1101100	VMH + 44	VML + 44	1101100
	0101101	VMH - 19	VML - 19	1101101	VMH + 45	VML + 45	1101101	VMH + 45	VML + 45	1101101	VMH + 45	VML + 45	1101101
	0101110	VMH - 18	VML - 18	1101110	VMH + 46	VML + 46	1101110	VMH + 46	VML + 46	1101110	VMH + 46	VML + 46	1101110
	0101111	VMH - 17	VML - 17	1101111	VMH + 47	VML + 47	1101111	VMH + 47	VML + 47	1101111	VMH + 47	VML + 47	1101111
	0110000	VMH - 16	VML - 16	1110000	VMH + 48	VML + 48	1110000	VMH + 48	VML + 48	1110000	VMH + 48	VML + 48	1110000
	0110001	VMH - 15	VML - 15	1110001	VMH + 49	VML + 49	1110001	VMH + 49	VML + 49	1110001	VMH + 49	VML + 49	1110001
	0110010	VMH - 14	VML - 14	1110010	VMH + 50	VML + 50	1110010	VMH + 50	VML + 50	1110010	VMH + 50	VML + 50	1110010
	0110011	VMH - 13	VML - 13	1110011	VMH + 51	VML + 51	1110011	VMH + 51	VML + 51	1110011	VMH + 51	VML + 51	1110011
	0110100	VMH - 12	VML - 12	1110100	VMH + 52	VML + 52	1110100	VMH + 52	VML + 52	1110100	VMH + 52	VML + 52	1110100

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		0110101	VMH - 11	VML - 11	1110101	VMH + 53	VML + 53															
		0110110	VMH - 10	VML - 10	1110110	VMH + 54	VML + 54															
		0110111	VMH - 9	VML - 9	1110111	VMH + 55	VML + 55															
		0111000	VMH - 8	VML - 8	1111000	VMH + 56	VML + 56															
		0111001	VMH - 7	VML - 7	1111001	VMH + 57	VML + 57															
		0111010	VMH - 6	VML - 6	1111010	VMH + 58	VML + 58															
		0111011	VMH - 5	VML - 5	1111011	VMH + 59	VML + 59															
		0111100	VMH - 4	VML - 4	1111100	VMH + 60	VML + 60															
		0111101	VMH - 3	VML - 3	1111101	VMH + 61	VML + 61															
		0111110	VMH - 2	VML - 2	1111110	VMH + 62	VML + 62															
		0111111	VMH - 1	VML - 1	1111111	VMH + 63	VML + 63															
Restriction		EXTC should be high to enable this command																				
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>							Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																					
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																					
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																					
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																					
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																					
Sleep IN	Yes																					
Default		<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>nVM</th> <th>VMF [6:0]</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>1'b1</td> <td>7'h40h</td> </tr> <tr> <td>SW Reset</td> <td>1'b1</td> <td>7'h40h</td> </tr> <tr> <td>HW Reset</td> <td>1'b1</td> <td>7'h40h</td> </tr> </tbody> </table>							Status	Default Value		nVM	VMF [6:0]	Power ON Sequence	1'b1	7'h40h	SW Reset	1'b1	7'h40h	HW Reset	1'b1	7'h40h
Status	Default Value																					
	nVM	VMF [6:0]																				
Power ON Sequence	1'b1	7'h40h																				
SW Reset	1'b1	7'h40h																				
HW Reset	1'b1	7'h40h																				

### 8.3.20. NV Memory Write (D0h)

NVMWR (NV Memory Write)																											
D0h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h														
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	0	PGM_ADR [2:0]	00																
2 <sup>nd</sup> Parameter	1	1	↑	XX	PGM_DATA [7:0]								XX														
Description	This command is used to program the NV memory data. After a successful MTP operation, the information of PGM_DATA [7:0] will be programmed to NV memory.  <b>PGM_ADR [2:0]:</b> The select bits of ID1, ID2, ID3 and VMF [6:0] programming can be OTP x 3 times.																										
	<table border="1"> <tr> <td>PGM_ADR [2:0]</td> <td>Programmed NV Memory Selection</td> </tr> <tr> <td>0 0 0</td> <td>ID1 programming</td> </tr> <tr> <td>0 0 1</td> <td>ID2 programming</td> </tr> <tr> <td>0 1 0</td> <td>ID3 programming</td> </tr> <tr> <td>1 0 0</td> <td>VMF [6:0] programming</td> </tr> <tr> <td>Others</td> <td>Reserved</td> </tr> </table> <b>PGM_DATA [7:0]:</b> The programmed data.													PGM_ADR [2:0]	Programmed NV Memory Selection	0 0 0	ID1 programming	0 0 1	ID2 programming	0 1 0	ID3 programming	1 0 0	VMF [6:0] programming	Others	Reserved		
PGM_ADR [2:0]	Programmed NV Memory Selection																										
0 0 0	ID1 programming																										
0 0 1	ID2 programming																										
0 1 0	ID3 programming																										
1 0 0	VMF [6:0] programming																										
Others	Reserved																										
Restriction	EXTC should be high to enable this command																										
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																										
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																										
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																										
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																										
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																										
Sleep IN	Yes																										
Default	<table border="1"> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>PGM_ADR [2:0]</th> <th>PGM_DATA [7:0]</th> </tr> <tr> <td>Power ON Sequence</td> <td>3'b000</td> <td>MTP value</td> </tr> <tr> <td>SW Reset</td> <td>3'b000</td> <td>MTP value</td> </tr> <tr> <td>HW Reset</td> <td>3'b000</td> <td>MTP value</td> </tr> </table>													Status	Default Value		PGM_ADR [2:0]	PGM_DATA [7:0]	Power ON Sequence	3'b000	MTP value	SW Reset	3'b000	MTP value	HW Reset	3'b000	MTP value
Status	Default Value																										
	PGM_ADR [2:0]	PGM_DATA [7:0]																									
Power ON Sequence	3'b000	MTP value																									
SW Reset	3'b000	MTP value																									
HW Reset	3'b000	MTP value																									

### 8.3.21. NV Memory Protection Key (D1h)

D1h		NVMPKEY (NV Memory Protection Key)																								
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command		0	1	↑	XX	1	1	0	1	0	0	0	1	D1h												
1 <sup>st</sup> Parameter		1	1	↑	XX					KEY [23:16]				55h												
2 <sup>nd</sup> Parameter		1	1	↑	XX					KEY [15:8]				AAh												
3 <sup>rd</sup> Parameter		1	1	↑	XX					KEY [7:0]				66h												
Description	<b>KEY [23:0]:</b> NV memory programming protection key. When writing MTP data to D1h, this register must be set to 0x55AA66h to enable MTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.																									
Restriction	EXTC should be high to enable this command																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes	
Status	Availability																									
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																									
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																									
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																									
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																									
Sleep IN	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>KEY [23:0]=55AA66h</td> </tr> <tr> <td>SW Reset</td> <td>KEY [23:0]=55AA66h</td> </tr> <tr> <td>HW Reset</td> <td>KEY [23:0]=55AA66h</td> </tr> </tbody> </table>													Status	Default Value	Power ON Sequence	KEY [23:0]=55AA66h	SW Reset	KEY [23:0]=55AA66h	HW Reset	KEY [23:0]=55AA66h					
Status	Default Value																									
Power ON Sequence	KEY [23:0]=55AA66h																									
SW Reset	KEY [23:0]=55AA66h																									
HW Reset	KEY [23:0]=55AA66h																									

### 8.3.22. NV Memory Status Read (D2h)

D2h	RDNVM (NV Memory Status Read)																																										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																														
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h																														
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X																														
2 <sup>nd</sup> Parameter	1	↑	1	XX	0	ID2_CNT [2:0]			0	ID1_CNT [2:0]			XX																														
3 <sup>rd</sup> Parameter	1	↑	1	XX	BUSY	VMF_CNT [2:0]			0	ID3_CNT [2:0]			XX																														
Description	<b>ID1_CNT [2:0] / ID2_CNT [2:0] / ID3_CNT [2:0] / VMF_CNT [2:0]:</b> ID and VMF all can be OPT x 3 times, NV memory program record. The bits will increase “+1” automatically after writing the PGM_DATA [7:0] to NV memory.																																										
	<table border="1"> <thead> <tr> <th colspan="3">ID1_CNT [2:0] / ID2_CNT [2:0] ID3_CNT [2:0] / VMF_CNT [2:0]</th> <th>Description</th> </tr> <tr> <th colspan="3">Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>No Programmed</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>Programmed 1 time</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>Programmed 2 times</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>Programmed 3 times</td></tr> </tbody> </table> <p><b>BUSY:</b> The status bit of NV memory programming.</p> <table border="1"> <thead> <tr> <th>BUSY</th> <th>The Status of NV Memory</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Idle</td> </tr> <tr> <td>1</td> <td>Busy</td> </tr> </tbody> </table>													ID1_CNT [2:0] / ID2_CNT [2:0] ID3_CNT [2:0] / VMF_CNT [2:0]			Description	Status			Availability	0	0	0	No Programmed	0	0	1	Programmed 1 time	0	1	1	Programmed 2 times	1	1	1	Programmed 3 times	BUSY	The Status of NV Memory	0	Idle	1	Busy
ID1_CNT [2:0] / ID2_CNT [2:0] ID3_CNT [2:0] / VMF_CNT [2:0]			Description																																								
Status			Availability																																								
0	0	0	No Programmed																																								
0	0	1	Programmed 1 time																																								
0	1	1	Programmed 2 times																																								
1	1	1	Programmed 3 times																																								
BUSY	The Status of NV Memory																																										
0	Idle																																										
1	Busy																																										
Restriction	EXTC should be high to enable this command																																										
Register Availability	<table border="1"> <thead> <tr> <th colspan="3">Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Sleep IN</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Sleep IN</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Sleep IN</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Sleep IN</td> <td>Yes</td> <td></td> <td></td> </tr> </tbody> </table>													Status			Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Normal Mode ON, Idle Mode ON, Sleep OUT	Partial Mode ON, Idle Mode OFF, Sleep OUT	Partial Mode ON, Idle Mode ON, Sleep OUT	Sleep IN	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Partial Mode ON, Idle Mode OFF, Sleep OUT	Partial Mode ON, Idle Mode ON, Sleep OUT	Sleep IN	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Partial Mode ON, Idle Mode ON, Sleep OUT	Sleep IN	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Sleep IN	Yes								
Status			Availability																																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Normal Mode ON, Idle Mode ON, Sleep OUT	Partial Mode ON, Idle Mode OFF, Sleep OUT	Partial Mode ON, Idle Mode ON, Sleep OUT	Sleep IN	Yes																																						
Normal Mode ON, Idle Mode ON, Sleep OUT	Partial Mode ON, Idle Mode OFF, Sleep OUT	Partial Mode ON, Idle Mode ON, Sleep OUT	Sleep IN	Yes																																							
Partial Mode ON, Idle Mode OFF, Sleep OUT	Partial Mode ON, Idle Mode ON, Sleep OUT	Sleep IN	Yes																																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Sleep IN	Yes																																									
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="5">Default Value</th> </tr> <tr> <th>ID3_CNT</th> <th>ID2_CNT</th> <th>ID1_CNT</th> <th>VMF_CNT</th> <th>BUSY</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>SW Reset</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>HW Reset</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> </tbody> </table>													Status	Default Value					ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY	Power ON Sequence	X	X	X	X	X	SW Reset	X	X	X	X	X	HW Reset	X	X	X	X	X	
Status	Default Value																																										
	ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY																																						
Power ON Sequence	X	X	X	X	X																																						
SW Reset	X	X	X	X	X																																						
HW Reset	X	X	X	X	X																																						

**8.3.23. Read ID4 (D3h)**

D3h	RDID4 (Read ID4)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h												
1 <sup>st</sup> Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00h												
3 <sup>rd</sup> Parameter	1	↑	1	XX	1	0	0	1	0	0	1	1	93h												
4 <sup>th</sup> Parameter	1	↑	1	XX	0	1	0	0	0	0	0	1	41h												
Description	Read IC device code. The 1 <sup>st</sup> parameter is dummy read period. The 2 <sup>nd</sup> parameter means the IC version. The 3 <sup>rd</sup> and 4 <sup>th</sup> parameter mean the IC model name.																								
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>24'h009341h</td></tr> <tr> <td>SW Reset</td><td>24'h009341h</td></tr> <tr> <td>HW Reset</td><td>24'h009341h</td></tr> </tbody> </table>													Status	Default Value	Power ON Sequence	24'h009341h	SW Reset	24'h009341h	HW Reset	24'h009341h				
Status	Default Value																								
Power ON Sequence	24'h009341h																								
SW Reset	24'h009341h																								
HW Reset	24'h009341h																								

### 8.3.24. Positive Gamma Correction (E0h)

E0h		PGAMCTRL (Positive Gamma Control)																								
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command		0	1	↑	XX	1	1	1	0	0	0	0	0	E0h												
1 <sup>st</sup> Parameter		1	1	↑	XX	0	0	0	0	VP63 [3:0]				08												
2 <sup>nd</sup> Parameter		1	1	↑	XX	0	0	VP62 [5:0]																		
3 <sup>rd</sup> Parameter		1	1	↑	XX	0	0	VP61 [5:0]																		
4 <sup>th</sup> Parameter		1	1	↑	X	0	0	0	0	VP59 [3:0]				05												
5 <sup>th</sup> Parameter		1	1	↑	XX	0	0	0	0	VP57 [4:0]																
6 <sup>th</sup> Parameter		1	1	↑	XX	0	0	0	0	VP50 [3:0]				09												
7 <sup>th</sup> Parameter		1	1	↑	XX	0	VP43 [6:0]																			
8 <sup>th</sup> Parameter		1	1	↑	XX	VP27 [3:0]				VP36 [3:0]																
9 <sup>th</sup> Parameter		1	1	↑	XX	0	VP20 [6:0]																			
10 <sup>th</sup> Parameter		1	1	↑	XX	0	0	0	0	VP13 [3:0]				0B												
11 <sup>th</sup> Parameter		1	1	↑	XX	0	0	0	0	VP6 [4:0]																
12 <sup>th</sup> Parameter		1	1	↑	XX	0	0	0	0	VP4 [3:0]				00												
13 <sup>th</sup> Parameter		1	1	↑	XX	0	0	VP2 [5:0]																		
14 <sup>th</sup> Parameter		1	1	↑	XX	0	0	VP1 [5:0]																		
15 <sup>th</sup> Parameter		1	1	↑	XX	0	0	0	0	VP0 [3:0]				00												
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.																									
Restriction	EXTC should be high to enable this command																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes	
Status	Availability																									
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																									
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																									
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																									
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																									
Sleep IN	Yes																									
Default																										

**8.3.25. Negative Gamma Correction (E1h)**

NGAMCTRL (Negative Gamma Correction)																									
E1h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h												
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	VN63 [3:0]					08											
2 <sup>nd</sup> Parameter	1	1	↑	XX	0	0	VN62 [5:0]																		
3 <sup>rd</sup> Parameter	1	1	↑	XX	0	0	VN61 [5:0]																		
4 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0	0	VN59 [3:0]					07											
5 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0	0	VN57 [4:0]																
6 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0	0	VN50 [3:0]					05											
7 <sup>th</sup> Parameter	1	1	↑	XX	0	VN43 [6:0]																			
8 <sup>th</sup> Parameter	1	1	↑	XX	VN36 [3:0]					VN27 [3:0]															
9 <sup>th</sup> Parameter	1	1	↑	XX	0	VN20 [6:0]																			
10 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0	0	VN13 [3:0]					04											
11 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0	0	VN6 [4:0]																
12 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0	0	VN4 [3:0]					0F											
13 <sup>th</sup> Parameter	1	1	↑	XX	0	0	VN2 [5:0]																		
14 <sup>th</sup> Parameter	1	1	↑	XX	0	0	VN1 [5:0]																		
15 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0	0	VN0 [3:0]					0F											
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.																								
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default																									

### 8.3.26. Digital Gamma Control 1 (E2h)

E2h		DGAMCTRL (Digital Gamma Control 1)																										
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command		0	1	↑	XX	1	1	1	0	0	0	1	0	E2h														
1 <sup>st</sup> Parameter		1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				XX														
:		1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				XX														
16 <sup>th</sup> Parameter		1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]				XX														
Description	<b>RCAx [3:0]:</b> Gamma Macro-adjustment registers for red gamma curve. <b>BCAx [3:0]:</b> Gamma Macro-adjustment registers for blue gamma curve.																											
Restriction	EXTC should be high to enable this command																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes			
Status	Availability																											
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																											
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Sleep IN	Yes																											
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>RCAx [3:0]</th> <th>BCAx [3:0]</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>TBD</td> <td>TBD</td> </tr> <tr> <td>SW Reset</td> <td>TBD</td> <td>TBD</td> </tr> <tr> <td>HW Reset</td> <td>TBD</td> <td>TBD</td> </tr> </tbody> </table>													Status	Default Value		RCAx [3:0]	BCAx [3:0]	Power ON Sequence	TBD	TBD	SW Reset	TBD	TBD	HW Reset	TBD	TBD	
Status	Default Value																											
	RCAx [3:0]	BCAx [3:0]																										
Power ON Sequence	TBD	TBD																										
SW Reset	TBD	TBD																										
HW Reset	TBD	TBD																										

### 8.3.27. Digital Gamma Control 2(E3h)

E3h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h																		
1 <sup>st</sup> Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				XX																		
:	1	1	↑	XX	RFAX [3:0]				BFAX [3:0]				XX																		
64 <sup>rd</sup> Parameter	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]				XX																		
Description	<b>RFAX [3:0]:</b> Gamma Micro-adjustment register for red gamma curve. <b>BFAX [3:0]:</b> Gamma Micro-adjustment register for blue gamma curve.																														
Restriction	EXTC should be high to enable this command																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td colspan="2">Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td colspan="2">Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td colspan="2">Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td colspan="2">Yes</td> </tr> <tr> <td>Sleep IN</td> <td colspan="2">Yes</td> </tr> </tbody> </table>													Status	Availability		Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes		Normal Mode ON, Idle Mode ON, Sleep OUT	Yes		Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes		Partial Mode ON, Idle Mode ON, Sleep OUT	Yes		Sleep IN	Yes	
Status	Availability																														
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																														
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																														
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																														
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																														
Sleep IN	Yes																														
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>RFAX [3:0]</th> <th>BFAX [3:0]</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>TBD</td> <td>TBD</td> </tr> <tr> <td>SW Reset</td> <td>TBD</td> <td>TBD</td> </tr> <tr> <td>HW Reset</td> <td>TBD</td> <td>TBD</td> </tr> </tbody> </table>													Status	Default Value		RFAX [3:0]	BFAX [3:0]	Power ON Sequence	TBD	TBD	SW Reset	TBD	TBD	HW Reset	TBD	TBD				
Status	Default Value																														
	RFAX [3:0]	BFAX [3:0]																													
Power ON Sequence	TBD	TBD																													
SW Reset	TBD	TBD																													
HW Reset	TBD	TBD																													

### 8.3.28. Interface Control (F6h)

F6h	IFCTL (16bits Data Format Selection)																										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h														
1 <sup>st</sup> Parameter	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	0	BGR_EOR	0	0	WE MODE	01														
2 <sup>nd</sup> Parameter	1	1	↑	XX	0	0	EPF [1]	EPF [0]	0	0	MDT [1]	MDT [0]	00														
3 <sup>rd</sup> Parameter	1	1	↑	XX	0	0	ENDIAN	0	DM [1]	DM [0]	RM	RIM	00														
Description	<b>MY_EOR / MX_EOR / MV_EOR / BGR_EOR:</b>  The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.  <b>MDT [1:0]:</b> Select the method of display data transferring.  <b>WEMODE:</b> Memory write control  WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.  <b>ENDIAN:</b> Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.																										
	<table border="1"> <thead> <tr> <th>ENDIAN</th> <th>Data transfer Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal (MSB first, default)</td> </tr> <tr> <td>1</td> <td>Little Endian (LSB first)</td> </tr> </tbody> </table>													ENDIAN	Data transfer Mode	0	Normal (MSB first, default)	1	Little Endian (LSB first)								
ENDIAN	Data transfer Mode																										
0	Normal (MSB first, default)																										
1	Little Endian (LSB first)																										
Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.																											
<p>The diagram illustrates the data flow for a 16-bit display. It shows two transfers: the 1st transfer (Lower byte) and the 2nd transfer (Upper byte). The input data bytes DB[7] to DB[0] are processed in pairs. The first pair (DB[7], DB[6]) becomes R4 and G5. The second pair (DB[5], DB[4]) becomes R0 and G3. The third pair (DB[3], DB[2]) becomes B4 and G2. The fourth pair (DB[1], DB[0]) becomes B0 and G1. The fifth pair (DB[7], DB[6]) becomes R2 and G4. The sixth pair (DB[5], DB[4]) becomes R1 and G3. The seventh pair (DB[3], DB[2]) becomes B2 and G0. The eighth pair (DB[1], DB[0]) becomes B1 and G0.</p>																											
<b>DM [1:0]:</b> Select the display operation mode.																											
<table border="1"> <thead> <tr> <th>DM [1]</th> <th>DM [0]</th> <th>Display Operation Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Internal clock operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>RGB Interface Mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>VSYNC interface mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting disabled</td> </tr> </tbody> </table>													DM [1]	DM [0]	Display Operation Mode	0	0	Internal clock operation	0	1	RGB Interface Mode	1	0	VSYNC interface mode	1	1	Setting disabled
DM [1]	DM [0]	Display Operation Mode																									
0	0	Internal clock operation																									
0	1	RGB Interface Mode																									
1	0	VSYNC interface mode																									
1	1	Setting disabled																									
The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface mode is prohibited.																											

**RM:** Select the interface to access the GRAM.

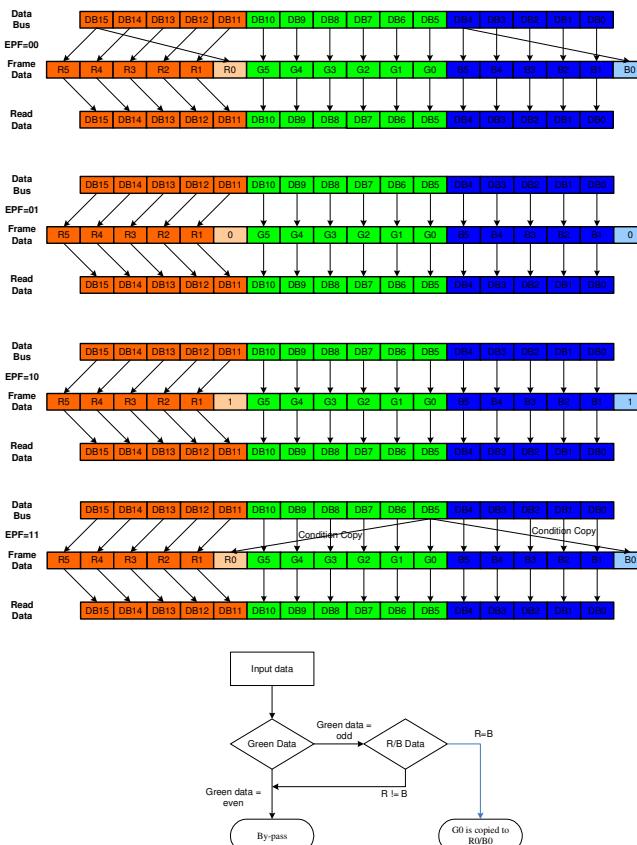
Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

**RIM:** Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

**EPF [1:0]:** 65K color mode data format.



		EPF [1:0]	Expand 16 bbp (R,G,B) to 18bbp (R,G,B)																																												
		00	MSB is inputted to LSB r [5:0] = {R [4:0], R [4]} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], B [4]}																																												
		01	'0" is inputted to LSB r [5:0] = {R [4:0], 0} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 0}  Exception: R [4:0], B[4:0] = 5'h1F → r [5:0], b[5:0] = 6'h3F																																												
		10	'1" is inputted to LSB r [5:0] = {R [4:0], 1} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 1}  Exception: R [4:0], B[4:0] = 5'h00 → r [5:0], b[5:0] = 6'h00																																												
		11	Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]} Case 2: R=B≠G → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 3: R=G≠B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]}																																												
Restriction	EXTC should be high to enable this command																																														
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Sleep IN	Yes																																														
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="7">Default Value</th> </tr> <tr> <th>EPF [1:0]</th> <th>MDT [1:0]</th> <th>ENDIAN</th> <th>WEMODE</th> <th>DM [1:0]</th> <th>RM</th> <th>RIM</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>2'b00</td> <td>2'b00</td> <td>1'b0</td> <td>1'b1</td> <td>2'b00</td> <td>1'b0</td> <td>1'b0</td> </tr> <tr> <td>SW Reset</td> <td>2'b00</td> <td>2'b00</td> <td>1'b0</td> <td>1'b1</td> <td>2'b00</td> <td>1'b0</td> <td>1'b0</td> </tr> <tr> <td>HW Reset</td> <td>2'b00</td> <td>2'b00</td> <td>1'b0</td> <td>1'b1</td> <td>2'b00</td> <td>1'b0</td> <td>1'b0</td> </tr> </tbody> </table>								Status	Default Value							EPF [1:0]	MDT [1:0]	ENDIAN	WEMODE	DM [1:0]	RM	RIM	Power ON Sequence	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0	SW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0	HW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0
Status	Default Value																																														
	EPF [1:0]	MDT [1:0]	ENDIAN	WEMODE	DM [1:0]	RM	RIM																																								
Power ON Sequence	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0																																								
SW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0																																								
HW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0																																								

## 8.4 Description of Extend register command

### 8.4.1 Power control A (CBh)

CBh	Power control A																																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																													
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	CBh																													
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	1	1	1	0	0	1	39																													
2 <sup>nd</sup> Parameter	1	1	↑	XX	0	0	1	0	1	1	0	0	2C																													
3 <sup>rd</sup> Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																													
4 <sup>th</sup> Parameter	1	1	↑	XX	0	0	1	1	0	REG_VD[2:0]			34																													
5 <sup>th</sup> Parameter	1	1	↑	XX	0	0	0	0	0	VBC[2:0]			02																													
Description	REG_VD[2:0]: vcore control																																									
	REG_VD[2:0]		Vcore(V)																																							
	000		1.55																																							
	001		1.4																																							
	010		1.5																																							
	011		1.65																																							
	100		1.6																																							
	101		1.7																																							
Description	VBC[2:0]: ddvdh control																																									
	VBC[2:0]		DDVDH(V)																																							
	000		5.8																																							
	001		5.7																																							
	010		5.6																																							
	011		5.5																																							
	100		5.4																																							
	101		5.3																																							
Restriction	EXTC should be high to enable this command																																									
	Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																
Status	Availability																																									
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																									
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Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																									
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																									
Sleep IN	Yes																																									
Default		<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="5">Default Value</th> </tr> <tr> <th>Parameter1</th> <th>Parameter2</th> <th>Parameter3</th> <th>Parameter4</th> <th>Parameter5</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>39</td> <td>2C</td> <td>00</td> <td>34</td> <td>02</td> </tr> <tr> <td>SW Reset</td> <td>39</td> <td>2C</td> <td>00</td> <td>34</td> <td>02</td> </tr> <tr> <td>HW Reset</td> <td>39</td> <td>2C</td> <td>00</td> <td>34</td> <td>02</td> </tr> </tbody> </table>												Status	Default Value					Parameter1	Parameter2	Parameter3	Parameter4	Parameter5	Power ON Sequence	39	2C	00	34	02	SW Reset	39	2C	00	34	02	HW Reset	39	2C	00	34	02
Status	Default Value																																									
	Parameter1	Parameter2	Parameter3	Parameter4	Parameter5																																					
Power ON Sequence	39	2C	00	34	02																																					
SW Reset	39	2C	00	34	02																																					
HW Reset	39	2C	00	34	02																																					

### 8.4.2 Power control B (CFh)

CFh	Power control B																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	1	0	0	1	1	1	1	CFh																			
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																			
2 <sup>nd</sup> Parameter	1	1	↑	XX	1	PCEQ	DRV_ena	Power control[1:0]			0	0	1																			
3 <sup>rd</sup> Parameter	1	1	↑	XX	DRV_vml[2:1]		1	DC_ena	DRV_vml[0]	DRV_vmh[2:0]			30																			
Description	2 <sup>nd</sup> parameter: power control[1:0]  Only setting power control [1:0]=11, the VGH and VGL voltage level follow the table below.																															
	<table border="1"> <tr> <th>BT [2:0]</th><th>DDVDH</th><th>VGH</th><th>VGL</th></tr> <tr> <td>0 0 0</td><td rowspan="4">VCI x 2</td><td rowspan="2">VCI x 7</td><td>-VCI x 4</td></tr> <tr> <td>0 0 1</td><td>-VCI x 3</td></tr> <tr> <td>0 1 0</td><td>VCI x 6</td><td>-VCI x 4</td></tr> <tr> <td>0 1 1</td><td></td><td>-VCI x 3</td></tr> </table>													BT [2:0]	DDVDH	VGH	VGL	0 0 0	VCI x 2	VCI x 7	-VCI x 4	0 0 1	-VCI x 3	0 1 0	VCI x 6	-VCI x 4	0 1 1		-VCI x 3			
BT [2:0]	DDVDH	VGH	VGL																													
0 0 0	VCI x 2	VCI x 7	-VCI x 4																													
0 0 1			-VCI x 3																													
0 1 0		VCI x 6	-VCI x 4																													
0 1 1			-VCI x 3																													
bit[5]: DRV_ena : For VCOM driving ability enhancement, DRV_ena = 1: Enable, and vice versa																																
bit[6]: PCEQ: PC and EQ operation for power saving																																
0:disable this function																																
1:enable this function																																
3 <sup>rd</sup> parameter: default: 30h																																
bit[2:0]: DRV_vmh[2:0] 3'b000 adjust over drive width for VMH(000: 1 op_clk ~111: 8 op_clk)																																
bit[3]: DRV_vml[0] 1'b0																																
bit[4]: DC_ena: Discharge path enable. Enable high for ESD protection, 1: enable and vice versa																																
bit[7:6] : DRV_vml[2:1] 2'b00																																
Restriction	EXTC should be high to enable this command																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes							
Status	Availability																															
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Sleep IN	Yes																															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>Parameter1</th><th>Parameter2</th><th>Parameter3</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>00</td><td>A2</td><td>F0</td></tr> <tr> <td>SW Reset</td><td>00</td><td>A2</td><td>F0</td></tr> <tr> <td>HW Reset</td><td>00</td><td>A2</td><td>F0</td></tr> </tbody> </table>													Status	Default Value			Parameter1	Parameter2	Parameter3	Power ON Sequence	00	A2	F0	SW Reset	00	A2	F0	HW Reset	00	A2	F0
Status	Default Value																															
	Parameter1	Parameter2	Parameter3																													
Power ON Sequence	00	A2	F0																													
SW Reset	00	A2	F0																													
HW Reset	00	A2	F0																													

**8.4.3 Driver timing control A (E8h)**

F6h	Driver timing control A	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command		0	1	↑	XX	1	1	1	0	1	0	0	0	E8h
1 <sup>st</sup> Parameter		1	1	↑	XX	1	0	0	0	0	1	0	NOW	84
2 <sup>nd</sup> Parameter		1	1	↑	XX	0	0	0	EQ	0	0	0	CR	11
3 <sup>rd</sup> Parameter		1	1	↑	XX	0	1	1	1	1	0	PC[1:0]	7A	
Description	EQ timing for Internal clock  1 <sup>st</sup> parameter:gate driver non-overlap timing control  0:default non-overlap time  1:default + 1unit   2 <sup>nd</sup> parameter:EQ timing control  0: default – 1unit  1:default EQ timing  parameter:CR timing control  0: default – 1unit  1:default CR timing   3 <sup>rd</sup> parameter:pre-charge timing control  11: reserved  10: default pre-charge timing  01:default – 1unit  00:default – 2unit													
Restriction	EXTC should be high to enable this command													
Register Availability		Status											Availability	
	Normal Mode ON, Idle Mode OFF, Sleep OUT												Yes	
	Normal Mode ON, Idle Mode ON, Sleep OUT												Yes	
	Partial Mode ON, Idle Mode OFF, Sleep OUT												Yes	
	Partial Mode ON, Idle Mode ON, Sleep OUT												Yes	
	Sleep IN												Yes	
Default		Status											Default Value	
	Power ON Sequence	Parameter1											Parameter2	
	SW Reset	84											Parameter3	
	HW Reset	84												

**8.4.4 Driver timing control A (E9h)**

F6h	Driver timing control A																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	1	1	0	1	0	0	0	E8h																			
1 <sup>st</sup> Parameter	1	1	↑	XX	1	0	0	0	0	1	0	NOWE	84																			
2 <sup>nd</sup> Parameter	1	1	↑	XX	0	0	0	EQE	0	0	0	CRE	11																			
3 <sup>rd</sup> Parameter	1	1	↑	XX	0	1	1	1	1	0	PCE[1:0]		7A																			
Description	EQE timing for External clock 1 <sup>st</sup> parameter:gate driver non-overlap timing control 0:default non-overlap time 1:default + 1unit  2 <sup>nd</sup> parameter:EQE timing control 0: default – 1unit 1:default EQE timing parameter:CRE timing control 0: default – 1unit 1:default CRE timing  3 <sup>rd</sup> parameter:pre-charge timing control 11: reserved 10: default pre-charge timing 01:default – 1unit 00:default – 2unit																															
Restriction	EXTC should be high to enable this command																															
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes							
Status	Availability																															
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Sleep IN	Yes																															
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>Parameter1</th> <th>Parameter2</th> <th>Parameter3</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>84</td> <td>11</td> <td>7A</td> </tr> <tr> <td>SW Reset</td> <td>84</td> <td>11</td> <td>7A</td> </tr> <tr> <td>HW Reset</td> <td>84</td> <td>11</td> <td>7A</td> </tr> </tbody> </table>													Status	Default Value			Parameter1	Parameter2	Parameter3	Power ON Sequence	84	11	7A	SW Reset	84	11	7A	HW Reset	84	11	7A
Status	Default Value																															
	Parameter1	Parameter2	Parameter3																													
Power ON Sequence	84	11	7A																													
SW Reset	84	11	7A																													
HW Reset	84	11	7A																													

### 8.4.5 Driver timing control B (EAh)

F6h		Driver timing control B												
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command		0	1	↑	XX	1	1	1	0	1	0	1	0	EAh
1 <sup>st</sup> Parameter		1	1	↑	XX	VG_SW_T4		VG_SW_T3		VG_SW_T2		VG_SW_T1		66
2 <sup>nd</sup> Parameter		1	1	↑	XX	X	X	X	X	X	X	0	0	00
Description	1 <sup>st</sup> parameter:gate driver timing control													
	VG_SW_T1[1:0]:EQ to GND													
	VG_SW_T2[1:0]:EQ to DDVDH													
	VG_SW_T3[1:0]:EQ to DDVDH													
	VG_SW_T4[1:0]:EQ to GND													
	00: 0 unit													
	01: 1 unit													
Restriction	02: 2 unit													
	03: 3 unit													
Register Availability	Restriction													
	EXTC should be high to enable this command													
Default														
Parameter														

### 8.4.6 Power on sequence control (EDh)

F6h		Power on sequence control																																				
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
Command		0	1	↑	XX	1	1	1	0	1	1	0	1	EDh																								
1 <sup>st</sup> Parameter		1	1	↑	XX	X	1	CP1 soft start		X	1	CP23 soft start		55																								
2 <sup>nd</sup> Parameter		1	1	↑	XX	X	0	En_vcl		X	0	En_ddvdh		01																								
3 <sup>rd</sup> Parameter		1	1	↑	XX	X	0	En_vgh		X	0	En_vgl		23																								
4 <sup>th</sup> Parameter		1	1	↑	XX	DDVDH_ENH	0	0	0	0	0	0	1	1																								
Description		1 <sup>st</sup> parameter:soft start control 00:soft start keep 3 frame 01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable  2 <sup>nd</sup> / 3 <sup>rd</sup> parameter:power on sequence control 00:1 <sup>st</sup> frame enable 01:2 <sup>nd</sup> frame enable 10:3 <sup>rd</sup> frame enable 11:4 <sup>th</sup> frame enable  4 <sup>th</sup> parameter:DDVDH enhance mode(only for 8 external capacitors) 0: disable 1: enable																																				
Restriction		EXTC should be high to enable this command																																				
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes												
Status	Availability																																					
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																					
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																																					
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																					
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																					
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Status	Default Value																																					
	Parameter1	Parameter2	Parameter3	Parameter4																																		
Power ON Sequence	55	01	23	01																																		
SW Reset	55	01	23	01																																		
HW Reset	55	01	23	01																																		

**8.4.7 Enable 3G (F2h)**

F6h	Enable_3G																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h												
1 <sup>st</sup> Parameter	1	1	↑	XX	0	0	0	0	0	0	1	3G_enb	02												
Description	1 <sup>st</sup> Parameter: Enable 3 gamma control 3G_enb high for 3 gamma control enable																								
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <th>Parameter1</th> <td></td> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>02</td> </tr> <tr> <td>SW Reset</td> <td>02</td> </tr> <tr> <td>HW Reset</td> <td>02</td> </tr> </tbody> </table>													Status	Default Value	Parameter1		Power ON Sequence	02	SW Reset	02	HW Reset	02		
Status	Default Value																								
Parameter1																									
Power ON Sequence	02																								
SW Reset	02																								
HW Reset	02																								

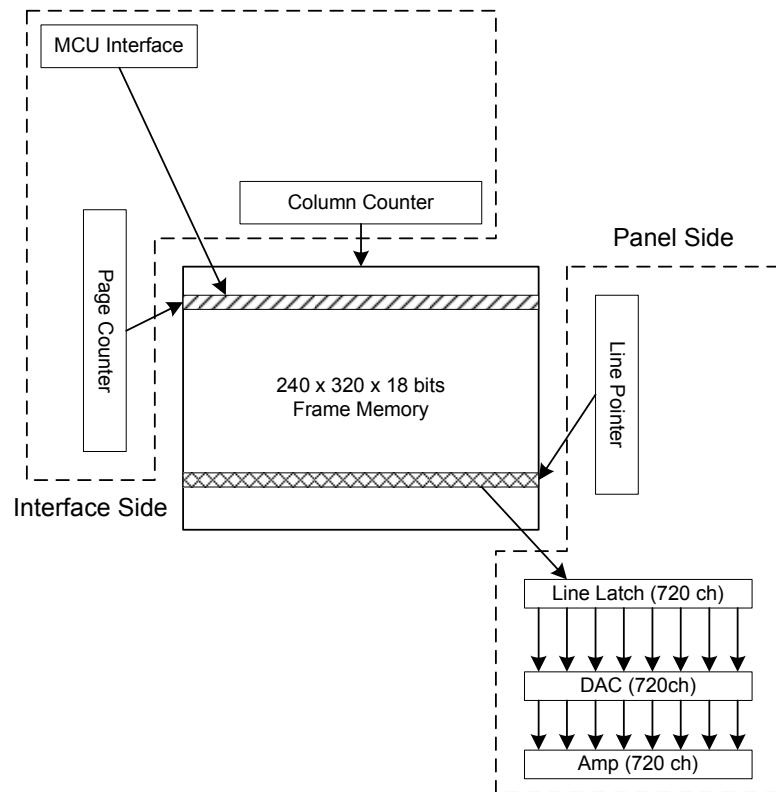
**8.4.8 Pump ratio control (F7h)**

F6h	Pump ratio control																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F7h												
1 <sup>st</sup> Parameter	1	1	↑	XX	X	X	Ratio[1:0]		0	0	0	0	10												
Description	1 <sup>st</sup> parameter:ratio control  00:reserved  01:reserved  10:DDVDH=2xVCI  11:DDVDH=3xVCI																								
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <th>Parameter1</th> <td></td> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>10</td> </tr> <tr> <td>SW Reset</td> <td>10</td> </tr> <tr> <td>HW Reset</td> <td>10</td> </tr> </tbody> </table>													Status	Default Value	Parameter1		Power ON Sequence	10	SW Reset	10	HW Reset	10		
Status	Default Value																								
Parameter1																									
Power ON Sequence	10																								
SW Reset	10																								
HW Reset	10																								

## 9. Display Data RAM

### 9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

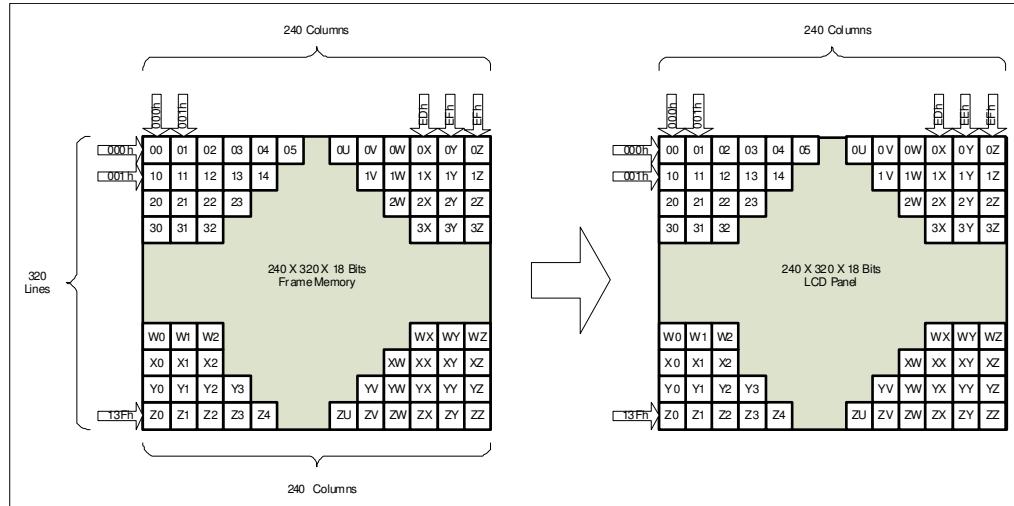


## 9.2. Memory to Display Address Mapping

### 9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

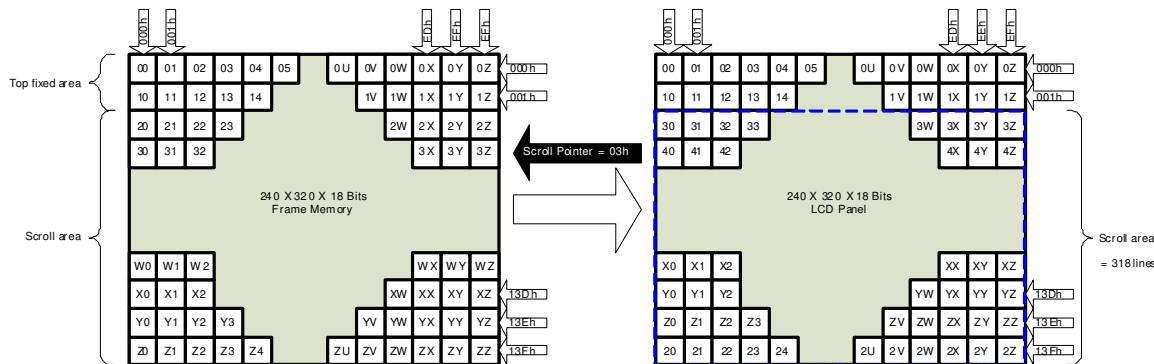


### 9.2.2. Vertical Scroll Mode

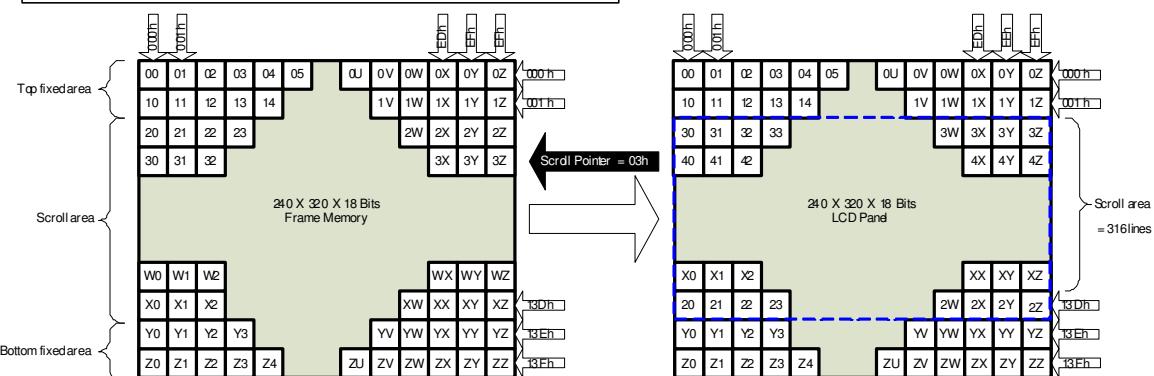
There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.

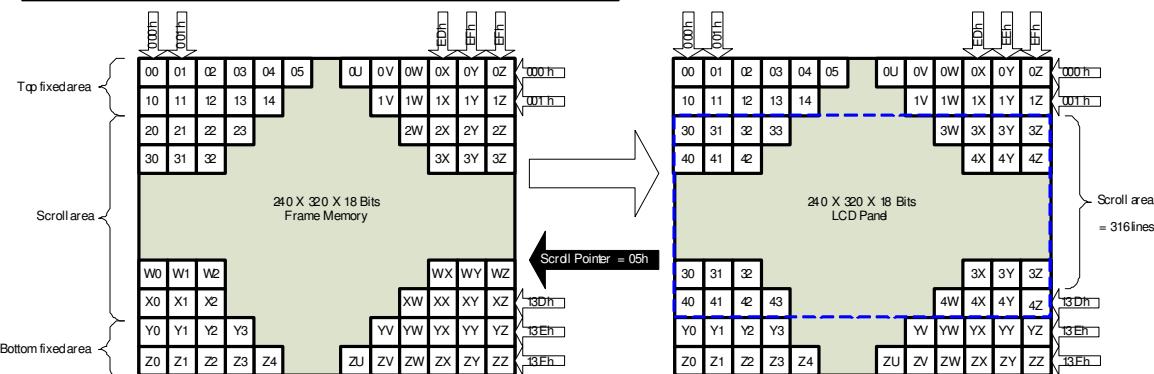
TFA=2, VSA=318, BFA=0 when MADCTL ML bit = 0



TFA=2, VSA=316, BFA=2 when MADCTL ML bit = 0



TFA=2, VSA=316, BFA=4 when MADCTL ML bit = 0



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

### 9.2.3. Vertical Scroll Example

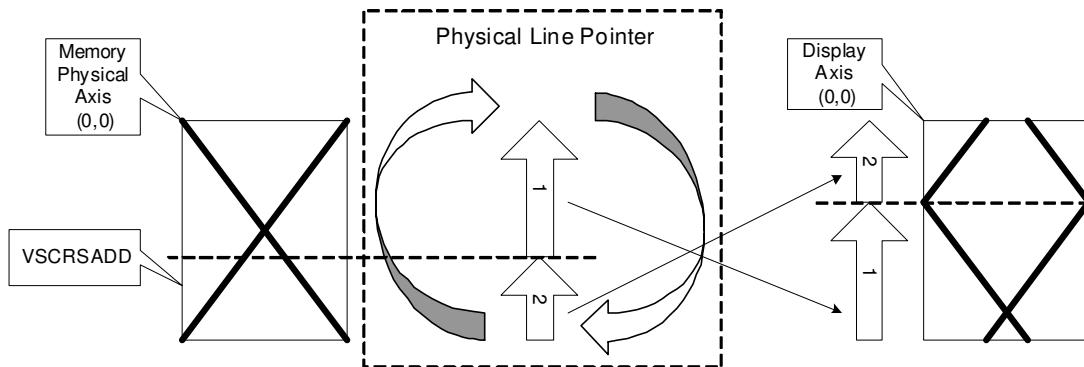
#### 9.2.4. Case1: TFA+VSA+BFA < 320

This setting is prohibited, unless unexpected picture will be shown.

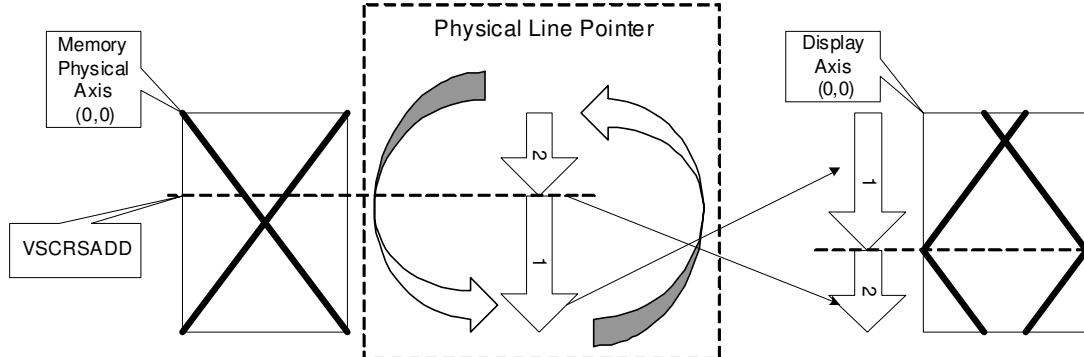
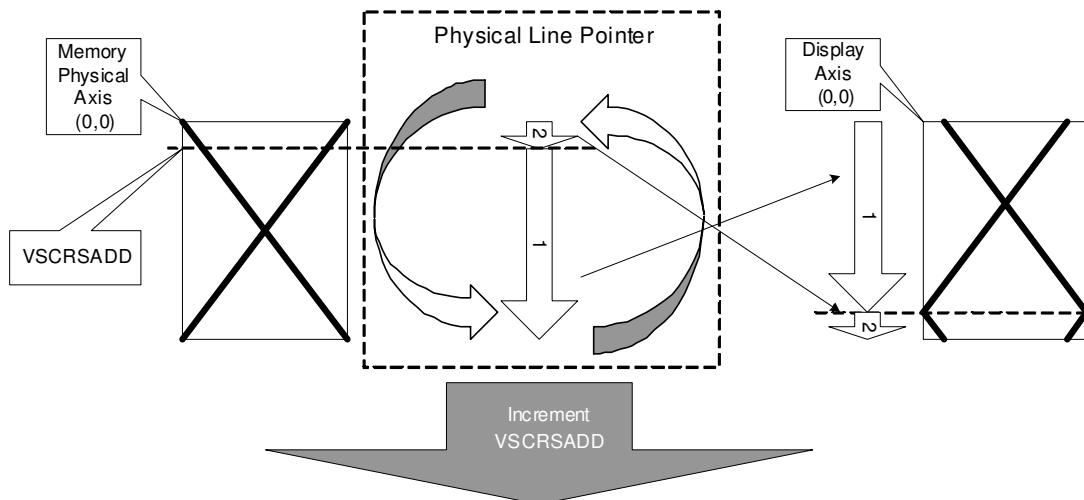
#### 9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

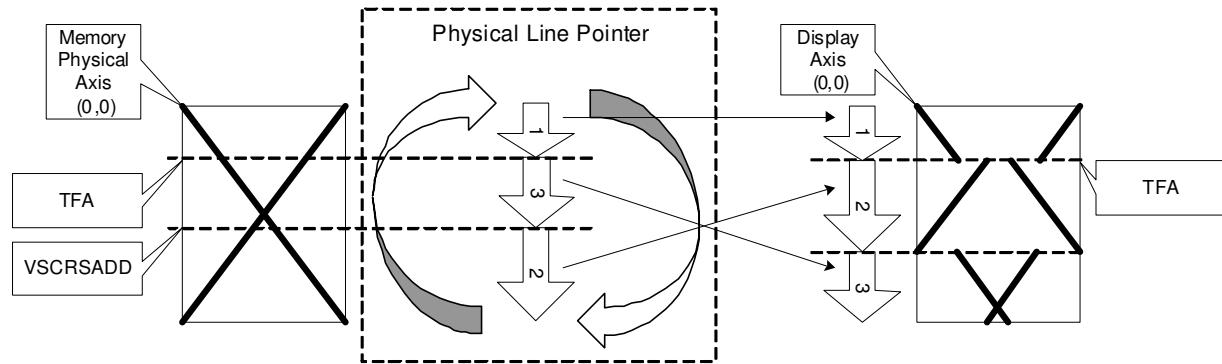
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 1



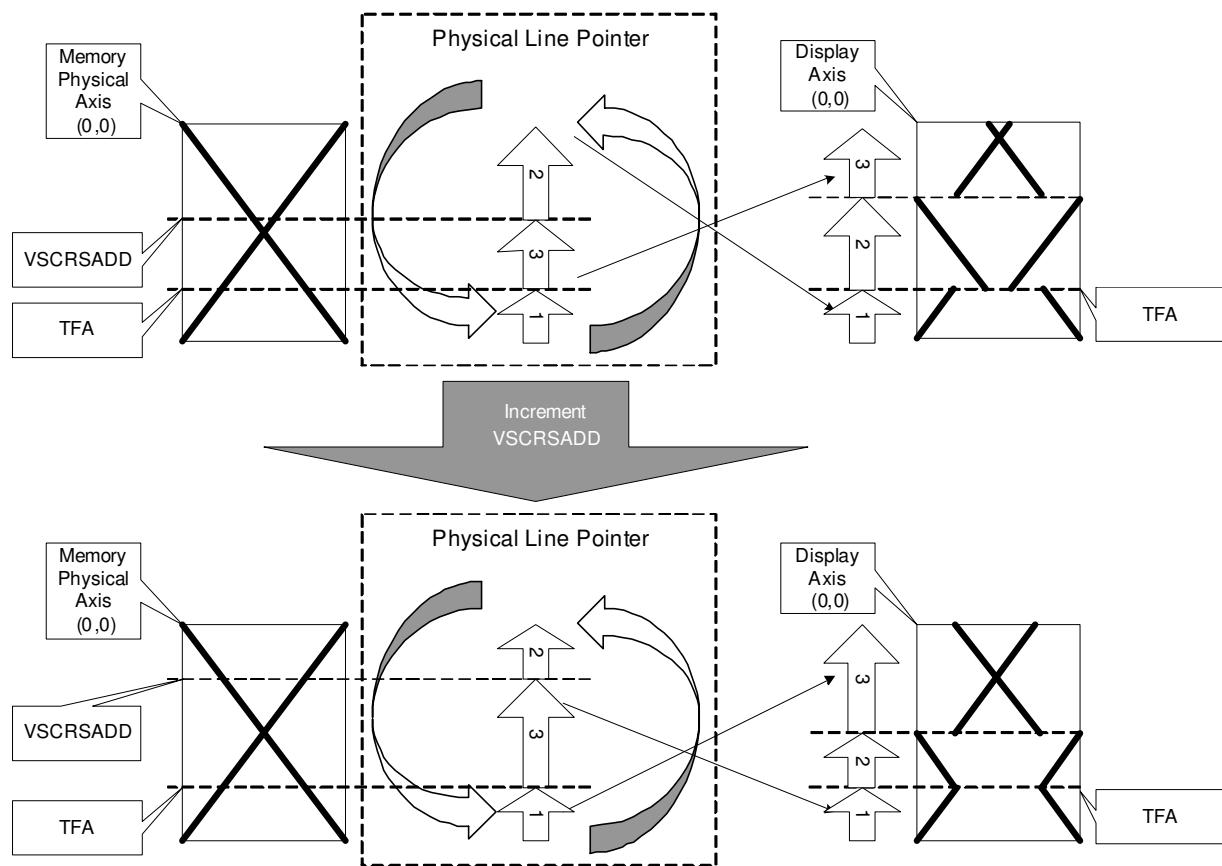
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



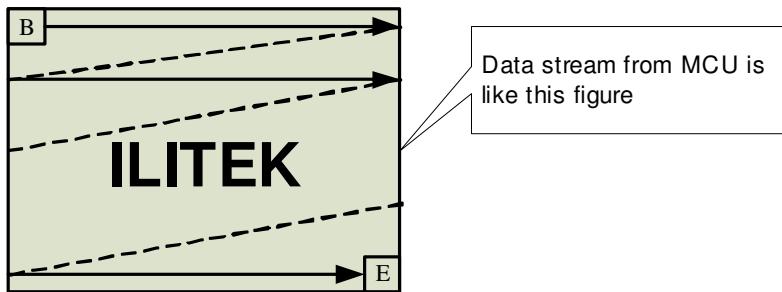
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



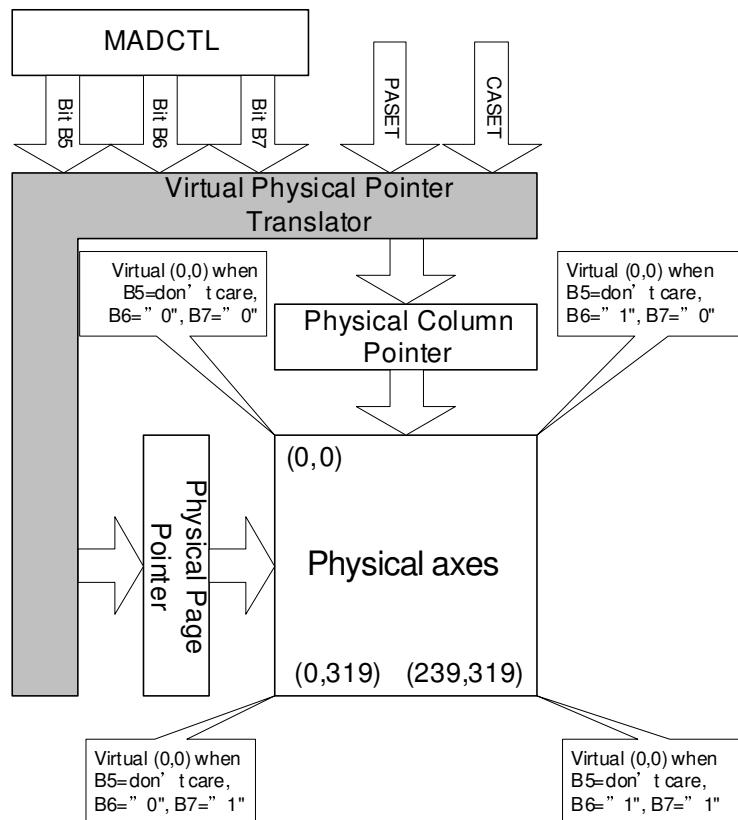
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



### 9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)
Condition			Column Counter	Page counter
When RAMWR/RAMRD command is accepted			Return to "Start column"	Return to "Start Page"
Complete Pixel Read/Write action			Increment by 1	No change
The Column values is large than "End Column"			Return to "Start column"	Increment by 1
The Page counter is large than "End Page"			Return to "Start column"	Return to "Start Page"

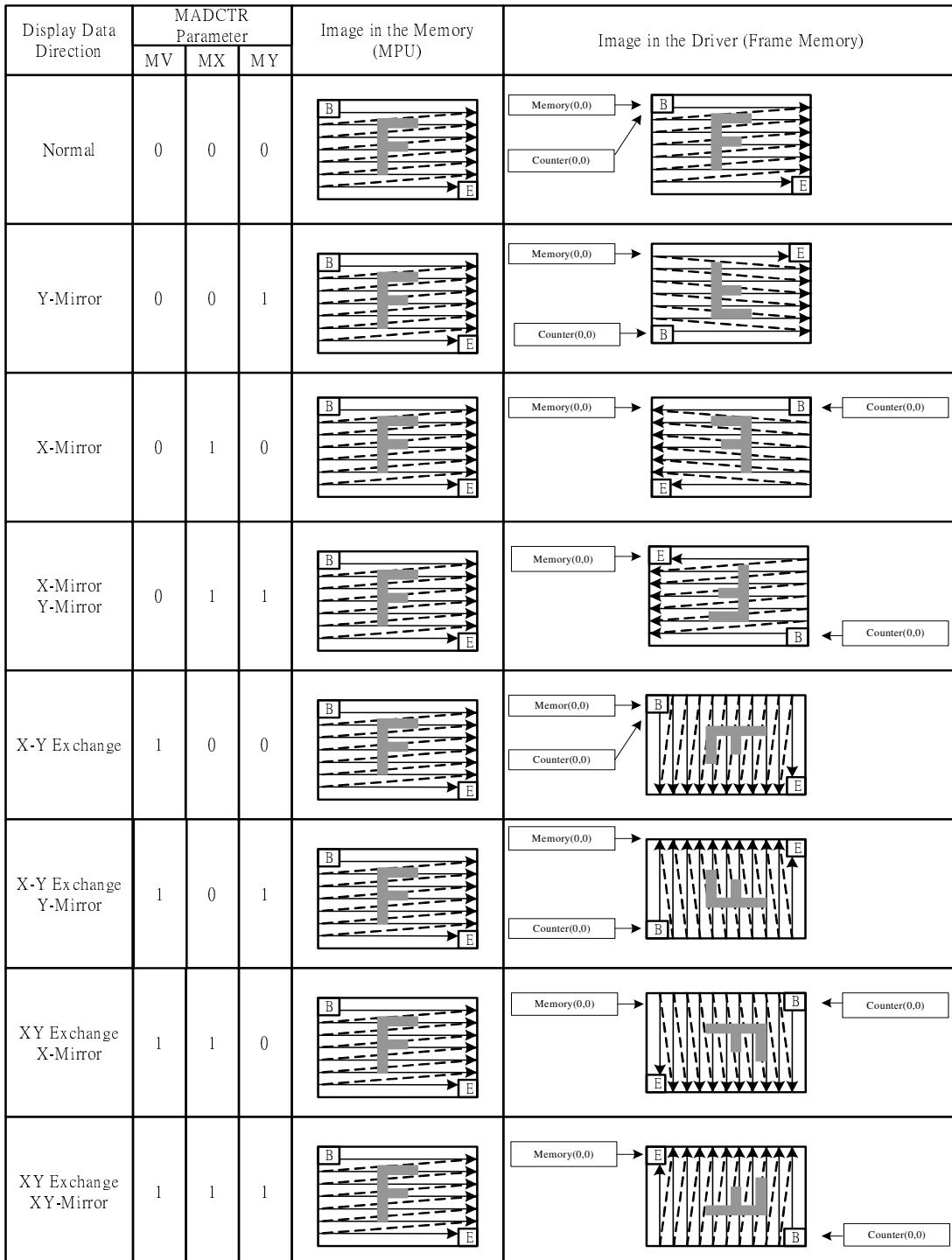
The information contained herein is the exclusive property of ILI Technology Corp. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of ILI Technology Corp.

**Note:**

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.



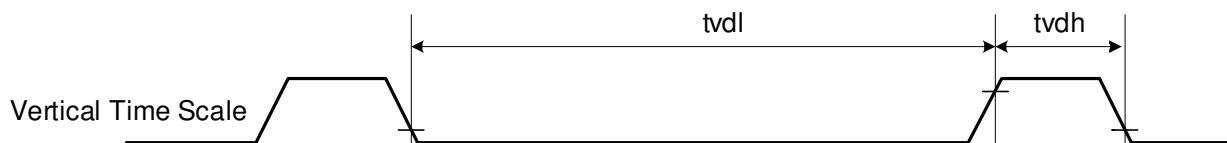
## 10. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

### 10.1. Tearing Effect Line Modes

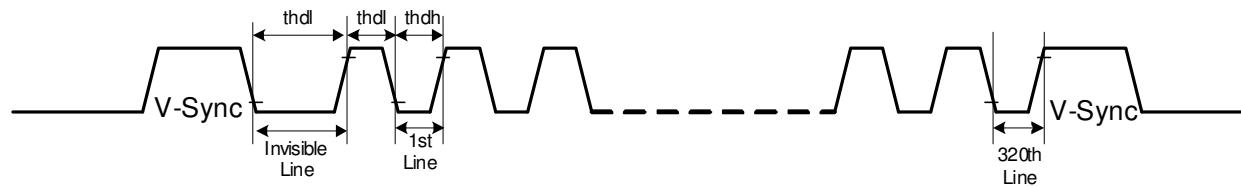
**Mode 1**, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

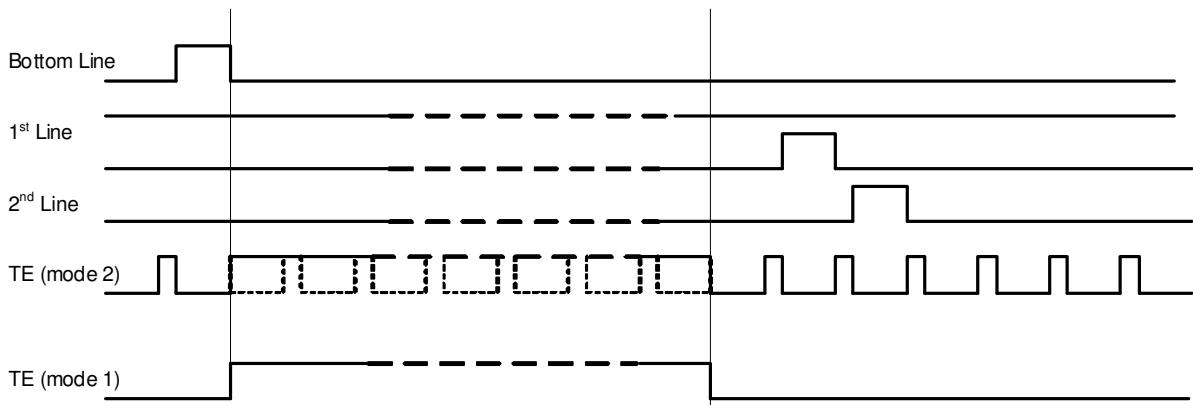
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

**Mode 2**, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

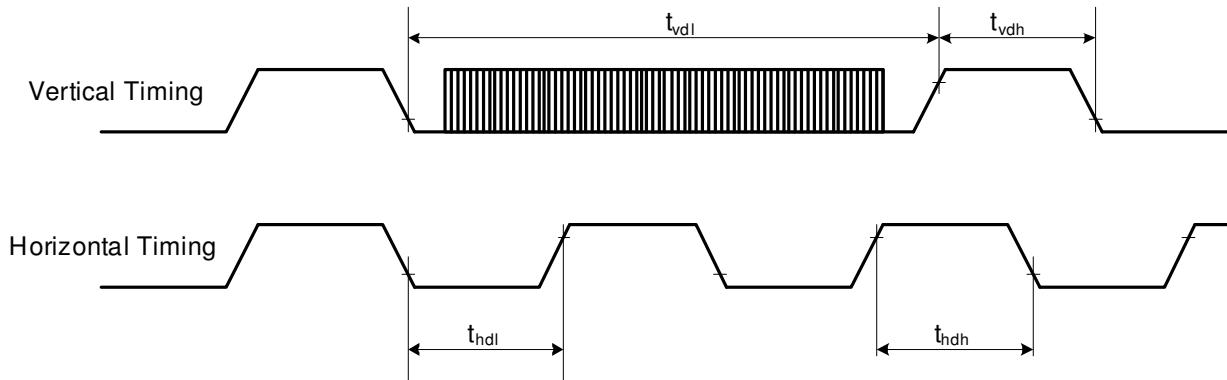
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



*Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.*

## 10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

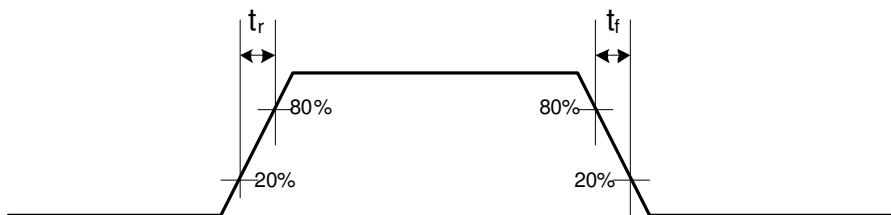


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
$t_{vdL}$	Vertical timing low duration	--	--	--	ms	
$t_{vdh}$	Vertical timing high duration	1000	--	--	us	
$t_{hdl}$	Horizontal timing low duration	--	--	--	us	
$t_{hdh}$	Horizontal timing high duration	--	--	500	us	

Note:

1. The timings in Table as above apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times ( $t_f$ ,  $t_r$ ) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

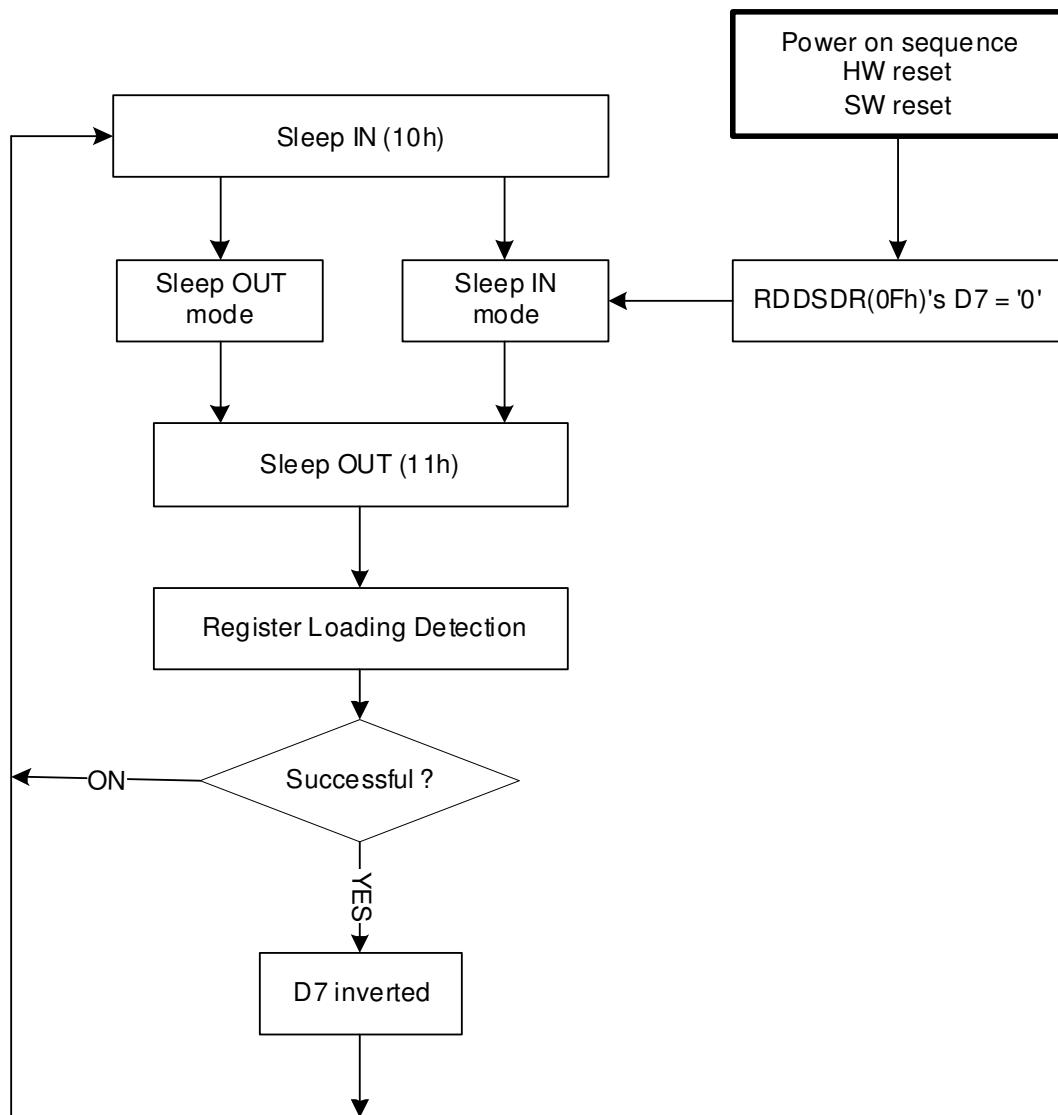
## 11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

### 11.1. Register loading Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

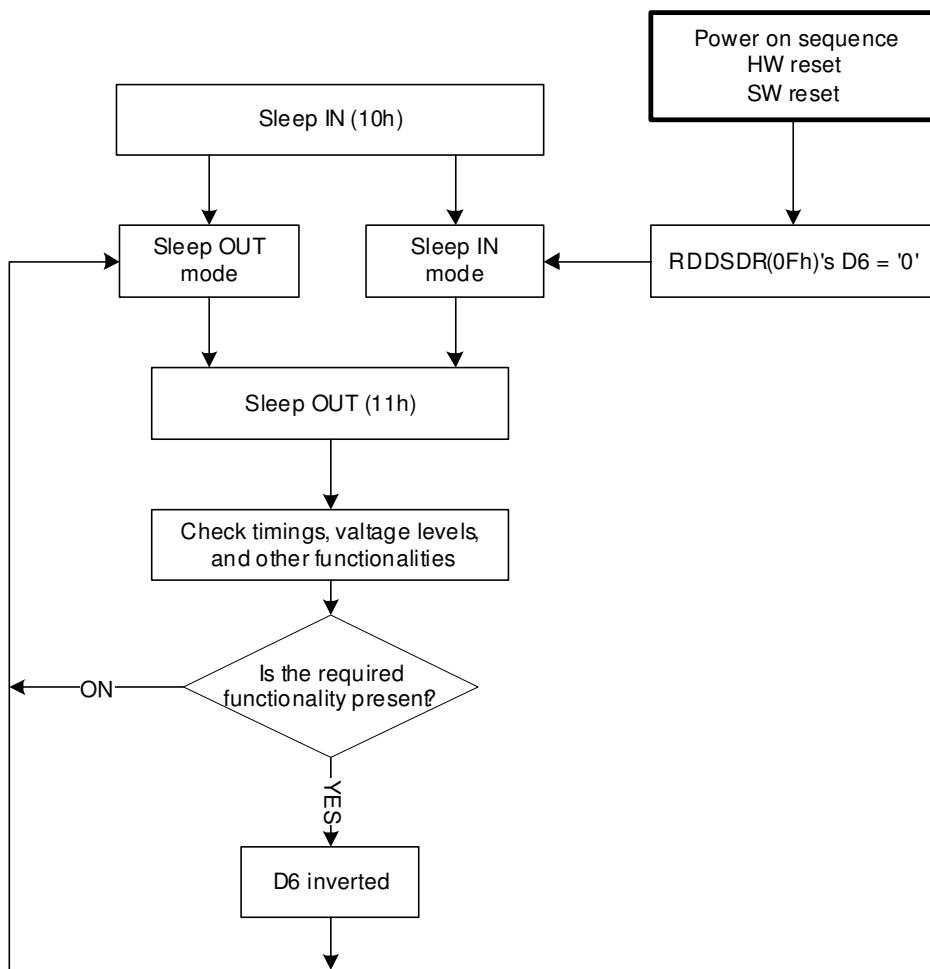


## 11.2. Functionality Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



*Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if User's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.*

## 12. Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

*Note 1: There will be no damage to the display module if the power sequences are not met.*

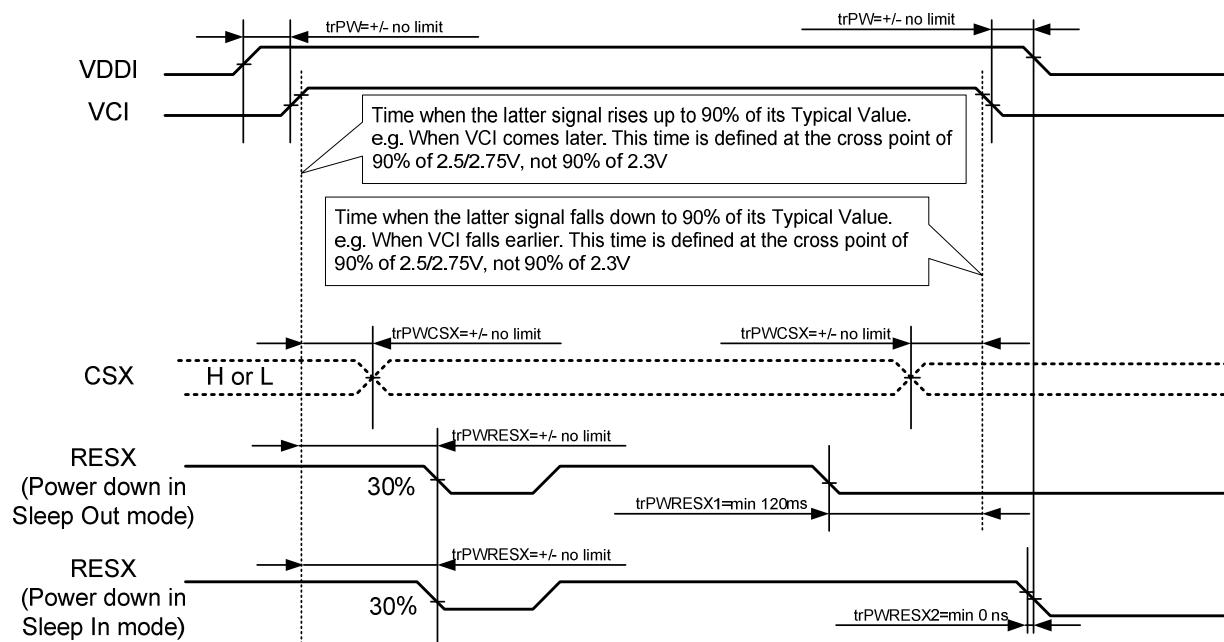
*Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*

*Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*

*Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*

### 12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

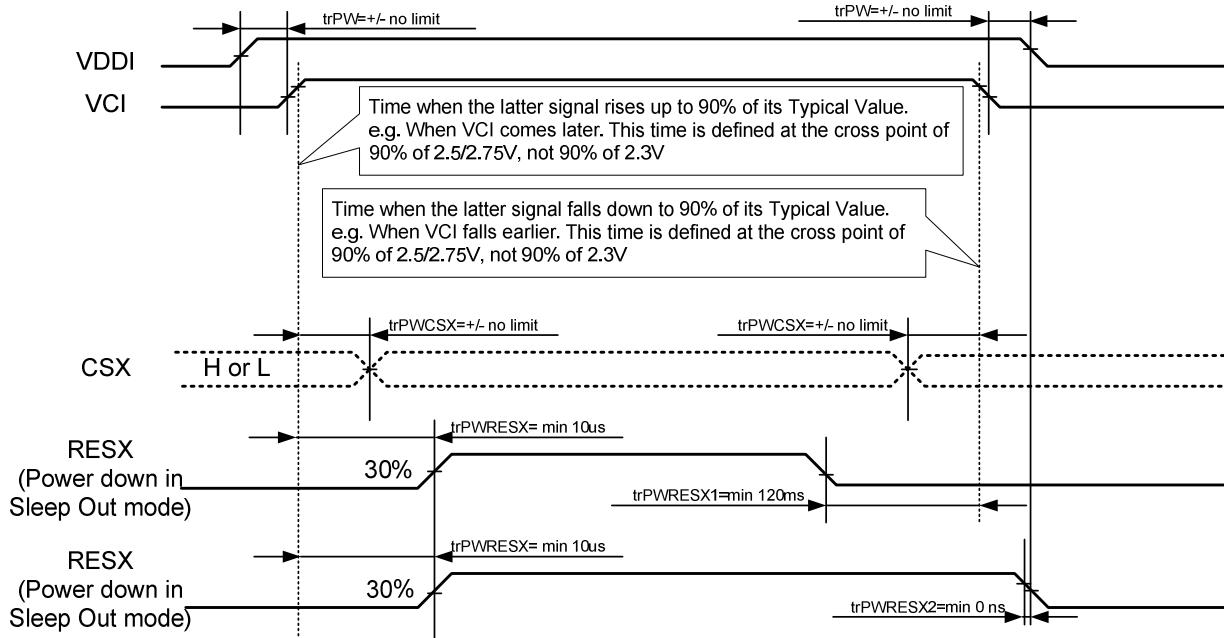
trPWRESX2 is applied to RESX falling in the Sleep In Mode

*Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.*

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## 12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10μsec after both VCI and VDDI have been applied.



$trPWRESX1$  is applied to RESX falling in the Sleep Out Mode  
 $trPWRESX2$  is applied to RESX falling in the Sleep In Mode

*Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.*

### 12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9341 will force the display to blank and will not be any abnormal visible effects within 1 second on the display and remains blank until "Power On Sequence" activates.

## 13. Power Level Definition

### 13.1. Power Levels

7 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

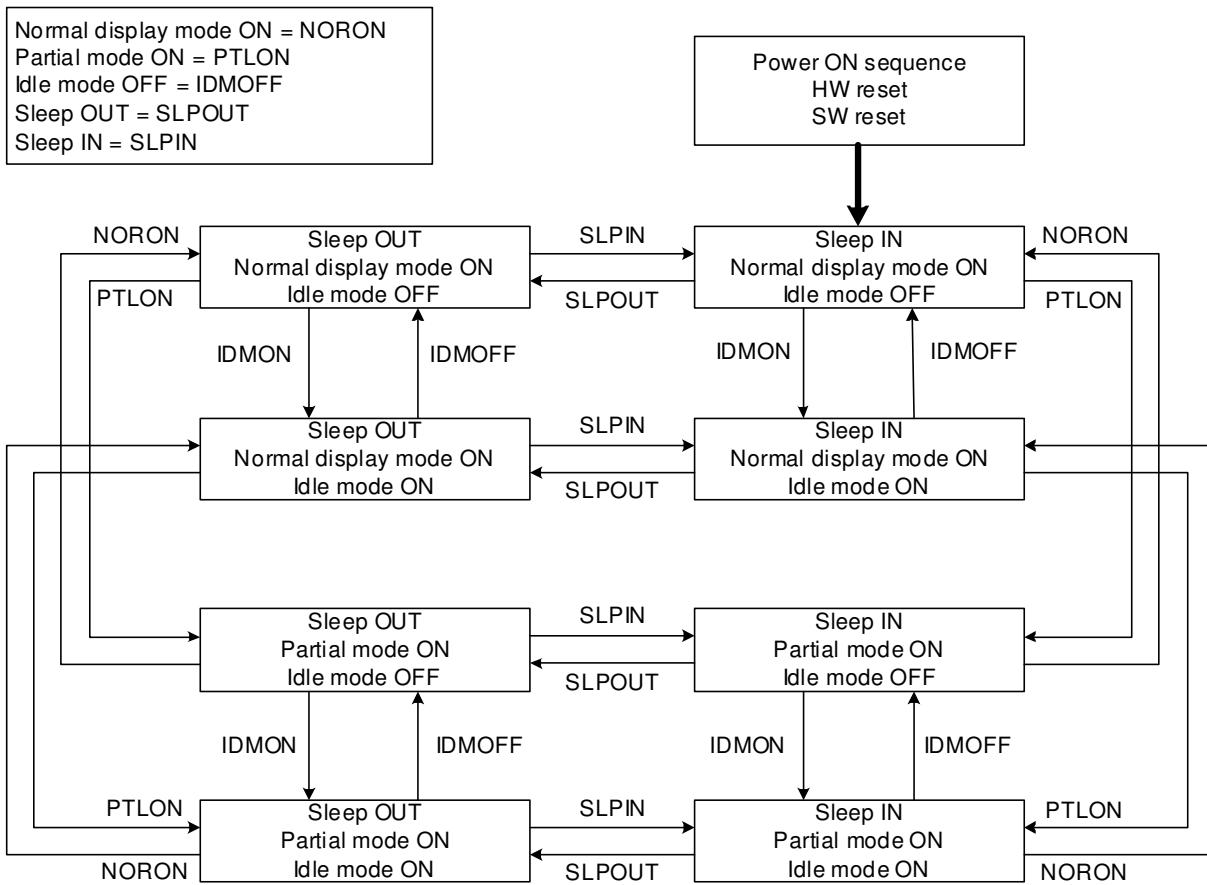
In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode.

In this mode, both VCI and VDDI are removed.

*Note1: Transition between modes 1-5 is controllable by MCU commands.*

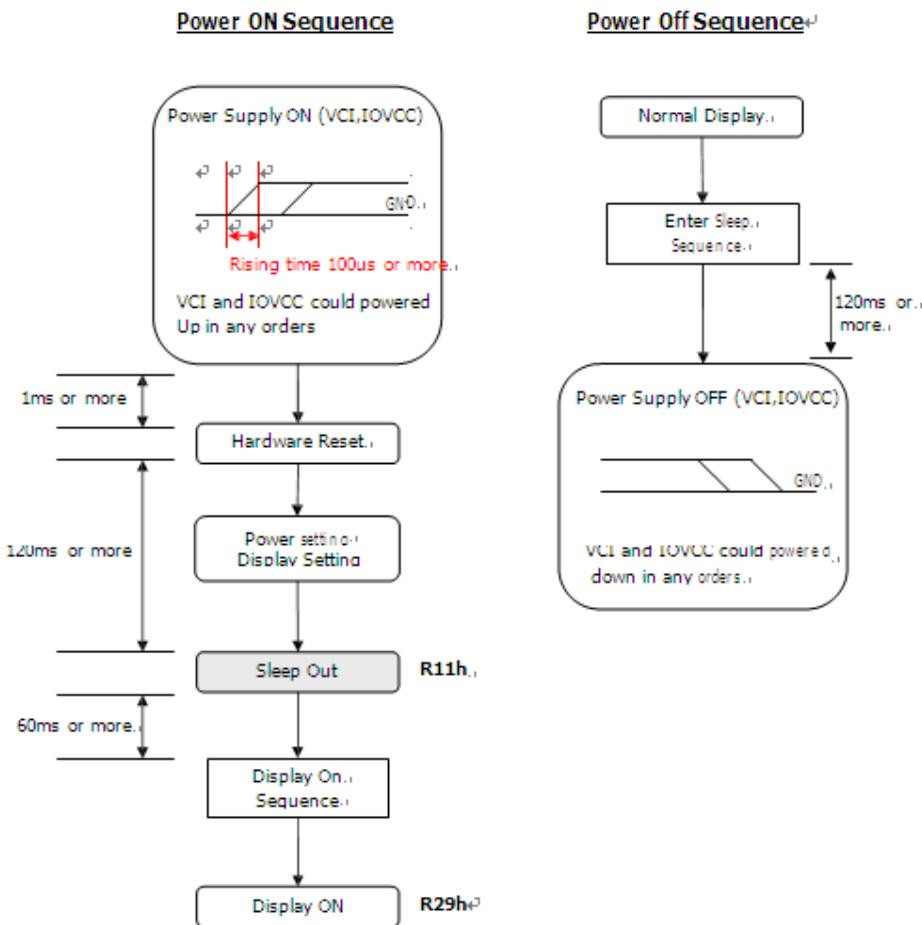
## 13.2. Power Flow Chart



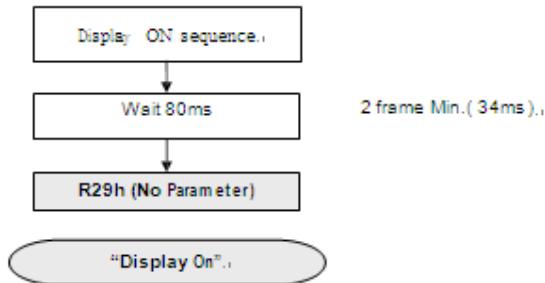
*Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.*

*Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.*

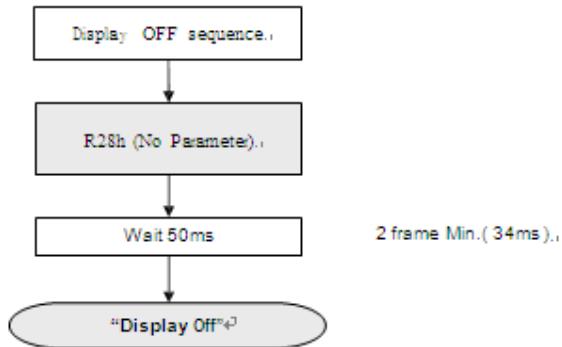
Power On /Off Sequence..



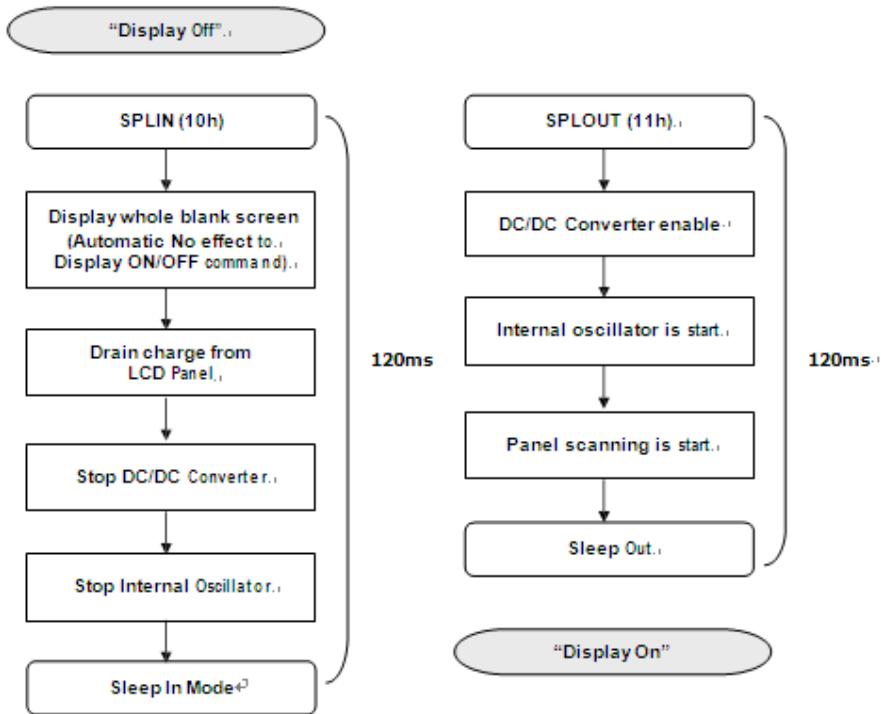
Display On Sequence Setting..

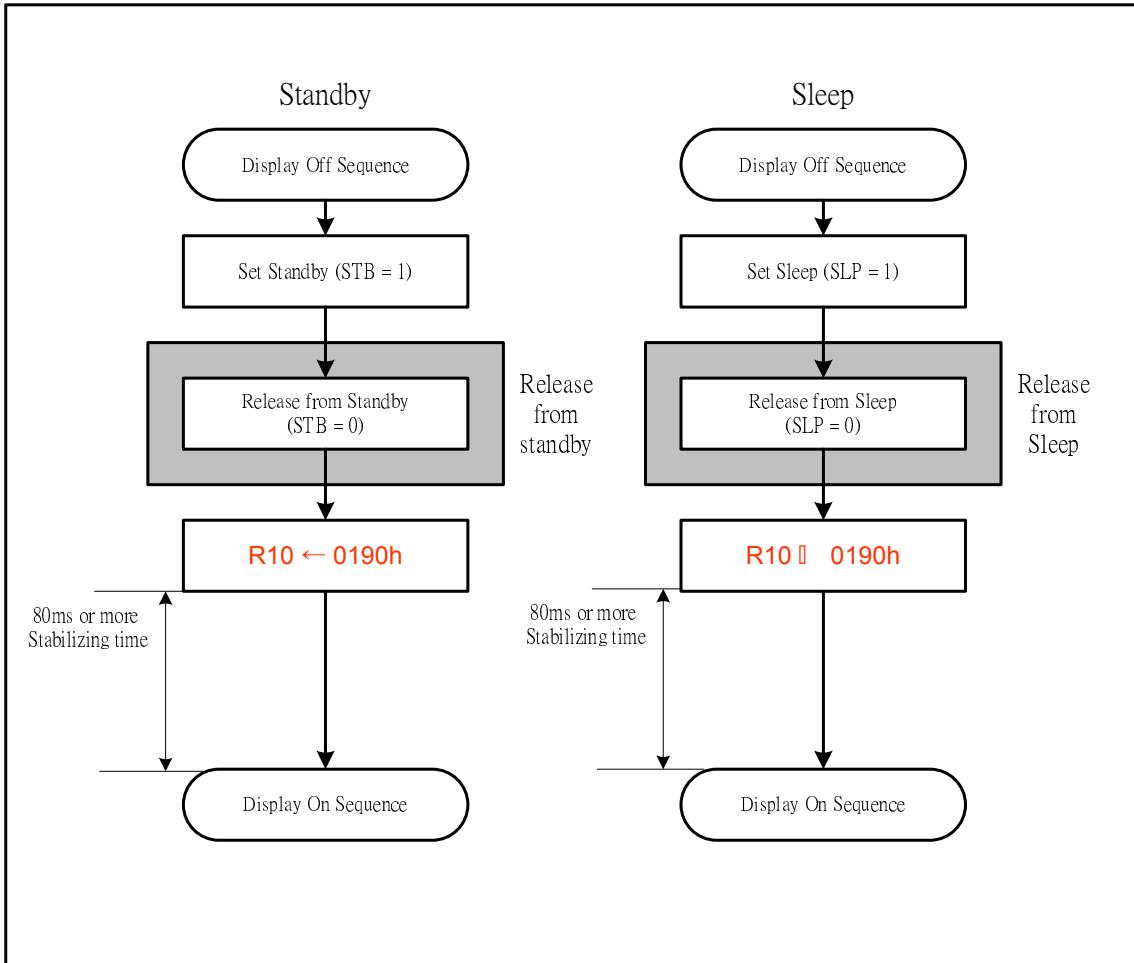


Display OFF Sequence Setting..



LCD Sleep Mode In/Out..





## 14. Gamma Curves Selection

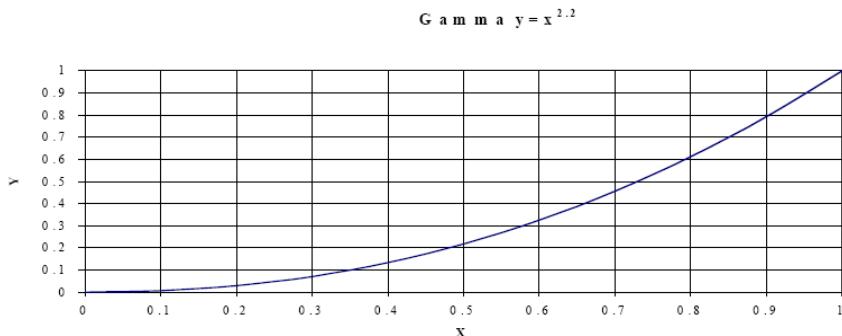
ILI9341 provide one gamma curve Gamma2.2. The gamma curve can be selected by the GCO settings.

### 14.1. Gamma Default Values (for NW type LC)

Data	Output Voltage	
	VCOM = Low	VCOM = High
Gamma	2.2	2.2
0	V0P 4.084	V0N 0.277
1	V1P 4.015	V1N 0.346
2	V2P 3.843	V2N 0.482
3	V3P 3.681	V3N 0.629
4	V4P 3.518	V4N 0.776
5	V5P 3.445	V5N 0.924
6	V6P 3.371	V6N 1.071
7	V7P 3.285	V7N 1.157
8	V8P 3.199	V8N 1.242
9	V9P 3.128	V9N 1.314
10	V10P 3.056	V10N 1.385
11	V11P 2.985	V11N 1.456
12	V12P 2.928	V12N 1.513
13	V13P 2.871	V13N 1.570
14	V14P 2.802	V14N 1.619
15	V15P 2.733	V15N 1.668
16	V16P 2.674	V16N 1.710
17	V17P 2.615	V17N 1.753
18	V18P 2.557	V18N 1.795
19	V19P 2.508	V19N 1.830
20	V20P 2.458	V20N 1.865
21	V21P 2.425	V21N 1.899
22	V22P 2.391	V22N 1.932
23	V23P 2.357	V23N 1.966
24	V24P 2.323	V24N 2.000
25	V25P 2.289	V25N 2.034
26	V26P 2.256	V26N 2.068
27	V27P 2.222	V27N 2.102
28	V28P 2.193	V28N 2.129
29	V29P 2.165	V29N 2.155
30	V30P 2.136	V30N 2.182
31	V31P 2.108	V31N 2.208
32	V32P 2.080	V32N 2.235
33	V33P 2.051	V33N 2.262
34	V34P 2.023	V34N 2.288
35	V35P 1.994	V35N 2.315
36	V36P 1.966	V36N 2.342
37	V37P 1.942	V37N 2.368
38	V38P 1.917	V38N 2.395
39	V39P 1.893	V39N 2.421
40	V40P 1.869	V40N 2.448
41	V41P 1.845	V41N 2.475
42	V42P 1.820	V42N 2.501
43	V43P 1.796	V43N 2.528
44	V44P 1.776	V44N 2.549
45	V45P 1.755	V45N 2.571
46	V46P 1.730	V46N 2.597
47	V47P 1.706	V47N 2.623
48	V48P 1.681	V48N 2.649
49	V49P 1.653	V49N 2.679
50	V50P 1.624	V50N 2.710
51	V51P 1.598	V51N 2.735
52	V52P 1.573	V52N 2.761
53	V53P 1.541	V53N 2.793
54	V54P 1.508	V54N 2.825
55	V55P 1.476	V55N 2.857
56	V56P 1.438	V56N 2.895
57	V57P 1.400	V57N 2.933
58	V58P 1.359	V58N 2.982
59	V59P 1.319	V59N 3.031
60	V60P 1.246	V60N 3.109
61	V61P 1.173	V61N 3.186
62	V62P 1.070	V62N 3.289
63	V63P 0.279	V63N 4.083

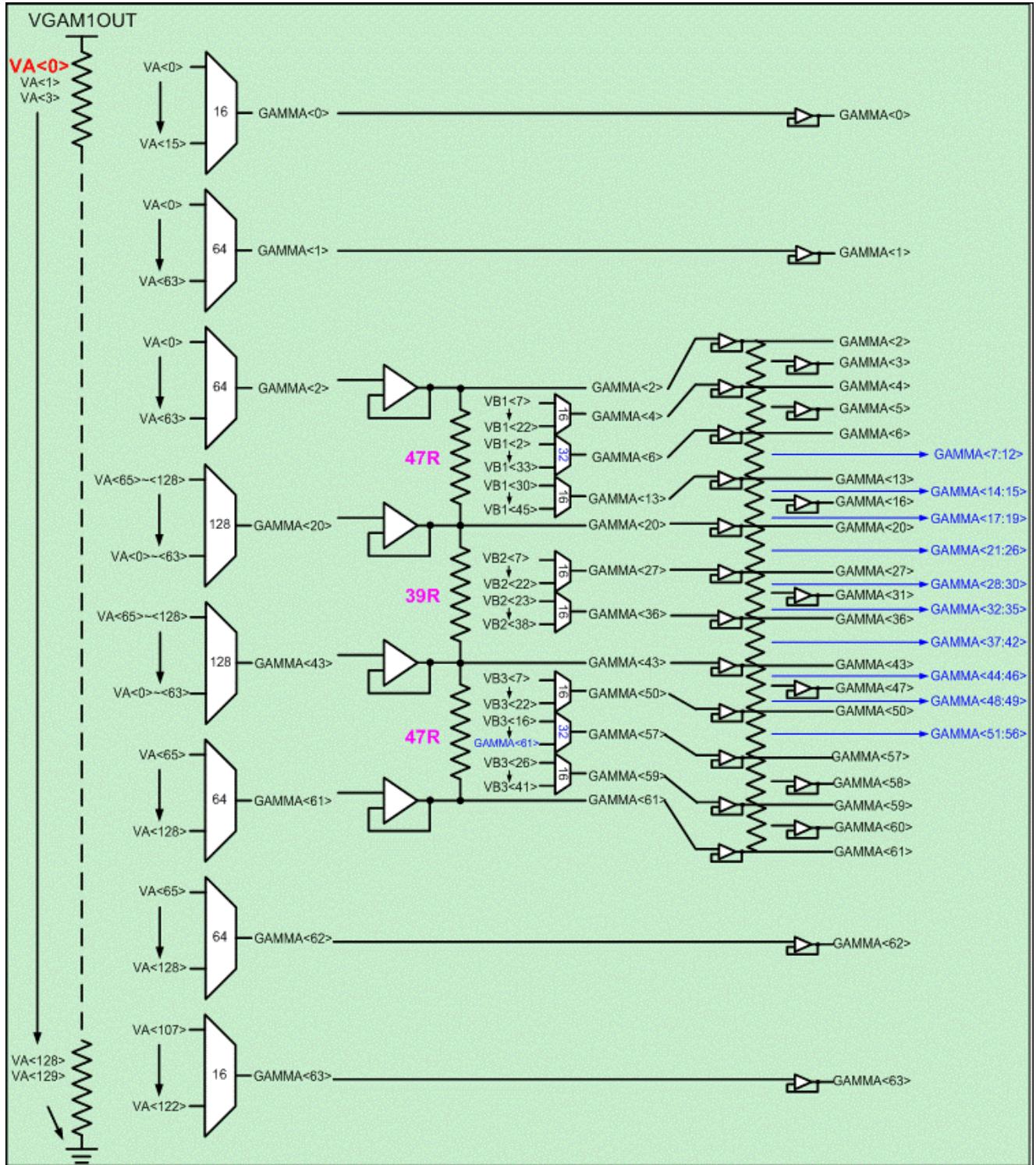
## 14.2. Gamma Curves

### 14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



## 14.3. Gamma Curves

### 14.3.1. Grayscale Voltage Generation



### 14.3.2. Positive Gamma Correction

Gamma Level	Value "X" in Formula	Formula	
VP0	VP0[3:0]		$(VREG1-VGS)*(130R-X^R)/130R$
VP1	VP1[5:0]		$(VREG1-VGS)*(130R-X^R)/130R$
VP2	VP2[5:0]		$(VREG1-VGS)*(130R-X^R)/130R$
VP3	—		$(VP2-VP4)*35R/(35R^2)+VP4$
VP4	VP4[3:0]		$(VP2-VP20)*(47R-X^R-7R)/47R+VP20$
VP5	—		$(VP4-VP6)*35R/(35R^2)+VP6$
VP6	VP6[4:0]		$(VP2-VP20)*(47R-X^R-2R)/47R+VP20$
VP7	—		$(VP6-VP13)*(12R+10R^3+8R^2)/(12R^2+10R^3+8R^2)+VP13$
VP8	—		$(VP6-VP13)*(10R^3+8R^2)/(12R^2+10R^3+8R^2)+VP13$
VP9	—		$(VP6-VP13)*(10R^2+8R^2)/(12R^2+10R^3+8R^2)+VP13$
VP10	—		$(VP6-VP13)*(10R+8R^2)/(12R^2+10R^3+8R^2)+VP13$
VP11	—		$(VP6-VP13)*(8R^2)/(12R^2+10R^3+8R^2)+VP13$
VP12	—		$(VP6-VP13)*8R/(12R^2+10R^3+8R^2)+VP13$
VP13	VP13[3:0]		$(VP2-VP20)*(47R-X^R-30R)/47R+VP20$
VP14	—		$(VP13-VP20)*(14R+12R^3+10R^2)/(14R^2+12R^3+10R^2)+VP20$
VP15	—		$(VP13-VP20)*(12R^3+10R^2)/(14R^2+12R^3+10R^2)+VP20$
VP16	—		$(VP13-VP20)*(12R^2+10R^2)/(14R^2+12R^3+10R^2)+VP20$
VP17	—		$(VP13-VP20)*(12R+10R^2)/(14R^2+12R^3+10R^2)+VP20$
VP18	—		$(VP13-VP20)*(10R^2)/(14R^2+12R^3+10R^2)+VP20$
VP19	—		$(VP13-VP20)*10R/(14R^2+12R^3+10R^2)+VP20$
VP20	VP20[6:0]	<64	$(VREG1-VGS)*(130R-X^R)/130R$
		>=64	$(VREG1-VGS)*(130R-X^R-1R)/130R$
VP21	—		$(VP20-VP27)*(12R^6)/(12R^7)+VP27$
VP22	—		$(VP20-VP27)*(12R^5)/(12R^7)+VP27$
VP23	—		$(VP20-VP27)*(12R^4)/(12R^7)+VP27$
VP24	—		$(VP20-VP27)*(12R^3)/(12R^7)+VP27$
VP25	—		$(VP20-VP27)*(12R^2)/(12R^7)+VP27$
VP26	—		$(VP20-VP27)*12R/(12R^7)+VP27$
VP27	VP27[3:0]		$(VP20-VP43)*(39R-X^R-7R)/39R+VP43$
VP28	—		$(VP27-VP36)*(8R^8)/(8R^9)+VP36$
VP29	—		$(VP27-VP36)*(8R^7)/(8R^9)+VP36$
VP30	—		$(VP27-VP36)*(8R^6)/(8R^9)+VP36$
VP31	—		$(VP27-VP36)*(8R^5)/(8R^9)+VP36$
VP32	—		$(VP27-VP36)*(8R^4)/(8R^9)+VP36$
VP33	—		$(VP27-VP36)*(8R^3)/(8R^9)+VP36$
VP34	—		$(VP27-VP36)*(8R^2)/(8R^9)+VP36$
VP35	—		$(VP27-VP36)*8R/(8R^9)+VP36$
VP36	VP36[3:0]		$(VP20-VP43)*(39R-X^R-23R)/39R+VP43$
VP37	—		$(VP36-VP43)*(12R^6)/(12R^7)+VP43$
VP38	—		$(VP36-VP43)*(12R^5)/(12R^7)+VP43$
VP39	—		$(VP36-VP43)*(12R^4)/(12R^7)+VP43$
VP40	—		$(VP36-VP43)*(12R^3)/(12R^7)+VP43$
VP41	—		$(VP36-VP43)*(12R^2)/(12R^7)+VP43$
VP42	—		$(VP36-VP43)*12R/(12R^7)+VP43$
VP43	VP43[6:0]	<64	$(VREG1-VGS)*(130R-X^R)/130R$
		>=64	$(VREG1-VGS)*(130R-X^R-1R)/130R$
VP44	—		$(VP43-VP50)*(14R^2+12R^3+10R)/(14R^2+12R^3+10R^2)+VP50$
VP45	—		$(VP43-VP50)*(14R^2+12R^3)/(14R^2+12R^3+10R^2)+VP50$
VP46	—		$(VP43-VP50)*(14R^2+12R^2)/(14R^2+12R^3+10R^2)+VP50$
VP47	—		$(VP43-VP50)*(14R^2+12R)/(14R^2+12R^3+10R^2)+VP50$
VP48	—		$(VP43-VP50)*(14R^2)/(14R^2+12R^3+10R^2)+VP50$
VP49	—		$(VP43-VP50)*14R/(14R^2+12R^3+10R^2)+VP50$
VP50	VP50[3:0]		$(VP43-VP61)*(47R-X^R-7R)/47R+VP61$
VP51	—		$(VP50-VP57)*(12R^2+10R^3+8R)/(12R^2+10R^3+8R^2)+VP57$
VP52	—		$(VP50-VP57)*(12R^2+10R^3)/(12R^2+10R^3+8R^2)+VP57$
VP53	—		$(VP50-VP57)*(12R^2+10R^2)/(12R^2+10R^3+8R^2)+VP57$
VP54	—		$(VP50-VP57)*(12R^2+10R)/(12R^2+10R^3+8R^2)+VP57$
VP55	—		$(VP50-VP57)*(12R^2)/(12R^2+10R^3+8R^2)+VP57$
VP56	—		$(VP50-VP57)*12R/(12R^2+10R^3+8R^2)+VP57$
VP57	VP57[4:0]		$(VP43-VP61)*(47R-X^R-16R)/47R+VP61$
VP58	—		$(VP57-VP59)*35R/(35R^2)+VP59$
VP59	VP59[3:0]		$(VP43-VP61)*(47R-X^R-26R)/47R+VP61$
VP60	—		$(VP59-VP61)*35R/(35R^2)+VP61$
VP61	VP61[5:0]		$(VREG1-VGS)*(65R-X^R)/130R$
VP62	VP62[5:0]		$(VREG1-VGS)*(65R-X^R)/130R$
VP63	VP63[3:0]		$(VREG1-VGS)*(23R-X^R)/130R$

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### 14.3.3. Negative Gamma Correction

Gamma Level	Value "X" in Formula	Formula				
<b>VN63</b>	VN63[3:0]	$(VREG1-VGS)*(130R-X^R)/130R$				
<b>VN62</b>	VN62[5:0]	$(VREG1-VGS)*(130R-X^R)/130R$				
<b>VN61</b>	VN61[5:0]	$(VREG1-VGS)*(130R-X^R)/130R$				
<b>VN60</b>	—	$(VN61-VN59)*35R/(35R^2)+VN59$				
<b>VN59</b>	VN59[3:0]	$(VN61-VN43)*(47R-X^R-7R)/47R+VN43$				
<b>VN58</b>	—	$(VN59-VN57)*35R/(35R^2)+VN57$				
<b>VN57</b>	VN57[4:0]	$(VN61-VN43)*(47R-X^R-2R)/47R+VN43$				
<b>VN56</b>	—	$(VN57-VN50)*(12R+10R^3+8R^2)/(12R^2+10R^3+8R^2)+VN50$				
<b>VN55</b>	—	$(VN57-VN50)*(10R^3+8R^2)/(12R^2+10R^3+8R^2)+VN50$				
<b>VN54</b>	—	$(VN57-VN50)*(10R^2+8R^2)/(12R^2+10R^3+8R^2)+VN50$				
<b>VN53</b>	—	$(VN57-VN50)*(10R+8R^2)/(12R^2+10R^3+8R^2)+VN50$				
<b>VN52</b>	—	$(VN57-VN50)*(8R^2)/(12R^2+10R^3+8R^2)+VN50$				
<b>VN51</b>	—	$(VN57-VN50)*8R/(12R^2+10R^3+8R^2)+VN50$				
<b>VN50</b>	VN50[3:0]	$(VN61-VN43)*(47R-X^R-30R)/47R+VN43$				
<b>VN49</b>	—	$(VN50-VN43)*(14R+12R^3+10R^2)/(14R^2+12R^3+10R^2)+VN43$				
<b>VN48</b>	—	$(VN50-VN43)*(12R^3+10R^2)/(14R^2+12R^3+10R^2)+VN43$				
<b>VN47</b>	—	$(VN50-VN43)*(12R^2+10R^2)/(14R^2+12R^3+10R^2)+VN43$				
<b>VN46</b>	—	$(VN50-VN43)*(12R+10R^2)/(14R^2+12R^3+10R^2)+VN43$				
<b>VN45</b>	—	$(VN50-VN43)*(10R^2)/(14R^2+12R^3+10R^2)+VN43$				
<b>VN44</b>	—	$(VN50-VN43)*10R/(14R^2+12R^3+10R^2)+VN43$				
<b>VN43</b>	VN43[6:0]	<table border="1"> <tr> <td>&lt;64</td> <td><math>(VREG1-VGS)*(130R-X^R)/130R</math></td> </tr> <tr> <td>&gt;=64</td> <td><math>(VREG1-VGS)*(130R-X^R-1R)/130R</math></td> </tr> </table>	<64	$(VREG1-VGS)*(130R-X^R)/130R$	>=64	$(VREG1-VGS)*(130R-X^R-1R)/130R$
<64	$(VREG1-VGS)*(130R-X^R)/130R$					
>=64	$(VREG1-VGS)*(130R-X^R-1R)/130R$					
<b>VN42</b>	—	$(VN43-VN36)*(12R^6)/(12R^7)+VN36$				
<b>VN41</b>	—	$(VN43-VN36)*(12R^5)/(12R^7)+VN36$				
<b>VN40</b>	—	$(VN43-VN36)*(12R^4)/(12R^7)+VN36$				
<b>VN39</b>	—	$(VN43-VN36)*(12R^3)/(12R^7)+VN36$				
<b>VN38</b>	—	$(VN43-VN36)*(12R^2)/(12R^7)+VN36$				
<b>VN37</b>	—	$(VN43-VN36)*12R/(12R^7)+VN36$				
<b>VN36</b>	VN36[3:0]	$(VN43-VN20)*(39R-X^R-7R)/39R+VN20$				
<b>VN35</b>	—	$(VN36-VN27)*(8R^8)/(8R^9)+VN27$				
<b>VN34</b>	—	$(VN36-VN27)*(8R^7)/(8R^9)+VN27$				
<b>VN33</b>	—	$(VN36-VN27)*(8R^6)/(8R^9)+VN27$				
<b>VN32</b>	—	$(VN36-VN27)*(8R^5)/(8R^9)+VN27$				
<b>VN31</b>	—	$(VN36-VN27)*(8R^4)/(8R^9)+VN27$				
<b>VN30</b>	—	$(VN36-VN27)*(8R^3)/(8R^9)+VN27$				
<b>VN29</b>	—	$(VN36-VN27)*(8R^2)/(8R^9)+VN27$				
<b>VN28</b>	—	$(VN36-VN27)*8R/(8R^9)+VN27$				
<b>VN27</b>	VN27[3:0]	$(VN43-VN20)*(39R-X^R-23R)/39R+VN20$				
<b>VN26</b>	—	$(VN27-VN20)*(12R^6)/(12R^7)+VN20$				
<b>VN25</b>	—	$(VN27-VN20)*(12R^5)/(12R^7)+VN20$				
<b>VN24</b>	—	$(VN27-VN20)*(12R^4)/(12R^7)+VN20$				
<b>VN23</b>	—	$(VN27-VN20)*(12R^3)/(12R^7)+VN20$				
<b>VN22</b>	—	$(VN27-VN20)*(12R^2)/(12R^7)+VN20$				
<b>VN21</b>	—	$(VN27-VN20)*12R/(12R^7)+VN20$				
<b>VN20</b>	VN20[6:0]	<table border="1"> <tr> <td>&lt;64</td> <td><math>(VREG1-VGS)*(130R-X^R)/130R</math></td> </tr> <tr> <td>&gt;=64</td> <td><math>(VREG1-VGS)*(130R-X^R-1R)/130R</math></td> </tr> </table>	<64	$(VREG1-VGS)*(130R-X^R)/130R$	>=64	$(VREG1-VGS)*(130R-X^R-1R)/130R$
<64	$(VREG1-VGS)*(130R-X^R)/130R$					
>=64	$(VREG1-VGS)*(130R-X^R-1R)/130R$					
<b>VN19</b>	—	$(VN20-VN13)*(14R^2+12R^3+10R)/(14R^2+12R^3+10R^2)+VN13$				
<b>VN18</b>	—	$(VN20-VN13)*(14R^2+12R^3)/(14R^2+12R^3+10R^2)+VN13$				
<b>VN17</b>	—	$(VN20-VN13)*(14R^2+12R^2)/(14R^2+12R^3+10R^2)+VN13$				
<b>VN16</b>	—	$(VN20-VN13)*(14R^2+12R)/(14R^2+12R^3+10R^2)+VN13$				
<b>VN15</b>	—	$(VN20-VN13)*(14R^2)/(14R^2+12R^3+10R^2)+VN13$				
<b>VN14</b>	—	$(VN20-VN13)*14R/(14R^2+12R^3+10R^2)+VN13$				
<b>VN13</b>	VN13[3:0]	$(VN20-VN2)*(47R-X^R-7R)/47R+VN2$				
<b>VN12</b>	—	$(VN13-VN6)*(12R^2+10R^3+8R)/(12R^2+10R^3+8R^2)+VN6$				
<b>VN11</b>	—	$(VN13-VN6)*(12R^2+10R^3)/(12R^2+10R^3+8R^2)+VN6$				
<b>VN10</b>	—	$(VN13-VN6)*(12R^2+10R^2)/(12R^2+10R^3+8R^2)+VN6$				
<b>VN9</b>	—	$(VN13-VN6)*(12R^2+10R)/(12R^2+10R^3+8R^2)+VN6$				
<b>VN8</b>	—	$(VN13-VN6)*(12R^2)/(12R^2+10R^3+8R^2)+VN6$				
<b>VN7</b>	—	$(VN13-VN6)*12R/(12R^2+10R^3+8R^2)+VN6$				
<b>VN6</b>	VN6[4:0]	$(VN20-VN2)*(47R-X^R-16R)/47R+VN2$				
<b>VN5</b>	—	$(VN6-VN4)*35R/(35R^2)+VN4$				
<b>VN4</b>	VN4[3:0]	$(VN20-VN2)*(47R-X^R-26R)/47R+VN2$				
<b>VN3</b>	—	$(VN4-VN2)*35R/(35R^2)+VN2$				
<b>VN2</b>	VN2[5:0]	$(VREG1-VGS)*(65R-X^R)/130R$				
<b>VN1</b>	VN1[5:0]	$(VREG1-VGS)*(65R-X^R)/130R$				
<b>VN0</b>	VN0[3:0]	$(VREG1-VGS)*(23R-X^R)/130R$				

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## 15. Reset

### 15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's B5=0:00EF h If MADCTL's B5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's B5 = 0:013F h If MADCTL's B5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	013F h	013F h	013F h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

*Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.*

*Note 2: After Powered-On Reset finishes within 10μs after both VCI & VDDI are applied.*

*Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.*

## 15.2. Output Pins, I/O Pins

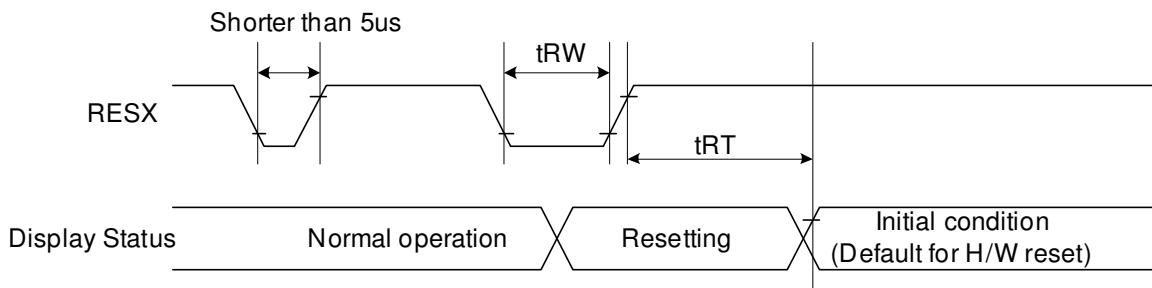
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

*Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.*

## 15.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

## 15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

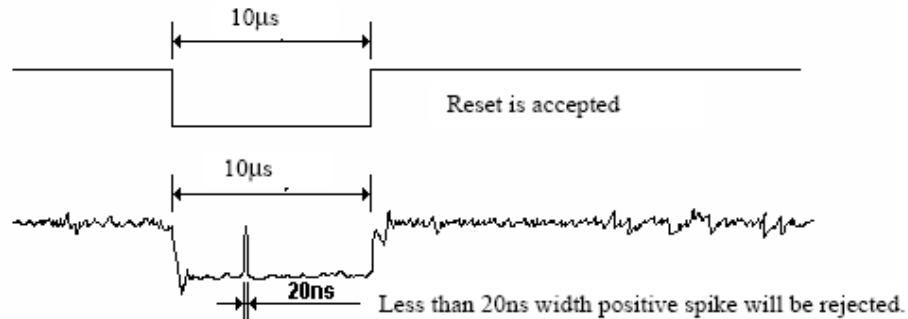
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

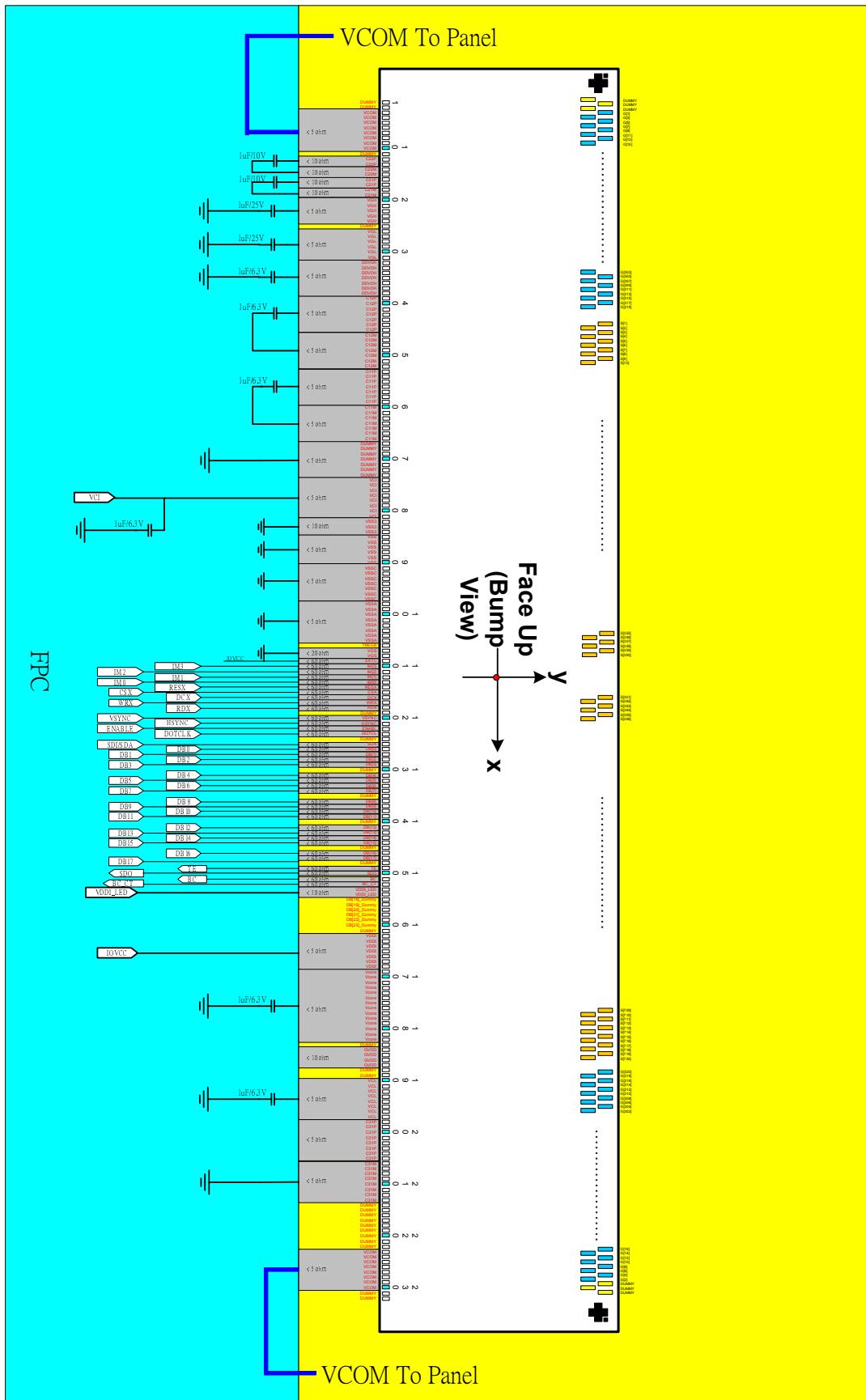


Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 16. Configuration of Power Supply Circuit

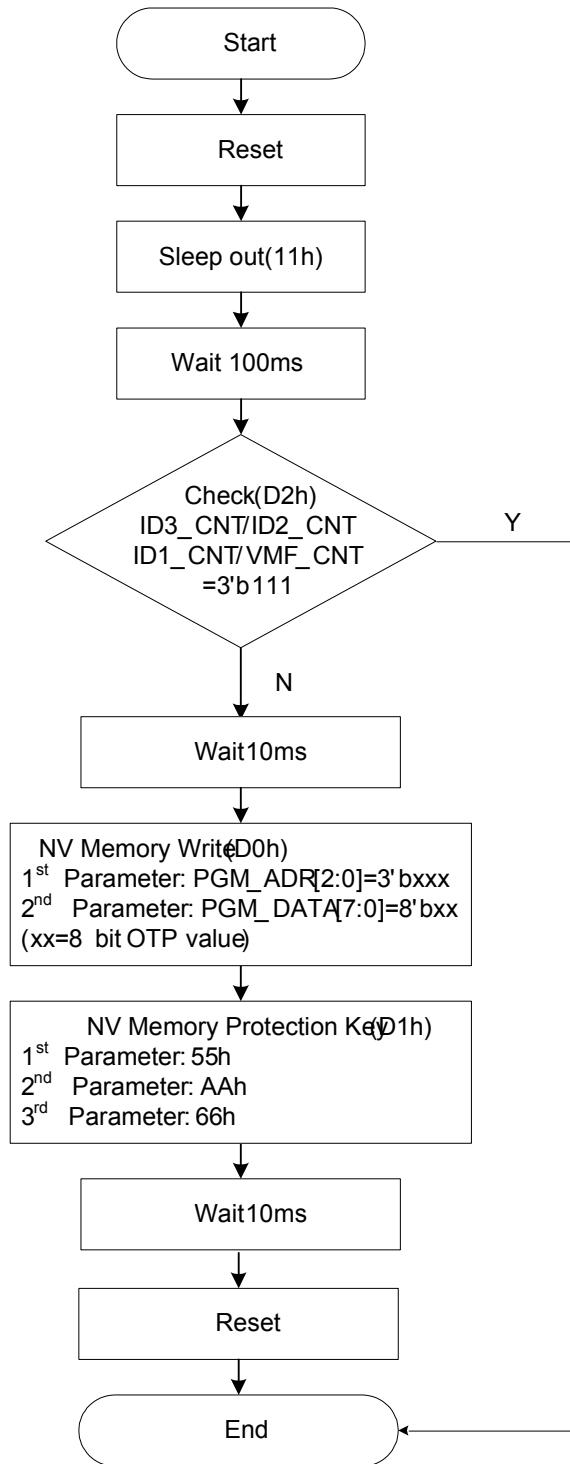


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The Following tables shows specifications of external elements connected to the ILI9341's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 μF (B characteristics)	6.3V	DDVDH ,VCL,C11P/M,C12P/M,Vcore,VCI
	10V	C21P/M,C22P/M
	25V	VGL, VGH

## 17. NV Memory Programming Flow



## 18. Electrical Characteristics

### 18.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9341 is used out of the absolute maximum ratings, ILI9341 may be permanently damaged. To use ILI9341 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9341 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.0
Driver supply voltage	VGH-VGL	V	-0.3 ~ +28.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	°C	-40 ~ +85
Storage temperature	Tstg	°C	-55 ~ +110

*Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.*

## 18.2 DC Characteristics

### 18.2.1 General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
<b>Power and Operation Voltage</b>							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	<b>3.3</b>	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	<b>3.3</b>	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	<b>18.0</b>	Note3
Gate Driver Low Voltage	VGL	V	-	-	<b>-10.0</b>	-5.0	Note3
Driver Supply Voltage	-	V	VGH-VGL	15	-	28	Note3
Current consumption during standby mode	I <sub>ST</sub>	μA	VCI=2.8V , Ta=25 °C	-	-	100	-
<b>Input and Output</b>							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
<b>VCOM Operation</b>							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	VCOMH-VCOML	4.0	-	5.5	Note3
<b>Source Driver</b>							
Source Output Range	Vsout	V	-	0.1	-	DDVDH-0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3
Output Deviation Voltage (Source Output channel)	Vdev	mV	Sout>=4.2V Sout<=0.8V 4.2V>Sout>0.8V	-	-	20 15	Note4 -
Output Offset Voltage	VOFSET	mV	-	-	-	35	Note7
<b>Booster Operation</b>							
1 <sup>st</sup> Booster (VCIx2) Voltage	DDVDH	V	-	4.95 (Note 5)	-	5.8 (Note 6)	Note3
1 <sup>st</sup> Booster (VCIx2 Drop Voltage	VCIx2 drop	%	loading=1mA	-	-	5	Note3
Liner Range	Vliner	V	-	0.2	-	DDVDH-0.2	

Note 1: VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage) °C.

Note2: Please supply digital VDDI voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

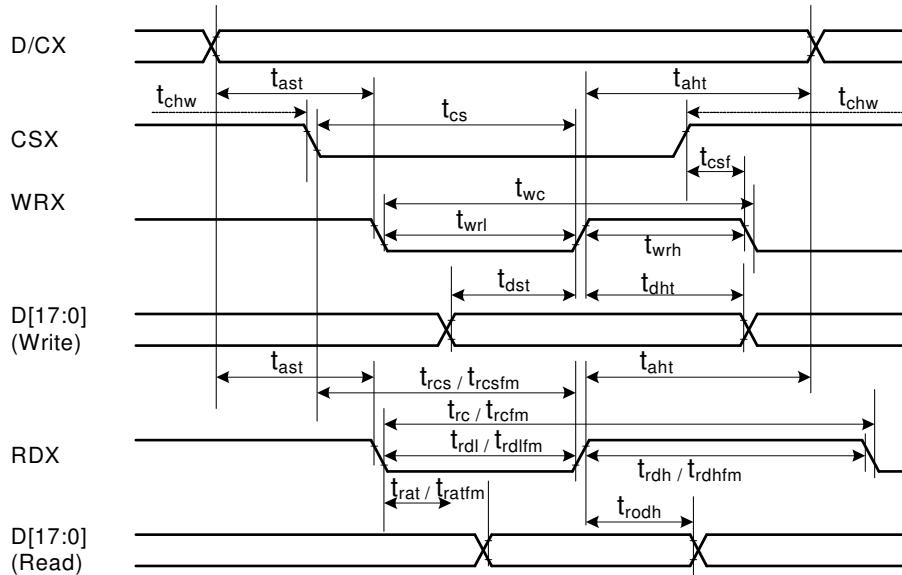
Note5: VCI=2.6V

Note6: VCI=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

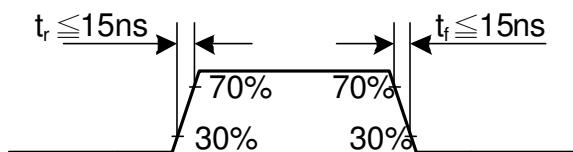
## 18.3 AC Characteristics

### 18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)

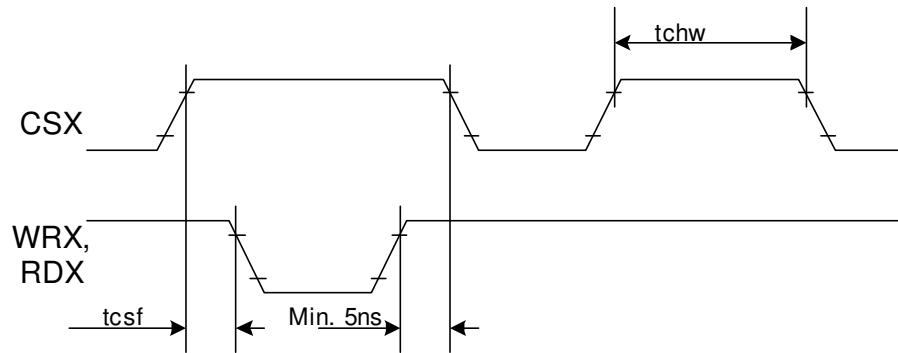


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tch	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note:  $T_a = -30$  to  $70$  °C,  $VDDI=1.65V$  to  $3.3V$ ,  $VCI=2.5V$  to  $3.3V$ ,  $VSS=0V$

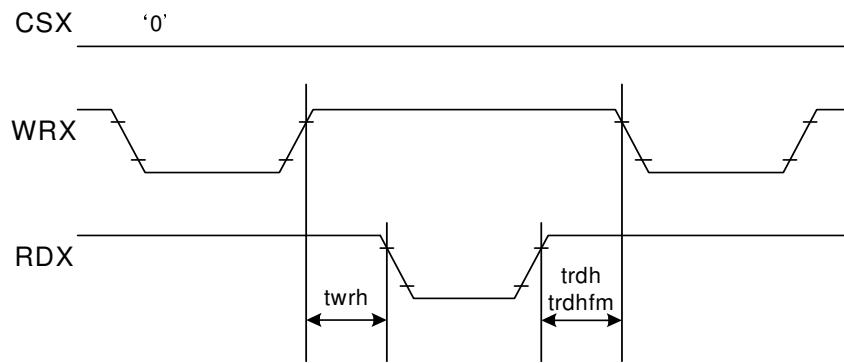


CSX timings :

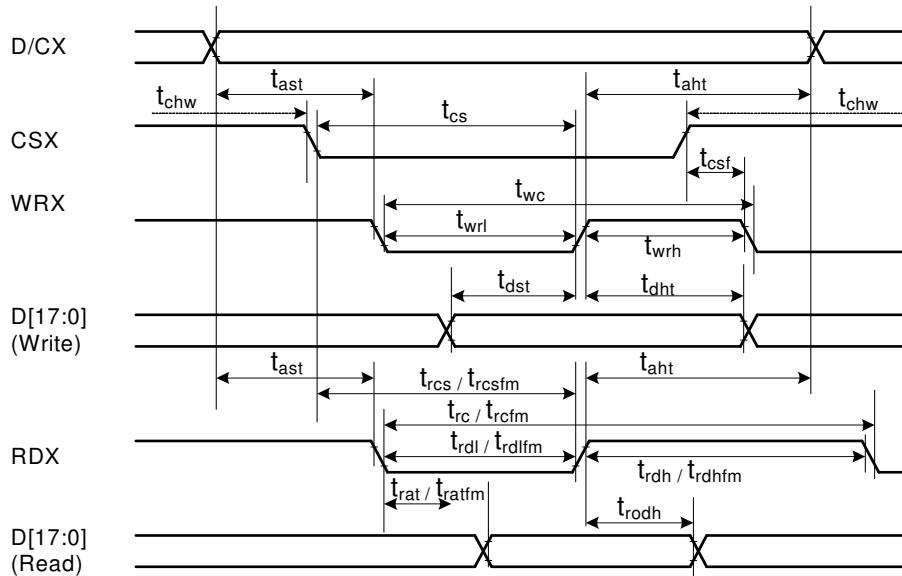


*Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*

Write to read or read to write timings:

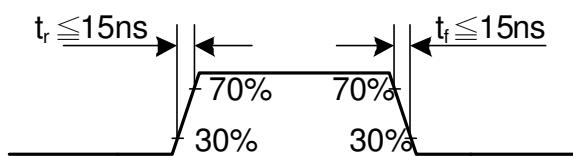


*Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*

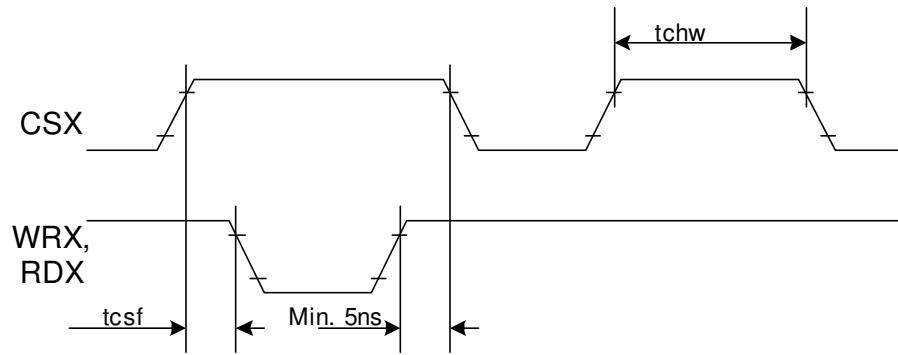
**18.3.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-II system)**


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t <sub>ast</sub>	Address setup time	0	-	ns	
	t <sub>aht</sub>	Address hold time (Write/Read)	0	-	ns	
CSX	t <sub>chw</sub>	CSX "H" pulse width	0	-	ns	
	t <sub>cs</sub>	Chip Select setup time (Write)	15	-	ns	
	t <sub>r<sub>cs</sub></sub>	Chip Select setup time (Read ID)	45	-	ns	
	t <sub>r<sub>csfm</sub></sub>	Chip Select setup time (Read FM)	355	-	ns	
	t <sub>csf</sub>	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t <sub>twc</sub>	Write cycle	66	-	ns	
	t <sub>wrh</sub>	Write Control pulse H duration	15	-	ns	
	t <sub>wrl</sub>	Write Control pulse L duration	15	-	ns	
RDX (FM)	t <sub>rcfm</sub>	Read Cycle (FM)	450	-	ns	
	t <sub>rdhfm</sub>	Read Control pulse H duration (FM)	90	-	ns	
	t <sub>rdlfm</sub>	Read Control pulse L duration (FM)	355	-	ns	
RDX (ID)	t <sub>rc</sub>	Read cycle (ID)	160	-	ns	
	t <sub>rdh</sub>	Read Control pulse H duration	90	-	ns	
	t <sub>rdl</sub>	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	t <sub>dst</sub>	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t <sub>dht</sub>	Write data hold time	10	-	ns	
	t <sub>rat</sub>	Read access time	-	40	ns	
	t <sub>ratfm</sub>	Read access time	-	340	ns	
	t <sub>roodh</sub>	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

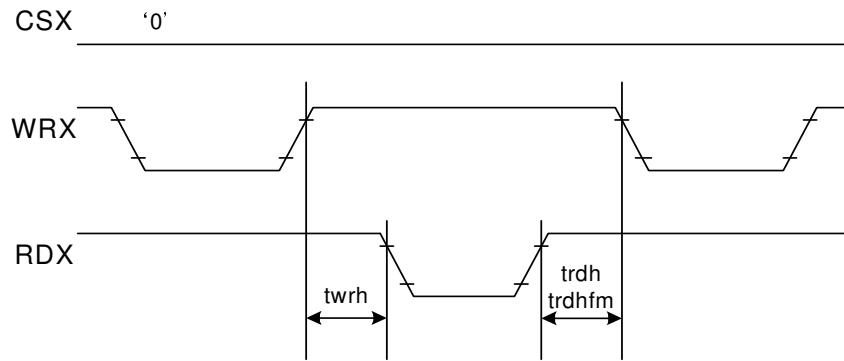


CSX timings :



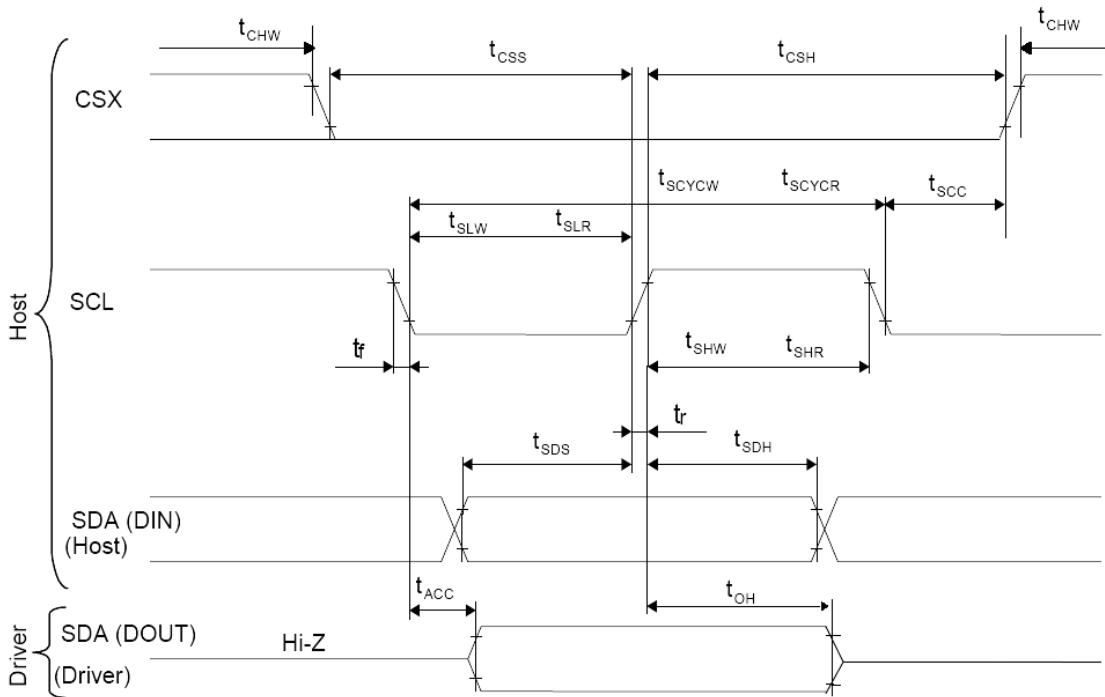
*Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*

Write to read or read to write timings:



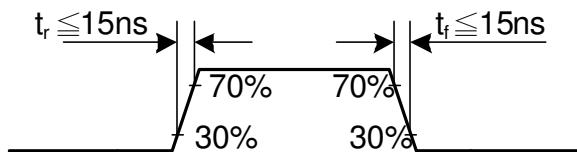
*Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*

### 18.3.3 Display Serial Interface Timing Characteristics (3-line SPI system)

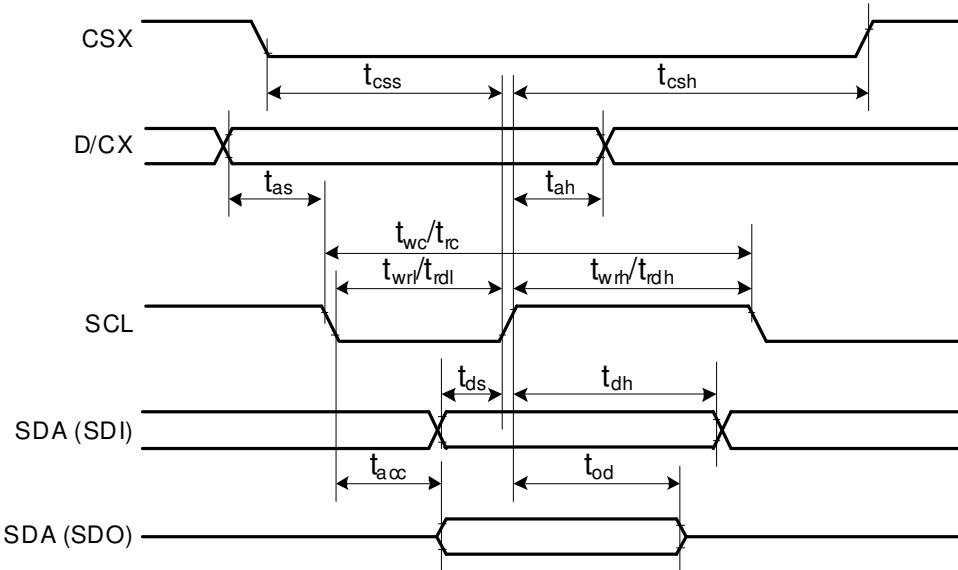


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsd		65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

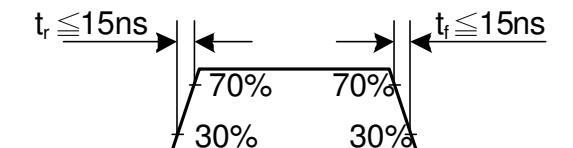


### 18.3.4 Display Serial Interface Timing Characteristics (4-line SPI system)

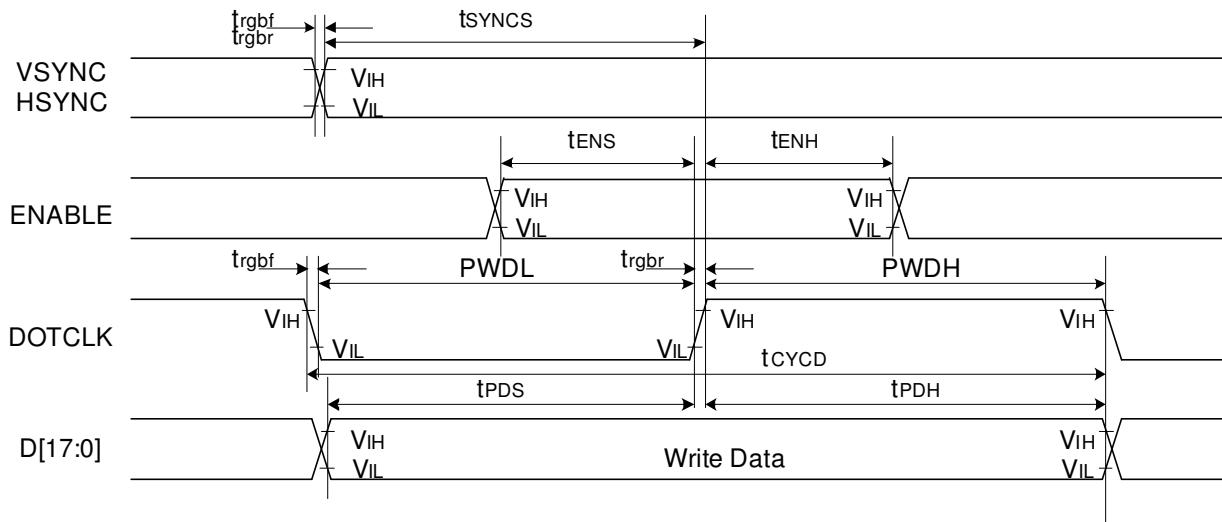


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t <sub>css</sub>	Chip select time (Write)	40	-	ns	
	t <sub>csh</sub>	Chip select hold time (Read)	40	-	ns	
SCL	t <sub>wc</sub>	Serial clock cycle (Write)	100	-	ns	
	t <sub>wrh</sub>	SCL "H" pulse width (Write)	40	-	ns	
	t <sub>wrh</sub>	SCL "L" pulse width (Write)	40	-	ns	
	t <sub>rc</sub>	Serial clock cycle (Read)	150	-	ns	
	t <sub>rdh</sub>	SCL "H" pulse width (Read)	60	-	ns	
	t <sub>rdl</sub>	SCL "L" pulse width (Read)	60	-	ns	
D/CX	t <sub>as</sub>	D/CX setup time	10	-	ns	
	t <sub>tah</sub>	D/CX hold time (Write / Read)	10	-	ns	
SDA / SDI (Input)	t <sub>ds</sub>	Data setup time (Write)	30	-	ns	
	t <sub>dh</sub>	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t <sub>aacc</sub>	Access time (Read)	10	-	ns	For maximum CL=30pF
	t <sub>od</sub>	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note:  $T_a = 25^\circ C$ ,  $VDDI=1.65V$  to  $3.3V$ ,  $VCI=2.5V$  to  $3.3V$ ,  $AGND=VSS=0V$

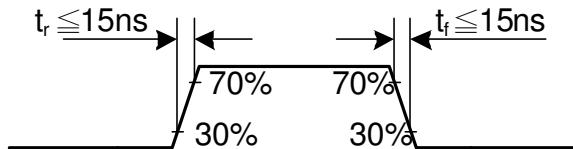


### 18.3.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t <sub>SYNCS</sub>	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t <sub>SYNCH</sub>	VSYNC/HSYNC hold time	15	-	ns	
DE	t <sub>E</sub> <sub>NS</sub>	DE setup time	15	-	ns	18/16-bit bus RGB interface mode
	t <sub>E</sub> <sub>NH</sub>	DE hold time	15	-	ns	
D[17:0]	t <sub>P</sub> <sub>OS</sub>	Data setup time	15	-	ns	6-bit bus RGB interface mode
	t <sub>P</sub> <sub>DH</sub>	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	18/16-bit bus RGB interface mode
	PWDL	DOTCLK low-level period	15	-	ns	
	t <sub>CYCD</sub>	DOTCLK cycle time	100	-	ns	
	t <sub>r</sub> <sub>gbf</sub> , t <sub>r</sub> <sub>gbfr</sub>	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t <sub>SYNCS</sub>	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t <sub>SYNCH</sub>	VSYNC/HSYNC hold time	15	-	ns	
DE	t <sub>E</sub> <sub>NS</sub>	DE setup time	15	-	ns	6-bit bus RGB interface mode
	t <sub>E</sub> <sub>NH</sub>	DE hold time	15	-	ns	
D[17:0]	t <sub>P</sub> <sub>OS</sub>	Data setup time	15	-	ns	6-bit bus RGB interface mode
	t <sub>P</sub> <sub>DH</sub>	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	6-bit bus RGB interface mode
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t <sub>CYCD</sub>	DOTCLK cycle time	100	-	ns	
	t <sub>r</sub> <sub>gbf</sub> , t <sub>r</sub> <sub>gbfr</sub>	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

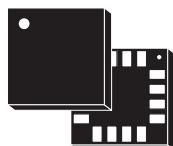


## 19 Revision History

Version No.	Date	Page	Description
V1.00	2010/10/12	All	New Created.
V1.01	2010/10/12	179	Update charge pump ratio
V1.02	2010/12/17	35,195~200	Add description of extend register command
V1.03	2010/12/20	196	Modify description of pumping
V1.04	2010/12/24	All	Update extend register and OTP flow
V1.05	2011/01/05	All	Update extend register
V1.06	2011/01/20	16,230	No.75 pad location, DC Characteristics
V1.07	2011/02/24	199,226,227	Modify register, external element.
V1.08	2011/03/04	179,196,227,228	Analog supply voltage naming, external element, DDVDH Max, Modify C1h,CFh default setting
V1.09	2011/03/15	9,159,197,199,226	Update clock timing, IC Configuration, E8h, EDh
V1.10	2011/04/15	226	Update for general FPC application
V1.11	2011/06/10	13 15 166	Rename pad 231, 232 as INT_TEST1 and INT_TEST2 (please leave these pins as open) Modify chip size 15860u x 650u Modify SM bit gate arrangement
V1.12	2011/07/15	8,14, 230, 231	Modify VGH from 16V to 18V
V1.13	2011/07/20	183, 185, 196, 198, 219-222	Add OTP: ID and VMF x 3 times Add "E9h register, Add power on sequence flow chart Add CFH, Bit[5], Bit[6] and all 3 <sup>rd</sup> parameter description

## MEMS motion sensor: three-axis digital output gyroscope

Datasheet - production data



**LGA-16 (4x4x1 mm)**

### Features

- Three selectable full scales (250/500/2000 dps)
- I<sup>2</sup>C/SPI digital output interface
- 16 bit-rate value data output
- 8-bit temperature data output
- Two digital output lines (interrupt and data ready)
- Integrated low- and high-pass filters with user-selectable bandwidth
- Wide supply voltage: 2.4 V to 3.6 V
- Low voltage-compatible IOs (1.8 V)
- Embedded power-down and sleep mode
- Embedded temperature sensor
- Embedded FIFO
- High shock survivability
- Extended operating temperature range (-40 °C to +85 °C)
- ECOPACK® RoHS and “Green” compliant

### Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics

### Description

The L3GD20 is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface capable of providing the measured angular rate to the external world through a digital interface (I<sup>2</sup>C/SPI).

The sensing element is manufactured using a dedicated micro-machining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics. The L3GD20 has a full scale of ±250/±500/ ±2000 dps and is capable of measuring rates with a user-selectable bandwidth.

The L3GD20 is available in a plastic land grid array (LGA) package and can operate within a temperature range of -40 °C to +85 °C.

**Table 1. Device summary**

Order code	Temperature range (°C)	Package	Packing
L3GD20	-40 to +85	LGA-16 (4x4x1 mm)	Tray
L3GD20TR	-40 to +85	LGA-16 (4x4x1 mm)	Tape and reel

## Contents

<b>1</b>	<b>Block diagram and pin description</b>	<b>6</b>
1.1	Pin description	6
<b>2</b>	<b>Mechanical and electrical specifications</b>	<b>8</b>
2.1	Mechanical characteristics	8
2.2	Electrical characteristics	9
2.3	Temperature sensor characteristics	9
2.4	Communication interface characteristics	10
2.4.1	SPI - serial peripheral interface	10
2.4.2	I2C - Inter IC control interface	11
2.5	Absolute maximum ratings	12
2.6	Terminology	13
2.6.1	Sensitivity	13
2.6.2	Zero-rate level	13
2.7	Soldering information	13
<b>3</b>	<b>Application hints</b>	<b>14</b>
<b>4</b>	<b>Digital main blocks</b>	<b>15</b>
4.1	Block diagram	15
4.2	FIFO	15
4.2.1	Bypass mode	16
4.2.2	FIFO mode	16
4.2.3	Stream mode	17
4.2.4	Bypass-to-stream mode	19
4.2.5	Stream-to-FIFO mode	19
4.2.6	Retrieve data from FIFO	20
<b>5</b>	<b>Digital interfaces</b>	<b>21</b>
5.1	I2C serial interface	21
5.1.1	I2C operation	22
5.2	SPI bus interface	23
5.2.1	SPI read	25

5.2.2	SPI write .....	26
5.2.3	SPI read in 3-wire mode .....	26
<b>6</b>	<b>Output register mapping .....</b>	<b>28</b>
<b>7</b>	<b>Register description .....</b>	<b>30</b>
7.1	WHO_AM_I (0Fh) .....	30
7.2	CTRL_REG1 (20h) .....	30
7.3	CTRL_REG2 (21h) .....	31
7.4	CTRL_REG3 (22h) .....	32
7.5	CTRL_REG4 (23h) .....	33
7.6	CTRL_REG5 (24h) .....	33
7.7	REFERENCE/DATACAPTURE (25h) .....	34
7.8	OUT_TEMP (26h) .....	34
7.9	STATUS_REG (27h) .....	35
7.10	OUT_X_L (28h), OUT_X_H (29h) .....	35
7.11	OUT_Y_L (2Ah), OUT_Y_H (2Bh) .....	35
7.12	OUT_Z_L (2Ch), OUT_Z_H (2Dh) .....	35
7.13	FIFO_CTRL_REG (2Eh) .....	35
7.14	FIFO_SRC_REG (2Fh) .....	36
7.15	INT1_CFG (30h) .....	36
7.16	INT1_SRC (31h) .....	37
7.17	INT1_THS_XH (32h) .....	38
7.18	INT1_THS_XL (33h) .....	38
7.19	INT1_THS_YH (34h) .....	38
7.20	INT1_THS_YL (35h) .....	38
7.21	INT1_THS_ZH (36h) .....	39
7.22	INT1_THS_ZL (37h) .....	39
7.23	INT1_DURATION (38h) .....	39
<b>8</b>	<b>Package information .....</b>	<b>41</b>
<b>9</b>	<b>Revision history .....</b>	<b>42</b>

## List of tables

Table 2.	Pin description . . . . .	6
Table 4.	Mechanical characteristics . . . . .	7
Table 5.	Electrical characteristics . . . . .	8
Table 6.	Electrical characteristics . . . . .	8
Table 7.	SPI slave timing values. . . . .	9
Table 8.	I2C slave timing values (TBC) . . . . .	10
Table 9.	Absolute maximum ratings . . . . .	11
Table 10.	Serial interface pin description . . . . .	20
Table 11.	I2C terminology. . . . .	20
Table 12.	SAD+read/write patterns. . . . .	21
Table 13.	Transfer when master is writing one byte to slave . . . . .	21
Table 14.	Transfer when master is writing multiple bytes to slave . . . . .	22
Table 15.	Transfer when master is receiving (reading) one byte of data from slave . . . . .	22
Table 16.	Transfer when master is receiving (reading) multiple bytes of data from slave . . . . .	22
Table 17.	Register address map. . . . .	27
Table 18.	WHO_AM_I register . . . . .	29
Table 19.	CTRL_REG1 register . . . . .	29
Table 20.	CTRL_REG1 description . . . . .	29
Table 21.	DR and BW configuration setting . . . . .	29
Table 22.	Power mode selection configuration. . . . .	30
Table 23.	CTRL_REG2 register . . . . .	30
Table 24.	CTRL_REG2 description . . . . .	30
Table 25.	High-pass filter mode configuration . . . . .	31
Table 26.	High-pass filter cut off frequency configuration [Hz] . . . . .	31
Table 27.	CTRL_REG1 register . . . . .	31
Table 28.	CTRL_REG3 description . . . . .	31
Table 29.	CTRL_REG4 register . . . . .	32
Table 30.	CTRL_REG4 description . . . . .	32
Table 31.	CTRL_REG5 register . . . . .	32
Table 32.	CTRL_REG5 description . . . . .	32
Table 33.	REFERENCE register. . . . .	33
Table 34.	REFERENCE register description . . . . .	33
Table 35.	OUT_TEMP register . . . . .	33
Table 36.	OUT_TEMP register description. . . . .	33
Table 37.	STATUS_REG register. . . . .	34
Table 38.	STATUS_REG description . . . . .	34
Table 39.	REFERENCE register. . . . .	34
Table 40.	REFERENCE register description . . . . .	35
Table 41.	FIFO mode configuration . . . . .	35
Table 42.	FIFO_SRC register. . . . .	35
Table 43.	FIFO_SRC register description. . . . .	35
Table 44.	INT1_CFG register . . . . .	35
Table 45.	INT1_CFG description . . . . .	36
Table 46.	INT1_SRC register . . . . .	36
Table 47.	INT1_SRC description . . . . .	36
Table 48.	INT1_THS_XH register. . . . .	37
Table 49.	INT1_THS_XH description . . . . .	37
Table 50.	INT1_THS_XL register . . . . .	37

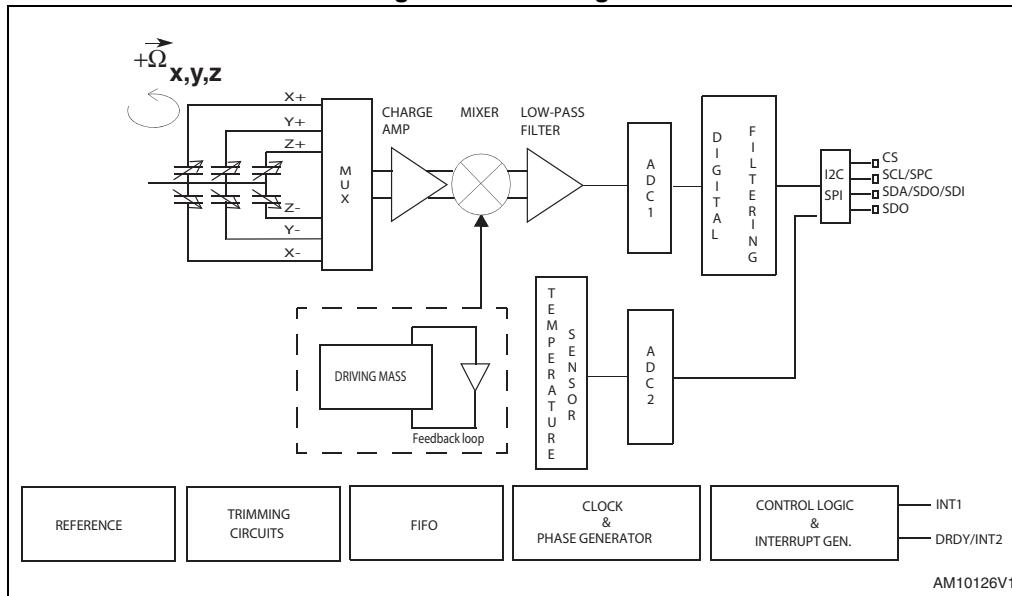
Table 51.	INT1_THS_XL description . . . . .	37
Table 52.	INT1_THS_YH register. . . . .	37
Table 53.	INT1_THS_YH description . . . . .	37
Table 54.	INT1_THS_YL register . . . . .	37
Table 55.	INT1_THS_YL description . . . . .	37
Table 56.	INT1_THS_ZH register . . . . .	38
Table 57.	INT1_THS_ZH description . . . . .	38
Table 58.	INT1_THS_ZL register . . . . .	38
Table 59.	INT1_THS_ZL description . . . . .	38
Table 60.	INT1_DURATION register . . . . .	38
Table 61.	INT1_DURATION description . . . . .	38
Table 62.	Document revision history . . . . .	41

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Pin connection . . . . .	5
Figure 3.	SPI slave timing diagram . . . . .	9
Figure 4.	I2C slave timing diagram . . . . .	10
Figure 5.	L3GD20 electrical connections and external component values . . . . .	13
Figure 6.	Block diagram . . . . .	14
Figure 7.	Bypass mode . . . . .	15
Figure 8.	FIFO mode . . . . .	16
Figure 9.	Stream mode . . . . .	17
Figure 10.	Bypass-to-stream mode . . . . .	18
Figure 11.	Trigger stream mode . . . . .	18
Figure 12.	Read and write protocol . . . . .	23
Figure 13.	SPI read protocol . . . . .	24
Figure 14.	Multiple byte SPI read protocol (2-byte example) . . . . .	24
Figure 15.	SPI write protocol . . . . .	25
Figure 16.	Multiple byte SPI write protocol (2-byte example) . . . . .	25
Figure 17.	SPI read protocol in 3-wire mode . . . . .	26
Figure 18.	INT1_Sel and Out_Sel configuration block diagram . . . . .	33
Figure 19.	Wait disabled . . . . .	39
Figure 20.	Wait enabled . . . . .	39
Figure 21.	LGA-16: mechanical data and package dimensions . . . . .	40

# 1 Block diagram and pin description

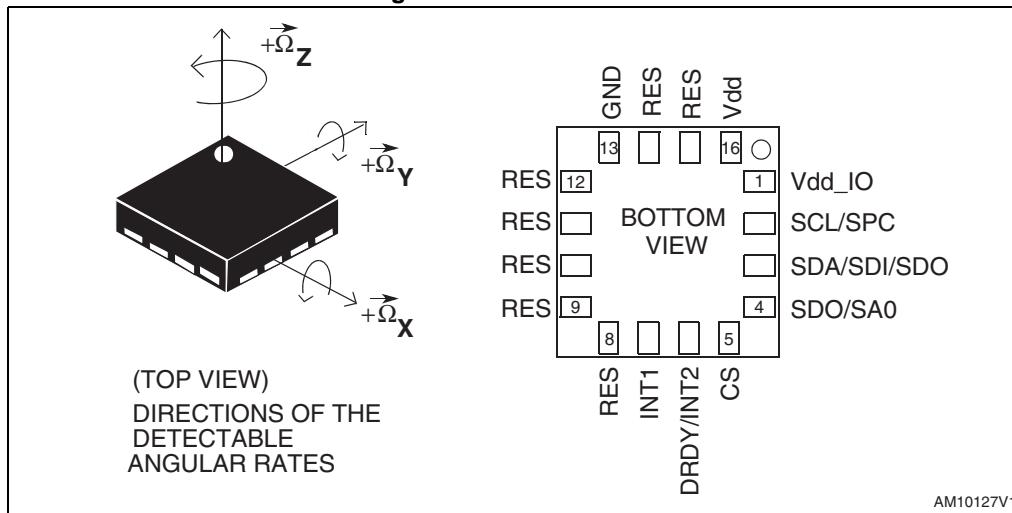
Figure 1. Block diagram



Note: The vibration of the structure is maintained by drive circuitry in a feedback loop. The sensing signal is filtered and appears as a digital signal at the output.

## 1.1 Pin description

Figure 2. Pin connection



**Table 2. Pin description****Table 3.**

Pin#	Name	Function
1	Vdd_IO <sup>(1)</sup>	Power supply for I/O pins
2	SCL SPC	I <sup>2</sup> C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I <sup>2</sup> C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I <sup>2</sup> C less significant bit of the device address (SA0)
5	CS	I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)
6	DRDY/INT2	Data ready/FIFO interrupt (Watermark/Overrun/Empty)
7	INT1	Programmable interrupt
8	Reserved	Connect to GND
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND
12	Reserved	Connect to GND
13	GND	0 V supply
14	Reserved	Connect to GND with ceramic capacitor <sup>(2)</sup>
15	Reserved	Connect to Vdd
16	Vdd <sup>(3)</sup>	Power supply

1. 100 nF filter capacitor recommended.
2. 1 nF min value must be guaranteed under 11 V bias condition.
3. 100 nF plus 10  $\mu$ F capacitors recommended.

## 2 Mechanical and electrical specifications

### 2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted.

**Table 4. Mechanical characteristics<sup>(1)</sup>**

Symbol	Parameter	Test condition	Min.	Typ. <sup>(2)</sup>	Max.	Unit
FS	Measurement range	User-selectable		±250		dps
				±500		
				±2000		
So	Sensitivity	FS = 250 dps		8.75		mdps/digit
		FS = 500 dps		17.50		
		FS = 2000 dps		70		
SoDr	Sensitivity change vs. temperature	From -40 °C to +85 °C		±2		%
DVoff	Digital zero-rate level	FS = 250 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±75		
OffDr	Zero-rate level change vs. temperature	FS = 250 dps		±0.03		dps/°C
		FS = 2000 dps		±0.04		dps/°C
NL	Non linearity	Best fit straight line		0.2		% FS
Rn	Rate noise density			0.03		ips/(√Hz)
ODR	Digital output data rate			95/190/ 380/760		Hz
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V. The operational power supply range is specified in [Table 5](#).

2. Typical specifications are not guaranteed.

## 2.2 Electrical characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

**Table 5. Electrical characteristics (1)**

Symbol	Parameter	Test condition	Min.	Typ. <sup>(2)</sup>	Max.	Unit
Vdd	Supply voltage		2.4	3.0	3.6	V
Vdd_IO	I/O pins supply voltage <sup>(3)</sup>		1.71		Vdd+0.1	V
Idd	Supply current			6.1		mA
IddSL	Supply current in sleep mode <sup>(4)</sup>	Selectable by digital interface		2		mA
IddPdn	Supply current in power-down mode	Selectable by digital interface		5		µA
VIH	Digital high level input voltage		0.8*Vdd_I_O			V
VIL	Digital low level input voltage				0.2*Vdd_I_O	V
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd\_IO without blocking the communication busses; in this condition the measurement chain is powered off.
4. Sleep mode introduces a faster turn-on time relative to power-down mode.

## 2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

**Table 6. Electrical characteristics (1)**

Symbol	Parameter	Test condition	Min.	Typ. <sup>(2)</sup>	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.

## 2.4 Communication interface characteristics

### 2.4.1 SPI - serial peripheral interface

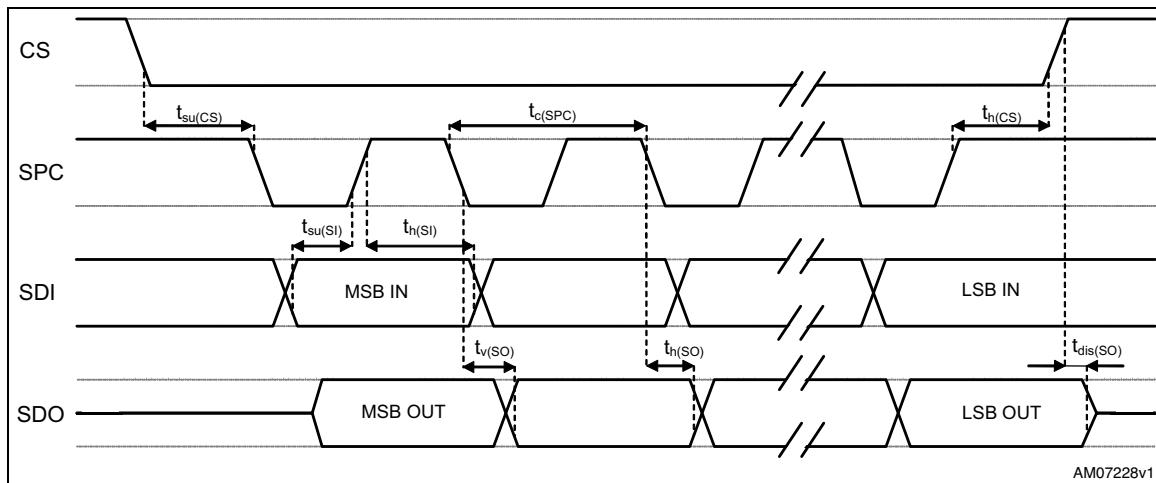
Subject to general operating conditions for Vdd and  $T_{op}$ .

**Table 7. SPI slave timing values**

Symbol	Parameter	Value <sup>(1)</sup>		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	6		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at a 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results; not tested in production.

**Figure 3. SPI slave timing diagram (a)**



a. Measurement points are at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both input and output port.

## 2.4.2 I<sup>2</sup>C - Inter IC control interface

Subject to general operating conditions for Vdd and T<sub>op</sub>.

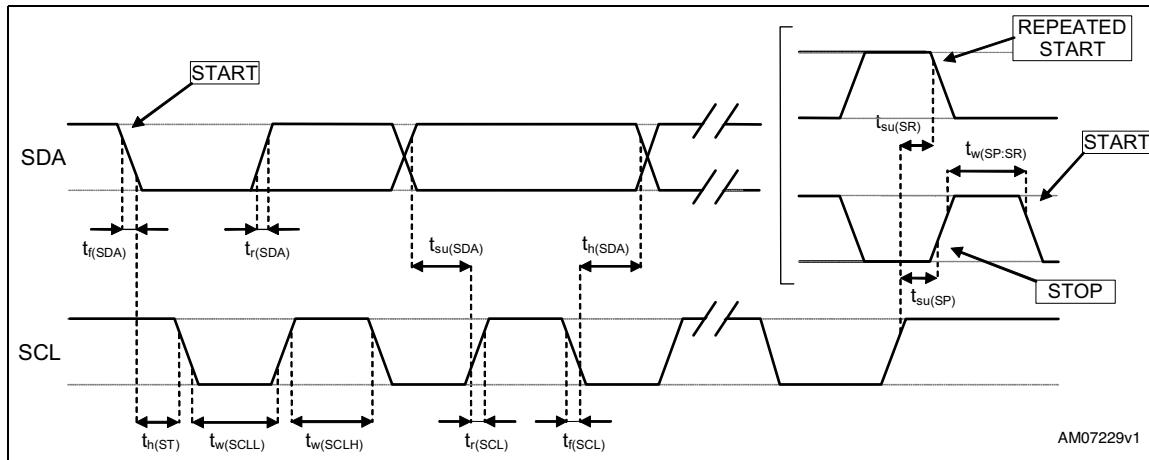
**Table 8. I<sup>2</sup>C slave timing values (TBC)**

Symbol	Parameter	I <sup>2</sup> C standard mode <sup>(1)</sup>		I <sup>2</sup> C fast mode <sup>(1)</sup>		Unit
		Min	Max	Min	Max	
f <sub>(SCL)</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>w(SCLL)</sub>	SCL clock low time	4.7		1.3		$\mu$ s
t <sub>w(SCLH)</sub>	SCL clock high time	4.0		0.6		
t <sub>su(SDA)</sub>	SDA setup time	250		100		
t <sub>h(SDA)</sub>	SDA data hold time	0	3.45	0	0.9	
t <sub>r(SDA)</sub> t <sub>r(SCL)</sub>	SDA and SCL rise time		1000	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	
t <sub>f(SDA)</sub> t <sub>f(SCL)</sub>	SDA and SCL fall time		300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	
t <sub>h(ST)</sub>	START condition hold time	4		0.6		
t <sub>su(SR)</sub>	Repeated START condition setup time	4.7		0.6		
t <sub>su(SP)</sub>	STOP condition setup time	4		0.6		
t <sub>w(SP:SR)</sub>	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I<sup>2</sup>C protocol requirement; not tested in production.

2. C<sub>b</sub> = total capacitance of one bus line, in pF.

**Figure 4. I<sup>2</sup>C slave timing diagram<sup>(b)</sup>**



b. Measurement points are at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both ports.

## 2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 9. Absolute maximum ratings**

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T <sub>STG</sub>	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	g
ESD	Electrostatic discharge protection	2 (HBM)	kV
		1.5 (CDM)	kV
		200 (MM)	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V

*Note:* Supply voltage on any pin should never exceed 4.8 V

 This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

 This is an ESD sensitive device, improper handling can cause permanent damage to the part

## 2.6 Terminology

### 2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counter-clockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

### 2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

## 2.7 Soldering information

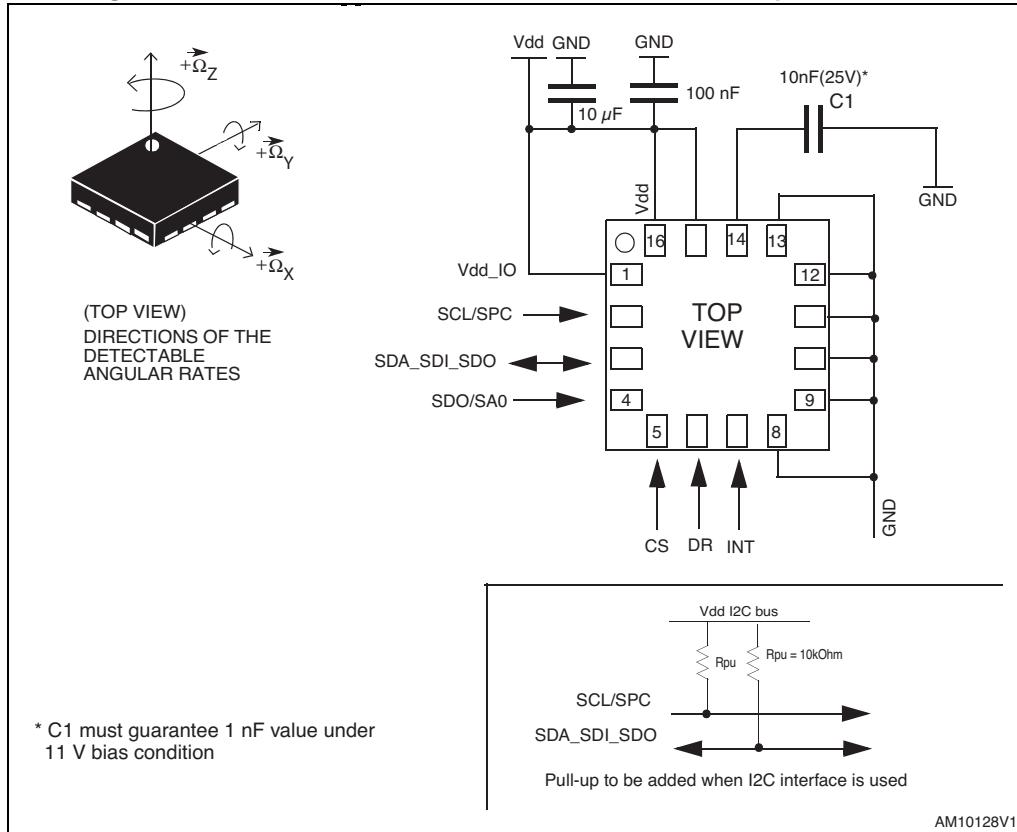
The LGA package is compliant with the ECOPACK<sup>®</sup>, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at [www.st.com/mems](http://www.st.com/mems).

### 3 Application hints

**Figure 5. L3GD20 electrical connections and external component values**



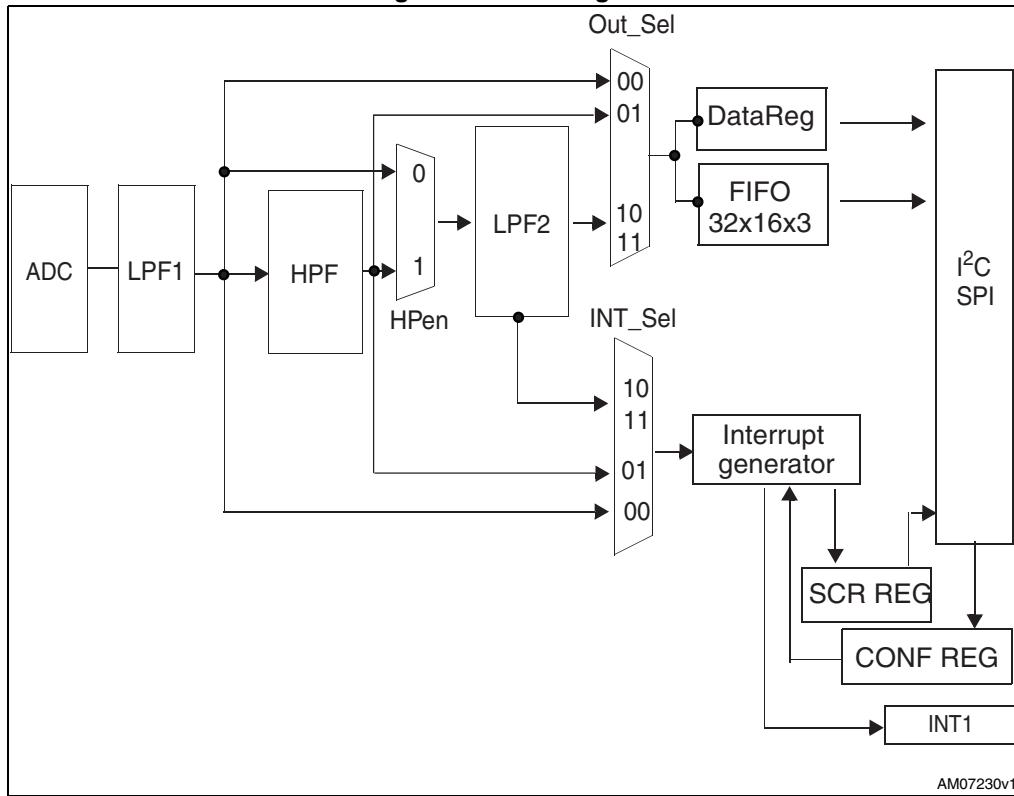
Power supply decoupling capacitors (100 nF + 10  $\mu$ F) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd\_IO are not connected together, 100 nF and 10  $\mu$ F decoupling capacitors must be placed between Vdd and common ground, and 100 nF between Vdd\_IO and common ground. Capacitors should be placed as near as possible to the device (common design practice).

## 4 Digital main blocks

### 4.1 Block diagram

Figure 6. Block diagram

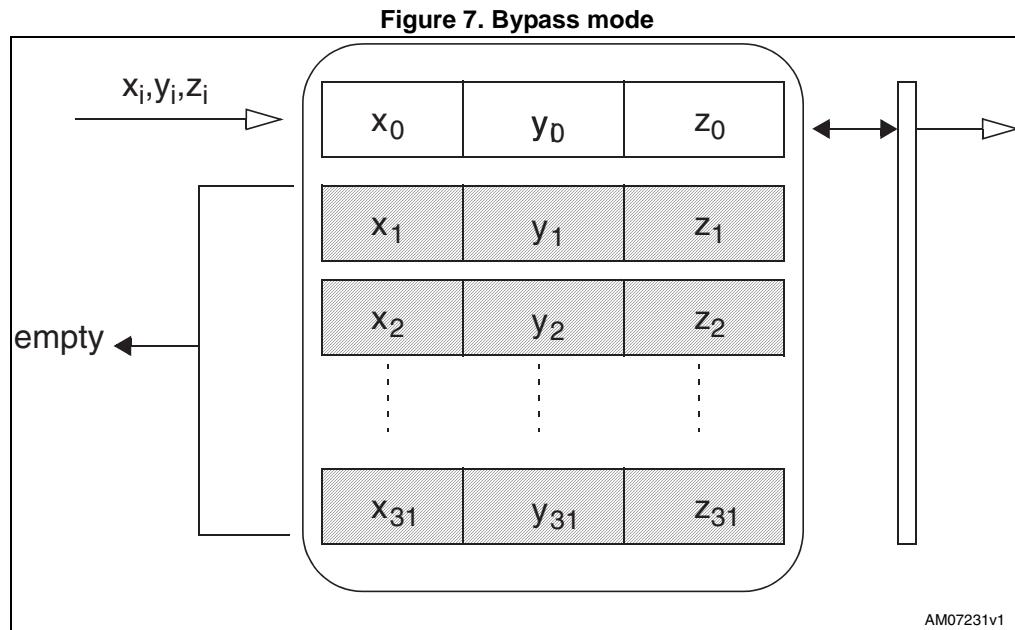


### 4.2 FIFO

The L3GD20 embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO\_MODE bits in the FIFO\_CTRL\_REG (2Eh). Programmable Watermark level, FIFO\_empty or FIFO\_Full events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL\_REG3 (22h) and event detection information is available in FIFO\_SRC\_REG (2Fh). Watermark level can be configured to WTM4:0 in FIFO\_CTRL\_REG (2Eh).

#### 4.2.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in [Figure 7](#) below, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.

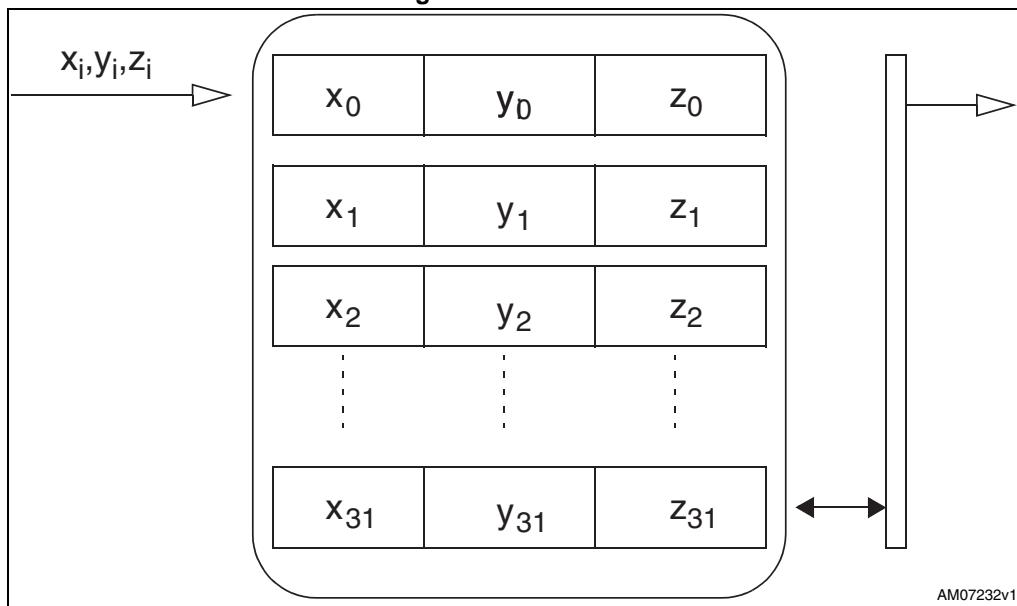


#### 4.2.2 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2\_WMK bit into CTRL\_REG3 (22h)) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of FIFO\_CTRL\_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, the FIFO\_CTRL\_REG (2Eh) must be written back to Bypass mode.

FIFO mode is represented in [Figure 8: FIFO mode](#).

Figure 8. FIFO mode

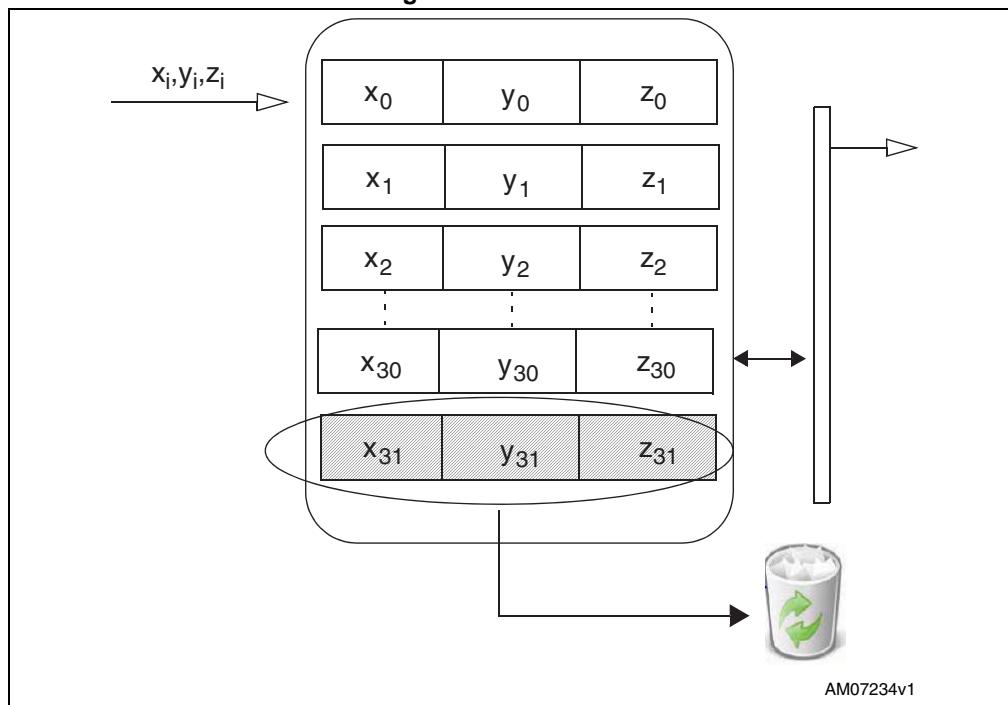


AM07232v1

#### 4.2.3 Stream mode

In Stream mode, data from yaw, pitch and roll measurement are stored in the FIFO. A watermark interrupt can be enabled and set as in the FIFO mode. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL\_REG3 (22h)).

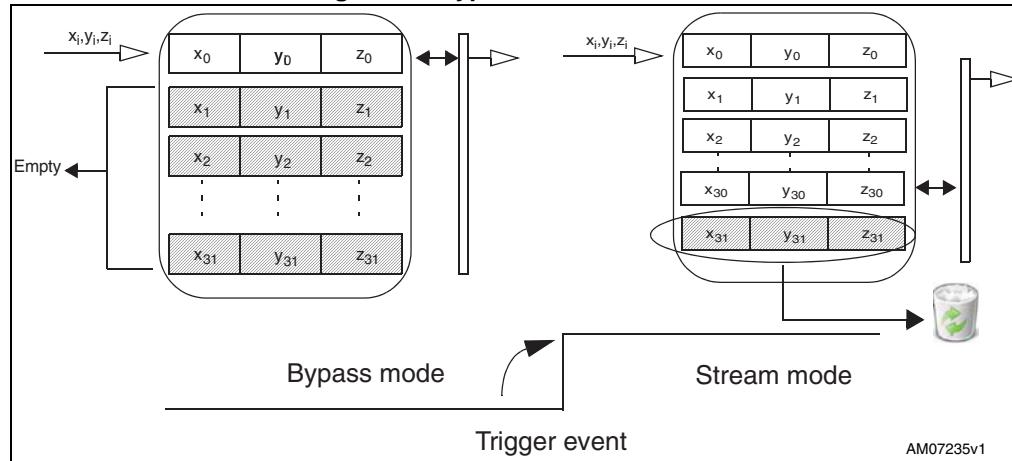
Stream mode is represented in [Figure 9: Stream mode](#).

**Figure 9. Stream mode**

#### 4.2.4 Bypass-to-stream mode

In Bypass-to-stream mode, the FIFO begins operating in Bypass mode and once a trigger event occurs (related to INT1\_CFG (30h) register events), the FIFO starts operating in Stream mode. Refer to [Figure 10](#) below.

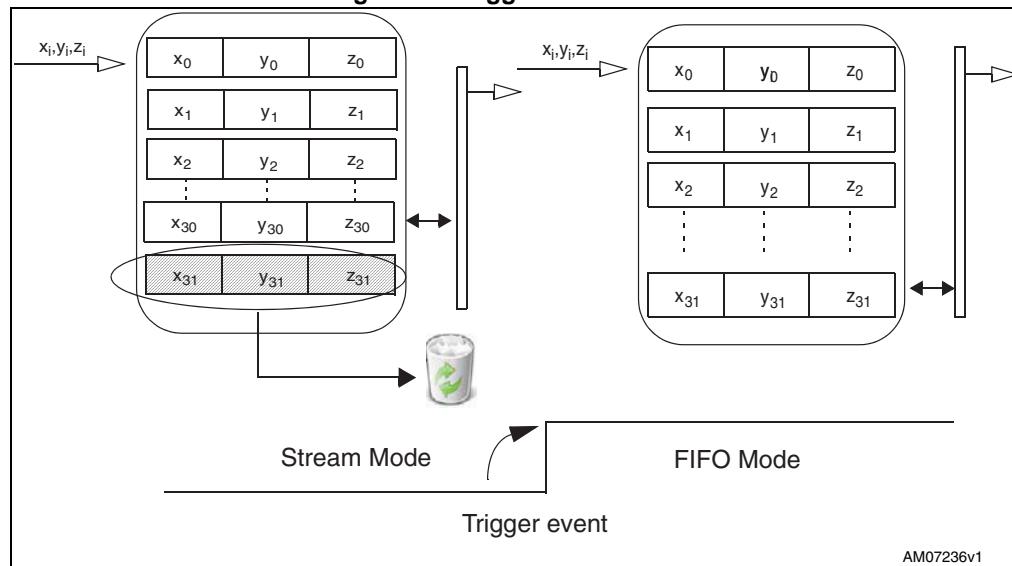
**Figure 10. Bypass-to-stream mode**



#### 4.2.5 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled on pin DRDY/INT2 by setting the I2\_WTM bit in CTRL\_REG3 (22h) in order to be raised when the FIFO is filled to the level specified in the WTM4:0 bits of FIFO\_CTRL\_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to INT1\_CFG (30h) register events), the FIFO starts operating in FIFO mode. Refer to [Figure 11](#) below.

**Figure 11. Trigger stream mode**



#### 4.2.6 Retrieve data from FIFO

FIFO data is read through OUT\_X (Addr reg 28h,29h), OUT\_Y (Addr reg 2Ah,2Bh) and OUT\_Z (Addr reg 2Ch,2Dh). When the FIFO is in Stream, Trigger or FIFO mode, a read operation of the OUT\_X, OUT\_Y or OUT\_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll and yaw data is placed in the OUT\_X, OUT\_Y and OUT\_Z registers and both single read and read\_burst (X,Y & Z with auto-incrementing address) operations can be used. When data included in OUT\_Z\_H (2Dh) is read, the system restarts to read information from addr OUT\_X\_L (28h).

## 5 Digital interfaces

The registers embedded in the L3GD20 may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (i.e connected to Vdd\_IO).

**Table 10. Serial interface pin description**

Pin name	Pin description
CS	I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)
SCL/SPC	I <sup>2</sup> C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I <sup>2</sup> C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO) I <sup>2</sup> C less significant bit of the device address

### 5.1 I<sup>2</sup>C serial interface

The L3GD20 I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write data into registers whose content can also be read back.

The relevant I<sup>2</sup>C terminology is given in the table below.

**Table 11. I<sup>2</sup>C terminology**

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd\_IO through external pull-up resistors. When the bus is free, both lines are high.

The I<sup>2</sup>C interface is compliant with fast mode (400 kHz) I<sup>2</sup>C standards as well as with normal mode.

### 5.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated with the L3GD20 is 110101xb. The **SDO** pin can be used to modify the less significant bit of the device address. If the SDO pin is connected to voltage supply, LSb is '1' (address 1101011b). Otherwise, if the SDO pin is connected to ground, the LSb value is '0' (address 1101010b). This solution allows to connect and address two different gyroscopes to the same I<sup>2</sup>C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obligated to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded in the L3GD20 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. [Table 12](#) explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

**Table 12. SAD+read/write patterns**

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5)
Write	110101	0	0	11010100 (D4)
Read	110101	1	1	11010111 (D7)
Write	110101	1	0	11010110 (D6)

**Table 13. Transfer when master is writing one byte to slave**

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

**Table 14. Transfer when master is writing multiple bytes to slave**

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

**Table 15. Transfer when master is receiving (reading) one byte of data from slave**

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

**Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave**

Master	ST	SAD+W		SUB		SR	SAD+R		MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA	

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to '1' while SUB(6-0) represents the address of the first register to be read.

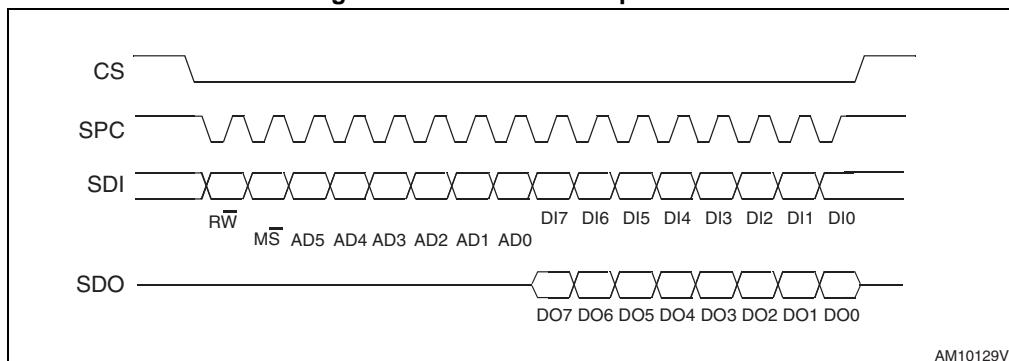
In the communication format presented, MAK is Master Acknowledge and NMAK is No Master Acknowledge.

## 5.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 12. Read and write protocol



**CS** is the Serial Port Enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0:** **RW** bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

**bit 1:** **MS** bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address will be auto-incremented in multiple read/write commands.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

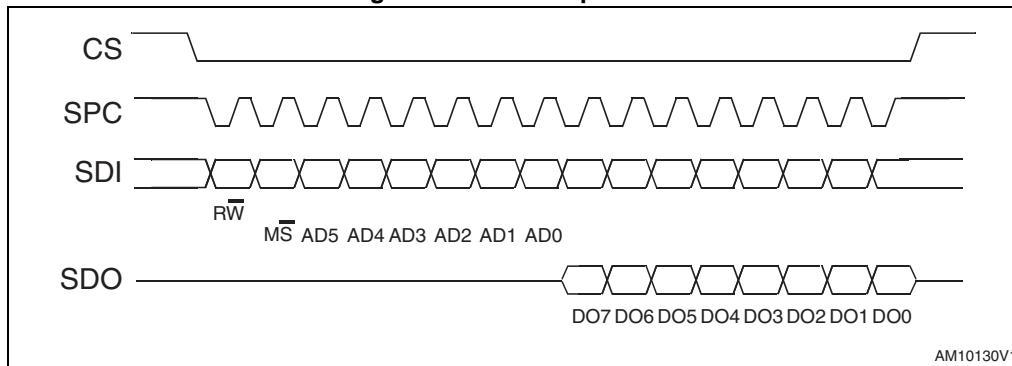
**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods will be added. When the **MS** bit is 0, the address used to read/write data remains the same for every block. When the **MS** bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 5.2.1 SPI read

Figure 13. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0:** READ bit. The value is 1.

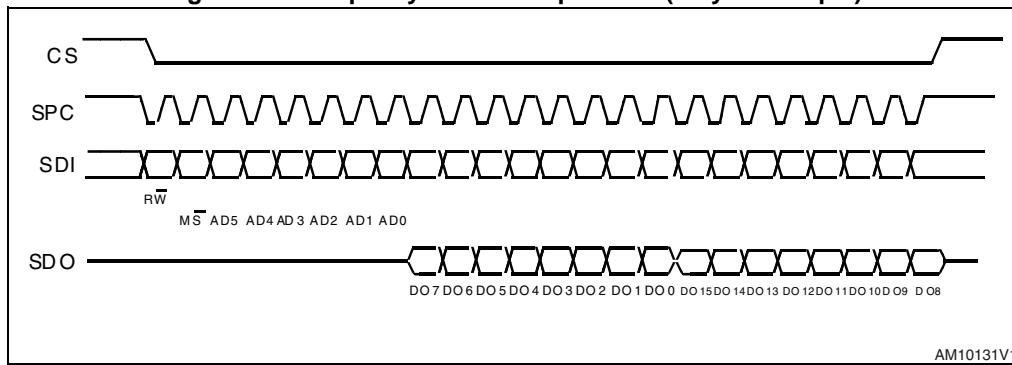
**bit 1:**  $\overline{MS}$  bit. When 0 do not increment address; when 1 increment address in multiple reading.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

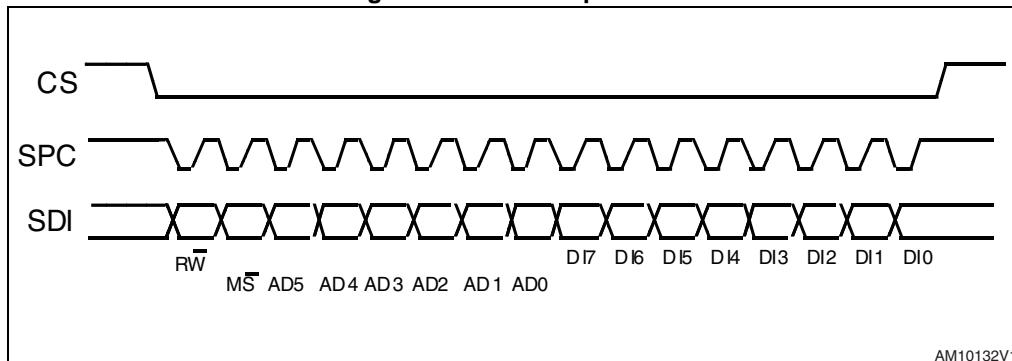
**bit 16-...** : data DO(...-8). Further data in multiple byte reading.

Figure 14. Multiple byte SPI read protocol (2-byte example)



### 5.2.2 SPI write

Figure 15. SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0:** WRITE bit. The value is 0.

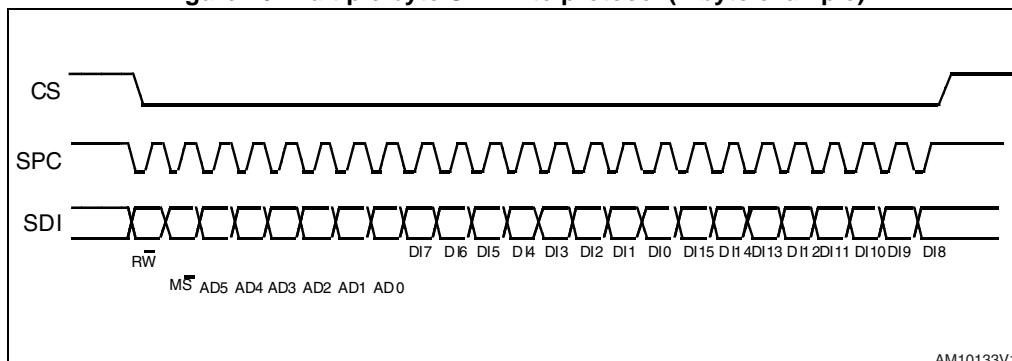
**bit 1:**  $\overline{MS}$  bit. When 0, do not increment address; when 1, increment address in multiple writing.

**bit 2 -7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writing.

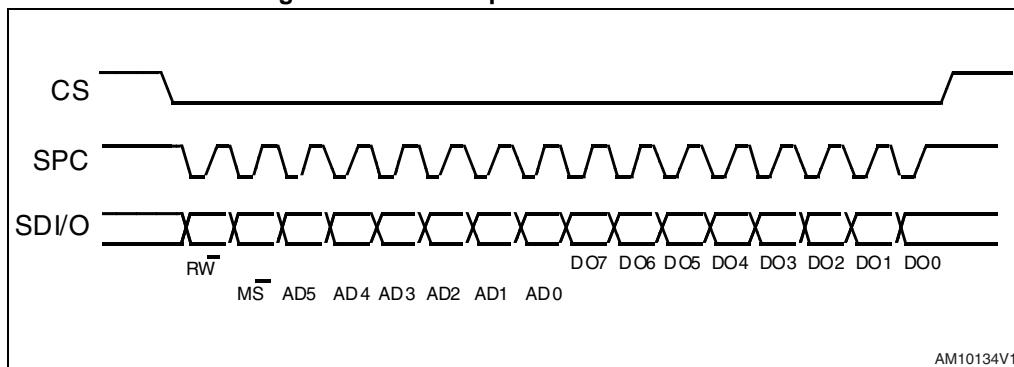
Figure 16. Multiple byte SPI write protocol (2-byte example)



### 5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the bit SIM (SPI serial interface mode selection) to '1' in CTRL\_REG2.

Figure 17. SPI read protocol in 3-wire mode



AM10134V1

The SPI Read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1:**  $\overline{MS}$  bit. When 0, do not increment address; when 1, increment address in multiple reading.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wire mode.

## 6 Output register mapping

The table below provides a listing of the 8-bit registers embedded in the device, and the related addresses:

**Table 17. Register address map**

Name	Type	Register address		Default
		Hex	Binary	
Reserved	-	00-0E	-	-
WHO_AM_I	r	0F	000 1111	11010100
Reserved	-	10-1F	-	-
CTRL_REG1	rw	20	010 0000	00000111
CTRL_REG2	rw	21	010 0001	00000000
CTRL_REG3	rw	22	010 0010	00000000
CTRL_REG4	rw	23	010 0011	00000000
CTRL_REG5	rw	24	010 0100	00000000
REFERENCE	rw	25	010 0101	00000000
OUT_TEMP	r	26	010 0110	output
STATUS_REG	r	27	010 0111	output
OUT_X_L	r	28	010 1000	output
OUT_X_H	r	29	010 1001	output
OUT_Y_L	r	2A	010 1010	output
OUT_Y_H	r	2B	010 1011	output
OUT_Z_L	r	2C	010 1100	output
OUT_Z_H	r	2D	010 1101	output
FIFO_CTRL_REG	rw	2E	010 1110	00000000
FIFO_SRC_REG	r	2F	010 1111	output
INT1_CFG	rw	30	011 0000	00000000
INT1_SRC	r	31	011 0001	output
INT1_TSH_XH	rw	32	011 0010	00000000
INT1_TSH_XL	rw	33	011 0011	00000000
INT1_TSH_YH	rw	34	011 0100	00000000
INT1_TSH_YL	rw	35	011 0101	00000000
INT1_TSH_ZH	rw	36	011 0110	00000000
INT1_TSH_ZL	rw	37	011 0111	00000000
INT1_DURATION	rw	38	011 1000	00000000

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

### 7.1 WHO\_AM\_I (0Fh)

**Table 18. WHO\_AM\_I register**

1	1	0	1	0	1	0	0
---	---	---	---	---	---	---	---

Device identification register.

### 7.2 CTRL\_REG1 (20h)

**Table 19. CTRL\_REG1 register**

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen
-----	-----	-----	-----	----	-----	-----	-----

**Table 20. CTRL\_REG1 description**

DR1-DR0	Output data rate selection. Refer to <a href="#">Table 21</a>
BW1-BW0	Bandwidth selection. Refer to <a href="#">Table 21</a>
PD	Power-down mode enable. Default value: 0 (0: power-down mode, 1: normal mode or sleep mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

**DR<1:0>** is used for ODR selection. **BW <1:0>** is used for Bandwidth selection.

In the [Table 21](#) all frequencies resulting in combinations of DR / BW bits are reported.

**Table 21. DR and BW configuration setting**

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	00	95	12.5
00	01	95	25
00	10	95	25

**Table 21. DR and BW configuration setting (continued)**

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

A combination of **PD**, **Zen**, **Yen**, **Xen** is used to set device to different modes (power-down / normal / sleep mode) in accordance with [Table 22](#) below.

**Table 22. Power mode selection configuration**

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

### 7.3 CTRL\_REG2 (21h)

**Table 23. CTRL\_REG2 register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	HPM1	HPM0	HPCF3	HPCF2	HPCF1	HPCF0
------------------	------------------	------	------	-------	-------	-------	-------

- These bits must be set to '0' to ensure proper operation of the device

**Table 24. CTRL\_REG2 description**

HPM1- HPM0	High-pass filter mode selection. Default value: 00 Refer to <a href="#">Table 25</a>
HPCF3- HPCF0	High-pass filter cutoff frequency selection Refer to <a href="#">Table 26</a>

**Table 25. High-pass filter mode configuration**

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

**Table 26. High-pass filter cut off frequency configuration [Hz]**

HPCF3-0	ODR=95 Hz	ODR=190 Hz	ODR=380 Hz	ODR=760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45
1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

## 7.4 CTRL\_REG3 (22h)

**Table 27. CTRL\_REG1 register**

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty
---------	---------	-----------	-------	---------	--------	---------	----------

**Table 28. CTRL\_REG3 description**

I1_Int1	Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT1. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT1. Default value 0. (0: high; 1:low)
PP_OD	Push-pull / Open drain. Default value: 0. (0: push-pull; 1: open drain)
I2_DRDY	Date-ready on DRDY/INT2. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)

## 7.5 CTRL\_REG4 (23h)

**Table 29. CTRL\_REG4 register**

BDU	BLE	FS1	FS0	-	0 <sup>(1)</sup>	0 <sup>(1)</sup>	SIM
-----	-----	-----	-----	---	------------------	------------------	-----

1. This value must not be changed.

**Table 30. CTRL\_REG4 description**

BDU	Block data update. Default value: 0 (0: continuos update; 1: output registers not updated until MSb and LSb reading)
BLE	Big/little endian data selection. Default value 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS1-FS0	Full scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

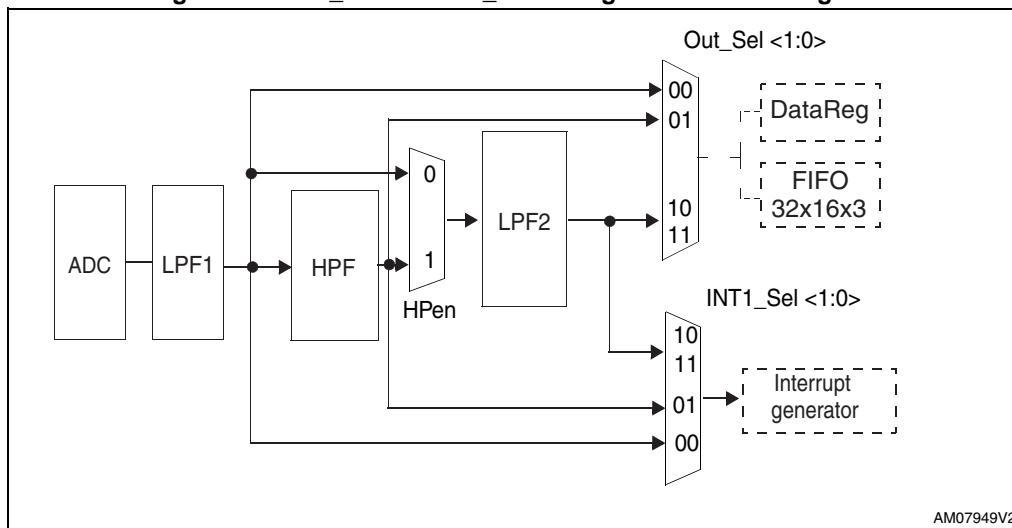
## 7.6 CTRL\_REG5 (24h)

**Table 31. CTRL\_REG5 register**

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0
------	---------	----	------	-----------	-----------	----------	----------

**Table 32. CTRL\_REG5 description**

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
HPen	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled See Figure 20)
INT1_Sel1-INT1_Sel0	INT1 selection configuration. Default value: 0 (See <a href="#">Figure 20</a> )
Out_Sel1-Out_Sel0	Out selection configuration. Default value: 0 (See <a href="#">Figure 20</a> )

**Figure 18. INT1\_Sel and Out\_Sel configuration block diagram**

## 7.7 REFERENCE/DATACAPTURE (25h)

**Table 33. REFERENCE register**

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0
------	------	------	------	------	------	------	------

**Table 34. REFERENCE register description**

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0
------------	--

## 7.8 OUT\_TEMP (26h)

**Table 35. OUT\_TEMP register**

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 36. OUT\_TEMP register description**

Temp7-Temp0	Temperature data
-------------	------------------

Temperature data (1LSB/deg - 8-bit resolution). The value is expressed as two's complement.

## 7.9 STATUS\_REG (27h)

Table 37. STATUS\_REG register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA
-------	-----	-----	-----	-------	-----	-----	-----

Table 38. STATUS\_REG description

ZYXOR	X, Y, Z -axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

## 7.10 OUT\_X\_L (28h), OUT\_X\_H (29h)

X-axis angular rate data. The value is expressed as two's complement.

## 7.11 OUT\_Y\_L (2Ah), OUT\_Y\_H (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

## 7.12 OUT\_Z\_L (2Ch), OUT\_Z\_H (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

## 7.13 FIFO\_CTRL\_REG (2Eh)

Table 39. REFERENCE register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0
-----	-----	-----	------	------	------	------	------

**Table 40. REFERENCE register description**

FM2-FM0	FIFO mode selection. Default value: 00 (see <a href="#">Table 41</a> )
WTM4-WTM0	FIFO threshold. Watermark level setting

**Table 41. FIFO mode configuration**

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

## 7.14 FIFO\_SRC\_REG (2Fh)

**Table 42. FIFO\_SRC register**

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0
-----	------	-------	------	------	------	------	------

**Table 43. FIFO\_SRC register description**

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

## 7.15 INT1\_CFG (30h)

**Table 44. INT1\_CFG register**

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
--------	-----	------	------	------	------	------	------

**Table 45. INT1\_CFG description**

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events)
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

## 7.16 INT1\_SRC (31h)

Interrupt source register. Read only register.

**Table 46. INT1\_SRC register**

0	IA	ZH	ZL	YH	YL	XH	XL
---	----	----	----	----	----	----	----

**Table 47. INT1\_SRC description**

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Reading at this address clears INT1\_SRC IA bit (and eventually the interrupt signal on the INT1 pin) and allows the refresh of data in the INT1\_SRC register if the latched option was chosen.

## 7.17 INT1\_THS\_XH (32h)

**Table 48. INT1\_THS\_XH register**

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8
---	--------	--------	--------	--------	--------	-------	-------

**Table 49. INT1\_THS\_XH description**

THSX14 - THSX9	Interrupt threshold. Default value: 0000 0000
----------------	---

## 7.18 INT1\_THS\_XL (33h)

**Table 50. INT1\_THS\_XL register**

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 51. INT1\_THS\_XL description**

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000
---------------	---

## 7.19 INT1\_THS\_YH (34h)

**Table 52. INT1\_THS\_YH register**

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8
---	--------	--------	--------	--------	--------	-------	-------

**Table 53. INT1\_THS\_YH description**

THSY14 - THSY9	Interrupt threshold. Default value: 0000 0000
----------------	---

## 7.20 INT1\_THS\_YL (35h)

**Table 54. INT1\_THS\_YL register**

THSY7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0
-------	-------	-------	-------	-------	-------	-------	-------

**Table 55. INT1\_THS\_YL description**

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000
---------------	---

## 7.21 INT1\_THS\_ZH (36h)

Table 56. INT1\_THS\_ZH register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8
---	--------	--------	--------	--------	--------	-------	-------

Table 57. INT1\_THS\_ZH description

THSZ14 - THSZ9	Interrupt threshold. Default value: 0000 0000
----------------	---

## 7.22 INT1\_THS\_ZL (37h)

Table 58. INT1\_THS\_ZL register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0
-------	-------	-------	-------	-------	-------	-------	-------

Table 59. INT1\_THS\_ZL description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000
---------------	---

## 7.23 INT1\_DURATION (38h)

Table 60. INT1\_DURATION register

WAIT	D6	D5	D4	D3	D2	D1	D0
------	----	----	----	----	----	----	----

Table 61. INT1\_DURATION description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following definitions:

Wait = '0': the interrupt falls immediately if the signal crosses the selected threshold

Wait = '1': if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 19. Wait disabled

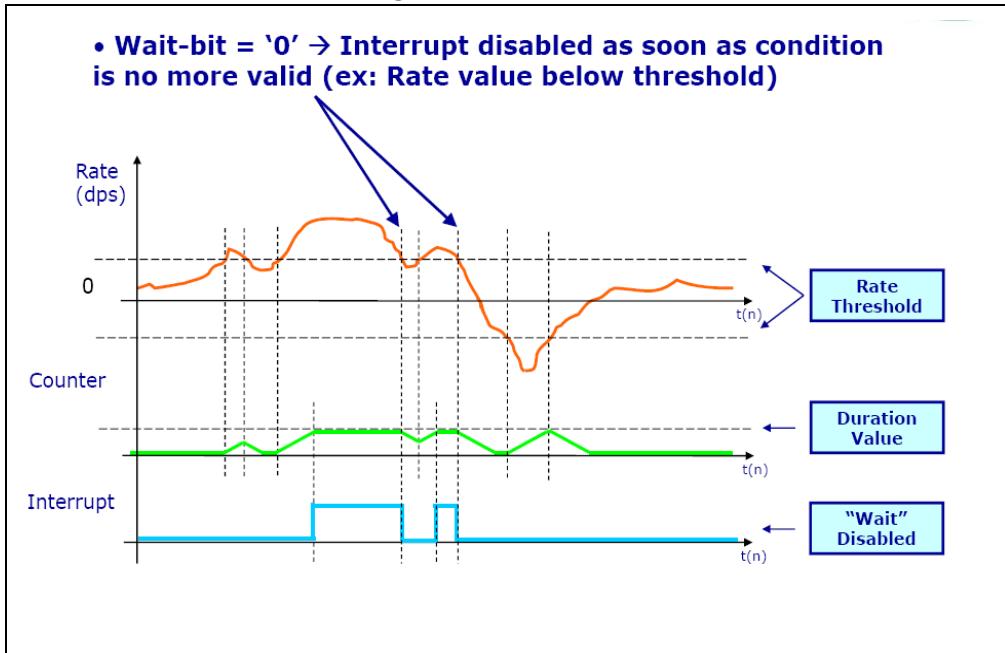
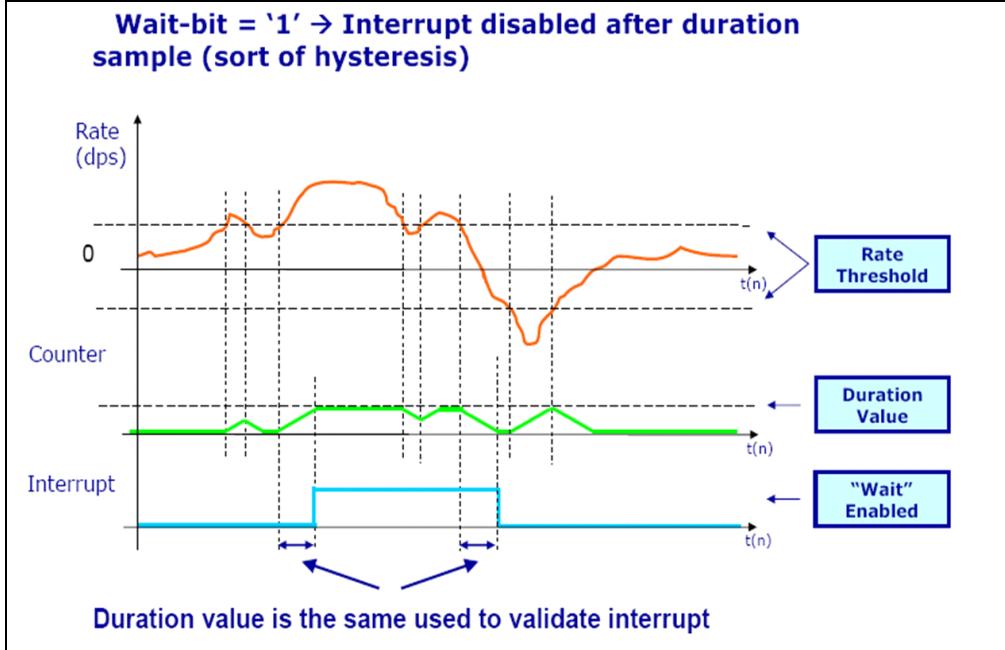


Figure 20. Wait enabled



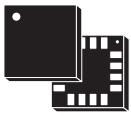
## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
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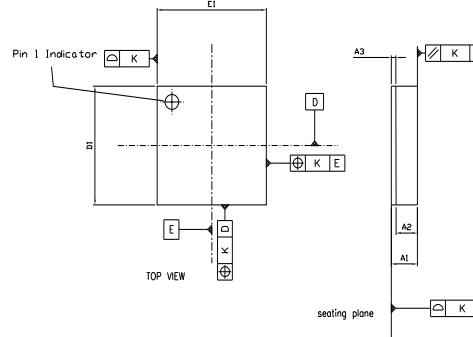
**Figure 21. LGA-16: mechanical data and package dimensions**

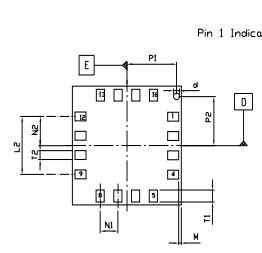
Ref.	Dimensions			inch		
	mm		Max.	Min.		Typ.
	Min.	Typ.		Max.	Min.	
A1		1.000			0.0394	
A2	0.785			0.0309		
A3	0.200			0.0079		
d	0.300			0.0118		
D1	3.850	4.000	4.150	0.1516	0.1575	0.1634
E1	3.850	4.000	4.150	0.1516	0.1575	0.1634
L2	1.950			0.0768		
M	0.100			0.0039		
N1	0.650			0.0256		
N2	0.975			0.0384		
P1	1.750			0.0689		
P2	1.525			0.0600		
T1	0.400			0.0157		
T2	0.300			0.0118		
k	0.050			0.0020		

**Outline and mechanical data**



**LGA-16 (4x4x1mm)  
Land Grid Array Package**





8125097\_A

## 9 Revision history

**Table 62. Document revision history**

Date	Revision	Changes
18-Aug-2011	1	Initial release.
27-Feb-2013	2	Updated <a href="#">Table 12: SAD+read/write patterns</a> and <a href="#">Table 23: CTRL_REG2 register</a> .

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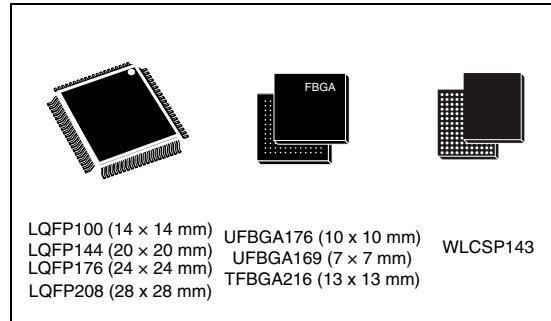
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32b Arm® Cortex®-M4 MCU+FPU, 225DMIPS, up to 2MB Flash/256+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 20 com. interfaces, camera & LCD-TFT

Datasheet - production data

## Features

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 180 MHz, MPU, 225 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 2 MB of Flash memory organized into two banks allowing read-while-write
  - Up to 256+4 KB of SRAM including 64-KB of CCM (core coupled memory) data RAM
  - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, Compact Flash/NOR/NAND memories
- LCD parallel interface, 8080/6800 modes
- LCD-TFT controller with fully programmable resolution (total width up to 4096 pixels, total height up to 2048 lines and pixel clock up to 83 MHz)
- Chrom-ART Accelerator™ for enhanced graphic content creation (DMA2D)
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - $V_{BAT}$  supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 180 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input



- Debug mode
  - SWD & JTAG interfaces
  - Cortex-M4 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
  - Up to 164 fast I/Os up to 90 MHz
  - Up to 166 5 V-tolerant I/Os
- Up to 21 communication interfaces
  - Up to 3 × I<sup>2</sup>C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/4 UARTs (11.25 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 6 SPIs (45 Mbit/s), 2 with muxed full-duplex I<sup>2</sup>S for audio class accuracy via internal audio PLL or external clock
  - 1 x SAI (serial audio interface)
  - 2 × CAN (2.0B Active) and SDIO interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

**Table 1. Device summary**

Reference	Part number
STM32F427xx	STM32F427VG, STM32F427ZG, STM32F427IG, STM32F427AG, STM32F427VI, STM32F427ZI, STM32F427II, STM32F427AI
STM32F429xx	STM32F429VG, STM32F429ZG, STM32F429IG, STM32F429BG, STM32F429NG, STM32F429AG, STM32F429VI, STM32F429ZI, STM32F429II, STM32F429BI, STM32F429NI, STM32F429AI, STM32F429VE, STM32F429ZE, STM32F429IE, STM32F429BE, STM32F429NE

## Contents

<b>1</b>	<b>Introduction</b>	<b>13</b>
<b>2</b>	<b>Description</b>	<b>14</b>
2.1	Full compatibility throughout the family	18
<b>3</b>	<b>Functional overview</b>	<b>21</b>
3.1	Arm® Cortex®-M4 with FPU and embedded Flash and SRAM	21
3.2	Adaptive real-time memory accelerator (ART Accelerator™)	21
3.3	Memory protection unit	21
3.4	Embedded Flash memory	22
3.5	CRC (cyclic redundancy check) calculation unit	22
3.6	Embedded SRAM	22
3.7	Multi-AHB bus matrix	22
3.8	DMA controller (DMA)	23
3.9	Flexible memory controller (FMC)	24
3.10	LCD-TFT controller (available only on STM32F429xx)	24
3.11	Chrom-ART Accelerator™ (DMA2D)	25
3.12	Nested vectored interrupt controller (NVIC)	25
3.13	External interrupt/event controller (EXTI)	25
3.14	Clocks and startup	25
3.15	Boot modes	26
3.16	Power supply schemes	26
3.17	Power supply supervisor	26
3.17.1	Internal reset ON	26
3.17.2	Internal reset OFF	27
3.18	Voltage regulator	28
3.18.1	Regulator ON	28
3.18.2	Regulator OFF	29
3.18.3	Regulator ON/OFF and internal reset ON/OFF availability	32
3.19	Real-time clock (RTC), backup SRAM and backup registers	32
3.20	Low-power modes	33
3.21	$V_{BAT}$ operation	34

3.22	Timers and watchdogs . . . . .	34
3.22.1	Advanced-control timers (TIM1, TIM8) . . . . .	36
3.22.2	General-purpose timers (TIMx) . . . . .	36
3.22.3	Basic timers TIM6 and TIM7 . . . . .	36
3.22.4	Independent watchdog . . . . .	37
3.22.5	Window watchdog . . . . .	37
3.22.6	SysTick timer . . . . .	37
3.23	Inter-integrated circuit interface (I <sup>2</sup> C) . . . . .	37
3.24	Universal synchronous/asynchronous receiver transmitters (USART) . . . . .	37
3.25	Serial peripheral interface (SPI) . . . . .	38
3.26	Inter-integrated sound (I <sup>2</sup> S) . . . . .	39
3.27	Serial Audio interface (SAI1) . . . . .	39
3.28	Audio PLL (PLLI2S) . . . . .	39
3.29	Audio and LCD PLL(PLLSAI) . . . . .	39
3.30	Secure digital input/output interface (SDIO) . . . . .	40
3.31	Ethernet MAC interface with dedicated DMA and IEEE 1588 support . . . . .	40
3.32	Controller area network (bxCAN) . . . . .	40
3.33	Universal serial bus on-the-go full-speed (OTG_FS) . . . . .	41
3.34	Universal serial bus on-the-go high-speed (OTG_HS) . . . . .	41
3.35	Digital camera interface (DCMI) . . . . .	42
3.36	Random number generator (RNG) . . . . .	42
3.37	General-purpose input/outputs (GPIOs) . . . . .	42
3.38	Analog-to-digital converters (ADCs) . . . . .	42
3.39	Temperature sensor . . . . .	43
3.40	Digital-to-analog converter (DAC) . . . . .	43
3.41	Serial wire JTAG debug port (SWJ-DP) . . . . .	43
3.42	Embedded Trace Macrocell™ . . . . .	44
<b>4</b>	<b>Pinouts and pin description . . . . .</b>	<b>45</b>
<b>5</b>	<b>Memory mapping . . . . .</b>	<b>86</b>
<b>6</b>	<b>Electrical characteristics . . . . .</b>	<b>91</b>
6.1	Parameter conditions . . . . .	91
6.1.1	Minimum and maximum values . . . . .	91

6.1.2	Typical values . . . . .	91
6.1.3	Typical curves . . . . .	91
6.1.4	Loading capacitor . . . . .	91
6.1.5	Pin input voltage . . . . .	91
6.1.6	Power supply scheme . . . . .	92
6.1.7	Current consumption measurement . . . . .	93
6.2	Absolute maximum ratings . . . . .	93
6.3	Operating conditions . . . . .	95
6.3.1	General operating conditions . . . . .	95
6.3.2	VCAP1/VCAP2 external capacitor . . . . .	97
6.3.3	Operating conditions at power-up / power-down (regulator ON) . . . . .	98
6.3.4	Operating conditions at power-up / power-down (regulator OFF) . . . . .	98
6.3.5	Reset and power control block characteristics . . . . .	99
6.3.6	Over-drive switching characteristics . . . . .	100
6.3.7	Supply current characteristics . . . . .	101
6.3.8	Wakeup time from low-power modes . . . . .	117
6.3.9	External clock source characteristics . . . . .	118
6.3.10	Internal clock source characteristics . . . . .	122
6.3.11	PLL characteristics . . . . .	124
6.3.12	PLL spread spectrum clock generation (SSCG) characteristics . . . . .	127
6.3.13	Memory characteristics . . . . .	129
6.3.14	EMC characteristics . . . . .	131
6.3.15	Absolute maximum ratings (electrical sensitivity) . . . . .	133
6.3.16	I/O current injection characteristics . . . . .	134
6.3.17	I/O port characteristics . . . . .	135
6.3.18	NRST pin characteristics . . . . .	141
6.3.19	TIM timer characteristics . . . . .	142
6.3.20	Communications interfaces . . . . .	142
6.3.21	12-bit ADC characteristics . . . . .	157
6.3.22	Temperature sensor characteristics . . . . .	163
6.3.23	V <sub>BAT</sub> monitoring characteristics . . . . .	164
6.3.24	Reference voltage . . . . .	164
6.3.25	DAC electrical characteristics . . . . .	165
6.3.26	FMC characteristics . . . . .	168
6.3.27	Camera interface (DCMI) timing specifications . . . . .	193
6.3.28	LCD-TFT controller (LTDC) characteristics . . . . .	194
6.3.29	SD/SDIO MMC card host interface (SDIO) characteristics . . . . .	196

---

6.3.30	RTC characteristics . . . . .	197
<b>7</b>	<b>Package information . . . . .</b>	<b>198</b>
7.1	LQFP100 package information . . . . .	198
7.2	WLCSP143 package information . . . . .	202
7.3	LQFP144 package information . . . . .	205
7.4	LQFP176 package information . . . . .	209
7.5	LQFP208 package information . . . . .	213
7.6	UFBGA169 package information . . . . .	217
7.7	UFBGA176+25 package information . . . . .	220
7.8	TFBGA216 package information . . . . .	223
7.9	Thermal characteristics . . . . .	225
<b>8</b>	<b>Part numbering . . . . .</b>	<b>226</b>
<b>Appendix A</b>	<b>Recommendations when using internal reset OFF . . . . .</b>	<b>227</b>
A.1	Operating conditions . . . . .	227
<b>Appendix B</b>	<b>Application block diagrams . . . . .</b>	<b>228</b>
B.1	USB OTG full speed (FS) interface solutions . . . . .	228
B.2	USB OTG high speed (HS) interface solutions . . . . .	230
B.3	Ethernet interface solutions . . . . .	231
<b>9</b>	<b>Revision history . . . . .</b>	<b>233</b>

## List of tables

Table 1.	Device summary . . . . .	2
Table 2.	STM32F427xx and STM32F429xx features and peripheral counts . . . . .	16
Table 3.	Voltage regulator configuration mode versus device operating mode . . . . .	29
Table 4.	Regulator ON/OFF and internal reset ON/OFF availability. . . . .	32
Table 5.	Voltage regulator modes in stop mode . . . . .	33
Table 6.	Timer feature comparison . . . . .	35
Table 7.	Comparison of I2C analog and digital filters . . . . .	37
Table 8.	USART feature comparison . . . . .	38
Table 9.	Legend/abbreviations used in the pinout table . . . . .	53
Table 10.	STM32F427xx and STM32F429xx pin and ball definitions . . . . .	53
Table 11.	FMC pin definition . . . . .	72
Table 12.	STM32F427xx and STM32F429xx alternate function mapping . . . . .	75
Table 13.	STM32F427xx and STM32F429xx register boundary addresses. . . . .	87
Table 14.	Voltage characteristics . . . . .	93
Table 15.	Current characteristics . . . . .	94
Table 16.	Thermal characteristics. . . . .	94
Table 17.	General operating conditions . . . . .	95
Table 18.	Limitations depending on the operating power supply range . . . . .	97
Table 19.	VCAP1/VCAP2 operating conditions . . . . .	97
Table 20.	Operating conditions at power-up / power-down (regulator ON) . . . . .	98
Table 21.	Operating conditions at power-up / power-down (regulator OFF). . . . .	98
Table 22.	reset and power control block characteristics . . . . .	99
Table 23.	Over-drive switching characteristics . . . . .	100
Table 24.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM . . . . .	102
Table 25.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled). . . . .	103
Table 26.	Typical and maximum current consumption in Sleep mode . . . . .	104
Table 27.	Typical and maximum current consumptions in Stop mode . . . . .	105
Table 28.	Typical and maximum current consumptions in Standby mode . . . . .	106
Table 29.	Typical and maximum current consumptions in $V_{BAT}$ mode. . . . .	106
Table 30.	Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), $VDD=1.7\text{ V}$ . . . . .	108
Table 31.	Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch). . . . .	109
Table 32.	Typical current consumption in Sleep mode, regulator ON, $VDD=1.7\text{ V}$ . . . . .	110
Table 33.	Tyical current consumption in Sleep mode, regulator OFF. . . . .	111
Table 34.	Switching output I/O current consumption . . . . .	113
Table 35.	Peripheral current consumption . . . . .	114
Table 36.	Low-power mode wakeup timings . . . . .	117
Table 37.	High-speed external user clock characteristics. . . . .	118
Table 38.	Low-speed external user clock characteristics . . . . .	119
Table 39.	HSE 4–26 MHz oscillator characteristics . . . . .	120
Table 40.	LSE oscillator characteristics ( $f_{LSE} = 32.768\text{ kHz}$ ) . . . . .	121
Table 41.	HSI oscillator characteristics . . . . .	122
Table 42.	LSI oscillator characteristics . . . . .	123
Table 43.	Main PLL characteristics. . . . .	124

Table 44.	PLL2S (audio PLL) characteristics . . . . .	125
Table 45.	PLLISAI (audio and LCD-TFT PLL) characteristics . . . . .	126
Table 46.	SSCG parameters constraint . . . . .	127
Table 47.	Flash memory characteristics . . . . .	129
Table 48.	Flash memory programming . . . . .	129
Table 49.	Flash memory programming with V <sub>PP</sub> . . . . .	130
Table 50.	Flash memory endurance and data retention . . . . .	131
Table 51.	EMS characteristics . . . . .	131
Table 52.	EMI characteristics . . . . .	132
Table 53.	ESD absolute maximum ratings . . . . .	133
Table 54.	Electrical sensitivities . . . . .	133
Table 55.	I/O current injection susceptibility . . . . .	134
Table 56.	I/O static characteristics . . . . .	135
Table 57.	Output voltage characteristics . . . . .	138
Table 58.	I/O AC characteristics . . . . .	139
Table 59.	NRST pin characteristics . . . . .	141
Table 60.	TIMx characteristics . . . . .	142
Table 61.	I2C analog filter characteristics . . . . .	143
Table 62.	SPI dynamic characteristics . . . . .	143
Table 63.	I <sup>2</sup> S dynamic characteristics . . . . .	146
Table 64.	SAI characteristics . . . . .	148
Table 65.	USB OTG full speed startup time . . . . .	150
Table 66.	USB OTG full speed DC electrical characteristics . . . . .	150
Table 67.	USB OTG full speed electrical characteristics . . . . .	151
Table 68.	USB HS DC electrical characteristics . . . . .	151
Table 69.	USB HS clock timing parameters . . . . .	152
Table 70.	Dynamic characteristics: USB ULPI . . . . .	153
Table 71.	Dynamics characteristics: Ethernet MAC signals for SMI . . . . .	154
Table 72.	Dynamics characteristics: Ethernet MAC signals for RMII . . . . .	155
Table 73.	Dynamics characteristics: Ethernet MAC signals for MII . . . . .	156
Table 74.	ADC characteristics . . . . .	157
Table 75.	ADC static accuracy at f <sub>ADC</sub> = 18 MHz . . . . .	158
Table 76.	ADC static accuracy at f <sub>ADC</sub> = 30 MHz . . . . .	159
Table 77.	ADC static accuracy at f <sub>ADC</sub> = 36 MHz . . . . .	159
Table 78.	ADC dynamic accuracy at f <sub>ADC</sub> = 18 MHz - limited test conditions . . . . .	159
Table 79.	ADC dynamic accuracy at f <sub>ADC</sub> = 36 MHz - limited test conditions . . . . .	159
Table 80.	Temperature sensor characteristics . . . . .	163
Table 81.	Temperature sensor calibration values . . . . .	163
Table 82.	V <sub>BAT</sub> monitoring characteristics . . . . .	164
Table 83.	internal reference voltage . . . . .	164
Table 84.	Internal reference voltage calibration values . . . . .	164
Table 85.	DAC characteristics . . . . .	165
Table 86.	Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings . . . . .	169
Table 87.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings . . . . .	170
Table 88.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . . .	171
Table 89.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings . . . . .	172
Table 90.	Asynchronous multiplexed PSRAM/NOR read timings . . . . .	173
Table 91.	Asynchronous multiplexed PSRAM/NOR read-NWAIT timings . . . . .	173
Table 92.	Asynchronous multiplexed PSRAM/NOR write timings . . . . .	174

Table 93.	Asynchronous multiplexed PSRAM/NOR write-NWAIT timings . . . . .	175
Table 94.	Synchronous multiplexed NOR/PSRAM read timings . . . . .	176
Table 95.	Synchronous multiplexed PSRAM write timings . . . . .	178
Table 96.	Synchronous non-multiplexed NOR/PSRAM read timings . . . . .	179
Table 97.	Synchronous non-multiplexed PSRAM write timings . . . . .	180
Table 98.	Switching characteristics for PC Card/CF read and write cycles in attribute/common space. . . . .	185
Table 99.	Switching characteristics for PC Card/CF read and write cycles in I/O space . . . . .	186
Table 100.	Switching characteristics for NAND Flash read cycles . . . . .	188
Table 101.	Switching characteristics for NAND Flash write cycles . . . . .	189
Table 102.	SDRAM read timings . . . . .	190
Table 103.	LPSDR SDRAM read timings . . . . .	190
Table 104.	SDRAM write timings . . . . .	192
Table 105.	LPSDR SDRAM write timings . . . . .	192
Table 106.	DCMI characteristics. . . . .	193
Table 107.	LTDC characteristics . . . . .	194
Table 108.	Dynamic characteristics: SD / MMC characteristics . . . . .	197
Table 109.	RTC characteristics . . . . .	197
Table 110.	LQFP100 100-pin, 14 x 14 mm low-profile quad flat package mechanical data . . . . .	199
Table 111.	WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data . . . . .	203
Table 112.	WLCSP143 recommended PCB design rules (0.4 mm pitch) . . . . .	204
Table 113.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data . . . . .	206
Table 114.	LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data . . . . .	209
Table 115.	LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package mechanical data . . . . .	214
Table 116.	UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data . . . . .	217
Table 117.	UFBGA169 recommended PCB design rules (0.5 mm pitch BGA) . . . . .	218
Table 118.	UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data . . . . .	220
Table 119.	UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA) . . . . .	221
Table 120.	TFBGA216 - 216 ball 13 x 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data . . . . .	223
Table 121.	Package thermal characteristics . . . . .	225
Table 122.	Ordering information scheme . . . . .	226
Table 123.	Limitations depending on the operating power supply range . . . . .	227
Table 124.	Document revision history . . . . .	233

## List of figures

Figure 1.	Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package . . . . .	18
Figure 2.	Compatible board design between STM32F10xx/STM32F2xx/STM32F4xx for LQFP144 package . . . . .	19
Figure 3.	Compatible board design between STM32F2xx and STM32F4xx for LQFP176 and UFBGA176 packages . . . . .	19
Figure 4.	STM32F427xx and STM32F429xx block diagram . . . . .	20
Figure 5.	STM32F427xx and STM32F429xx Multi-AHB matrix . . . . .	23
Figure 6.	Power supply supervisor interconnection with internal reset OFF . . . . .	27
Figure 7.	PDR_ON control with internal reset OFF . . . . .	28
Figure 8.	Regulator OFF . . . . .	30
Figure 9.	Startup in regulator OFF: slow V <sub>DD</sub> slope - power-down reset risen after V <sub>CAP_1</sub> /V <sub>CAP_2</sub> stabilization . . . . .	31
Figure 10.	Startup in regulator OFF mode: fast V <sub>DD</sub> slope - power-down reset risen before V <sub>CAP_1</sub> /V <sub>CAP_2</sub> stabilization . . . . .	31
Figure 11.	STM32F42x LQFP100 pinout . . . . .	45
Figure 12.	STM32F42x WLCSP143 ballout . . . . .	46
Figure 13.	STM32F42x LQFP144 pinout . . . . .	47
Figure 14.	STM32F42x LQFP176 pinout . . . . .	48
Figure 15.	STM32F42x LQFP208 pinout . . . . .	49
Figure 16.	STM32F42x UFBGA169 ballout . . . . .	50
Figure 17.	STM32F42x UFBGA176 ballout . . . . .	51
Figure 18.	STM32F42x TFBGA216 ballout . . . . .	52
Figure 19.	Memory map . . . . .	86
Figure 20.	Pin loading conditions . . . . .	91
Figure 21.	Pin input voltage . . . . .	91
Figure 22.	Power supply scheme . . . . .	92
Figure 23.	Current consumption measurement scheme . . . . .	93
Figure 24.	External capacitor C <sub>EXT</sub> . . . . .	97
Figure 25.	Typical V <sub>BAT</sub> current consumption (LSE and RTC ON/backup RAM OFF) . . . . .	107
Figure 26.	Typical V <sub>BAT</sub> current consumption (LSE and RTC ON/backup RAM ON) . . . . .	107
Figure 27.	High-speed external clock source AC timing diagram . . . . .	119
Figure 28.	Low-speed external clock source AC timing diagram . . . . .	120
Figure 29.	Typical application with an 8 MHz crystal . . . . .	121
Figure 30.	Typical application with a 32.768 kHz crystal . . . . .	122
Figure 31.	ACCHSI accuracy versus temperature . . . . .	123
Figure 32.	ACC <sub>LSI</sub> versus temperature . . . . .	124
Figure 33.	PLL output clock waveforms in center spread mode . . . . .	128
Figure 34.	PLL output clock waveforms in down spread mode . . . . .	128
Figure 35.	FT I/O input characteristics . . . . .	137
Figure 36.	I/O AC characteristics definition . . . . .	140
Figure 37.	Recommended NRST pin protection . . . . .	141
Figure 38.	SPI timing diagram - slave mode and CPHA = 0 . . . . .	144
Figure 39.	SPI timing diagram - slave mode and CPHA = 1 . . . . .	145
Figure 40.	SPI timing diagram - master mode . . . . .	145
Figure 41.	I <sup>2</sup> S slave timing diagram (Philips protocol) <sup>(1)</sup> . . . . .	147
Figure 42.	I <sup>2</sup> S master timing diagram (Philips protocol) <sup>(1)</sup> . . . . .	147
Figure 43.	SAI master timing waveforms . . . . .	149

Figure 44.	SAI slave timing waveforms . . . . .	149
Figure 45.	USB OTG full speed timings: definition of data signal rise and fall time . . . . .	151
Figure 46.	ULPI timing diagram . . . . .	152
Figure 47.	Ethernet SMI timing diagram . . . . .	154
Figure 48.	Ethernet RMII timing diagram . . . . .	155
Figure 49.	Ethernet MII timing diagram . . . . .	156
Figure 50.	ADC accuracy characteristics . . . . .	160
Figure 51.	Typical connection diagram using the ADC . . . . .	161
Figure 52.	Power supply and reference decoupling ( $V_{REF+}$ not connected to $V_{DDA}$ ) . . . . .	162
Figure 53.	Power supply and reference decoupling ( $V_{REF+}$ connected to $V_{DDA}$ ) . . . . .	163
Figure 54.	12-bit buffered /non-buffered DAC . . . . .	167
Figure 55.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . . .	169
Figure 56.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . . .	171
Figure 57.	Asynchronous multiplexed PSRAM/NOR read waveforms . . . . .	172
Figure 58.	Asynchronous multiplexed PSRAM/NOR write waveforms . . . . .	174
Figure 59.	Synchronous multiplexed NOR/PSRAM read timings . . . . .	176
Figure 60.	Synchronous multiplexed PSRAM write timings . . . . .	177
Figure 61.	Synchronous non-multiplexed NOR/PSRAM read timings . . . . .	179
Figure 62.	Synchronous non-multiplexed PSRAM write timings . . . . .	180
Figure 63.	PC Card/CompactFlash controller waveforms for common memory read access . . . . .	182
Figure 64.	PC Card/CompactFlash controller waveforms for common memory write access . . . . .	182
Figure 65.	PC Card/CompactFlash controller waveforms for attribute memory read access . . . . .	183
Figure 66.	PC Card/CompactFlash controller waveforms for attribute memory write access . . . . .	184
Figure 67.	PC Card/CompactFlash controller waveforms for I/O space read access . . . . .	184
Figure 68.	PC Card/CompactFlash controller waveforms for I/O space write access . . . . .	185
Figure 69.	NAND controller waveforms for read access . . . . .	187
Figure 70.	NAND controller waveforms for write access . . . . .	187
Figure 71.	NAND controller waveforms for common memory read access . . . . .	188
Figure 72.	NAND controller waveforms for common memory write access . . . . .	188
Figure 73.	SDRAM read access waveforms (CL = 1) . . . . .	189
Figure 74.	SDRAM write access waveforms . . . . .	191
Figure 75.	DCMI timing diagram . . . . .	193
Figure 76.	LCD-TFT horizontal timing diagram . . . . .	195
Figure 77.	LCD-TFT vertical timing diagram . . . . .	195
Figure 78.	SDIO high-speed mode . . . . .	196
Figure 79.	SD default mode . . . . .	196
Figure 80.	LQFP100 -100-pin, 14 x 14 mm low-profile quad flat package outline . . . . .	198
Figure 81.	LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint . . . . .	200
Figure 82.	LQFP100 marking example (package top view) . . . . .	201
Figure 83.	WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline . . . . .	202
Figure 84.	WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint . . . . .	203
Figure 85.	WLCSP143 marking example (package top view) . . . . .	204
Figure 86.	LQFP144-144-pin, 20 x 20 mm low-profile quad flat package outline . . . . .	205
Figure 87.	LQPF144- 144-pin,20 x 20 mm low-profile quad flat package recommended footprint . . . . .	207
Figure 88.	LQFP144 marking example (package top view) . . . . .	208
Figure 89.	LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package outline . . . . .	209

Figure 90. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint .....	211
Figure 91. LQFP176 marking (package top view) .....	212
Figure 92. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline .....	213
Figure 93. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package recommended footprint .....	215
Figure 94. LQFP208 marking example (package top view) .....	216
Figure 95. UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline .....	217
Figure 96. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint .....	218
Figure 97. UFBGA169 marking example (package top view) .....	219
Figure 98. UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline .....	220
Figure 99. UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint .....	221
Figure 100. UFBGA176+25 marking example (package top view) .....	222
Figure 101. TFBGA216 - 216 ball 13 x 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline .....	223
Figure 102. TFBGA176 marking example (package top view) .....	224
Figure 103. USB controller configured as peripheral-only and used in Full speed mode .....	228
Figure 104. USB controller configured as host-only and used in full speed mode .....	228
Figure 105. USB controller configured in dual mode and used in full speed mode .....	229
Figure 106. USB controller configured as peripheral, host, or dual-mode and used in high speed mode .....	230
Figure 107. MII mode using a 25 MHz crystal .....	231
Figure 108. RMII with a 50 MHz oscillator .....	231
Figure 109. RMII with a 25 MHz crystal and PHY with PLL .....	232

## 1 Introduction

This datasheet provides the description of the STM32F427xx and STM32F429xx line of microcontrollers. For more details on the whole STMicroelectronics STM32 family, please refer to [Section 2.1: Full compatibility throughout the family](#).

The STM32F427xx and STM32F429xx datasheet should be read in conjunction with the STM32F4xx reference manual.

For information on the Cortex<sup>®</sup>-M4 core, please refer to the Cortex<sup>®</sup>-M4 programming manual (PM0214), available from [www.st.com](http://www.st.com).

## 2 Description

The STM32F427xx and STM32F429xx devices are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F427xx and STM32F429xx devices incorporate high-speed embedded memories (Flash memory up to 2 Mbyte, up to 256 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. They also feature standard and advanced communication interfaces.

- Up to three I<sup>2</sup>Cs
- Six SPIs, two I<sup>2</sup>Ss full duplex. To achieve audio class accuracy, the I<sup>2</sup>S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- One SAI serial audio interface
- An SDIO/MMC interface
- Ethernet and camera interface
- LCD-TFT display controller
- Chrom-ART Accelerator™.

Advanced peripherals include an SDIO, a flexible memory control (FMC) interface, a camera interface for CMOS sensors. Refer to [Table 2: STM32F427xx and STM32F429xx features and peripheral counts](#) for the list of peripherals available on each part number.

The STM32F427xx and STM32F429xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F427xx and STM32F429xx devices offer devices in 8 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F427xx and STM32F429xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

*Figure 4* shows the general block diagram of the device family.

**arm**

Description

STM32F427XX STM32F429XX

Table 2. STM32F427xx and STM32F429xx features and peripheral counts

Peripherals		STM32F427 Vx		STM32F429Vx		STM32F427 Zx		STM32F429Zx		STM32F427 Ax		STM32F429 Ax		STM32F427 Ix		STM32F429Ix		STM32F429Bx		STM32F429Nx		
Flash memory in Kbytes		1024	2048	512	1024	2048	1024	2048	512	1024	2048	1024	2048	1024	2048	512	1024	2048	512	1024	2048	
SRAM in Kbytes	System																					
	Backup																					
FMC memory controller																						
Ethernet																						
Timers	General-purpose																					
	Advanced-control																					
	Basic																					
Random number generator																						
Communication interfaces	SPI / I <sup>2</sup> S	4/2 (full duplex) <sup>(2)</sup>																				
	I <sup>2</sup> C																					
	USART/UART																					
	USB OTG FS																					
	USB OTG HS																					
	CAN																					
	SAI																					
SDIO																						
Camera interface																						
LCD-TFT (STM32F429xx only)	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes
Chrom-ART Accelerator™																						
GPIOs	82		114		130		140		168													
12-bit ADC Number of channels	16																					



**Table 2. STM32F427xx and STM32F429xx features and peripheral counts (continued)**

Peripherals	STM32F427 Vx	STM32F429Vx	STM32F427 Zx	STM32F429Zx	STM32F427 Ax	STM32F429 Ax	STM32F427 Ix	STM32F429Ix	STM32F429Bx	STM32F429Nx
12-bit DAC Number of channels					Yes	2				
Maximum CPU frequency					180 MHz					
Operating voltage					1.8 to 3.6 V <sup>(3)</sup>					
Operating temperatures					Ambient temperatures: -40 to +85 °C / -40 to +105 °C					
					Junction temperature: -40 to +125 °C					
Packages	LQFP100		WLCSP143 LQFP144		UFBGA169		UFBGA176 LQFP176		LQFP208	TFBGA216

1. For the LQFP100 package, only FMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package. For UFBGA169 package, only SDRAM, NAND and multiplexed static memories are supported.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3.  $V_{DD}/V_{DDA}$  minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).



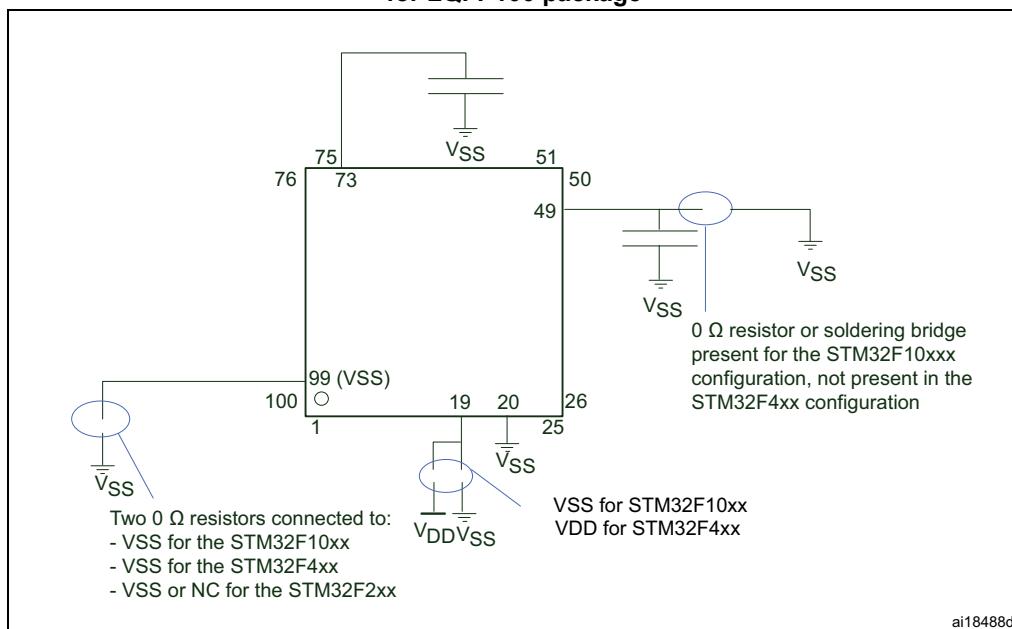
## 2.1 Full compatibility throughout the family

The STM32F427xx and STM32F429xx devices are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F427xx and STM32F429xx devices maintain a close compatibility with the whole STM32F10xx family. All functional pins are pin-to-pin compatible. The STM32F427xx and STM32F429xx, however, are not drop-in replacements for the STM32F10xx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xx to the STM32F42x family remains simple as only a few pins are impacted.

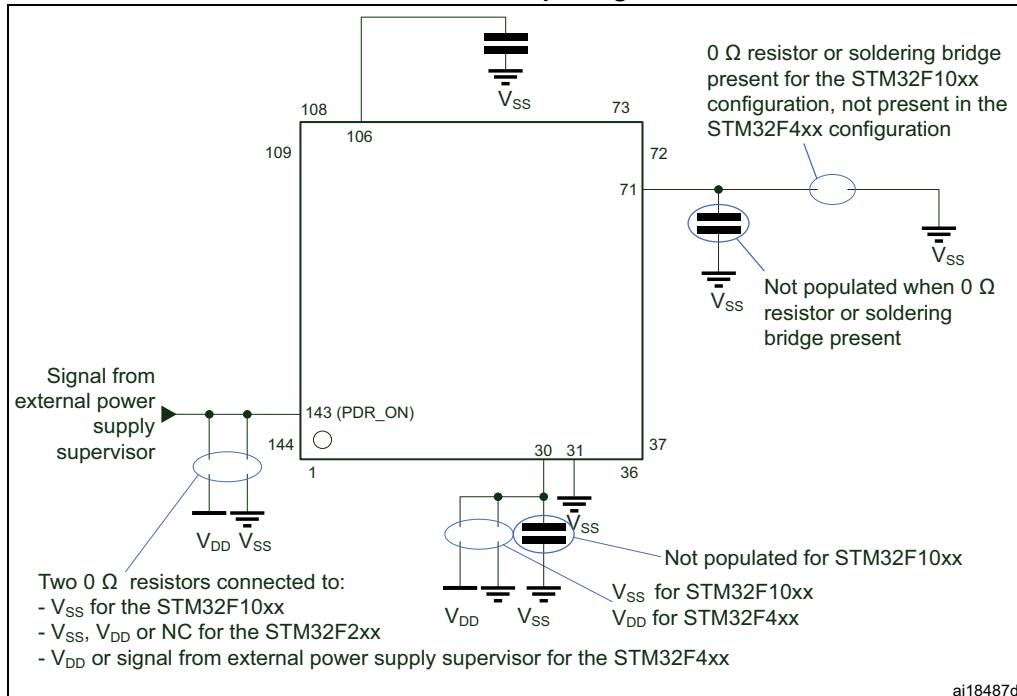
*Figure 1*, *Figure 2*, and *Figure 3*, give compatible board designs between the STM32F4xx, STM32F2xx, and STM32F10xx families.

**Figure 1. Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package**



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**Figure 2. Compatible board design between STM32F10xx/STM32F2xx/STM32F4xx for LQFP144 package**



**Figure 3. Compatible board design between STM32F2xx and STM32F4xx for LQFP176 and UFBGA176 packages**

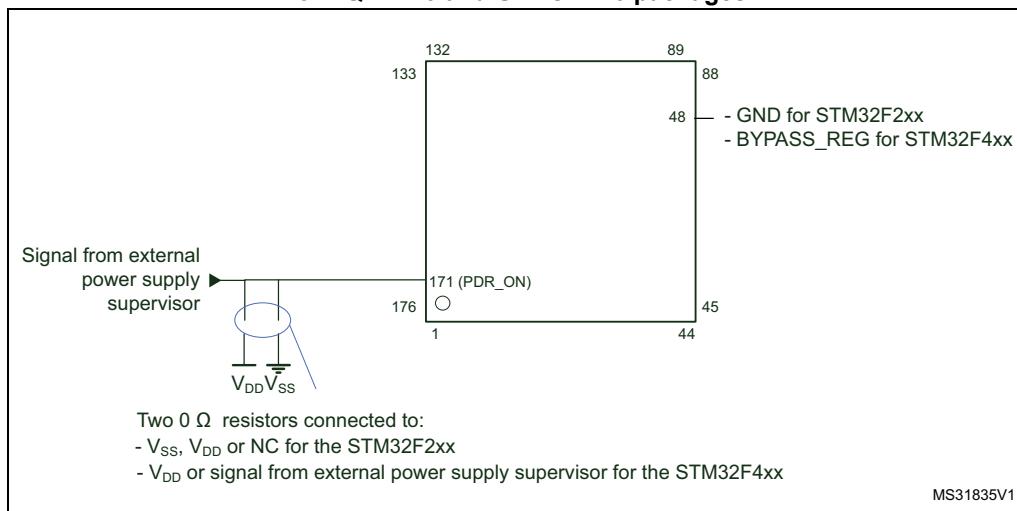
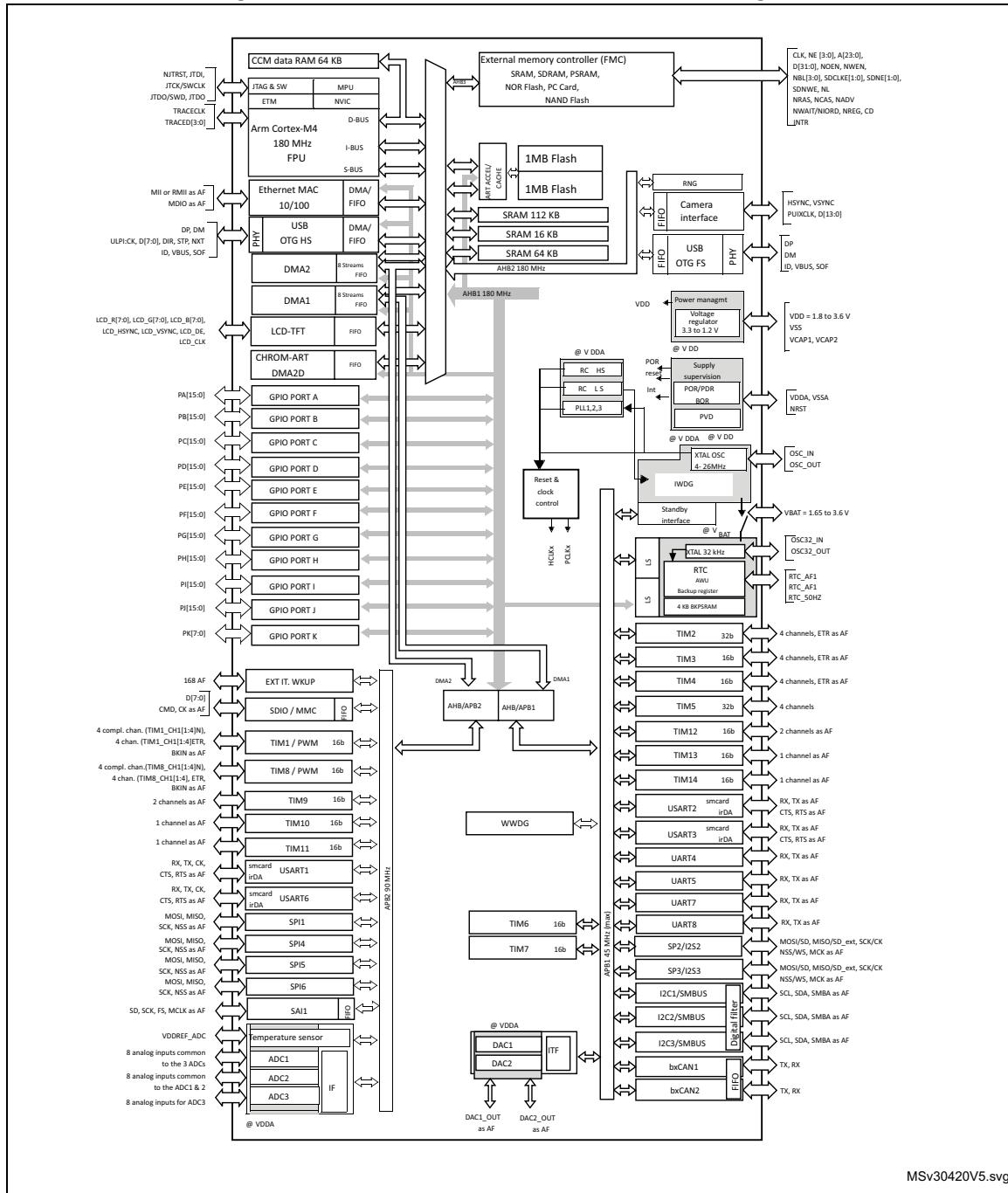


Figure 4. STM32F427xx and STM32F429xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 180 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 90 MHz or 180 MHz depending on TIMPRE bit configuration in the RCC\_DCKCFGR register.
2. The LCD-TFT is available only on STM32F429xx devices.

### 3 Functional overview

#### 3.1 Arm® Cortex®-M4 with FPU and embedded Flash and SRAM

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F42x family is compatible with all Arm tools and software.

*Figure 4* shows the general block diagram of the STM32F42x family.

*Note:* Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

#### 3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

#### 3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

### 3.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

### 3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 3.6 Embedded SRAM

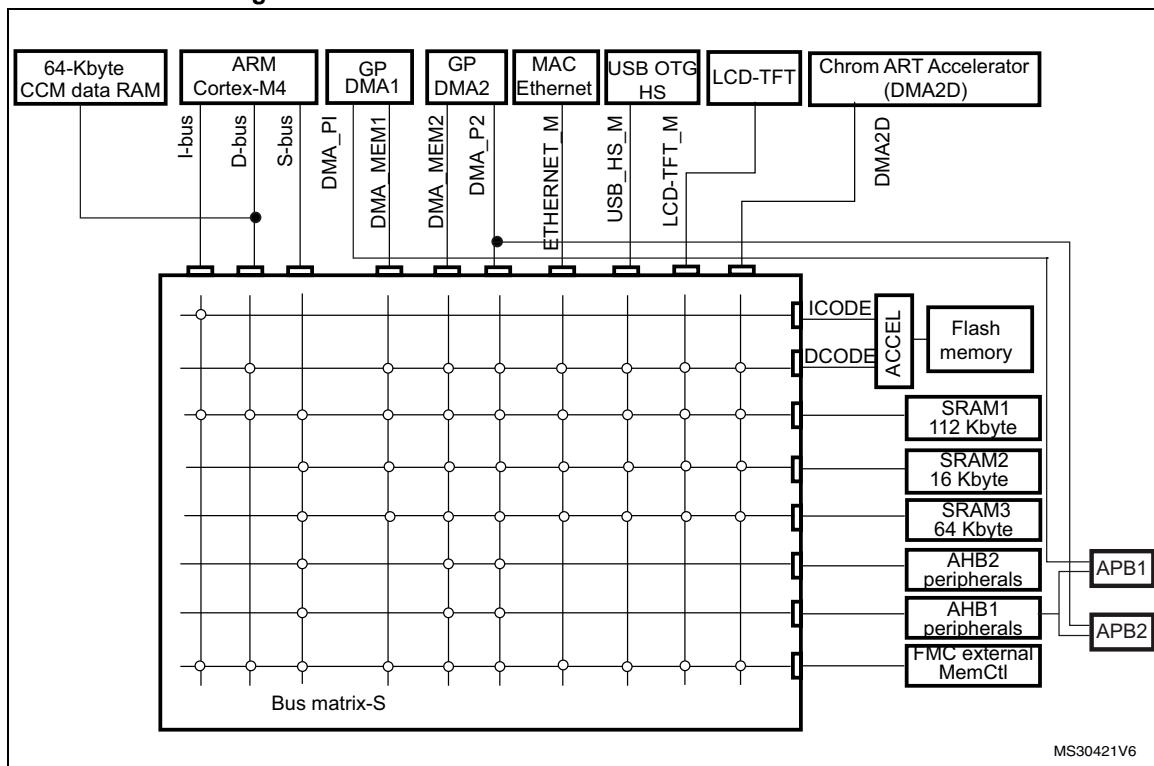
All devices embed:

- Up to 256Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM  
RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM  
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

### 3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. STM32F427xx and STM32F429xx Multi-AHB matrix



### 3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I<sup>2</sup>S
- I<sup>2</sup>C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC
- SAI1.

### 3.9 Flexible memory controller (FMC)

All devices embed an FMC. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SDRAM/LPSDR SDRAM, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- 8-,16-, 32-bit data bus width
- Read FIFO for SDRAM controller
- Write FIFO
- Maximum FMC\_CLK/FMC\_SDCLK frequency for synchronous accesses is 90 MHz.

#### LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

### 3.10 LCD-TFT controller (available only on STM32F429xx)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

### 3.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

### 3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 91 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

### 3.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

### 3.14 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is

detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 180 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 180 MHz while the maximum frequency of the high-speed APB domains is 90 MHz. The maximum allowed frequency of the low-speed APB domain is 45 MHz.

The devices embed a dedicated PLL (PLLI2S) and PLLSAI which allows to achieve audio class performance. In this case, the I<sup>2</sup>S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

### 3.15 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface. Refer to application note AN2606 for details.

### 3.16 Power supply schemes

- $V_{DD} = 1.7$  to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through  $V_{DD}$  pins.
- $V_{SSA}, V_{DDA} = 1.7$  to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL.  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD}$  and  $V_{SS}$ , respectively.
- $V_{BAT} = 1.65$  to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present.

**Note:**  $V_{DD}/V_{DDA}$  minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)). Refer to [Table 3: Voltage regulator configuration mode versus device operating mode](#) to identify the packages supporting this option.

### 3.17 Power supply supervisor

#### 3.17.1 Internal reset ON

On packages embedding the PDR\_ON pin, the power supply supervisor is enabled by holding PDR\_ON high. On the other package, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is

reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$  or  $V_{BOR}$ , without the need for an external reset circuit.

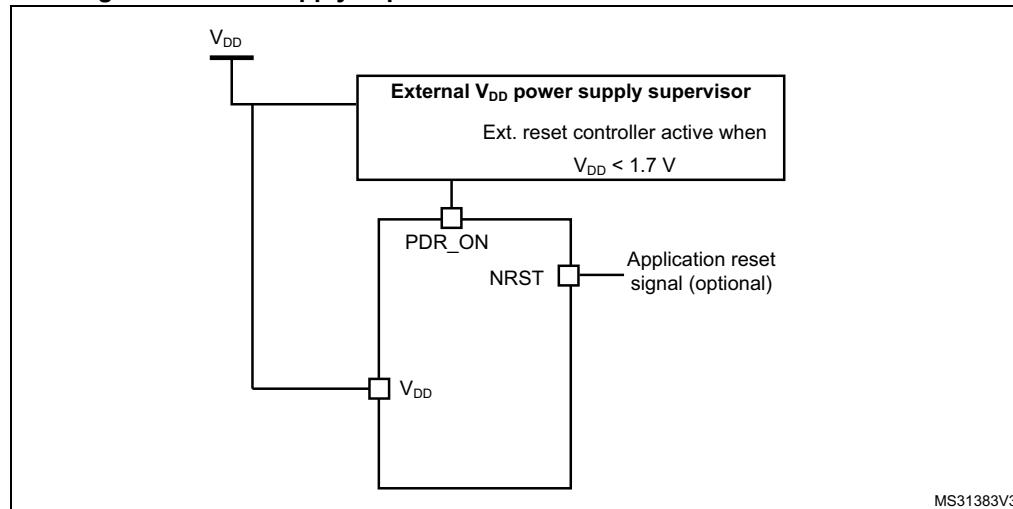
The device also features an embedded programmable voltage detector (PVD) that monitors the  $V_{DD}/V_{DDA}$  power supply and compares it to the  $V_{PVD}$  threshold. An interrupt can be generated when  $V_{DD}/V_{DDA}$  drops below the  $V_{PVD}$  threshold and/or when  $V_{DD}/V_{DDA}$  is higher than the  $V_{PVD}$  threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.17.2 Internal reset OFF

This feature is available only on packages featuring the PDR\_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR\_ON pin.

An external power supply supervisor should monitor  $V_{DD}$  and should maintain the device in reset mode as long as  $V_{DD}$  is below a specified threshold. PDR\_ON should be connected to this external power supply supervisor. Refer to [Figure 6: Power supply supervisor interconnection with internal reset OFF](#).

**Figure 6. Power supply supervisor interconnection with internal reset OFF**



The  $V_{DD}$  specified threshold, below which the device must be maintained under reset, is 1.7 V (see [Figure 7](#)).

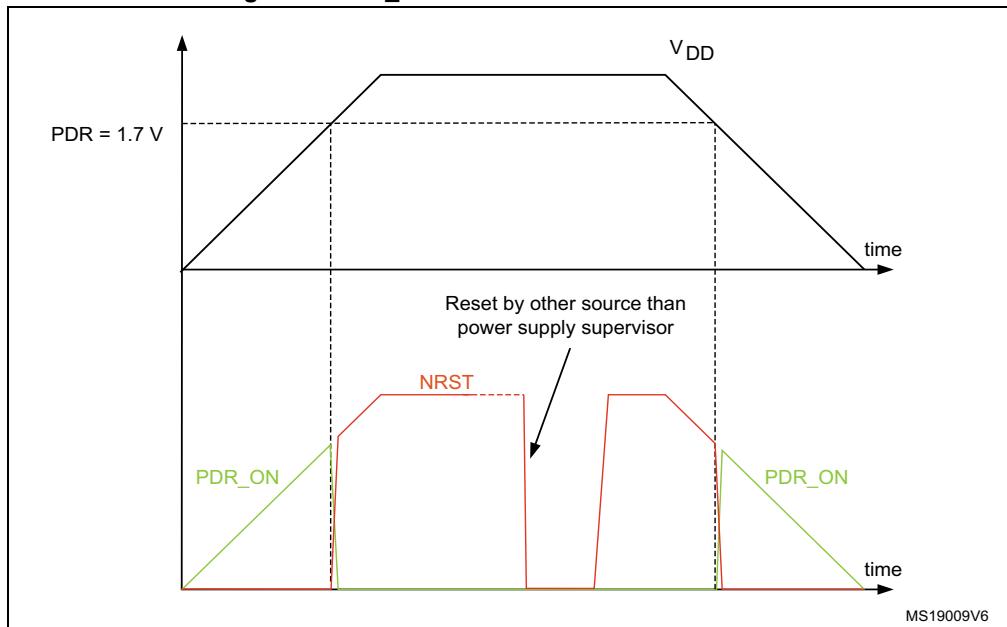
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- $V_{BAT}$  functionality is no more available and  $V_{BAT}$  pin should be connected to  $V_{DD}$ .

All packages, except for the LQFP100, allow to disable the internal reset through the PDR\_ON signal.

Figure 7. PDR\_ON control with internal reset OFF



## 3.18 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

### 3.18.1 Regulator ON

On packages embedding the BYPASS\_REG pin, the regulator is enabled by holding BYPASS\_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep mode

The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.

- The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
- In Stop modes
    - The MR can be configured in two ways during stop mode:
      - MR operates in normal mode (default mode of MR in stop mode)
      - MR operates in under-drive mode (reduced leakage mode).
  - LPR is used in the Stop modes:
    - The LP regulator mode is configured by software when entering Stop mode.
    - Like the MR mode, the LPR can be configured in two ways during stop mode:
      - LPR operates in normal mode (default mode when LPR is ON)
      - LPR operates in under-drive mode (reduced leakage mode).
  - Power-down is used in Standby mode.
    - The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to [Table 3](#) for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on  $V_{CAP\_1}$  and  $V_{CAP\_2}$  pin. Refer to [Figure 22: Power supply scheme](#) and [Table 19: VCAP1/VCAP2 operating conditions](#).

All packages have the regulator ON feature.

**Table 3. Voltage regulator configuration mode versus device operating mode<sup>(1)</sup>**

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode <sup>(2)</sup>	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.

2. The over-drive mode is not available when  $V_{DD} = 1.7$  to 2.1 V.

### 3.18.2 Regulator OFF

This feature is available only on packages featuring the BYPASS\_REG pin. The regulator is disabled by holding BYPASS\_REG high. The regulator OFF mode allows to supply externally a  $V_{12}$  voltage source through  $V_{CAP\_1}$  and  $V_{CAP\_2}$  pins.

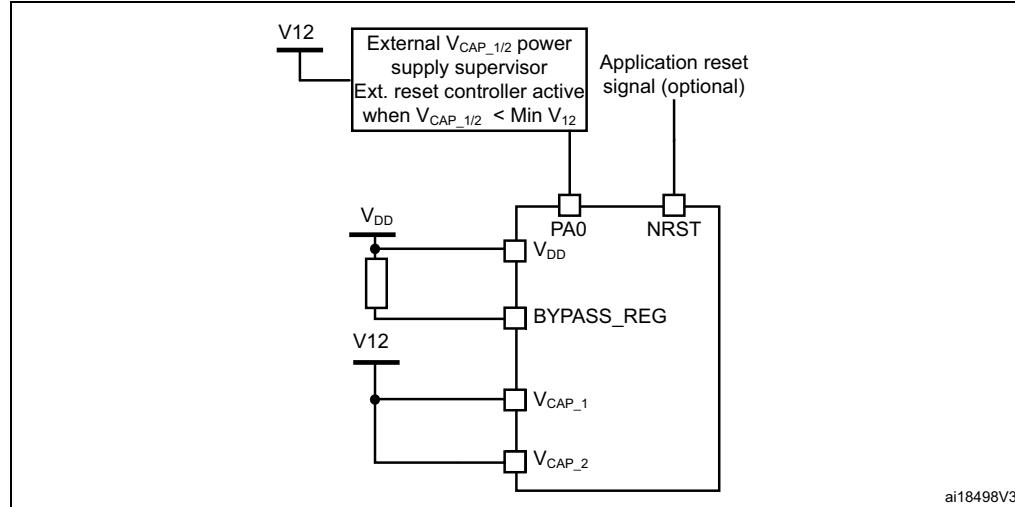
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to [Table 17: General operating conditions](#). The two 2.2  $\mu$ F ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to [Figure 22: Power supply scheme](#).

When the regulator is OFF, there is no more internal monitoring on  $V_{12}$ . An external power supply supervisor should be used to monitor the  $V_{12}$  of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on  $V_{12}$  power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V<sub>12</sub> logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

**Figure 8. Regulator OFF**

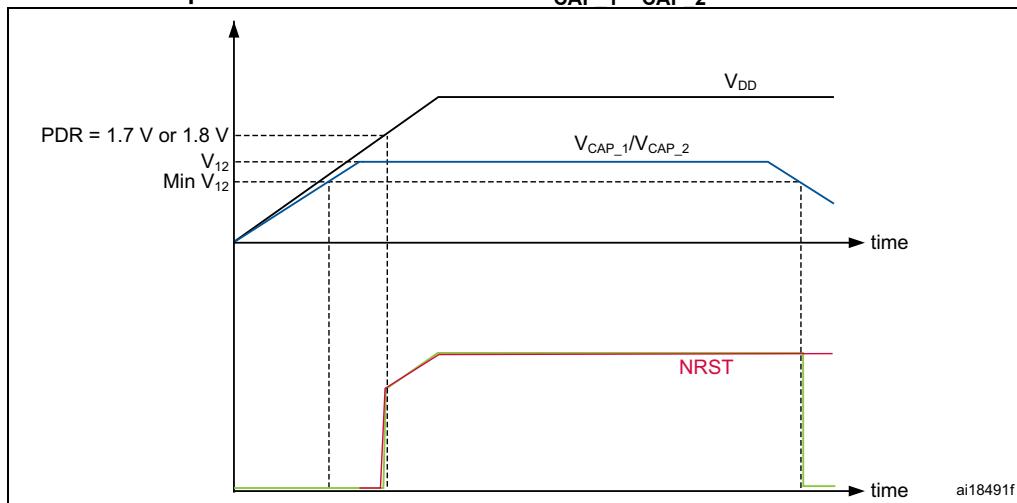


The following conditions must be respected:

- V<sub>DD</sub> should always be higher than V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> to avoid current injection between power domains.
- If the time for V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> to reach V<sub>12</sub> minimum value is faster than the time for V<sub>DD</sub> to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> reach V<sub>12</sub> minimum value and until V<sub>DD</sub> reaches 1.7 V (see [Figure 9](#)).
- Otherwise, if the time for V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> to reach V<sub>12</sub> minimum value is slower than the time for V<sub>DD</sub> to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 10](#)).
- If V<sub>CAP\_1</sub> and V<sub>CAP\_2</sub> go below V<sub>12</sub> minimum value and V<sub>DD</sub> is higher than 1.7 V, then a reset must be asserted on PA0 pin.

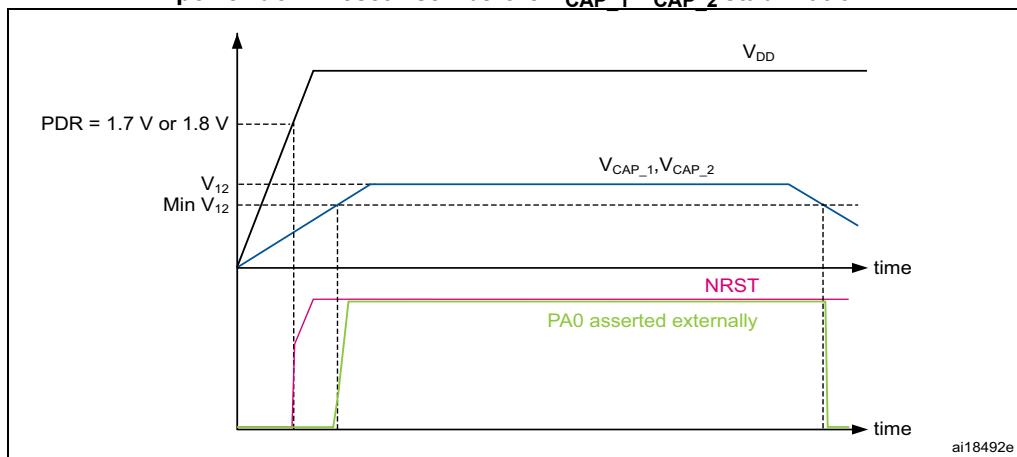
**Note:** The minimum value of V<sub>12</sub> depends on the maximum frequency targeted in the application (see [Table 17: General operating conditions](#)).

**Figure 9. Startup in regulator OFF: slow  $V_{DD}$  slope  
- power-down reset risen after  $V_{CAP\_1}/V_{CAP\_2}$  stabilization**



1. This figure is valid whatever the internal reset mode (ON or OFF).

**Figure 10. Startup in regulator OFF mode: fast  $V_{DD}$  slope  
- power-down reset risen before  $V_{CAP\_1}/V_{CAP\_2}$  stabilization**



1. This figure is valid whatever the internal reset mode (ON or OFF).

### 3.18.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP100	Yes	No	Yes	No
LQFP144, LQFP208			Yes PDR_ON set to $V_{DD}$	Yes PDR_ON connected to an external power supply supervisor
WLCSP143, LQFP176, UFBGA169, UFBGA176, TFBGA216	Yes BYPASS_REG set to $V_{SS}$	Yes BYPASS_REG set to $V_{DD}$		

## 3.19 Real-time clock (RTC), backup SRAM and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120  $\mu$ s to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The 4-Kbyte backup SRAM is an EEPROM-like memory area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled by default to minimize power consumption (see [Section 3.20: Low-power modes](#)). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when  $V_{DD}$  power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see [Section 3.20: Low-power modes](#)).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V<sub>DD</sub> supply when present or from the V<sub>BAT</sub> pin.

### 3.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

**Table 5. Voltage regulator modes in stop mode**

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

### 3.21 V<sub>BAT</sub> operation

The V<sub>BAT</sub> pin allows to power the device V<sub>BAT</sub> domain from an external battery, an external supercapacitor, or from V<sub>DD</sub> when no external battery and an external supercapacitor are present.

V<sub>BAT</sub> operation is activated when V<sub>DD</sub> is not present.

The V<sub>BAT</sub> pin supplies the RTC, the backup registers and the backup SRAM.

*Note:* When the microcontroller is supplied from V<sub>BAT</sub>, external interrupts and RTC alarm/events do not exit it from V<sub>BAT</sub> operation.

When PDR\_ON pin is not connected to V<sub>DD</sub> (Internal Reset OFF), the V<sub>BAT</sub> functionality is no more available and V<sub>BAT</sub> pin should be connected to V<sub>DD</sub>.

### 3.22 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

[Table 6](#) compares the features of the advanced-control, general-purpose and basic timers.

**Table 6. Timer feature comparison**

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) (1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	90	180
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	90	180
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	90	180
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	45	90/180
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	45	90/180
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	45	90/180

1. The maximum timer clock is either 90 or 180 MHz depending on TIMPRE bit configuration in the RCC\_DCKCFGR register.

### 3.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

### 3.22.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F42x devices (see [Table 6](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F42x include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

### 3.22.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

### 3.22.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 3.22.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 3.22.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.23 Inter-integrated circuit interface (I<sup>2</sup>C)

Up to three I<sup>2</sup>C bus interfaces can operate in multimaster and slave modes. They can support the standard (up to 100 KHz), and fast (up to 400 KHz) modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see [Table 7](#)).

**Table 7. Comparison of I<sup>2</sup>C analog and digital filters**

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I <sup>2</sup> C peripheral clocks

## 3.24 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7, and UART8).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to



communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

**Table 8. USART feature comparison<sup>(1)</sup>**

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
UART7	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART8	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)

1. X = feature supported.

### 3.25 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 45 Mbit/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

### 3.26 Inter-integrated sound (I<sup>2</sup>S)

Two standard I<sup>2</sup>S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I<sup>2</sup>S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

*Note:* For I2S2 full-duplex mode, I2S2\_CK and I2S2\_WS signals can be used only on GPIO Port B and GPIO Port D.

### 3.27 Serial Audio interface (SAI1)

The serial audio interface (SAI1) is based on two independent audio sub-blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub-blocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 can be served by the DMA controller.

### 3.28 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I<sup>2</sup>S and SAI applications. It allows to achieve error-free I<sup>2</sup>S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I<sup>2</sup>S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I<sup>2</sup>S/SAI flow with an external PLL (or Codec output).

### 3.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

### 3.30 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

### 3.31 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F4xx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

### 3.32 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive

FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

### 3.33 Universal serial bus on-the-go full-speed (OTG\_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of  $320 \times 35$  bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

### 3.34 Universal serial bus on-the-go high-speed (OTG\_HS)

The devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of  $1 \text{ Kbit} \times 35$  with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

### 3.35 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

### 3.36 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

### 3.37 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 90 MHz.

### 3.38 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

### 3.39 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as  $V_{BAT}$ , ADC1\_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and  $V_{BAT}$  conversion are enabled at the same time, only  $V_{BAT}$  conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

### 3.40 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 10-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference  $V_{REF+}$

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

### 3.41 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

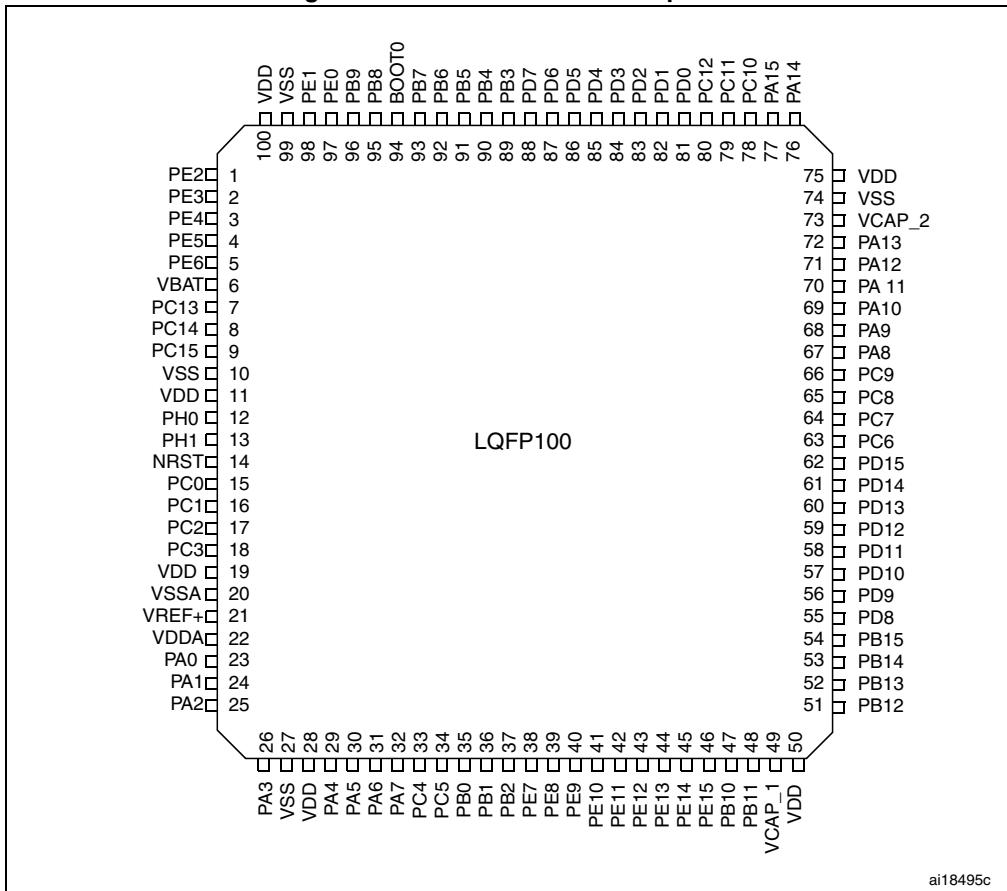
### 3.42 Embedded Trace Macrocell™

The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F42x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

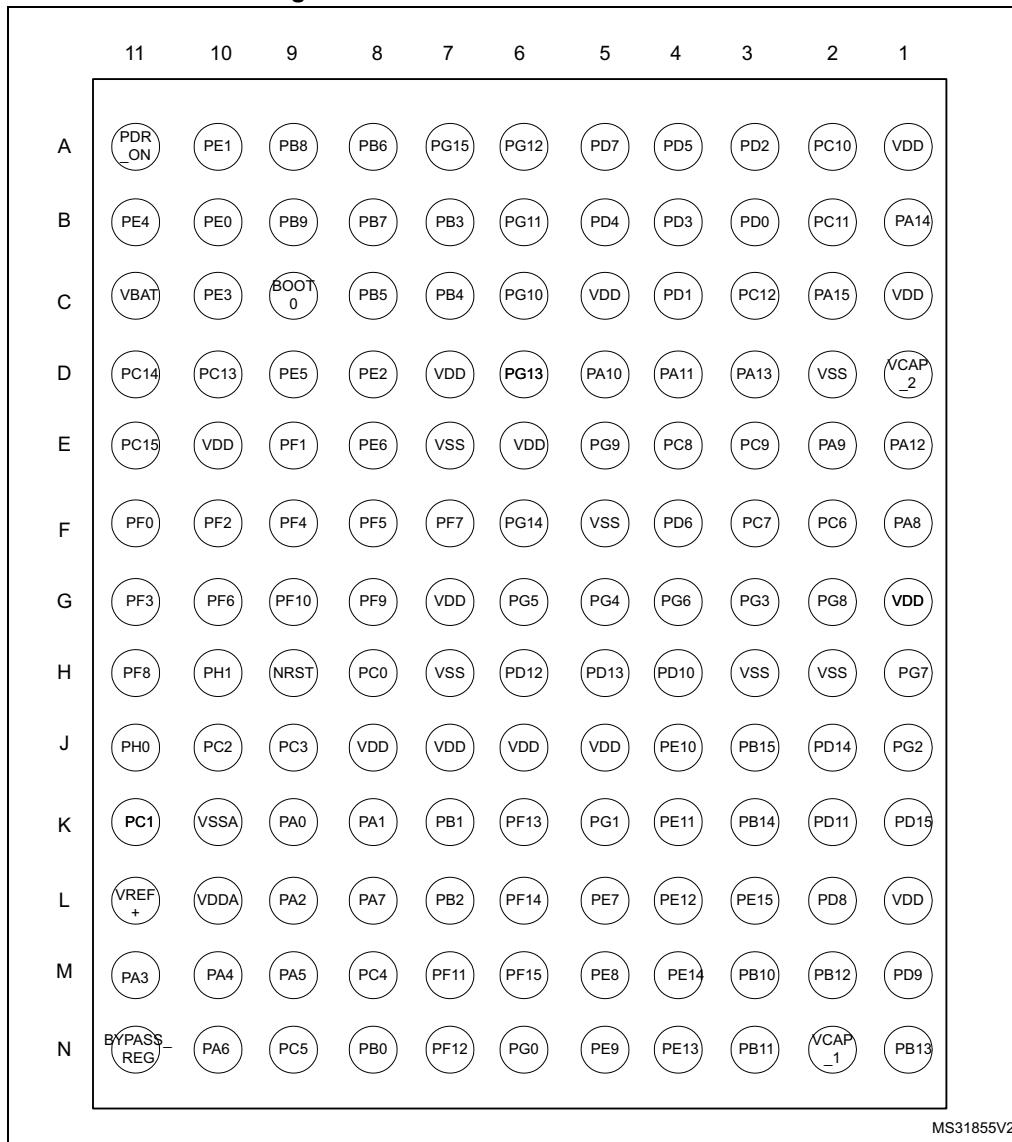
## 4 Pinouts and pin description

Figure 11. STM32F42x LQFP100 pinout



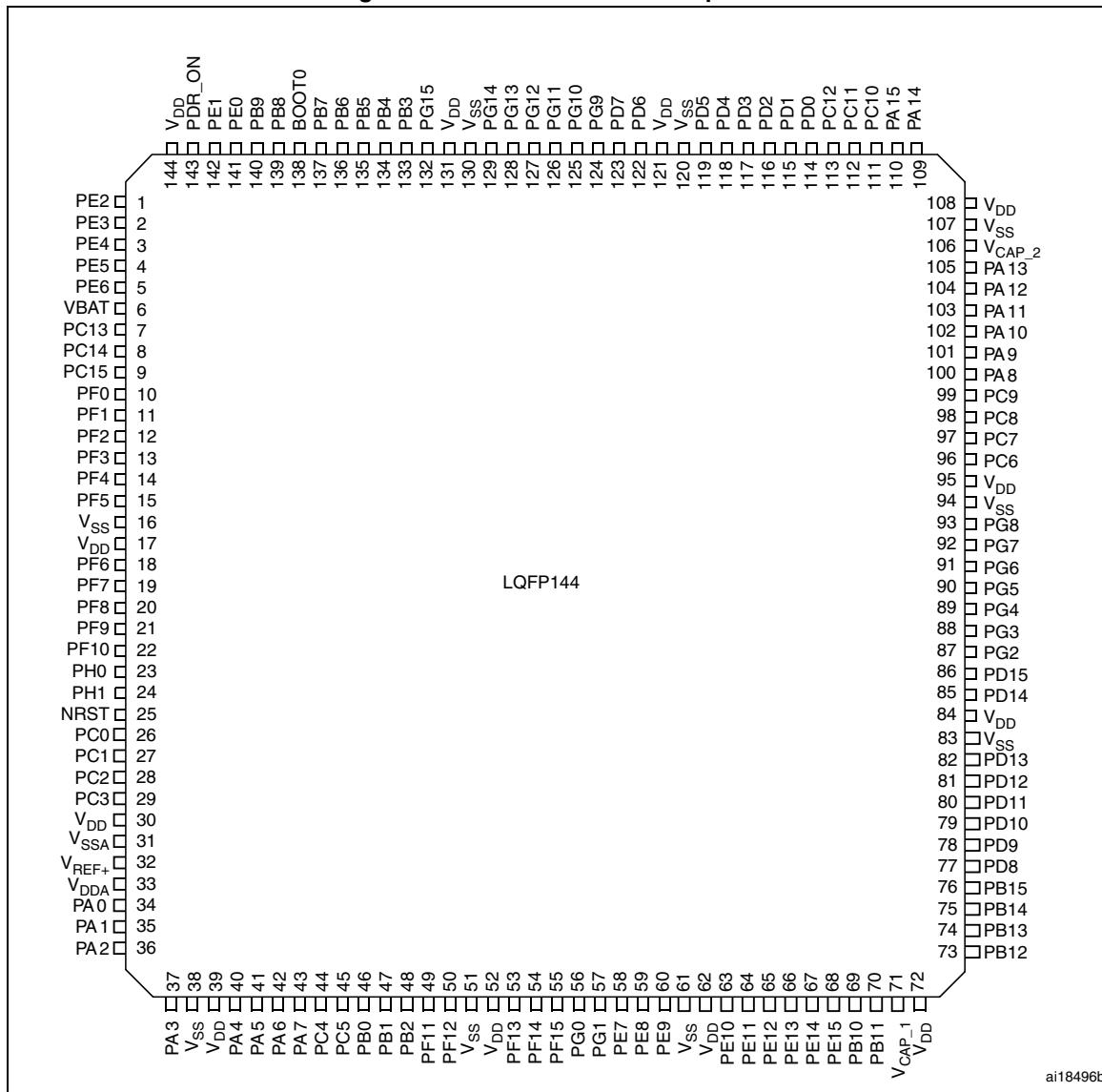
1. The above figure shows the package top view.

Figure 12. STM32F42x WLCSP143 ballout



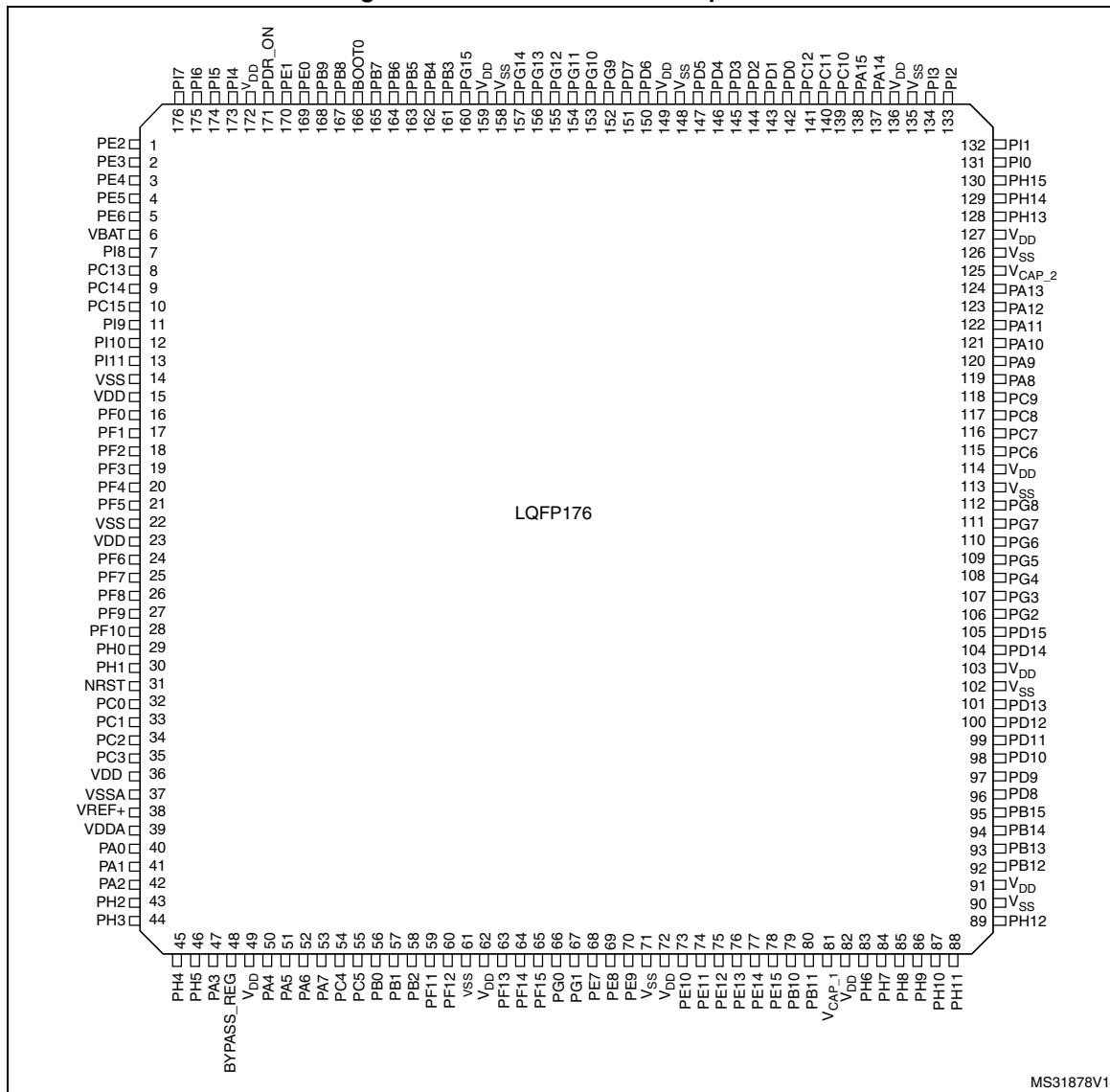
- The above figure shows the package bump view.

Figure 13. STM32F42x LQFP144 pinout



- The above figure shows the package top view.

Figure 14. STM32F42x LQFP176 pinout



- The above figure shows the package top view.

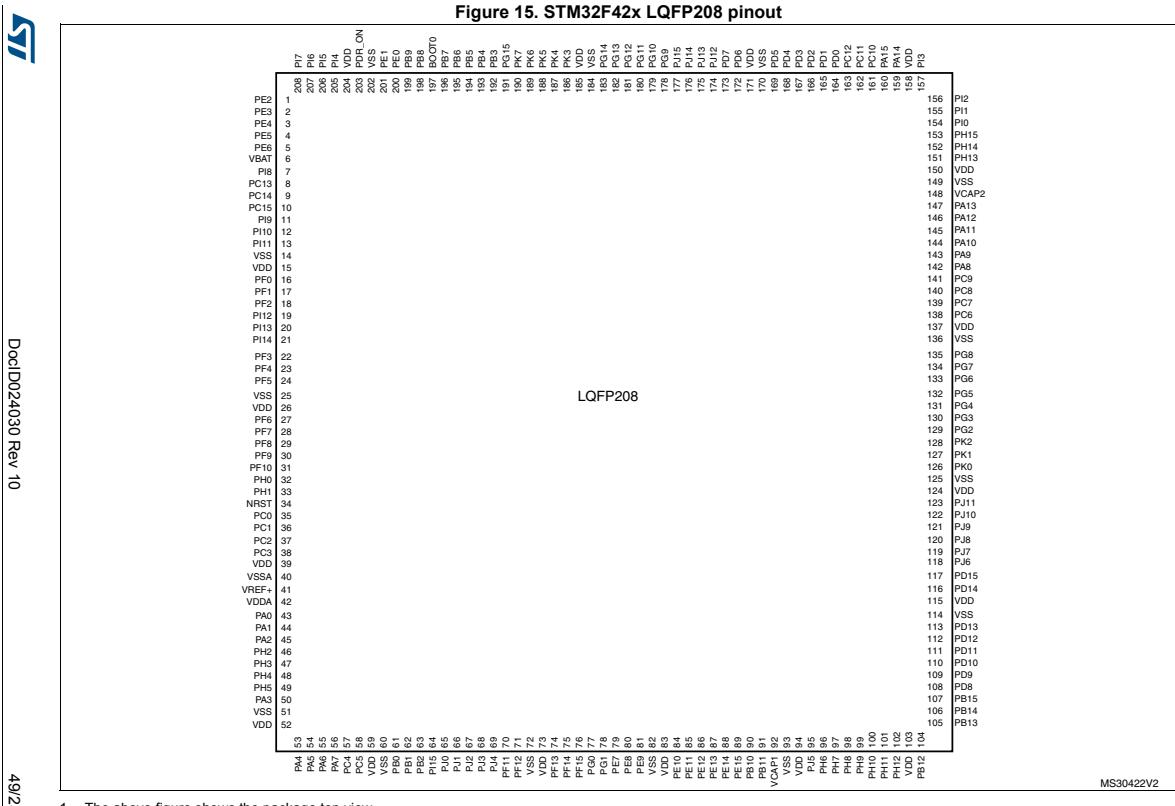
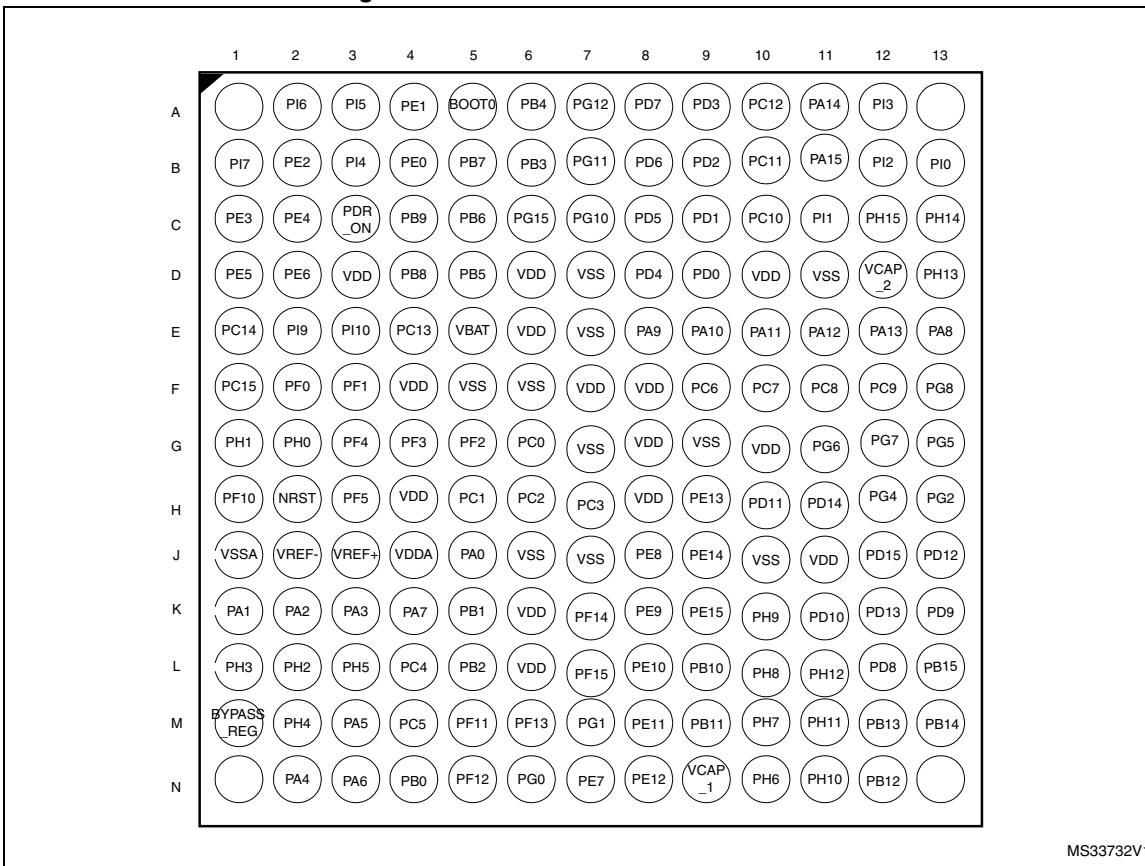
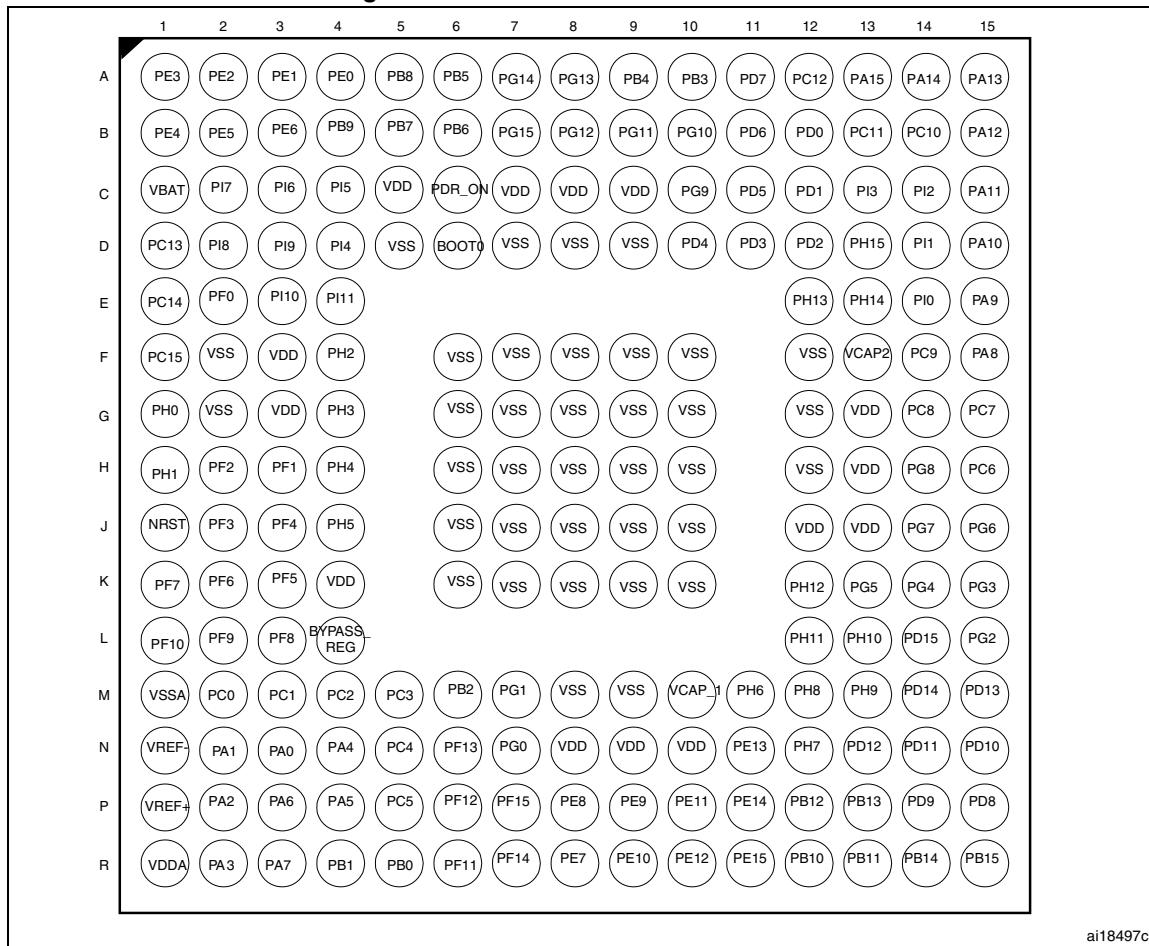


Figure 16. STM32F42x UFBGA169 ballout



1. The above figure shows the package top view.
2. The 4 corners balls, A1,A13, N1 and N13, are not bonded internally and should be left not connected on the PCB.

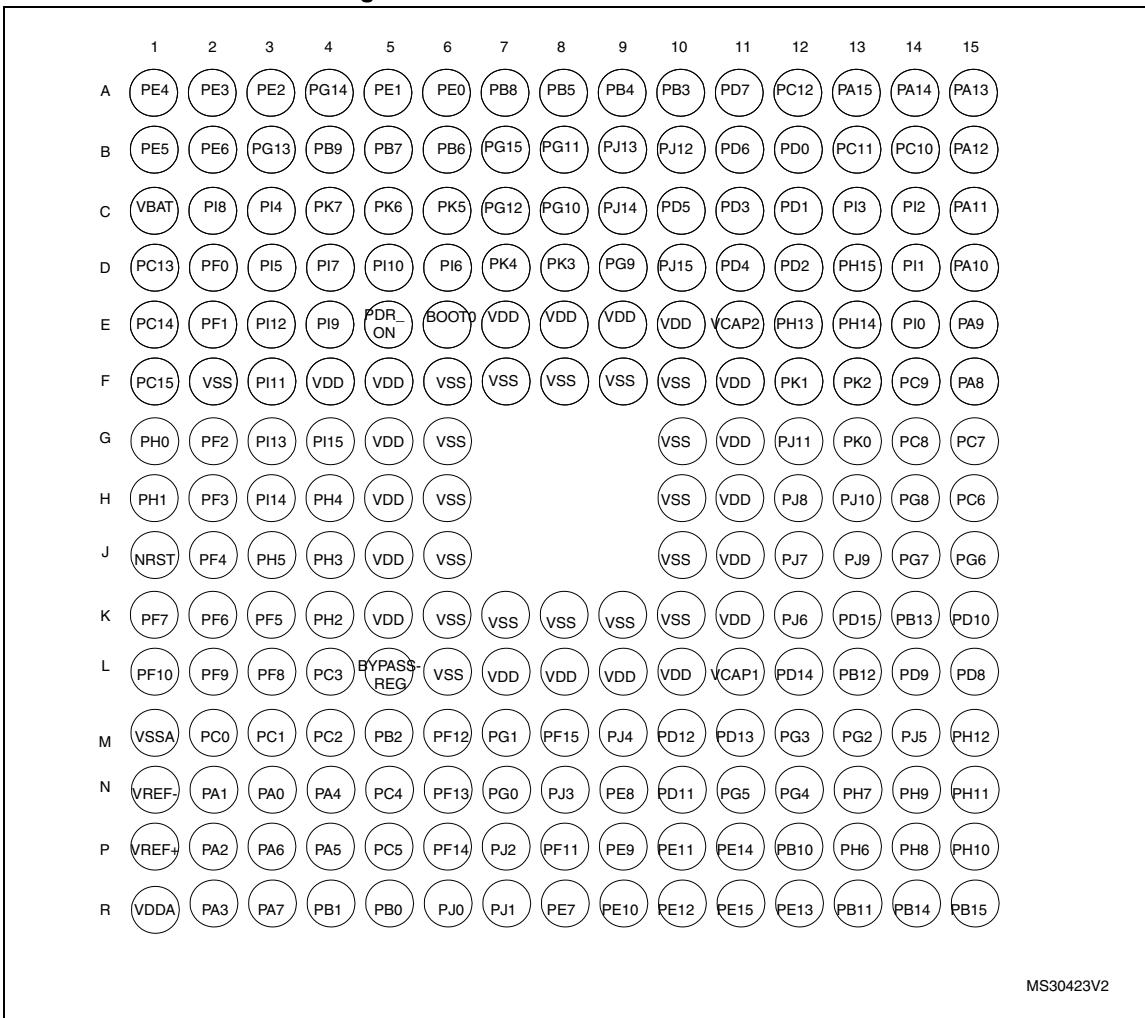
Figure 17. STM32F42x UFBGA176 ballout



ai18497c

- The above figure shows the package top view.

Figure 18. STM32F42x TFBGA216 ballout



1. The above figure shows the package top view.

**Table 9. Legend/abbreviations used in the pinout table**

Name	Abbreviation	Definition					
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name						
Pin type	S	Supply pin					
	I	Input only pin					
	I/O	Input / output pin					
I/O structure	FT	5 V tolerant I/O					
	TTa	3.3 V tolerant I/O directly connected to ADC					
	B	Dedicated BOOT0 pin					
	RST	Bidirectional reset pin with weak pull-up resistor					
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset						
Alternate functions	Functions selected through GPIOx_AFR registers						
Additional functions	Functions directly selected/enabled through peripheral registers						

**Table 10. STM32F427xx and STM32F429xx pin and ball definitions**

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216						
1	1	B2	A2	1	D8	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	C1	A1	2	C10	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
3	3	C2	B1	3	B11	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216						
4	4	D1	B2	4	D9	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	5	D2	B3	5	E8	5	B2	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	-	G6	V <sub>SS</sub>	S	-	-	-	-
-	-	-	-	-	-	-	F5	V <sub>DD</sub>	S	-	-	-	-
6	6	E5	C1	6	C11	6	C1	V <sub>BAT</sub>	S	-	-	-	-
-	-	NC <sup>(2)</sup>	D2	7	-	7	C2	PI8	I/O	FT <sup>(3) (4)</sup>	EVENTOUT	TAMP_2	
7	7	E4	D1	8	D10	8	D1	PC13	I/O	FT <sup>(3) (4)</sup>	EVENTOUT	TAMP_1	
8	8	E1	E1	9	D11	9	E1	PC14- OSC32_IN (PC14)	I/O	FT <sup>(3) (4)</sup>	EVENTOUT	OSC32_IN <sup>(5)</sup>	
9	9	F1	F1	10	E11	10	F1	PC15- OSC32_OUT (PC15)	I/O	FT <sup>(3) (4)</sup>	EVENTOUT	OSC32_OUT <sup>(5)</sup>	
-	-	-	-	-	-	-	G5	V <sub>DD</sub>	S	-	-	-	-
-	-	E2	D3	11	-	11	E4	PI9	I/O	FT	-	CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	E3	12	-	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	NC <sup>(2)</sup>	E4	13	-	13	F3	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	F6	F2	14	E7	14	F2	V <sub>SS</sub>	S	-	-	-	-
-	-	F4	F3	15	E10	15	F4	V <sub>DD</sub>	S	-	-	-	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216						
-	10	F2	E2	16	F11	16	D2	PF0	I/O	FT	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	11	F3	H3	17	E9	17	E2	PF1	I/O	FT	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	12	G5	H2	18	F10	18	G2	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	-	-	19	E3	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	-	-	-	20	G3	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	-	-	21	H3	PI14	I/O	FT		LCD_CLK, EVENTOUT	-
-	13	G4	J2	19	G11	22	H2	PF3	I/O	FT	<sup>(5)</sup>	FMC_A3, EVENTOUT	ADC3_IN9
-	14	G3	J3	20	F9	23	J2	PF4	I/O	FT	<sup>(5)</sup>	FMC_A4, EVENTOUT	ADC3_IN14
-	15	H3	K3	21	F8	24	K3	PF5	I/O	FT	<sup>(5)</sup>	FMC_A5, EVENTOUT	ADC3_IN15
10	16	G7	G2	22	H7	25	H6	V <sub>SS</sub>	S	-	-	-	-
11	17	G8	G3	23	-	26	H5	V <sub>DD</sub>	S	-	-	-	-
-	18	NC <sup>(2)</sup>	K2	24	G10	27	K2	PF6	I/O	FT	<sup>(5)</sup>	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_Rx, FMC_NIORD, EVENTOUT	ADC3_IN4
-	19	NC <sup>(2)</sup>	K1	25	F7	28	K1	PF7	I/O	FT	<sup>(5)</sup>	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, FMC_NREG, EVENTOUT	ADC3_IN5
-	20	NC <sup>(2)</sup>	L3	26	H11	29	L3	PF8	I/O	FT	<sup>(5)</sup>	SPI5_MISO, SAI1_SCK_B, TIM13_CH1, FMC_NIOWR, EVENTOUT	ADC3_IN6

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions	
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
-	21	NC <sup>(2)</sup>		L2	27	G8	30	L2	PF9	I/O	FT	<sup>(5)</sup>	SPI5_MOSI, SAI1_FS_B, TIM14_CH1, FMC_CD, EVENTOUT	ADC3_IN7
-	22	H1	L1	28	G9	31	L1	PF10	I/O	FT	<sup>(5)</sup>	FMC_INTR, DCMI_D11, LCD_DE, EVENTOUT	ADC3_IN8	
12	23	G2	G1	29	J11	32	G1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN <sup>(5)</sup>	
13	24	G1	H1	30	H10	33	H1	PH1- OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT <sup>(5)</sup>	
14	25	H2	J1	31	H9	34	J1	NRST	I/O	RS_T	-	-	-	
15	26	G6	M2	32	H8	35	M2	PC0	I/O	FT	<sup>(5)</sup>	OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT	ADC123_IN10	
16	27	H5	M3	33	K11	36	M3	PC1	I/O	FT	<sup>(5)</sup>	ETH_MDC, EVENTOUT	ADC123_IN11	
17	28	H6	M4	34	J10	37	M4	PC2	I/O	FT	<sup>(5)</sup>	SPI2_MISO, I2S2ext_SD, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_IN12	
18	29	H7	M5	35	J9	38	L4	PC3	I/O	FT	<sup>(5)</sup>	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC123_IN13	
19	30	-	-	36	G7	39	J5	V <sub>DD</sub>	S	-	-	-	-	
-	-	-	-	-	-	-	J6	V <sub>SS</sub>	S	-	-	-	-	
20	31	J1	M1	37	K10	40	M1	V <sub>SSA</sub>	S	-	-	-	-	
-	-	J2	N1	-	-	-	N1	V <sub>REF-</sub>	S	-	-	-	-	
21	32	J3	P1	38	L11	41	P1	V <sub>REF+</sub>	S	-	-	-	-	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
22	33	J4	R1	39	L10	42	R1	V <sub>DDA</sub>	S	-	-		-	-
23	34	J5	N3	40	K9	43	N3	PA0-WKUP (PA0)	I/O	FT	(6)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, ETH_MII CRS, EVENTOUT	ADC123_IN0/WKUP (5)	
24	35	K1	N2	41	K8	44	N2	PA1	I/O	FT	(5)	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, EVENTOUT	ADC123_IN1	
25	36	K2	P2	42	L9	45	P2	PA2	I/O	FT	(5)	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, ETH_MDIO, EVENTOUT	ADC123_IN2	
-	-	L2	F4	43	-	46	K4	PH2	I/O	FT	-	ETH_MII CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-	
-	-	L1	G4	44	-	47	J4	PH3	I/O	FT	-	ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-	
-	-	M2	H4	45	-	48	H4	PH4	I/O	FT	-	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-	
-	-	L3	J4	46	-	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-	
26	37	K3	R2	47	M11	50	R2	PA3	I/O	FT	(5)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_IN3	
27	38	-	-	-	-	51	K6	V <sub>SS</sub>	S	-	-	-	-	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216						
-	-	M1	L4	48	N11	-	L5	BYPASS_REG	I	FT	-	-	-
28	39	J11	K4	49	J8	52	K5	VDD	S	-	-	-	-
29	40	N2	N4	50	M10	53	N4	PA4	I/O	TTa	(5)	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_IN4 /DAC_OUT1
30	41	M3	P4	51	M9	54	P4	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK, OTG_HS_ULPI_CK, EVENTOUT	ADC12_IN5/DAC_OUT2
31	42	N3	P3	52	N10	55	P3	PA6	I/O	FT	(5)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_IN6
32	43	K4	R3	53	L8	56	R3	PA7	I/O	FT	(5)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, EVENTOUT	ADC12_IN7
33	44	L4	N5	54	M8	57	N5	PC4	I/O	FT	(5)	ETH_MII_RXD0/ETH_RMII_RXD0, EVENTOUT	ADC12_IN14
34	45	M4	P5	55	N9	58	P5	PC5	I/O	FT	(5)	ETH_MII_RXD1/ETH_RMII_RXD1, EVENTOUT	ADC12_IN15
-	-	-	-	-	J7	59	L7	VDD	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216						
35	46	N4	R5	56	N8	61	R5	PB0	I/O	FT	(5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT	ADC12_IN8
36	47	K5	R4	57	K7	62	R4	PB1	I/O	FT	(5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT	ADC12_IN9
37	48	L5	M6	58	L7	63	M5	PB2-BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	-	-	67	P7	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-
-	-	-	-	-	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	M5	R6	59	M7	70	P8	PF11	I/O	FT	-	SPI5_MOSI, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	N5	P6	60	N7	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	51	G9	M8	61	-	72	K7	VSS	S		-	-	-
-	52	D10	N8	62	-	73	L8	VDD	S		-	-	-
-	53	M6	N6	63	K6	74	N6	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	54	K7	R7	64	L6	75	P6	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	55	L7	P7	65	M6	76	M8	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	56	N6	N7	66	N6	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	M7	67	K5	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
38	58	N7	R8	68	L5	79	R8	PE7	I/O	FT	-	TIM1_ETR, UART7_Rx, FMC_D4, EVENTOUT	-	
39	59	J8	P8	69	M5	80	N9	PE8	I/O	FT	-	TIM1_CH1N, UART7_Tx, FMC_D5, EVENTOUT	-	
40	60	K8	P9	70	N5	81	P9	PE9	I/O	FT	-	TIM1_CH1, FMC_D6, EVENTOUT	-	
-	61	J6	M9	71	H3	82	K8	V <sub>SS</sub>	S		-		-	
-	62	G10	N9	72	J5	83	L9	V <sub>DD</sub>	S		-		-	
41	63	L8	R9	73	J4	84	R9	PE10	I/O	FT	-	TIM1_CH2N, FMC_D7, EVENTOUT	-	
42	64	M8	P10	74	K4	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, FMC_D8, LCD_G3, EVENTOUT	-	
43	65	N8	R10	75	L4	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, FMC_D9, LCD_B4, EVENTOUT	-	
44	66	H9	N11	76	N4	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, FMC_D10, LCD_DE, EVENTOUT	-	
45	67	J9	P11	77	M4	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, FMC_D11, LCD_CLK, EVENTOUT	-	
46	68	K9	R11	78	L3	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-	
47	69	L9	R12	79	M3	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-	
48	70	M9	R13	80	N3	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_ RMII_TX_EN, LCD_G5, EVENTOUT	-	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
49	71	N9	M10	81	N2	92	L11	V <sub>CAP_1</sub>	S	-	-	-	-	-
-	-	-	-	-	H2	93	K9	V <sub>SS</sub>	S	-	-	-	-	-
50	72	F8	N10	82	J6	94	L10	V <sub>DD</sub>	S	-	-	-	-	-
-	-	-	-	-	-	95	M14	PJ5	I/O	-	-	LCD_R6, EVENTOUT	-	-
-	-	N10	M11	83	-	96	P13	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-	-
-	-	M10	N12	84	-	97	N13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-	-
-	-	L10	M12	85	-	98	P14	PH8	I/O	FT	-	I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-	-
-	-	K10	M13	86	-	99	N14	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-	-
-	-	N11	L13	87	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-	-
-	-	M11	L12	88	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-	-
-	-	L11	K12	89	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-	-
-	-	E7	H12	90	-	-	K10	V <sub>SS</sub>	S	-	-	-	-	-
-	-	H8	J12	91	-	103	K11	V <sub>DD</sub>	S	-	-	-	-	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216						
51	73	N12	P12	92	M2	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2 NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_R MII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	M12	P13	93	N1	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_R MII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	M13	R14	94	K3	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
54	76	L13	R15	95	J3	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
55	77	L12	P15	96	L2	108	L15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
56	78	K13	P14	97	M1	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
57	79	K11	N15	98	H4	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
58	80	H10	N14	99	K2	111	N10	PD11	I/O	FT	-	USART3_CTS, FMC_A16, EVENTOUT	-	
59	81	J13	N13	100	H6	112	M10	PD12	I/O	FT	-	TIM4_CH1, USART3_RTS, FMC_A17, EVENTOUT	-	
60	82	K12	M15	101	H5	113	M11	PD13	I/O	FT	-	TIM4_CH2, FMC_A18, EVENTOUT	-	
-	83	-	-	102	-	114	J10	V <sub>SS</sub>	S		-	-	-	
-	84	F7	J13	103	L1	115	J11	V <sub>DD</sub>	S		-	-	-	
61	85	H11	M14	104	J2	116	L12	PD14	I/O	FT	-	TIM4_CH3, FMC_D0, EVENTOUT	-	
62	86	J12	L14	105	K1	117	K13	PD15	I/O	FT	-	TIM4_CH4, FMC_D1, EVENTOUT	-	
-	-	-	-	-	-	118	K12	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-	
-	-	-	-	-	-	119	J12	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-	
-	-	-	-	-	-	120	H12	PJ8	I/O	FT	-	LCD_G1, EVENTOUT	-	
-	-	-	-	-	-	121	J13	PJ9	I/O	FT	-	LCD_G2, EVENTOUT	-	
-	-	-	-	-	-	122	H13	PJ10	I/O	FT	-	LCD_G3, EVENTOUT	-	
-	-	-	-	-	-	123	G12	PJ11	I/O	FT	-	LCD_G4, EVENTOUT	-	
-	-	-	-	-	-	124	H11	V <sub>DD</sub>	I/O	FT	-	-	-	
-	-	-	-	-	-	125	H10	V <sub>SS</sub>	I/O	FT	-	-	-	
-	-	-	-	-	-	126	G13	PK0	I/O	FT	-	LCD_G5, EVENTOUT	-	
-	-	-	-	-	-	127	F12	PK1	I/O	FT	-	LCD_G6, EVENTOUT	-	
-	-	-	-	-	-	128	F13	PK2	I/O	FT	-	LCD_G7, EVENTOUT	-	
-	87	H13	L15	106	J1	129	M13	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-	
-	88	NC <sup>(2)</sup>	K15	107	G3	130	M12	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-	
-	89	H12	K14	108	G5	131	N12	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-	
-	90	G13	K13	109	G6	132	N11	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
-	91	G11	J15	110	G4	133	J15	PG6	I/O	FT	-	FMC_INT2, DCMI_D12, LCD_R7, EVENTOUT	-	
-	92	G12	J14	111	H1	134	J14	PG7	I/O	FT	-	USART6_CK, FMC_INT3, DCMI_D13, LCD_CLK, EVENTOUT	-	
-	93	F13	H14	112	G2	135	H14	PG8	I/O	FT	-	SPI6_NSS, USART6 RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT	-	
-	94	J7	G12	113	D2	136	G10	V <sub>SS</sub>	S		-	-	-	
-	95	E6	H13	114	G1	137	G11	V <sub>DD</sub>	S		-	-	-	
63	96	F9	H15	115	F2	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-	
64	97	F10	G15	116	F3	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDIO_D7, DCMI_D1, LCD_G6, EVENTOUT	-	
65	98	F11	G14	117	E4	140	G14	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-	
66	99	F12	F14	118	E3	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, SDIO_D1, DCMI_D3, EVENTOUT	-	
67	100	E13	F15	119	F1	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
68	101	E8	E15	120	E2	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_VBUS	
69	102	E9	D15	121	D5	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-	
70	103	E10	C15	122	D4	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, LCD_R4, OTG_FS_DM, EVENTOUT	-	
71	104	E11	B15	123	E1	146	B15	PA12	I/O	FT	-	TIM1_ETR, USART1 RTS, CAN1_TX, LCD_R5, OTG_FS_DP, EVENTOUT	-	
72	105	E12	A15	124	D3	147	A15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-	
73	106	D12	F13	125	D1	148	E11	V <sub>CAP_2</sub>	S		-	-	-	
74	107	J10	F12	126	D2	149	F10	V <sub>SS</sub>	S		-	-	-	
75	108	H4	G13	127	C1	150	F11	V <sub>DD</sub>	S		-	-	-	
-	-	D13	E12	128	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-	
-	-	C13	E13	129	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-	
-	-	C12	D13	130	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-	
-	-	B13	E14	131	-	154	E14	PIO	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS <sup>(7)</sup> , FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216						
-	-	C11	D14	132	-	155	D14	PI1	I/O	FT	-	SPI2_SCK/I2S2_CK <sup>(7)</sup> , FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	B12	C14	133	-	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, I2S2ext_SD, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	A12	C13	134	-	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D11	D9	135	F5	-	F9	V <sub>ss</sub>	S		-	-	-
-	-	D3	C9	136	A1	158	E10	V <sub>DD</sub>	S		-	-	-
76	109	A11	A14	137	B1	159	A14	PA14 (JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK/ EVENTOUT	-
77	110	B11	A13	138	C2	160	A13	PA15 (JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS, SPI3_NSS/I2S3_WS, EVENTOUT	-
78	111	C10	B14	139	A2	161	B14	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, SDIO_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	112	B10	B13	140	B2	162	B13	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, SDIO_D3, DCMI_D4, EVENTOUT	-
80	113	A10	A12	141	C3	163	A12	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDIO_CK, DCMI_D9, EVENTOUT	-
81	114	D9	B12	142	B3	164	B12	PD0	I/O	FT	-	CAN1_RX, FMC_D2, EVENTOUT	-

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
82	115	C9	C12	143	C4	165	C12	PD1	I/O	FT	-	CAN1_TX, FMC_D3, EVENTOUT	-	
83	116	B9	D12	144	A3	166	D12	PD2	I/O	FT	-	TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-	
84	117	A9	D11	145	B4	167	C11	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-	
85	118	D8	D10	146	B5	168	D11	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-	
86	119	C8	C11	147	A4	169	C10	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-	
-	120	-	D8	148	-	170	F8	V <sub>SS</sub>	S		-	-	-	
-	121	D6	C8	149	C5	171	E9	V <sub>DD</sub>	S		-	-	-	
87	122	B8	B11	150	F4	172	B11	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-	
88	123	A8	A11	151	A5	173	A11	PD7	I/O	FT	-	USART2_CK, FMC_NE1/FMC_NCE2, EVENTOUT	-	
-	-	-	-	-	-	174	B10	PJ12	I/O	FT	-	LCD_B0, EVENTOUT	-	
-	-	-	-	-	-	175	B9	PJ13	I/O	FT	-	LCD_B1, EVENTOUT	-	
-	-	-	-	-	-	176	C9	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-	
-	-	-	-	-	-	177	D10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-	
-	124	NC <sup>(2)</sup>	C10	152	E5	178	D9	PG9	I/O	FT	-	USART6_RX, FMC_NE2/FMC_NCE3, DCMI_VSYNC <sup>(8)</sup> , EVENTOUT	-	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
-	125	C7	B10	153	C6	179	C8	PG10	I/O	FT	-	LCD_G3, FMC_NCE4_1/FMC_N E3, DCMI_D2, LCD_B2, EVENTOUT	-	
-	126	B7	B9	154	B6	180	B8	PG11	I/O	FT	-	ETH_MII_TX_EN/ETH_ RMII_TX_EN, FMC_NCE4_2, DCMI_D3, LCD_B3, EVENTOUT	-	
-	127	A7	B8	155	A6	181	C7	PG12	I/O	FT	-	SPI6_MISO, USART6_RTS, LCD_B4, FMC_NE4, LCD_B1, EVENTOUT	-	
-	128	NC <sup>(2)</sup>	A8	156	D6	182	B3	PG13	I/O	FT	-	SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_R MII_TXD0, FMC_A24, EVENTOUT	-	
-	129	NC <sup>(2)</sup>	A7	157	F6	183	A4	PG14	I/O	FT	-	SPI6_MOSI, USART6_TX, ETH_MII_TXD1/ETH_R MII_TXD1, FMC_A25, EVENTOUT	-	
-	130	D7	D7	158	-	184	F7	Vss	S		-	-	-	
-	131	L6	C7	159	E6	185	E8	VDD	S		-	-	-	
-	-	-	-	-	-	186	D8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-	
-	-	-	-	-	-	187	D7	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-	
-	-	-	-	-	-	188	C6	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-	
-	-	-	-	-	-	189	C5	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-	
-	-	-	-	-	-	190	C4	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-	
-	132	C6	B7	160	A7	191	B7	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-	

**Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)**

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
89	133	B6	A10	161	B7	192	A10	PB3 (JTDO/TRACE SWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK/I2S3_CK, EVENTOUT	-	
90	134	A6	A9	162	C7	193	A9	PB4 (NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, EVENTOUT	-	
91	135	D5	A6	163	C8	194	A8	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, EVENTOUT	-	
92	136	C5	B6	164	A8	195	B6	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, FMC_SDNE1, DCMI_D5, EVENTOUT	-	
93	137	B5	B5	165	B8	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-	
94	138	A5	D6	166	C9	197	E6	BOOT0	I	B	-		V <sub>PP</sub>	
95	139	D4	A5	167	A9	198	A7	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT	-	

Table 10. STM32F427xx and STM32F429xx pin and ball definitions (continued)

Pin number									Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	UFBGA176	LQFP176	WL CSP143	LQFP208	TFBGA216							
96	140	C4	B4	168	B9	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-	
97	141	B4	A4	169	B10	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_RX, FMC_NBL0, DCMI_D2, EVENTOUT	-	
98	142	A4	A3	170	A10	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-	
99	-	F5	D5	-	-	202	F6	Vss	S		-		-	
-	143	C3	C6	171	A11	203	E5	PDR_ON	S		-		-	
100	144	K6	C5	172	D7	204	E7	VDD	S		-		-	
-	-	B3	D4	173	-	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-	
-	-	A3	C4	174	-	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-	
-	-	A2	C3	175	-	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-	
-	-	B1	C2	176	-	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-	

1. Function availability depends on the chosen device.
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF.
  - These I/Os must not be used as a current source (e.g. to drive an LED).

4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
6. If the device is delivered in an WLCSP143, UFBGA169, UFBGA176, LQFP176 or TFBGA216 package, and the BYPASS\_REG pin is set to  $V_{DD}$  (Regulator OFF/internal reset ON mode), then PA0 is used as an internal Reset (active low).
7. PI0 and PI1 cannot be used for I2S2 full-duplex mode.
8. The DCMI\_VSYNC alternate function on PG9 is only available on silicon revision 3.

Table 11. FMC pin definition

Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	A0			A0
PF1	A1	A1			A1
PF2	A2	A2			A2
PF3	A3	A3			A3
PF4	A4	A4			A4
PF5	A5	A5			A5
PF12	A6	A6			A6
PF13	A7	A7			A7
PF14	A8	A8			A8
PF15	A9	A9			A9
PG0	A10	A10			A10
PG1		A11			A11
PG2		A12			A12
PG3		A13			
PG4		A14			BA0
PG5		A15			BA1
PD11		A16	A16	CLE	
PD12		A17	A17	ALE	
PD13		A18	A18		
PE3		A19	A19		
PE4		A20	A20		
PE5		A21	A21		
PE6		A22	A22		
PE2		A23	A23		
PG13		A24	A24		
PG14		A25	A25		
PD14	D0	D0	DA0	D0	D0
PD15	D1	D1	DA1	D1	D1
PD0	D2	D2	DA2	D2	D2
PD1	D3	D3	DA3	D3	D3
PE7	D4	D4	DA4	D4	D4
PE8	D5	D5	DA5	D5	D5
PE9	D6	D6	DA6	D6	D6
PE10	D7	D7	DA7	D7	D7

Table 11. FMC pin definition (continued)

Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	D8	DA8	D8	D8
PE12	D9	D9	DA9	D9	D9
PE13	D10	D10	DA10	D10	D10
PE14	D11	D11	DA11	D11	D11
PE15	D12	D12	DA12	D12	D12
PD8	D13	D13	DA13	D13	D13
PD9	D14	D14	DA14	D14	D14
PD10	D15	D15	DA15	D15	D15
PH8		D16			D16
PH9		D17			D17
PH10		D18			D18
PH11		D19			D19
PH12		D20			D20
PH13		D21			D21
PH14		D22			D22
PH15		D23			D23
PI0		D24			D24
PI1		D25			D25
PI2		D26			D26
PI3		D27			D27
PI6		D28			D28
PI7		D29			D29
PI9		D30			D30
PI10		D31			D31
PD7		NE1	NE1	NCE2	
PG9		NE2	NE2	NCE3	
PG10	NCE4_1	NE3	NE3		
PG11	NCE4_2				
PG12		NE4	NE4		
PD3		CLK	CLK		
PD4	NOE	NOE	NOE	NOE	
PD5	NWE	NWE	NWE	NWE	
PD6	NWAIT	NWAIT	NWAIT	NWAIT	
PB7		NL(NADV)	NL(NADV)		

Table 11. FMC pin definition (continued)

Pin name	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF6	NIORD				
PF7	NREG				
PF8	NIOWR				
PF9	CD				
PF10	INTR				
PG6				INT2	
PG7				INT3	
PE0		NBL0	NBL0		NBL0
PE1		NBL1	NBL1		NBL1
PI4		NBL2			NBL2
PI5		NBL3			NBL3
PG8					SDCLK
PC0					SDNWE
PF11					SDNRAS
PG15					SDNCAS
PH2					SDCKE0
PH3					SDNE0
PH6					SDNE1
PH7					SDCKE1
PH5					SDNWE
PC2					SDNE0
PC3					SDCKE0
PB5					SDCKE1
PB6					SDNE1

Table 12. STM32F427xx and STM32F429xx alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ SAI1	USART6/ UART1/ 8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS/ OTG1_FS	ETH	FMC/SDIO/ OTG2_FS	DCMI	LCD	SYS	
Port A	PA0	-	TIM2_ CH1/TIM2_ _ETR	TIM5_ CH1	TIM8_ ETR	-	-	-	USART2_ CTS	UART4_TX	-	-	ETH_MII_ CRS	-	-	-	EVEN TOUT
	PA1	-	TIM2_ CH2	TIM5_ CH2	-	-	-	-	USART2_ RTS	UART4_RX	-	-	ETH_MII_ RX_CLK/E TH_RMII_ REF_CLK	-	-	-	EVEN TOUT
	PA2	-	TIM2_ CH3	TIM5_ CH3	TIM9_ CH1	-	-	-	USART2_ TX	-	-	-	ETH_MDI0	-	-	-	EVEN TOUT
	PA3	-	TIM2_ CH4	TIM5_ CH4	TIM9_ CH2	-	-	-	USART2_ RX	-	-	OTG_HS_ ULPI_D0	ETH_MII_ COL	-	-	LCD_B5	EVEN TOUT
	PA4	-	-	-	-	SPI1_ NSS	SPI3_ NSS/ I2S3_WS	USART2_ CK	-	-	-	OTG_HS_ SOF	DCMI_HSYNC	LCD_VSYNC	EVEN TOUT		
	PA5	-	TIM2_ CH1/TIM2_ _ETR	-	TIM8_ CH1N	-	SPI1_ SCK	-	-	-	-	OTG_HS_ ULPI_CK	-	-	-	EVEN TOUT	
	PA6	-	TIM1_ BKIN	TIM3_ CH1	TIM8_ BKIN	-	SPI1_ MISO	-	-	-	TIM13_CH1	-	-	DCMI_PIXCLK	LCD_G2	EVEN TOUT	
	PA7	-	TIM1_ CH1N	TIM3_ CH2	TIM8_ CH1N	-	SPI1_ MOSI	-	-	-	TIM14_CH1	-	ETH_MII_ RX_DV/ ETH_RMII_ CRS_DV	-	-	-	EVEN TOUT
	PA8	MCO1	TIM1_ CH1	-	-	I2C3_ SCL	-	-	USART1_ CK	-	-	OTG_FS_ SOF	-	-	-	LCD_R6	EVEN TOUT
	PA9	-	TIM1_ CH2	-	-	I2C3_ SMBA	-	-	USART1_ TX	-	-	-	-	-	DCMI_D0	-	EVEN TOUT
	PA10	-	TIM1_ CH3	-	-	-	-	-	USART1_ RX	-	-	OTG_FS_ ID	-	-	DCMI_D1	-	EVEN TOUT
	PA11	-	TIM1_ CH4	-	-	-	-	-	USART1_ CTS	-	CAN1_RX	OTG_FS_ DM	-	-	-	LCD_R4	EVEN TOUT
	PA12	-	TIM1_ ETR	-	-	-	-	-	USART1_ RTS	-	CAN1_TX	OTG_FS_ DP	-	-	-	LCD_R5	EVEN TOUT



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SA1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 I8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port A	PA13	JTMS-SWDI_O	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	-	-	-	-	-	-	-	-	EVEN TOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	-	EVEN TOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	-	EVEN TOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PB3	JTDO/TRAC_ESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK/I2S3_CK	-	-	-	-	-	-	-	-	EVEN TOUT
	PB4	NJTR_ST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	-	-	-	-	-	-	EVEN TOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBus	SPI1_MOSI	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	-	EVEN TOUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	FMC_SDNE1	DCMI_D5	-	EVEN TOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FMC_NL	DCMI_VSYNC	-	EVEN TOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDIO_D4	DCMI_D6	LCD_B6	EVEN TOUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	LCD_B7	EVEN TOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	-	LCD_G4	EVEN TOUT

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SA1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 _I8	CAN1/2/ TIM12/13/14 /_LCD	OTG2_HS /_OTG1_FS	ETH	FMC/SDIO /_OTG2_FS	DCMI	LCD	SYS
Port B	PB11	-	TIM2_ CH4	-	-	I2C2_ SDA	-	-	USART3_ RX	-	-	OTG_HS_ ULPI_D4	ETH_MII_ TX_EN/ ETH_RMII _TX_EN	-	-	LCD_G5	EVEN TOUT
	PB12	-	TIM1_ BKIN	-	-	I2C2_ SMBA	SPI2_ NSS/I2 S2_WS	-	USART3_ CK	-	CAN2_RX	OTG_HS_ ULPI_D5	ETH_MII_ TXD0/ETH _RMII _TXD0	OTG_HS_ID	-	-	EVEN TOUT
	PB13	-	TIM1_ CH1N	-	-	-	SPI2_ SCK/I2 S2_CK	-	USART3_ CTS	-	CAN2_TX	OTG_HS_ ULPI_D6	ETH_MII_ TXD1/ETH _RMII_TX D1	-	-	-	EVEN TOUT
	PB14	-	TIM1_ CH2N	-	TIM8_ CH2N	-	SPI2_ MISO	I2S2ext_ SD	USART3_ RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVEN TOUT
	PB15	RTC_REFIN	TIM1_ CH3N	-	TIM8_ CH3N	-	SPI2_ MOSI/I2 S2_SD	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVEN TOUT
Port C	PC0	-	-	-	-	-	-	-	-	-	-	OTG_HS_ ULPI_STP	-	FMC_SDN_WE	-	-	EVEN TOUT
	PC1	-	-	-	-	-	-	-	-	-	-	ETH_MDC	-	-	-	-	EVEN TOUT
	PC2	-	-	-	-	-	SPI2_ MISO	I2S2ext_ SD	-	-	-	OTG_HS_ ULPI_DIR	ETH_MII_ TXD2	FMC_SDNE0	-	-	EVEN TOUT
	PC3	-	-	-	-	-	SPI2_ MOSI/I2 S2_SD	-	-	-	-	OTG_HS_ ULPI_NXT	ETH_MII_ TX_CLK	FMC_SDCKE0	-	-	EVEN TOUT
	PC4	-	-	-	-	-	-	-	-	-	-	ETH_MII_ RXD0/ETH _RMII _RXD0	-	-	-	EVEN TOUT	
	PC5	-	-	-	-	-	-	-	-	-	-	ETH_MII_ RXD1/ETH _RMII _RXD1	-	-	-	EVEN TOUT	
	PC6	-	-	TIM3_ CH1	TIM8_ CH1	-	I2S2_MCK	-	-	USART6_ TX	-	-	-	SDIO_D6	DCMI_D0	LCD_HSYNC	EVEN TOUT
	PC7	-	-	TIM3_ CH2	TIM8_ CH2	-	-	I2S3_MCK	-	USART6_ RX	-	-	-	SDIO_D7	DCMI_D1	LCD_G6	EVEN TOUT



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/LCD	OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI	LCD	SYS
Port C	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVEN TOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	-	-	-	-	SDIO_D1	DCMI_D3	-	EVEN TOUT
	PC10	-	-	-	-	-	-	SPI3_SCKI2S_3_OCK	USART3_TX	UART4_TX	-	-	-	SDIO_D2	DCMI_D8	LCD_R2	EVEN TOUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	-	-	-	SDIO_D3	DCMI_D4	-	EVEN TOUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVEN TOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
Port D	PD0	-	-	-	-	-	-	-	-	CAN1_RX	-	-	-	FMC_D2	-	-	EVEN TOUT
	PD1	-	-	-	-	-	-	-	-	CAN1_TX	-	-	-	FMC_D3	-	-	EVEN TOUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDIO_CMD	DCMI_D11	-	EVEN TOUT
	PD3	-	-	-	-	-	SPI2_SCKII_2S2_CK	-	USART2_CTS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVEN TOUT
	PD4	-	-	-	-	-	-	-	USART2 RTS	-	-	-	-	FMC_NOE	-	-	EVEN TOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	EVEN TOUT
	PD6	-	-	-	-	-	SPI3_MOSI/I2S3_SD	SAI1_SD_A	USART2_RX	-	-	-	-	FMC_NWAIT	DCMI_D10	LCD_B2	EVEN TOUT

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 _I8	CAN1/2/ TIM12/13/14 /_LCD	OTG2_HS /_OTG1_ FS	ETH	FMC/SDIO /_OTG2_FS	DCMI	LCD	SYS	
Port D	PD7	-	-	-	-	-	-	-	USART2_	CK	-	-	-	-	FMC_NE1/ FMC_NCE2	-	-	EVEN TOUT
	PD8	-	-	-	-	-	-	-	USART3_	TX	-	-	-	-	FMC_D13	-	-	EVEN TOUT
	PD9	-	-	-	-	-	-	-	USART3_	RX	-	-	-	-	FMC_D14	-	-	EVEN TOUT
	PD10	-	-	-	-	-	-	-	USART3_	CK	-	-	-	-	FMC_D15	-	LCD_B3	EVEN TOUT
	PD11	-	-	-	-	-	-	-	USART3_	CTS	-	-	-	-	FMC_A16	-	-	EVEN TOUT
	PD12	-	-	TIM4_ CH1	-	-	-	-	USART3_	RTS	-	-	-	-	FMC_A17	-	-	EVEN TOUT
	PD13	-	-	TIM4_ CH2	-	-	-	-	-	-	-	-	-	-	FMC_A18	-	-	EVEN TOUT
	PD14	-	-	TIM4_ CH3	-	-	-	-	-	-	-	-	-	-	FMC_D0	-	-	EVEN TOUT
Port E	PE0	-	-	TIM4_ ETR	-	-	-	-	UART8_Rx	-	-	-	-	FMC_NBL0	DCMI_D2	-	EVEN TOUT	
	PE1	-	-	-	-	-	-	-	UART8_Tx	-	-	-	-	FMC_NBL1	DCMI_D3	-	EVEN TOUT	
	PE2	TRAC ECLK	-	-	-	-	SPI4_ SCK	SAI1_ MCLK_A	-	-	-	-	ETH_MII_	TXD3	FMC_A23	-	-	EVEN TOUT
	PE3	TRAC ED0	-	-	-	-	-	SAI1_ SD_B	-	-	-	-	-	-	FMC_A19	-	-	EVEN TOUT
	PE4	TRAC ED1	-	-	-	-	SPI4_ NSS	SAI1_ FS_A	-	-	-	-	-	-	FMC_A20	DCMI_D4	LCD_B0	EVEN TOUT
	PE5	TRAC ED2	-	-	TIM9_ CH1	-	SPI4_M_ ISO	SAI1_ SCK_A	-	-	-	-	-	-	FMC_A21	DCMI_D6	LCD_G0	EVEN TOUT
	PE6	TRAC ED3	-	-	TIM9_ CH2	-	SPI4_ MOSI	SAI1_ SD_A	-	-	-	-	-	-	FMC_A22	DCMI_D7	LCD_G1	EVEN TOUT



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ USART4/5/7 _I8	CAN1/2/ TIM12/13/14 /_LCD	OTG2_HS /_OTG1_FS	ETH	FMC/SDIO /_OTG2_FS	DCMI	LCD	SYS
Port E	PE7	-	TIM1_ETR	-	-	-	-	-	-	UART7_Rx	-	-	-	FMC_D4	-	-	EVEN TOUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	-	UART7_Tx	-	-	-	FMC_D5	-	-	EVEN TOUT
	PE9	-	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	FMC_D6	-	-	EVEN TOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	-	-	FMC_D7	-	-	EVEN TOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	-	-	-	-	-	-	FMC_D8	-	LCD_G3	EVEN TOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	LCD_B4	EVEN TOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	LCD_DE	EVEN TOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	-	-	FMC_D11	-	LCD_CLK	EVEN TOUT
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVEN TOUT
	PF1	-				I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVEN TOUT
	PF2	-	-	-	-	I2C2_SMB	-	-	-	-	-	-	-	FMC_A2	-	-	EVEN TOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVEN TOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVEN TOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVEN TOUT
	PF6	-	-	-	TIM10_CH1	-	SPI5_NSS	SAI1_SD_B	-	UART7_Rx	-	-	-	FMC_NIORD	-	-	EVEN TOUT
	PF7	-	-	-	TIM11_CH1	-	SPI5_SCK	SAI1_MCLK_B	-	UART7_Tx	-	-	-	FMC_NREG	-	-	EVEN TOUT

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 /I8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port F	PF8	-	-	-	-	-	SPI5_MISO	SAI1_SCK_B	-	-	TIM13_CH1	-	-	FMC_NIOWR	-	-	EVEN TOUT
	PF9	-	-	-	-	-	SPI5_MOSI	SAI1_FS_B	-	-	TIM14_CH1	-	-	FMC_CD	-	-	EVEN TOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FMC_INTR	DCMI_D11	LCD_DE	EVEN TOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	-	-	FMC_SDNRAS	DCMI_D12	-	EVEN TOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVEN TOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	EVEN TOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	EVEN TOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	EVEN TOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVEN TOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVEN TOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVEN TOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVEN TOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/ FMC_BA0	-	-	EVEN TOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/ FMC_BA1	-	-	EVEN TOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FMC_INT2	DCMI_D12	LCD_R7	EVEN TOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FMC_INT3	DCMI_D13	LCD_CLK	EVEN TOUT
	PG8	-	-	-	-	-	SPI6_NSS	-	-	USART6_RTS	-	-	ETH_PPS_OUT	FMC_SDC_LK	-	-	EVEN TOUT



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SA1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 _I8	CAN1/2/ TIM12/13/14 /_LCD	OTG2_HS /_OTG1_FS	ETH	FMC/SDIO /_OTG2_FS	DCMI	LCD	SYS	
Port G	PG9	-	-	-	-	-	-	-	-	USART6_RX	-	-	-	FMC_NE2/ FMC_NCE3	DCMI_VSYNC <sup>(1)</sup>	-	EVEN TOUT	
	PG10	-	-	-	-	-	-	-	-	-	LCD_G3	-	-	FMC_NCE4_1/ FMC_NE3	DCMI_D2	LCD_B2	EVEN TOUT	
	PG11	-	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_EN/ ETH_RMII_TX_EN	FMC_NCE4_2	DCMI_D3	LCD_B3	EVEN TOUT
	PG12	-	-	-	-	-	SPI6_MISO	-	-	USART6_RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVEN TOUT	
	PG13	-	-	-	-	-	SPI6_SCK	-	-	USART6_CTS	-	-	-	ETH_MII_TXD0/ ETH_RMII_TXD0	FMC_A24	-	-	EVEN TOUT
	PG14	-	-	-	-	-	SPI6_MOSI	-	-	USART6_TX	-	-	-	ETH_MII_TXD1/ ETH_RMII_TXD1	FMC_A25	-	-	EVEN TOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	DCMI_D13	-	-	EVEN TOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PH2	-	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVEN TOUT
	PH3	-	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_COL	FMC_SDN_E0	-	LCD_R1	EVEN TOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	-	EVEN TOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_N_SS	-	-	-	-	-	-	-	FMC_SDN_WE	-	-	EVEN TOUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	-	-	FMC_SDNE1	DCMI_D8	-	-



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SA1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 _I8	CAN1/2/ TIM12/13/14 /_LCD	OTG2_HS /_OTG1_FS	ETH	FMC/SDIO /_OTG2_FS	DCMI	LCD	SYS
Port H	PH7	-	-	-	-	I2C3_SCL	SPI6_MISO	-	-	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9	-	-
	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	EVEN TOUT
	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	FMC_D17	DCMI_D0	LCD_R3	EVEN TOUT
	PH10	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	EVEN TOUT
	PH11	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	-	FMC_D19	DCMI_D2	LCD_R5	EVEN TOUT
	PH12	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	EVEN TOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	-	CAN1_TX	-	-	FMC_D21	-	LCD_G2	EVEN TOUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	FMC_D22	DCMI_D4	LCD_G3	EVEN TOUT
Port I	PI5	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	FMC_D23	DCMI_D11	LCD_G4	EVEN TOUT
	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S_S2_WS	-	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVEN TOUT
	PI1	-	-	-	-	-	SPI2_SCK/I2S_S2_CK	-	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVEN TOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVEN TOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S_2_SD							FMC_D27	DCMI_D10		EVEN TOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	-	FMC_D28	DCMI_D5	LCD_B4	EVEN TOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	-	-	FMC_D29	DCMI_D6	LCD_B5	EVEN TOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	FMC_D30	DCMI_D7	LCD_B6	EVEN TOUT



Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SAI1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 _I8	CAN1/2/ TIM12/13/14 /_LCD	OTG2_HS /_OTG1_FS	ETH	FMC/SDIO /_OTG2_FS	DCMI	LCD	SYS
Port I	P17	-	-	-	TIM8_ CH3	-	-	-	-	-	-	-	-	FMC_D29	DCMI_D7	LCD_B7	EVEN TOUT
	P18	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	P19	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVEN TOUT
	P10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVEN TOUT
	P11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_DIR	-	-	-	-	EVEN TOUT
	P12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVEN TOUT
	P13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVEN TOUT
	P14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVEN TOUT
	P15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R0	EVEN TOUT
Port J	PJ0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R1	EVEN TOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVEN TOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVEN TOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVEN TOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVEN TOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVEN TOUT
	PJ6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVEN TOUT
	PJ7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVEN TOUT

Table 12. STM32F427xx and STM32F429xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/ 10/11	I2C1/ 2/3	SPI1/2/ 3/4/5/6	SPI2/3/ SA1	SPI3/ USART1/ 2/3	USART6/ UART4/5/7 I8	CAN1/2/ TIM12/13/14 /LCD	OTG2_HS /OTG1_FS	ETH	FMC/SDIO /OTG2_FS	DCMI	LCD	SYS
Port J	PJ8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G1	EVEN TOUT
	PJ9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G2	EVEN TOUT
	PJ10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G3	EVEN TOUT
	PJ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G4	EVEN TOUT
	PJ12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B0	EVEN TOUT
	PJ13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B1	EVEN TOUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVEN TOUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVEN TOUT
Port K	PK0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G5	EVEN TOUT
	PK1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G6	EVEN TOUT
	PK2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G7	EVEN TOUT
	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVEN TOUT
	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVEN TOUT
	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVEN TOUT
	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVEN TOUT
	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVEN TOUT

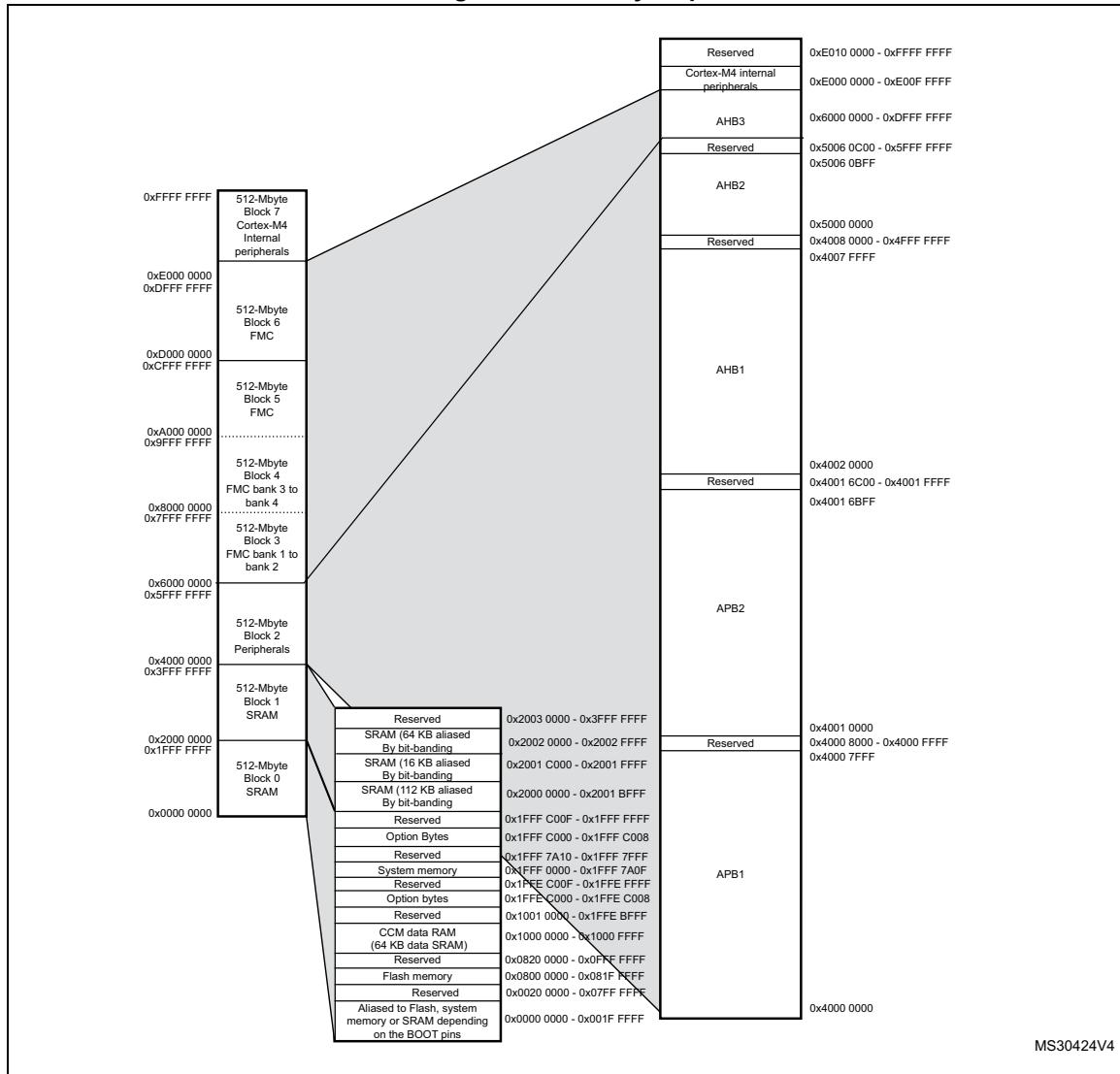
1. The DCMI\_VSYNC alternate function on PG9 is only available on silicon revision 3.



## 5 Memory mapping

The memory map is shown in [Figure 19](#).

**Figure 19. Memory map**



**Table 13. STM32F427xx and STM32F429xx register boundary addresses**

<b>Bus</b>	<b>Boundary address</b>	<b>Peripheral</b>
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 1000 - 0xBFFF FFFF	Reserved
	0xA000 0000- 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	FMC bank 4
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0X5006 0BFF	RNG
	0x5005 0400 - X5006 07FF	Reserved
	0x5005 0000 - 0X5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0X5003 FFFF	USB OTG FS

**Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)**

Bus	Boundary address	Peripheral
	0x4008 0000- 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00- 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	DMA2D
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	ETHERNET MAC
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0X4002 5000 - 0X4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0X4002 3400 - 0X4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0X4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

**Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)**

Bus	Boundary address	Peripheral
APB2	0x4001 6C00- 0x4001 FFFF	Reserved
	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 5C00 - 0x4001 67FF	Reserved
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

**Table 13. STM32F427xx and STM32F429xx register boundary addresses (continued)**

Bus	Boundary address	Peripheral
	0x4000 8000 - 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

## 6 Electrical characteristics

### 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V<sub>SS</sub>.

#### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T<sub>A</sub> = 25 °C and T<sub>A</sub> = T<sub>Amax</sub> (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

#### 6.1.2 Typical values

Unless otherwise specified, typical data are based on T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.3 V (for the 1.7 V ≤ V<sub>DD</sub> ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

#### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

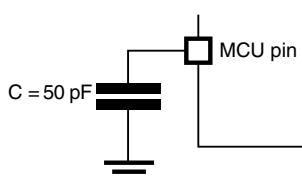
#### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 20](#).

#### 6.1.5 Pin input voltage

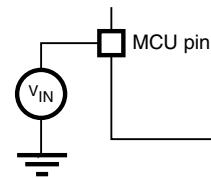
The input voltage measurement on a pin of the device is described in [Figure 21](#).

**Figure 20. Pin loading conditions**



MS19011V2

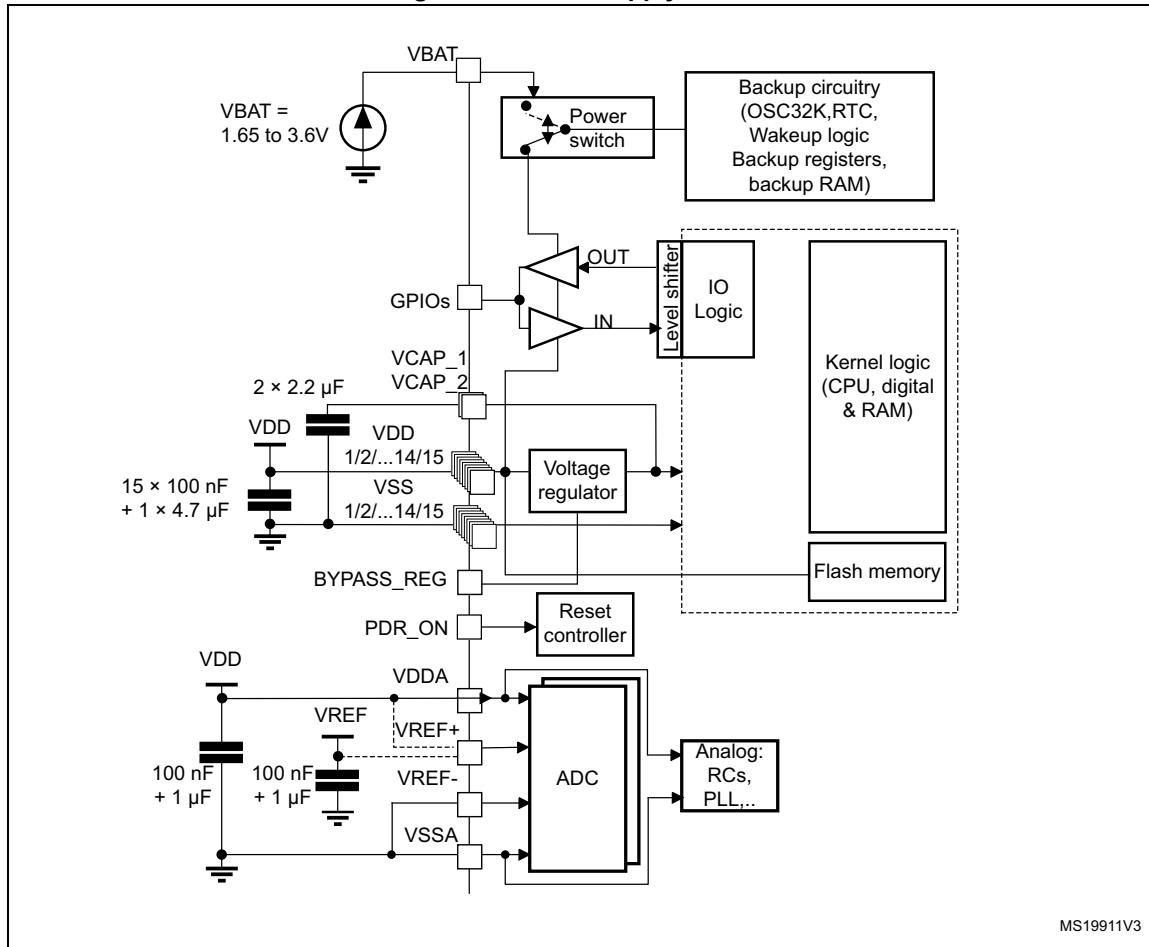
**Figure 21. Pin input voltage**



MS19010V2

### 6.1.6 Power supply scheme

Figure 22. Power supply scheme

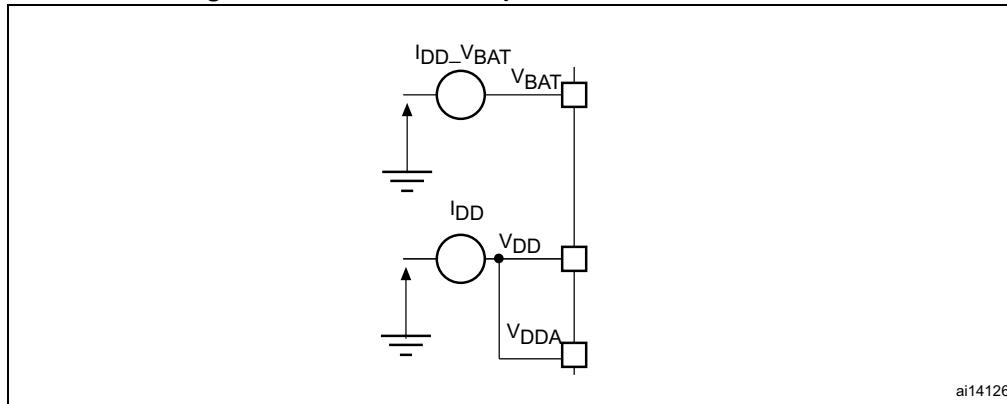


1. To connect BYPASS\_REG and PDR\_ON pins, refer to [Section 3.17: Power supply supervisor](#) and [Section 3.18: Voltage regulator](#)
2. The two  $2.2\ \mu F$  ceramic capacitors should be replaced by two  $100\ nF$  decoupling capacitors when the voltage regulator is OFF.
3. The  $4.7\ \mu F$  ceramic capacitor must be connected to one of the  $V_{DD}$  pin.
4.  $V_{DDA}=V_{DD}$  and  $V_{SSA}=V_{SS}$ .

**Caution:** Each power supply pair ( $V_{DD}/V_{SS}$ ,  $V_{DDA}/V_{SSA}$  ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

### 6.1.7 Current consumption measurement

Figure 23. Current consumption measurement scheme



## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 14: Voltage characteristics](#), [Table 15: Current characteristics](#), and [Table 16: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including $V_{DDA}$ , $V_{DD}$ and $V_{BAT}$ ) <sup>(1)</sup>	- 0.3	4.0	
$V_{IN}$	Input voltage on FT pins <sup>(2)</sup>	$V_{SS} - 0.3$	$V_{DD} + 4.0$	V
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT0 pin	$V_{SS}$	9.0	
$ \Delta V_{DDx} $	Variations between different $V_{DD}$ power pins	-	50	
$ V_{SSx} - V_{SSL} $	Variations between all the different ground pins including $V_{REF-}$	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section 6.3.15: Absolute maximum ratings (electrical sensitivity)</a>		

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2.  $V_{IN}$  maximum value must always be respected. Refer to [Table 15](#) for the values of the maximum allowed injected current.

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit	
$\Sigma I_{VDD}$	Total current into sum of all $V_{DD\_x}$ power lines (source) <sup>(1)</sup>	270	mA	
$\Sigma I_{VSS}$	Total current out of sum of all $V_{SS\_x}$ ground lines (sink) <sup>(1)</sup>	- 270		
$I_{VDD}$	Maximum current into each $V_{DD\_x}$ power line (source) <sup>(1)</sup>	100		
$I_{VSS}$	Maximum current out of each $V_{SS\_x}$ ground line (sink) <sup>(1)</sup>	- 100		
$I_{IO}$	Output current sunk by any I/O and control pin	25		
	Output current sourced by any I/Os and control pin	- 25		
$\Sigma I_{IO}$	Total output current sunk by sum of all I/O and control pins <sup>(2)</sup>	120		
	Total output current sourced by sum of all I/Os and control pins <sup>(2)</sup>	- 120		
$I_{INJ(PIN)}$ <sup>(3)</sup>	Injected current on FT pins <sup>(4)</sup>	- 5/+0		
	Injected current on NRST and BOOT0 pins <sup>(4)</sup>			
	Injected current on TTa pins <sup>(5)</sup>	±5		
$\Sigma I_{INJ(PIN)}$ <sup>(5)</sup>	Total injected current (sum of all I/O and control pins) <sup>(6)</sup>	±25		

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in [Section 6.3.21: 12-bit ADC characteristics](#).
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by  $V_{IN} > V_{DDA}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 14](#) for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	- 65 to +150	°C
$T_J$	Maximum junction temperature	125	°C

## 6.3 Operating conditions

### 6.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Unit
$f_{HCLK}$	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF	0	-	120	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF 0	-	144	
				-	168	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF 0	-	168	
				-	180	
$f_{PCLK1}$	Internal APB1 clock frequency	Over-drive OFF	0	-	42	V
		Over-drive ON	0	-	45	
$f_{PCLK2}$	Internal APB2 clock frequency	Over-drive OFF	0	-	84	
		Over-drive ON	0	-	90	
$V_{DD}$	Standard operating voltage		1.7 <sup>(2)</sup>	-	3.6	V
$V_{DDA}_{(3)(4)}$	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as $V_{DD}^{(5)}$	1.7 <sup>(2)</sup>	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
$V_{BAT}$	Backup operating voltage		1.65	-	3.6	
$V_{12}$	Regulator ON: 1.2 V internal voltage on $V_{CAP\_1}/V_{CAP\_2}$ pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 120 MHz HCLK max frequency	1.08	1.14	1.20	V
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 144 MHz HCLK max frequency with over-drive OFF or 168 MHz with over-drive ON	1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on $V_{CAP\_1}/V_{CAP\_2}$ pins <sup>(6)</sup>	Max frequency 120 MHz	1.10	1.14	1.20	
		Max frequency 144 MHz	1.20	1.26	1.32	
		Max frequency 168 MHz	1.26	1.32	1.38	

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Unit
$V_{IN}$	Input voltage on RST and FT pins <sup>(7)</sup>	$2 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-0.3	-	5.5	V
		$V_{DD} \leq 2 \text{ V}$	-0.3	-	5.2	
	Input voltage on TTa pins		-0.3	-	$V_{DDA} + 0.3$	
	Input voltage on BOOT0 pin		0	-	9	
$P_D$	Power dissipation at $T_A = 85^\circ\text{C}$ for suffix 6 or $T_A = 105^\circ\text{C}$ for suffix 7 <sup>(8)</sup>	LQFP100	-	-	465	mW
		WLCSP143	-	-	641	
		LQFP144	-	-	500	
		UFBGA169	-	-	385	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		LQFP208	-	-	1053	
		TFBGA216	-	-	690	
$T_A$	Ambient temperature for 6 suffix version	Maximum power dissipation	-40		85	$^\circ\text{C}$
		Low power dissipation <sup>(9)</sup>	-40		105	
$T_A$	Ambient temperature for 7 suffix version	Maximum power dissipation	-40		105	$^\circ\text{C}$
		Low power dissipation <sup>(9)</sup>	-40		125	
$T_J$	Junction temperature range	6 suffix version	-40		105	$^\circ\text{C}$
		7 suffix version	-40		125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2.  $V_{DD}/V_{DDA}$  minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).
3. When the ADC is used, refer to [Table 74: ADC characteristics](#).
4. If  $V_{REF+}$  pin is present, it must respect the following condition:  $V_{DDA}-V_{REF+} < 1.2 \text{ V}$ .
5. It is recommended to power  $V_{DD}$  and  $V_{DDA}$  from the same source. A maximum difference of 300 mV between  $V_{DD}$  and  $V_{DDA}$  can be tolerated during power-up and power-down operation.
6. The over-drive mode is not supported when the internal regulator is OFF.
7. To sustain a voltage higher than  $VDD+0.3$ , the internal Pull-up and Pull-Down resistors must be disabled
8. If  $T_A$  is lower, higher  $P_D$  values are allowed as long as  $T_J$  does not exceed  $T_{Jmax}$ .
9. In low power dissipation state,  $T_A$  can be extended to this range as long as  $T_J$  does not exceed  $T_{Jmax}$ .

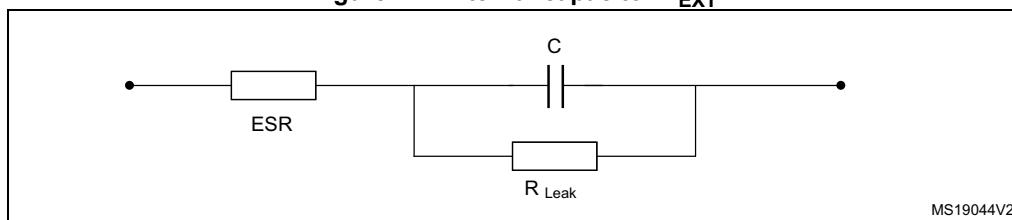
**Table 18. Limitations depending on the operating power supply range**

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ( $f_{Flashmax}$ )	Maximum HCLK frequency vs Flash memory wait states (1)(2)	I/O operation	Possible Flash memory operations
$V_{DD} = 1.7$ to $2.1$ V <sup>(3)</sup>	Conversion time up to 1.2 Msps	20 MHz <sup>(4)</sup>	168 MHz with 8 wait states and over-drive OFF	No I/O compensation	8-bit erase and program operations only
$V_{DD} = 2.1$ to $2.4$ V	Conversion time up to 1.2 Msps	22 MHz	180 MHz with 8 wait states and over-drive ON	No I/O compensation	16-bit erase and program operations
$V_{DD} = 2.4$ to $2.7$ V	Conversion time up to 2.4 Msps	24 MHz	180 MHz with 7 wait states and over-drive ON	I/O compensation works	16-bit erase and program operations
$V_{DD} = 2.7$ to $3.6$ V <sup>(5)</sup>	Conversion time up to 2.4 Msps	30 MHz	180 MHz with 5 wait states and over-drive ON	I/O compensation works	32-bit erase and program operations

- Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
- Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
- $V_{DD}/V_{DDA}$  minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).
- Prefetch is not available.
- The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

### 6.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor  $C_{EXT}$  to the VCAP1/VCAP2 pins.  $C_{EXT}$  is specified in [Table 19](#).

**Figure 24. External capacitor  $C_{EXT}$** 

- Legend: ESR is the equivalent series resistance.

**Table 19. VCAP1/VCAP2 operating conditions<sup>(1)</sup>**

Symbol	Parameter	Conditions
$C_{EXT}$	Capacitance of external capacitor	$2.2 \mu F$
ESR	ESR of external capacitor	$< 2 \Omega$

- When bypassing the voltage regulator, the two  $2.2 \mu F$   $V_{CAP}$  capacitors are not required and should be replaced by two  $100 nF$  decoupling capacitors.

### 6.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for  $T_A$ .

**Table 20. Operating conditions at power-up / power-down (regulator ON)**

Symbol	Parameter	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate	20	$\infty$	$\mu\text{s}/\text{V}$
	$V_{DD}$ fall time rate	20	$\infty$	

### 6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for  $T_A$ .

**Table 21. Operating conditions at power-up / power-down (regulator OFF)<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate	Power-up	20	$\infty$	$\mu\text{s}/\text{V}$
	$V_{DD}$ fall time rate	Power-down	20	$\infty$	
$t_{VCAP}$	$V_{CAP\_1}$ and $V_{CAP\_2}$ rise time rate	Power-up	20	$\infty$	$\mu\text{s}/\text{V}$
	$V_{CAP\_1}$ and $V_{CAP\_2}$ fall time rate	Power-down	20	$\infty$	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when  $V_{DD}$  reach below 1.08 V.

### 6.3.5 Reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#).

**Table 22. reset and power control block characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis		-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}^{(1)}$	PDR hysteresis		-	40	-	mV
$V_{BOR1}$	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V
$V_{BOR2}$	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
$V_{BOR3}$	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}^{(1)}$	BOR hysteresis		-	100	-	mV
$T_{RSTTEMPO}^{(1)(2)}$	POR reset temporization		0.5	1.5	3.0	ms

**Table 22. reset and power control block characteristics (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{RUSH}^{(1)}$	InRush current on voltage regulator power-on (POR or wakeup from Standby)		-	160	200	mA
$E_{RUSH}^{(1)}$	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	$V_{DD} = 1.7 \text{ V}$ , $T_A = 105^\circ\text{C}$ , $I_{RUSH} = 171 \text{ mA}$ for $31 \mu\text{s}$	-	-	5.4	$\mu\text{C}$

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from  $V_{BAT}$ ) to the instant when first instruction is read by the user application code.

### 6.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in [Table 23](#). They are subject to general operating conditions for  $T_A$ .

**Table 23. Over-drive switching characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	$\mu\text{s}$
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	$\mu\text{s}$
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

### 6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 23: Current consumption measurement scheme](#).

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at  $V_{DD}$  or  $V_{SS}$  (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to  $f_{HCLK}$  frequency and  $V_{DD}$  range (see [Table 18: Limitations depending on the operating power supply range](#)).
- Regulator ON
- The voltage scaling and over-drive mode are adjusted to  $f_{HCLK}$  frequency as follows:
  - Scale 3 for  $f_{HCLK} \leq 120$  MHz
  - Scale 2 for  $120 \text{ MHz} < f_{HCLK} \leq 144$  MHz
  - Scale 1 for  $144 \text{ MHz} < f_{HCLK} \leq 180$  MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK,  $f_{PCLK1} = f_{HCLK}/4$ , and  $f_{PCLK2} = f_{HCLK}/2$ .
- External clock frequency is 4 MHz and PLL is ON when  $f_{HCLK}$  is higher than 25 MHz.
- The maximum values are obtained for  $V_{DD} = 3.6$  V and a maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.3$  V unless otherwise specified.

**Table 24. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM<sup>(1)</sup>**

Symbol	Parameter	Conditions	$f_{HCLK}$ (MHz)	Typ	Max <sup>(2)</sup>			Unit
					$T_A = 25^\circ C$	$T_A = 85^\circ C$	$T_A = 105^\circ C$	
$I_{DD}$	Supply current in RUN mode	All Peripherals enabled <sup>(3)(4)</sup>	180	98	104 <sup>(5)</sup>	123	141 <sup>(5)</sup>	mA
			168	89	98 <sup>(5)</sup>	116	133 <sup>(5)</sup>	
			150	75	84	100	115	
			144	72	81	96	112	
			120	54	58	72	85	
			90	43	45	56	66	
			60	29	30	52	62	
			30	16	20	34	46	
			25	13	16	30	43	
			16	11	13	27	39	
			8	5	9	23	36	
			4	4	8	21	34	
			2	2	7	20	33	
		All Peripherals disabled <sup>(3)</sup>	180	44	47 <sup>(5)</sup>	69	87 <sup>(5)</sup>	
			168	41	45 <sup>(5)</sup>	66	83 <sup>(5)</sup>	
			150	36	39	57	73	
			144	33	37	56	72	
			120	25	29	43	56	
			90	20	23	41	53	
			60	14	16	34	45	
			30	8	12	26	39	

1. Code and data processing running from SRAM1 using boot pins.
2. Guaranteed by characterization.
3. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
4. When the ADC is ON (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
5. Guaranteed by test in production.

**Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)**

Symbol	Parameter	Conditions	$f_{HCLK}$ (MHz)	Typ	Max <sup>(1)</sup>			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
$I_{DD}$	Supply current in RUN mode	All Peripherals enabled <sup>(2)(3)</sup>	180	103	112	140	151	mA
			168	98	107	126	144	
			150	87	95	112	128	
			144	85	92	108	124	
			120	66	71	85	99	
			90	54	58	69	80	
			60	37	39	47	55	
			30	20	24	39	51	
			25	17	21	35	48	
			16	12	16	30	42	
			8	7	11	24	37	
			4	5	8	22	35	
			2	3	7	21	34	
		All Peripherals disabled <sup>(3)</sup>	180	57	62	87	106	
			168	50	54	76	93	
			150	46	50	70	86	
			144	45	49	68	84	
			120	36	41	56	69	
			90	29	34	46	57	
			60	21	24	33	41	
			30	13	17	31	44	
			25	11	15	28	41	
			16	8	12	25	38	
			8	5	9	23	35	
			4	4	7	21	34	
			2	3	6.5	20	33	

1. Guaranteed by characterization unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Table 26. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	$f_{HCLK}$ (MHz)	Typ	Max <sup>(1)</sup>			Unit
					$T_A = 25^\circ C$	$T_A = 85^\circ C$	$T_A = 105^\circ C$	
$I_{DD}$	Supply current in Sleep mode	All Peripherals enabled <sup>(2)</sup>	180	78	89 <sup>(3)</sup>	110	130 <sup>(3)</sup>	mA
			168	66	75 <sup>(3)</sup>	93	110 <sup>(3)</sup>	
			150	56	61	80	96	
			144	54	58	78	94	
			120	40	44	59	72	
			90	32	34	46	56	
			60	22	23	31	45	
			30	10	16	30	43	
			25	9	14	28	40	
			16	5	12	25	40	
			8	3	8	22	35	
			4	3	7	21	34	
		All Peripherals disabled	2	2	6.5	20	33	
			180	21	26 <sup>(3)</sup>	54	76 <sup>(3)</sup>	
			168	16	20 <sup>(3)</sup>	41	58 <sup>(3)</sup>	
			150	14	17	36	52	
			144	13	16.5	35	51	
			120	10	14	28	41	
			90	8	13	26	37	
			60	6	9	24	37	

1. Guaranteed by characterization unless otherwise specified.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Based on characterization, tested in production.

Table 27. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max <sup>(1)</sup>			Unit
				$V_{DD} = 3.6 \text{ V}$			
			$T_A = 25^\circ\text{C}$	$T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 105^\circ\text{C}$	
$I_{DD\_STOP\_NM}$ (normal mode)	Supply current in Stop mode with voltage regulator in main regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.40	1.50	14.00	25.00	mA
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.35	1.50	14.00	25.00	
	Supply current in Stop mode with voltage regulator in Low Power regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.29	1.10	10.00	18.00	
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.23	1.10	10.00	18.00	
$I_{DD\_STOP\_UDM}$ (under-drive mode)	Supply current in Stop mode with voltage regulator in main regulator and under-drive mode	Flash memory in Deep power down mode, main regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.19	0.50	6.00	9.00	
	Supply current in Stop mode with voltage regulator in Low Power regulator and under-drive mode	Flash memory in Deep power down mode, Low Power regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.10	0.40	4.00	7.00	

1. Data based on characterization, tested in production.

**Table 28. Typical and maximum current consumptions in Standby mode**

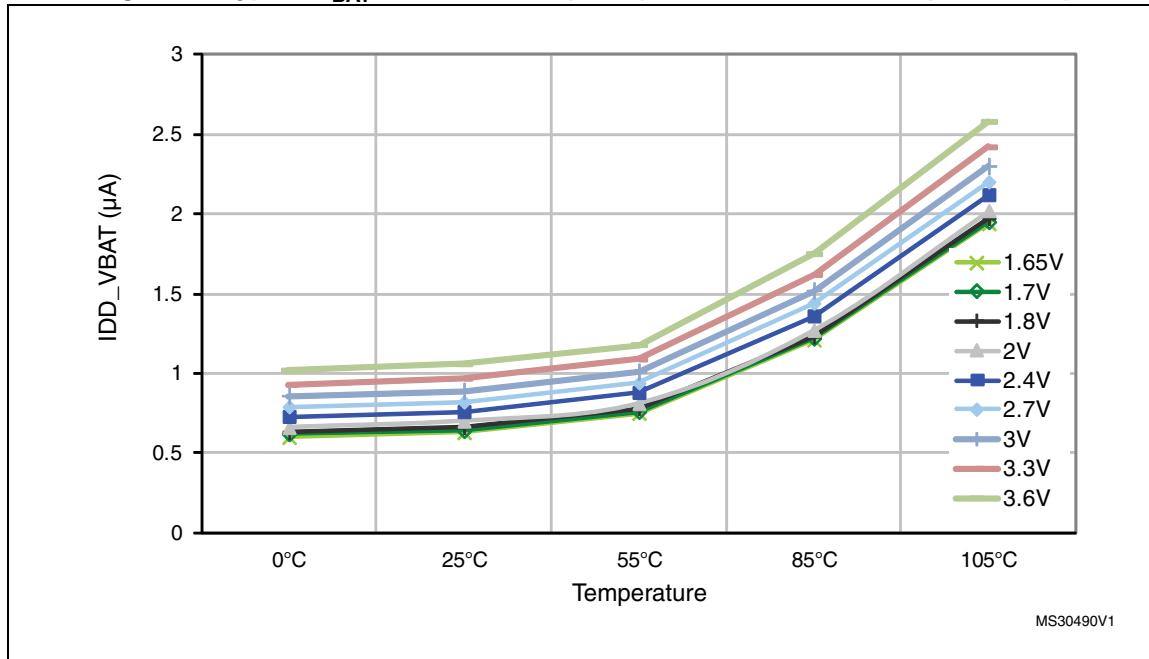
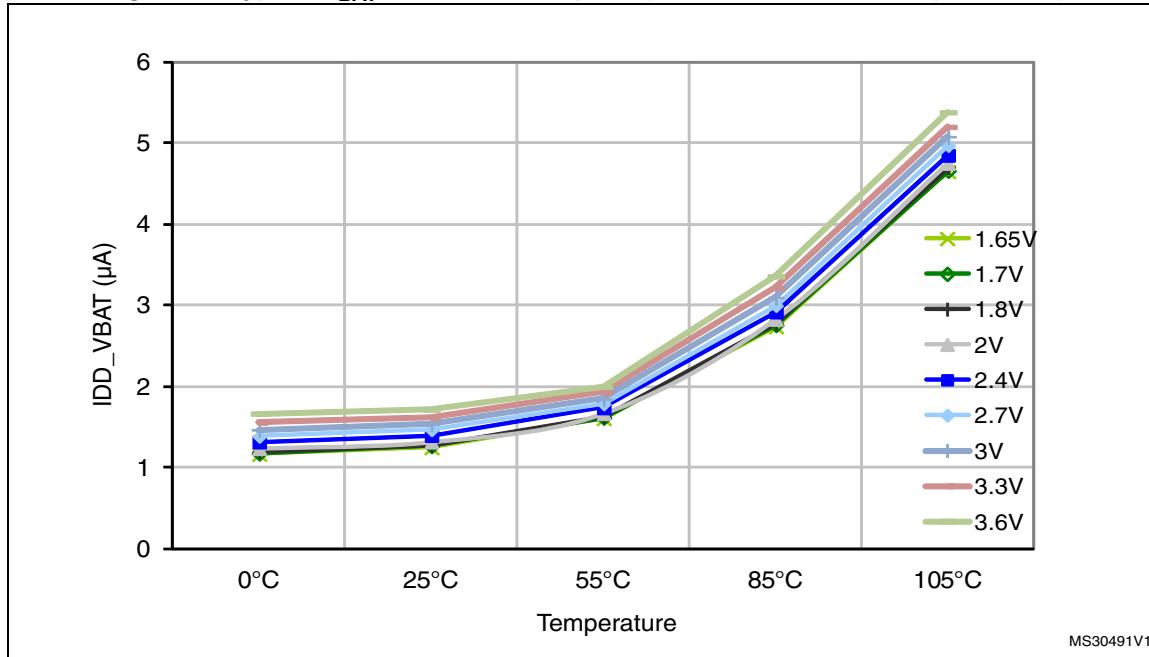
Symbol	Parameter	Conditions	Typ <sup>(1)</sup>			Max <sup>(2)</sup>			Unit
			T <sub>A</sub> = 25 °C			T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	
			V <sub>DD</sub> = 1.7 V	V <sub>DD</sub> = 2.4 V	V <sub>DD</sub> = 3.3 V	V <sub>DD</sub> = 3.6 V			
I <sub>DD_STBY</sub>	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator (LSE) and RTC ON	2.80	3.00	3.60	7.00	19.00	36.00	μA
		Backup SRAM OFF, low-speed oscillator (LSE) and RTC ON	2.30	2.60	3.10	6.00	16.00	31.00	
		Backup SRAM ON, RTC and LSE OFF	2.30	2.50	2.90	6.00 <sup>(3)</sup>	18.00 <sup>(3)</sup>	35.00 <sup>(3)</sup>	
		Backup SRAM OFF, RTC and LSE OFF	1.70	1.90	2.20	5.00 <sup>(3)</sup>	15.00 <sup>(3)</sup>	30.00 <sup>(3)</sup>	

1. The typical current consumption values are given with PDR OFF (internal reset OFF). When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 μA.
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

**Table 29. Typical and maximum current consumptions in V<sub>BAT</sub> mode**

Symbol	Parameter	Conditions <sup>(1)</sup>	Typ			Max <sup>(2)</sup>			Unit
			T <sub>A</sub> = 25 °C			T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C		
			V <sub>BAT</sub> = 1.7 V	V <sub>BAT</sub> = 2.4 V	V <sub>BAT</sub> = 3.3 V	V <sub>BAT</sub> = 3.6 V			
I <sub>DD_VBAT</sub>	Backup domain supply current	Backup SRAM ON, low-speed oscillator (LSE) and RTC ON	1.28	1.40	1.62	6	11		μA
		Backup SRAM OFF, low-speed oscillator (LSE) and RTC ON	0.66	0.76	0.97	3	5		
		Backup SRAM ON, RTC and LSE OFF	0.70	0.72	0.74	5	10		
		Backup SRAM OFF, RTC and LSE OFF	0.10	0.10	0.10	2	4		

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C<sub>L</sub> of 6 pF for typical values.
2. Guaranteed by characterization results.

**Figure 25. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/backup RAM OFF)****Figure 26. Typical  $V_{BAT}$  current consumption (LSE and RTC ON/backup RAM ON)**

### Additional current consumption

The MCU is placed under the following conditions:

- All I/O pins are configured in analog mode.
- The Flash memory access time is adjusted to fHCLK frequency.
- The voltage scaling is adjusted to fHCLK frequency as follows:
  - Scale 3 for  $f_{\text{HCLK}} \leq 120$  MHz,
  - Scale 2 for  $120 \text{ MHz} < f_{\text{HCLK}} \leq 144$  MHz
  - Scale 1 for  $144 \text{ MHz} < f_{\text{HCLK}} \leq 180$  MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK,  $f_{\text{PCLK1}} = f_{\text{HCLK}}/4$ , and  $f_{\text{PCLK2}} = f_{\text{HCLK}}/2$ .
- HSE crystal clock frequency is 25 MHz.
- When the regulator is OFF, V12 is provided externally as described in [Table 17: General operating conditions](#)
- $T_A = 25^\circ\text{C}$ .

**Table 30. Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch),  $V_{\text{DD}}=1.7$  V<sup>(1)</sup>**

Symbol	Parameter	Conditions	$f_{\text{HCLK}}$ (MHz)	Typ	Unit
$I_{\text{DD}}$	Supply current in RUN mode from $V_{\text{DD}}$ supply	All Peripheral enabled	168	88.2	mA
			150	74.3	
			144	71.3	
			120	52.9	
			90	42.6	
			60	28.6	
			30	15.7	
			25	12.3	
		All Peripheral disabled	168	40.6	
			150	30.6	
			144	32.6	
			120	24.7	
			90	19.7	
			60	13.6	
			30	7.7	
			25	6.7	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

**Table 31. Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch)<sup>(1)</sup>**

Symbol	Parameter	Conditions	$f_{HCLK}$ (MHz)	VDD=3.3 V		VDD=1.7 V		Unit
				$I_{DD12}$	$I_{DD}$	$I_{DD12}$	$I_{DD}$	
$I_{DD12} / I_{DD}$	Supply current in RUN mode from $V_{12}$ and $V_{DD}$ supply	All Peripherals enabled	168	77.8	1.3	76.8	1.0	mA
			150	70.8	1.3	69.8	1.0	
			144	64.5	1.3	63.6	1.0	
			120	49.9	1.2	49.3	0.9	
			90	39.2	1.3	38.7	1.0	
			60	27.2	1.2	26.8	0.9	
			30	15.6	1.2	15.4	0.9	
			25	13.6	1.2	13.5	0.9	
		All Peripherals disabled	168	38.2	1.3	37.0	1.0	
			150	34.6	1.3	33.4	1.0	
			144	31.3	1.3	30.3	1.0	
			120	24.0	1.2	23.2	0.9	
			90	18.1	1.4	18.0	1.0	
			60	12.9	1.2	12.5	0.9	
			30	7.2	1.2	6.9	0.9	
			25	6.3	1.2	6.1	0.9	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

**Table 32. Typical current consumption in Sleep mode, regulator ON,  $V_{DD}=1.7\text{ V}^{(1)}$** 

Symbol	Parameter	Conditions	$f_{HCLK}$ (MHz)	Typ	Unit
$I_{DD}$	Supply current in Sleep mode from $V_{DD}$ supply	All Peripherals enabled	168	65.5	mA
			150	55.5	
			144	53.5	
			120	39.0	
			90	31.6	
			60	21.7	
			30	9.8	
			25	8.8	
	All Peripherals disabled		168	15.7	
			150	13.7	
			144	12.7	
			120	9.7	
			90	7.7	
			60	5.7	
			30	4.7	
			25	2.8	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

**Table 33. Tyical current consumption in Sleep mode, regulator OFF<sup>(1)</sup>**

Symbol	Parameter	Conditions	f <sub>HCLK</sub> (MHz)	VDD=3.3 V		VDD=1.7 V		Unit
				I <sub>DD12</sub>	I <sub>DD</sub>	I <sub>DD12</sub>	I <sub>DD</sub>	
I <sub>DD12</sub> /I <sub>DD</sub>	Supply current in Sleep mode from V <sub>12</sub> and V <sub>DD</sub> supply	All Peripherals enabled	180	61.5	1.4	-	-	mA
			168	59.4	1.3	59.4	1.0	
			150	53.9	1.3	53.9	1.0	
			144	49.0	1.3	49.0	1.0	
			120	38.0	1.2	38.0	0.9	
			90	29.3	1.4	29.3	1.1	
			60	20.2	1.2	20.2	0.9	
			30	11.9	1.2	11.9	0.9	
			25	10.4	1.2	10.4	0.9	
		All Peripherals disabled	180	14.9	1.4	-	-	
			168	14.0	1.3	14.0	1.0	
			150	12.6	1.3	12.6	1.0	
			144	11.5	1.3	11.5	1.0	
			120	8.7	1.2	8.7	0.9	
			90	7.1	1.4	7.1	1.1	
			60	5.0	1.2	5.0	0.9	
			30	3.1	1.2	3.1	0.9	
			25	2.8	1.2	2.8	0.9	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC, or DAC) is not included.

## I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

### I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 56: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

### I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 35: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$  is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$  is the MCU supply voltage

$f_{SW}$  is the I/O switching frequency

$C$  is the total capacitance seen by the I/O pin:  $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 34. Switching output I/O current consumption<sup>(1)</sup>

Symbol	Parameter	Conditions	I/O toggling frequency (fsw)	Typ	Unit
$I_{DDIO}$	I/O switching Current	$V_{DD} = 3.3 \text{ V}$ $C = C_{INT}^{(2)}$	2 MHz	0.0	mA
			8 MHz	0.2	
			25 MHz	0.6	
			50 MHz	1.1	
			60 MHz	1.3	
			84 MHz	1.8	
			90 MHz	1.9	
		$V_{DD} = 3.3 \text{ V}$ $C_{EXT} = 0 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.1	
			8 MHz	0.4	
			25 MHz	1.23	
			50 MHz	2.43	
			60 MHz	2.93	
			84 MHz	3.86	
			90 MHz	4.07	
$I_{DDIO}$	I/O switching Current	$V_{DD} = 3.3 \text{ V}$ $C_{EXT} = 10 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.18	mA
			8 MHz	0.67	
			25 MHz	2.09	
			50 MHz	3.6	
			60 MHz	4.5	
			84 MHz	7.8	
			90 MHz	9.8	
		$V_{DD} = 3.3 \text{ V}$ $C_{EXT} = 22 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.26	
			8 MHz	1.01	
			25 MHz	3.14	
			50 MHz	6.39	
			60 MHz	10.68	
			2 MHz	0.33	
			8 MHz	1.29	
$I_{DDIO}$	I/O switching Current	$V_{DD} = 3.3 \text{ V}$ $C_{EXT} = 33 \text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	25 MHz	4.23	mA
			50 MHz	11.02	

1.  $C_S$  is the PCB board capacitance including the pad pin.  $C_S = 7 \text{ pF}$  (estimated value).

2. This test is performed by cutting the LQFP176 package pin (pad removal).

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
  - All peripherals are disabled unless otherwise mentioned.
  - I/O compensation cell enabled.
  - The ART accelerator is ON.
  - Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
  - HCLK is the system clock.  $f_{PCLK1} = f_{HCLK}/4$ , and  $f_{PCLK2} = f_{HCLK}/2$ .
- The given value is calculated by measuring the difference of current consumption
- with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{HCLK} = 180$  MHz (Scale1 + over-drive ON),  $f_{HCLK} = 144$  MHz (Scale 2),  
 $f_{HCLK} = 120$  MHz (Scale 3)"
- Ambient operating temperature is 25 °C and  $V_{DD}=3.3$  V.

**Table 35. Peripheral current consumption**

Peripheral	$I_{DD}$ ( Typ) <sup>(1)</sup>			Unit
	Scale 1	Scale 2	Scale 3	
AHB1 (up to 180 MHz)	GPIOA	2.50	2.36	2.08
	GPIOB	2.56	2.36	2.08
	GPIOC	2.44	2.29	2.00
	GPIOD	2.50	2.36	2.08
	GPIOE	2.44	2.29	2.00
	GPIOF	2.44	2.29	2.00
	GPIOG	2.39	2.22	2.00
	GPIOH	2.33	2.15	1.92
	GPIOI	2.39	2.22	2.00
	GPIOJ	2.33	2.15	1.92
	GPIOK	2.33	2.15	1.92
	OTG_HS+ULPI	27.00	24.86	21.92
	CRC	0.44	0.42	0.33
	BKPSRAM	0.78	0.69	0.58
	DMA1	25.33	23.26	20.50
	DMA2	24.72	22.71	20.00
	DMA2D	28.50	26.32	23.33
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	21.56	20.07	17.75

Table 35. Peripheral current consumption (continued)

Peripheral		I <sub>DD</sub> ( Typ) <sup>(1)</sup>			Unit
		Scale 1	Scale 2	Scale 3	
AHB2 (up to 180 MHz)	OTG_FS	25.67	26.67	23.58	µA/MHz
	DCMI	3.72	3.40	3.00	
	RNG	2.28	2.36	2.17	
AHB3 (up to 180 MHz)	FMC	21.39	19.79	17.50	µA/MHz
Bus matrix <sup>(2)</sup>		14.06	13.19	11.75	µA/MHz
APB1 (up to 45 MHz)	TIM2	17.56	16.42	14.47	µA/MHz
	TIM3	14.22	13.36	11.80	
	TIM4	14.89	13.64	12.13	
	TIM5	17.33	16.42	14.47	
	TIM6	2.89	2.53	2.47	
	TIM7	3.11	2.81	2.47	
	TIM12	7.33	6.97	6.13	
	TIM13	4.89	4.47	4.13	
	TIM14	5.56	5.31	4.80	
	PWR	11.11	10.31	9.13	
	USART2	4.22	3.92	3.47	
	USART3	4.44	4.19	3.80	
	UART4	4.00	3.92	3.47	
	UART5	4.00	3.92	3.47	
	UART7	4.00	3.92	3.47	
	UART8	3.78	3.92	3.47	
	I2C1	4.00	3.92	3.47	
	I2C2	4.00	3.92	3.47	
	I2C3	4.00	3.92	3.47	
	SPI2 <sup>(3)</sup>	3.11	3.08	2.80	
	SPI3 <sup>(3)</sup>	3.56	3.36	3.13	
	I2S2	2.89	2.81	2.47	
	I2S3	3.33	3.08	2.80	
	CAN1	6.89	6.42	5.80	
	CAN2	6.67	6.14	5.47	
	DAC <sup>(4)</sup>	2.89	2.25	2.13	
	WWDG	0.89	0.86	0.80	

Table 35. Peripheral current consumption (continued)

Peripheral	I <sub>DD</sub> ( Typ) <sup>(1)</sup>			Unit
	Scale 1	Scale 2	Scale 3	
APB2 (up to 90 MHz)	SDIO	8.11	8.75	7.83
	TIM1	17.11	15.97	14.17
	TIM8	17.33	16.11	14.33
	TIM9	7.22	6.67	6.00
	TIM10	4.56	4.31	3.83
	TIM11	4.78	4.44	4.00
	ADC1 <sup>(5)</sup>	4.67	4.31	3.83
	ADC2 <sup>(5)</sup>	4.78	4.44	4.00
	ADC3 <sup>(5)</sup>	4.56	4.17	3.67
	SPI1	1.44	1.39	1.17
	USART1	4.00	3.75	3.33
	USART6	4.00	3.75	3.33
	SPI4	1.44	1.39	1.17
	SPI5	1.44	1.39	1.17
	SPI6	1.44	1.39	1.17
	SYSCFG	0.78	0.69	0.67
	LCD_TFT	39.89	37.22	33.17
	SAI1	3.78	3.47	3.17

- 1. When the I/O compensation cell is ON, I<sub>DD</sub> typical value increases by 0.22 mA.
- 2. The BusMatrix is automatically active when at least one master is ON.
- 3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI\_I2SCFGR register.
- 4. When the DAC is ON and EN1/2 bits are set in DAC\_CR register, add an additional power consumption of 0.8 mA per DAC channel for the analog part.
- 5. When the ADC is ON (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

### 6.3.8      **Wakeup time from low-power modes**

The wakeup times given in [Table 36](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and  $V_{DD}=3.3$  V.

**Table 36. Low-power mode wakeup timings**

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	Max <sup>(1)</sup>	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	6	-	CPU clock cycle
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	13.6	-	$\mu$ s
		Main regulator is ON and Flash memory in Deep power down mode	93	111	
		Low power regulator is ON	22	32	
		Low power regulator is ON and Flash memory in Deep power down mode	103	126	
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	105	128	$\mu$ s
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode )	125	155	
$t_{WUSTDBY}^{(2)(3)}$	Wakeup from Standby mode		318	412	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first
3.  $t_{WUSTDBY}$  maximum value is given at  $-40^{\circ}\text{C}$ .

### 6.3.9 External clock source characteristics

#### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 56: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 27](#).

The characteristics given in [Table 37](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

**Table 37. High-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSE\_ext}$	External user clock source frequency <sup>(1)</sup>		1	-	50	MHz
$V_{HSEH}$	OSC_IN input pin high level voltage		0.7 $V_{DD}$	-	$V_{DD}$	V
$V_{HSEL}$	OSC_IN input pin low level voltage		$V_{SS}$	-	0.3 $V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time <sup>(1)</sup>		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time <sup>(1)</sup>		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance <sup>(1)</sup>		-	5	-	pF
$DuCy(HSE)$	Duty cycle		45	-	55	%
$I_L$	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 1$	$\mu A$

1. Guaranteed by design.

### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 56: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 28](#).

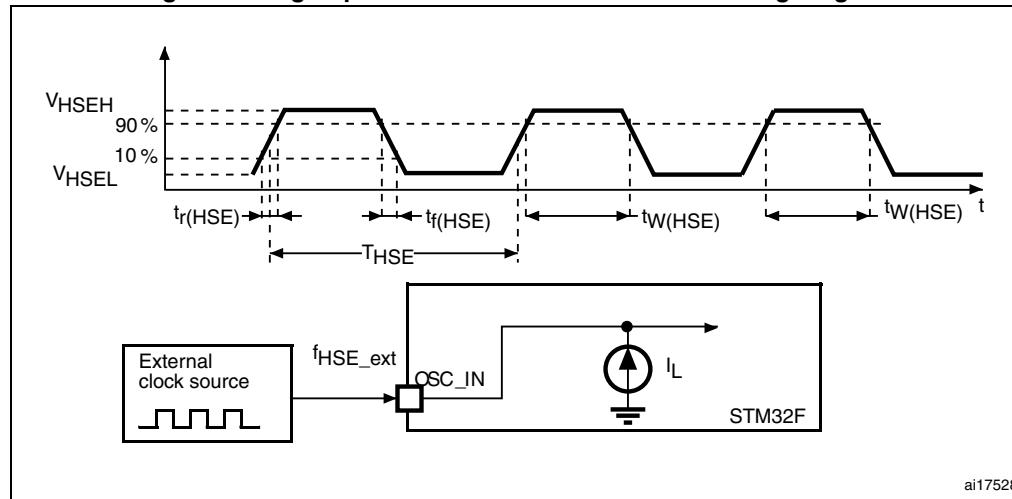
The characteristics given in [Table 38](#) result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

**Table 38. Low-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LSE\_ext}$	User External clock source frequency <sup>(1)</sup>		-	32.768	1000	kHz
$V_{LSEH}$	OSC32_IN input pin high level voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub>	V
$V_{LSEL}$	OSC32_IN input pin low level voltage		V <sub>SS</sub>	-	0.3V <sub>DD</sub>	
$t_w(LSE)$ $t_f(LSE)$	OSC32_IN high or low time <sup>(1)</sup>		450	-	-	ns
$t_r(LSE)$ $t_f(LSE)$	OSC32_IN rise or fall time <sup>(1)</sup>		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance <sup>(1)</sup>		-	5	-	pF
DuCy <sub>(LSE)</sub>	Duty cycle		30	-	70	%
$I_L$	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 1$	$\mu A$

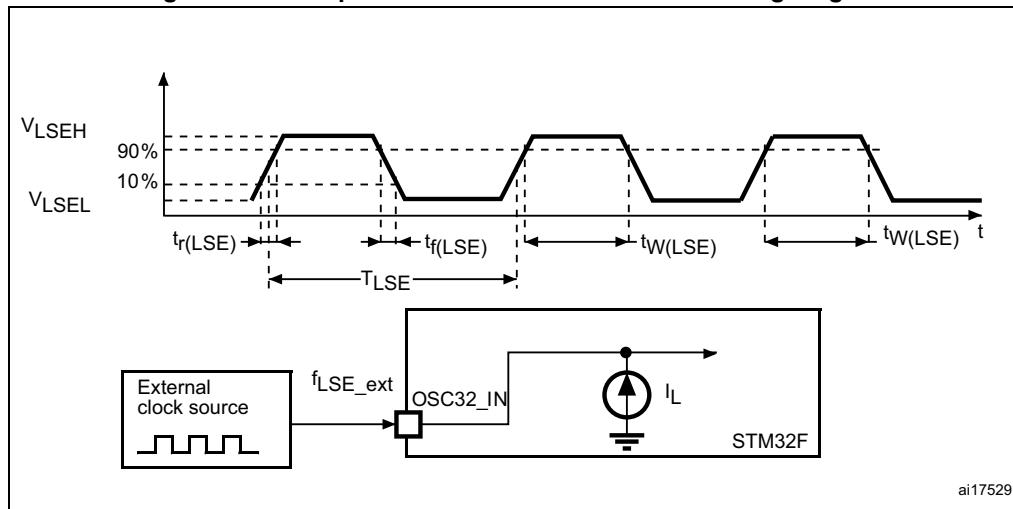
1. Guaranteed by design.

**Figure 27. High-speed external clock source AC timing diagram**



ai17528

Figure 28. Low-speed external clock source AC timing diagram



ai17529

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 39](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 39. HSE 4-26 MHz oscillator characteristics<sup>(1)</sup>

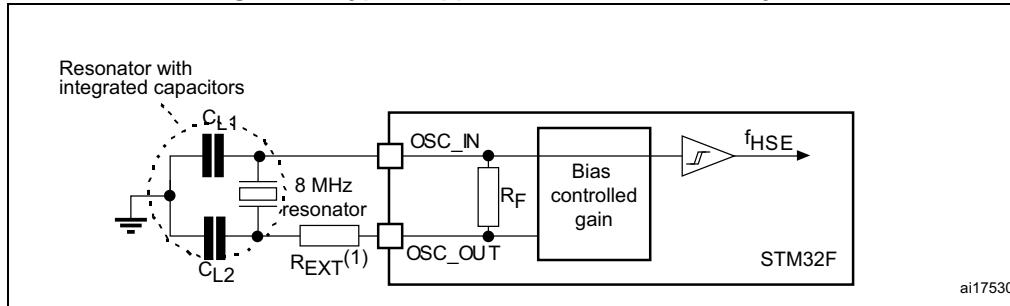
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{OSC\_IN}$	Oscillator frequency		4	-	26	MHz
$R_F$	Feedback resistor		-	200	-	kΩ
$I_{DD}$	HSE current consumption	$V_{DD}=3.3\text{ V}$ , $ESR= 30\text{ }\Omega$ , $C_L=5\text{ pF}@25\text{ MHz}$	-	450	-	μA
		$V_{DD}=3.3\text{ V}$ , $ESR= 30\text{ }\Omega$ , $C_L=10\text{ pF}@25\text{ MHz}$	-	530	-	
$ACC_{HSE}^{(2)}$	HSE accuracy		- 500	-	500	ppm
$G_m\_crit\_max$	Maximum critical crystal $g_m$	Startup	-	-	1	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	$V_{DD}$ is stabilized	-	2	-	ms

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For  $C_{L1}$  and  $C_{L2}$ , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 29](#)).  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing  $C_{L1}$  and  $C_{L2}$ .

**Note:** For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

**Figure 29. Typical application with an 8 MHz crystal**



1.  $R_{EXT}$  value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 40](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

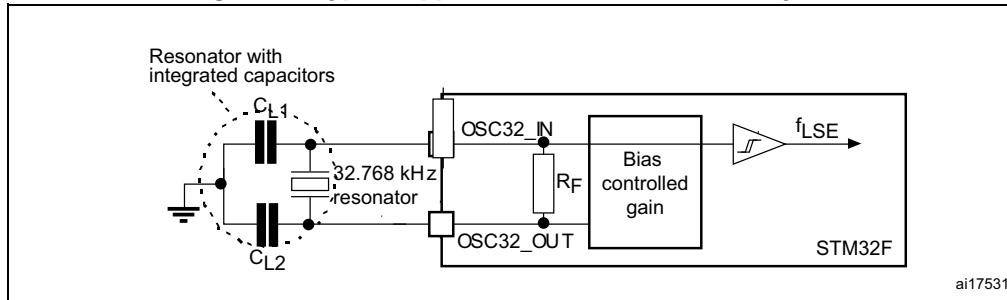
**Table 40. LSE oscillator characteristics ( $f_{LSE} = 32.768$  kHz)<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_F$	Feedback resistor		-	18.4	-	MΩ
$I_{DD}$	LSE current consumption		-	-	1	µA
$ACC_{LSE}^{(2)}$	LSE accuracy		-500	-	500	ppm
$G_m\_crit\_max$	Maximum critical crystal $g_m$	Startup	-	-	0.56	µA/V
$t_{SU(LSE)}^{(3)}$	startup time	$V_{DD}$ is stabilized	-	2	-	s

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. Refer to application note AN2867.
3.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

**Note:** For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website [www.st.com](http://www.st.com).

Figure 30. Typical application with a 32.768 kHz crystal



### 6.3.10 Internal clock source characteristics

The parameters given in [Table 41](#) and [Table 42](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#).

#### High-speed internal (HSI) RC oscillator

Table 41. HSI oscillator characteristics <sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSI}$	Frequency	-	-	16	-	MHz
	HSI user-trimming step <sup>(2)</sup>	-	-	-	1	%
ACC <sub>HSI</sub>	Accuracy of the HSI oscillator	$T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$ <sup>(3)</sup>	- 8	-	4.5	%
		$T_A = -10 \text{ to } 85 \text{ }^\circ\text{C}$ <sup>(3)</sup>	- 4	-	4	%
		$T_A = 25 \text{ }^\circ\text{C}$ <sup>(4)</sup>	- 1	-	1	%
$t_{su(HSI)}$ <sup>(2)</sup>	HSI oscillator startup time	-	-	2.2	4	$\mu\text{s}$
$I_{DD(HSI)}$ <sup>(2)</sup>	HSI oscillator power consumption	-	-	60	80	$\mu\text{A}$

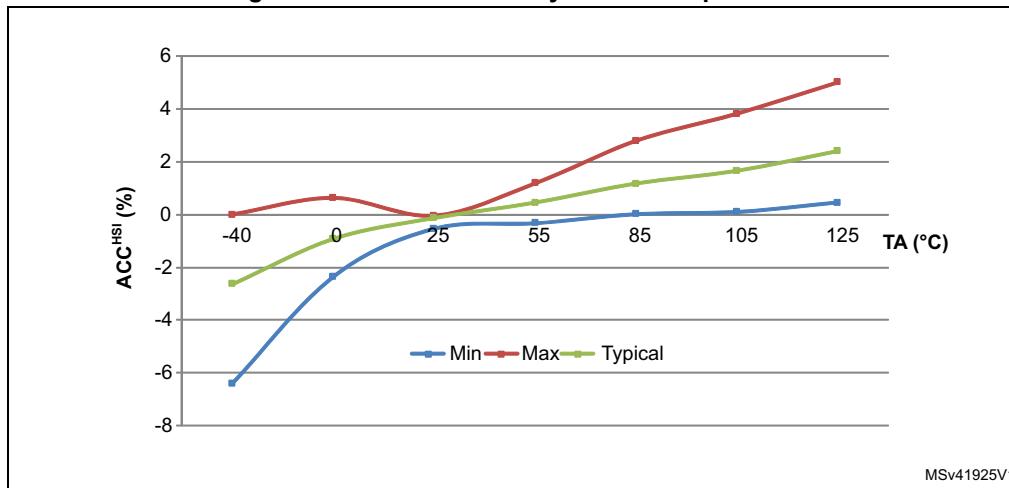
1.  $V_{DD} = 3.3 \text{ V}$ ,  $T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$  unless otherwise specified.

2. Guaranteed by design.

3. Guaranteed by characterization results.

4. Factory calibrated, parts not soldered.

Figure 31. ACCHSI accuracy versus temperature



1. Guaranteed by characterization results.

### Low-speed internal (LSI) RC oscillator

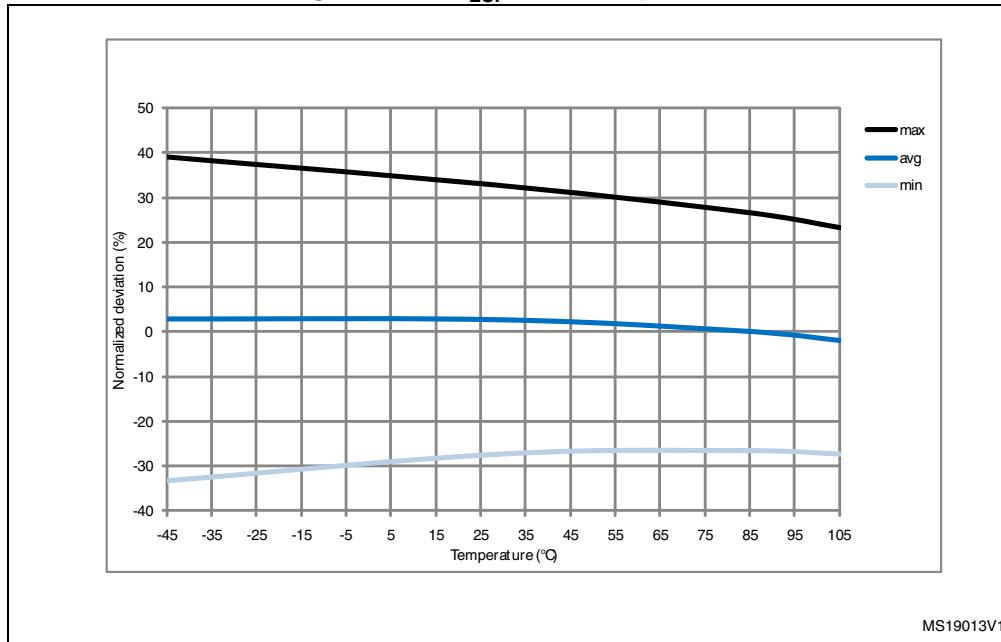
Table 42. LSI oscillator characteristics <sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Frequency	17	32	47	kHz
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	15	40	μs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	0.4	0.6	μA

1.  $V_{DD} = 3$  V,  $T_A = -40$  to  $105$  °C unless otherwise specified.

2. Guaranteed by characterization results.

3. Guaranteed by design.

Figure 32. ACC<sub>LSI</sub> versus temperature

### 6.3.11 PLL characteristics

The parameters given in [Table 43](#) and [Table 44](#) are derived from tests performed under temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 17](#).

Table 43. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>PLL_IN</sub>	PLL input clock <sup>(1)</sup>		0.95 <sup>(2)</sup>	1	2.10	MHz
f <sub>PLL_OUT</sub>	PLL multiplier output clock		24	-	180	MHz
f <sub>PLL48_OUT</sub>	48 MHz PLL multiplier output clock		-	48	75	MHz
f <sub>VCO_OUT</sub>	PLL VCO output		100	-	432	MHz
t <sub>LOCK</sub>	PLL lock time	VCO freq = 100 MHz	75	-	200	μs
		VCO freq = 432 MHz	100	-	300	

Table 43. Main PLL characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Jitter <sup>(3)</sup>	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-
			peak to peak	-	±150	-
	Period Jitter	System clock 120 MHz	RMS	-	15	-
			peak to peak	-	±200	-
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples	-	32	-	ps
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples	-	40	-	ps
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples	-	330	-	ps
I <sub>DD(PLL)</sub> <sup>(4)</sup>	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
I <sub>DDA(PLL)</sub> <sup>(4)</sup>	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

- Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
- Guaranteed by design.
- The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
- Guaranteed by characterization results.

Table 44. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>PLLI2S_IN</sub>	PLLI2S input clock <sup>(1)</sup>		0.95 <sup>(2)</sup>	1	2.10	MHz
f <sub>PLLI2S_OUT</sub>	PLLI2S multiplier output clock		-	-	216	MHz
f <sub>VCO_OUT</sub>	PLLI2S VCO output		100	-	432	MHz
t <sub>LOCK</sub>	PLLI2S lock time	VCO freq = 100 MHz	75	-	200	μs
		VCO freq = 432 MHz	100	-	300	
Jitter <sup>(3)</sup>	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-
			peak to peak	-	±280	-
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples	-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples	-	400	-	ps

**Table 44. PLLI2S (audio PLL) characteristics (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(\text{PLLI2S})}^{(4)}$	PLLI2S power consumption on $V_{DD}$	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(\text{PLLI2S})}^{(4)}$	PLLI2S power consumption on $V_{DDA}$	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

**Table 45. PLLISAI (audio and LCD-TFT PLL) characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{PLLSAI\_IN}}$	PLLSAI input clock <sup>(1)</sup>		0.95 <sup>(2)</sup>	1	2.10	MHz
$f_{\text{PLLSAI\_OUT}}$	PLLSAI multiplier output clock		-	-	216	MHz
$f_{\text{VCO\_OUT}}$	PLLSAI VCO output		100	-	432	MHz
$t_{\text{LOCK}}$	PLLSAI lock time	VCO freq = 100 MHz	75	-	200	$\mu\text{s}$
		VCO freq = 432 MHz	100	-	300	
Jitter <sup>(3)</sup>	Main SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS peak to peak	- -	90 $\pm 280$	- ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	- ps
		Cycle to cycle at 48 KHz on 1000 samples		-	400	- ps
$I_{DD(\text{PLLSAI})}^{(4)}$	PLLSAI power consumption on $V_{DD}$	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(\text{PLLSAI})}^{(4)}$	PLLSAI power consumption on $V_{DDA}$	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

### 6.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 52: EMI characteristics](#)). It is available only on the main PLL.

**Table 46. SSCG parameters constraint**

Symbol	Parameter	Min	Typ	Max <sup>(1)</sup>	Unit
f <sub>Mod</sub>	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	2 <sup>15</sup> - 1	-

1. Guaranteed by design.

#### Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$\text{MODEPER} = \text{round}[f_{\text{PLL\_IN}} / (4 \times f_{\text{Mod}})]$$

f<sub>PLL\_IN</sub> and f<sub>Mod</sub> must be expressed in Hz.

As an example:

If f<sub>PLL\_IN</sub> = 1 MHz, and f<sub>Mod</sub> = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$\text{MODEPER} = \text{round}[10^6 / (4 \times 10^3)] = 250$$

#### Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times md \times \text{PLLN} / (100 \times 5 \times \text{MODEPER})]$$

f<sub>VCO\_OUT</sub> must be expressed in MHz.

With a modulation depth (md) = ±2% (4% peak to peak), and PLLN = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times 2 \times 240 / (100 \times 5 \times 250)] = 126 \text{md(quantitazied)}\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{\text{quantized}}\% = (\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \text{PLLN})$$

As a result:

$$md_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(\text{peak})$$

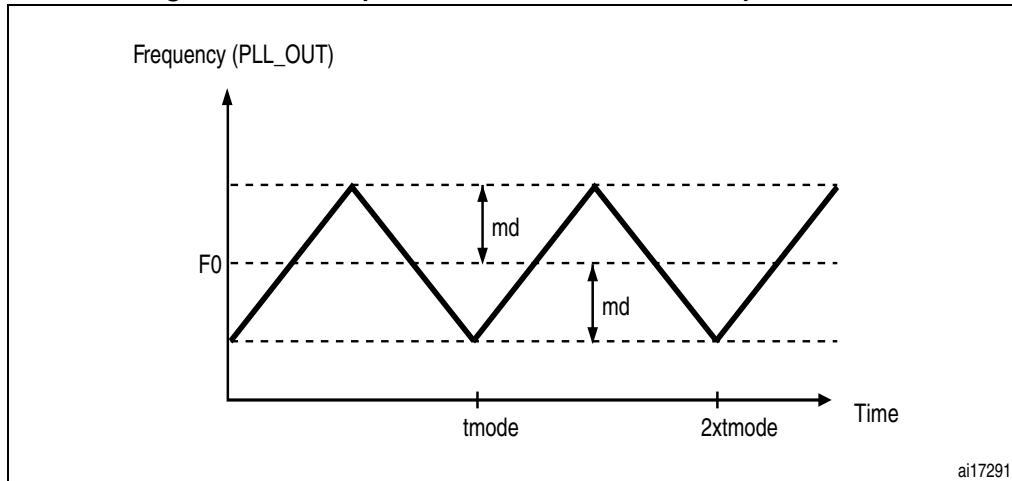
*Figure 33* and *Figure 34* show the main PLL output clock waveforms in center spread and down spread modes, where:

$F_0$  is  $f_{PLL\_OUT}$  nominal.

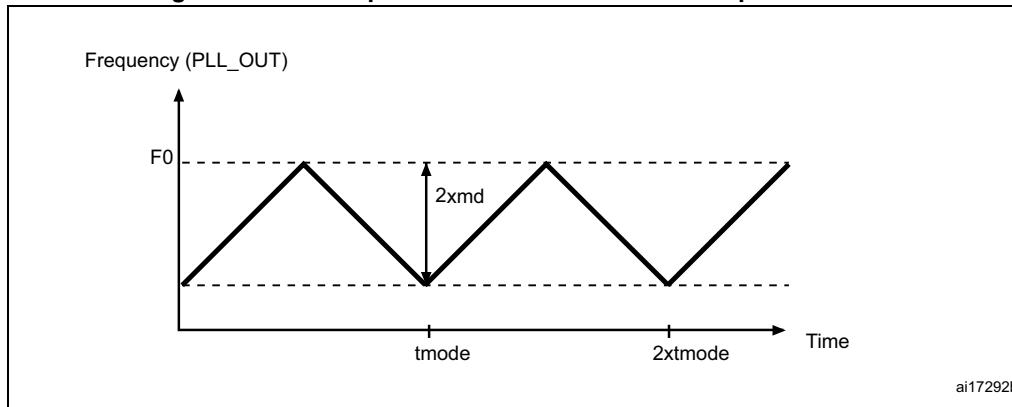
$T_{mode}$  is the modulation period.

$md$  is the modulation depth.

**Figure 33. PLL output clock waveforms in center spread mode**



**Figure 34. PLL output clock waveforms in down spread mode**



### 6.3.13 Memory characteristics

#### Flash memory

The characteristics are given at  $TA = -40$  to  $105^\circ\text{C}$  unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

**Table 47. Flash memory characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD}$	Supply current	Write / Erase 8-bit mode, $V_{DD} = 1.7\text{ V}$	-	5	-	mA
		Write / Erase 16-bit mode, $V_{DD} = 2.1\text{ V}$	-	8	-	
		Write / Erase 32-bit mode, $V_{DD} = 3.3\text{ V}$	-	12	-	

**Table 48. Flash memory programming**

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
$t_{\text{prog}}$	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100 <sup>(2)</sup>	$\mu\text{s}$
$t_{\text{ERASE16KB}}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{\text{ERASE64KB}}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{\text{ERASE128KB}}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
$t_{\text{ME}}$	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	

**Table 48. Flash memory programming (continued)**

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
t <sub>BE</sub>	Bank erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V <sub>prog</sub>	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.  
 2. The maximum programming time is measured after 100K erase operations.

**Table 49. Flash memory programming with V<sub>PP</sub>**

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
t <sub>prog</sub>	Double word programming	T <sub>A</sub> = 0 to +40 °C V <sub>DD</sub> = 3.3 V V <sub>PP</sub> = 8.5 V	-	16	100 <sup>(2)</sup>	μs
t <sub>ERASE16KB</sub>	Sector (16 KB) erase time		-	230	-	ms
t <sub>ERASE64KB</sub>	Sector (64 KB) erase time		-	490	-	
t <sub>ERASE128KB</sub>	Sector (128 KB) erase time		-	875	-	
t <sub>ME</sub>	Mass erase time		-	6.9	-	s
t <sub>BE</sub>	Bank erase time		-	6.9	-	s
V <sub>prog</sub>	Programming voltage		2.7	-	3.6	V
V <sub>PP</sub>	V <sub>PP</sub> voltage range		7	-	9	V
I <sub>PP</sub>	Minimum current sunk on the V <sub>PP</sub> pin		10	-	-	mA
t <sub>VPP</sub> <sup>(3)</sup>	Cumulative time during which V <sub>PP</sub> is applied		-	-	1	hour

1. Guaranteed by design.  
 2. The maximum programming time is measured after 100K erase operations.  
 3. V<sub>PP</sub> should only be connected during programming/erasing.

**Table 50. Flash memory endurance and data retention**

Symbol	Parameter	Conditions	Value	Unit
			Min <sup>(1)</sup>	
N <sub>END</sub>	Endurance	T <sub>A</sub> = -40 to +85 °C (6 suffix versions) T <sub>A</sub> = -40 to +105 °C (7 suffix versions)	10	kcycles
t <sub>RET</sub>	Data retention	1 kcycle <sup>(2)</sup> at T <sub>A</sub> = 85 °C	30	Years
		1 kcycle <sup>(2)</sup> at T <sub>A</sub> = 105 °C	10	
		10 kcycles <sup>(2)</sup> at T <sub>A</sub> = 55 °C	20	

1. Guaranteed by characterization results.

2. Cycling performed over the whole temperature range.

### 6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V<sub>DD</sub> and V<sub>SS</sub> through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 51](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 51. EMS characteristics**

Symbol	Parameter	Conditions	Level/ Class
V <sub>FESD</sub>	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V <sub>DD</sub> = 3.3 V, LQFP176, T <sub>A</sub> = +25 °C, f <sub>HCLK</sub> = 168 MHz, conforms to IEC 61000-4-2	2B
V <sub>EFTB</sub>	Fast transient voltage burst limits to be applied through 100 pF on V <sub>DD</sub> and V <sub>SS</sub> pins to induce a functional disturbance	V <sub>DD</sub> = 3.3 V, LQFP176, T <sub>A</sub> = +25 °C, f <sub>HCLK</sub> = 168 MHz, conforms to IEC 61000-4-2	4A

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, PH2, PH3, PH4, PH5, PA3, PA4, PA5, PA6, PA7, PC4, and PC5.

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC<sup>7</sup> code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

**Table 52. EMI characteristics**

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f <sub>HSE</sub> /f <sub>CPU</sub> ]	Max vs. [f <sub>HSE</sub> /f <sub>CPU</sub> ]	Unit
				25/168 MHz	25/180 MHz	
S <sub>EMI</sub>	Peak level	V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	16	19	dB $\mu$ V
			30 to 130 MHz	23	23	
			130 MHz to 1GHz	25	22	
			SAE EMI Level	4	4	
	Peak level	V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, ART ON, all peripheral clocks enabled, clock dithering enabled	0.1 to 30 MHz	17	16	dB $\mu$ V
			30 to 130 MHz	8	10	
			130 MHz to 1GHz	11	16	
			SAE EMI level	3.5	3.5	

### 6.3.15 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts  $\times$  (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESD S5.3.1 standards.

**Table 53. ESD absolute maximum ratings**

Symbol	Ratings	Conditions	Class	Maximum value <sup>(1)</sup>	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25^\circ\text{C}$ conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25^\circ\text{C}$ conforming to ANSI/ESD S5.3.1, LQFP100/144/176, UFBGA169/176, TFBGA176 and WLCSP143 packages	C3	250	
		$T_A = +25^\circ\text{C}$ conforming to ANSI/ESD S5.3.1, LQFP208 package	C3	250	

1. Guaranteed by characterization results.

#### Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

**Table 54. Electrical sensitivities**

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105^\circ\text{C}$ conforming to JESD78A	II level A

### 6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below  $V_{SS}$  or above  $V_{DD}$  (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of  $-5 \mu A/+0 \mu A$  range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in [Table 55](#).

**Table 55. I/O current injection susceptibility<sup>(1)</sup>**

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
$I_{INJ}$	Injected current on BOOT0 pin	- 0	NA	mA
	Injected current on NRST pin	- 0	NA	
	Injected current on PA0, PA1, PA2, PA3, PA6, PA7, PB0, PC0, PC1, PC2, PC3, PC4, PC5, PH1, PH2, PH3, PH4, PH5	- 0	NA	
	Injected current on TTa pins: PA4 and PA5	- 0	+5	
	Injected current on any other FT pin	- 5	NA	

1. NA = not applicable.

**Note:** *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

### 6.3.17 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 56: I/O static characteristics](#) are derived from tests performed under the conditions summarized in [Table 17](#). All I/Os are CMOS and TTL compliant.

**Table 56. I/O static characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	FT, TTa and NRST I/O input low level voltage	$1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	-	$0.35V_{DD} - 0.04^{(1)}$	V
	BOOT0 I/O input low level voltage	$1.75 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}, -40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$	-	-	$0.3V_{DD}^{(2)}$	
		$1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}, 0^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$	-	-	$0.1V_{DD} + 0.1^{(1)}$	
$V_{IH}$	FT, TTa and NRST I/O input high level voltage <sup>(5)</sup>	$1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$0.45V_{DD} + 0.3^{(1)}$	-	-	V
	BOOT0 I/O input high level voltage	$1.75 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}, -40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$	$0.7V_{DD}^{(2)}$	-	-	
		$1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}, 0^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$	$0.17V_{DD} + 0.7^{(1)}$	-	-	
$V_{HYS}$	FT, TTa and NRST I/O input hysteresis	$1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$10\%V_{DD}^{(3)}$	-	-	V
	BOOT0 I/O input hysteresis	$1.75 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}, -40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$	0.1	-	-	
		$1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}, 0^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$		-	-	
$I_{Ikg}$	I/O input leakage current <sup>(4)</sup>	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 1$	$\mu\text{A}$
	I/O FT input leakage current <sup>(5)</sup>	$V_{IN} = 5 \text{ V}$	-	-	3	

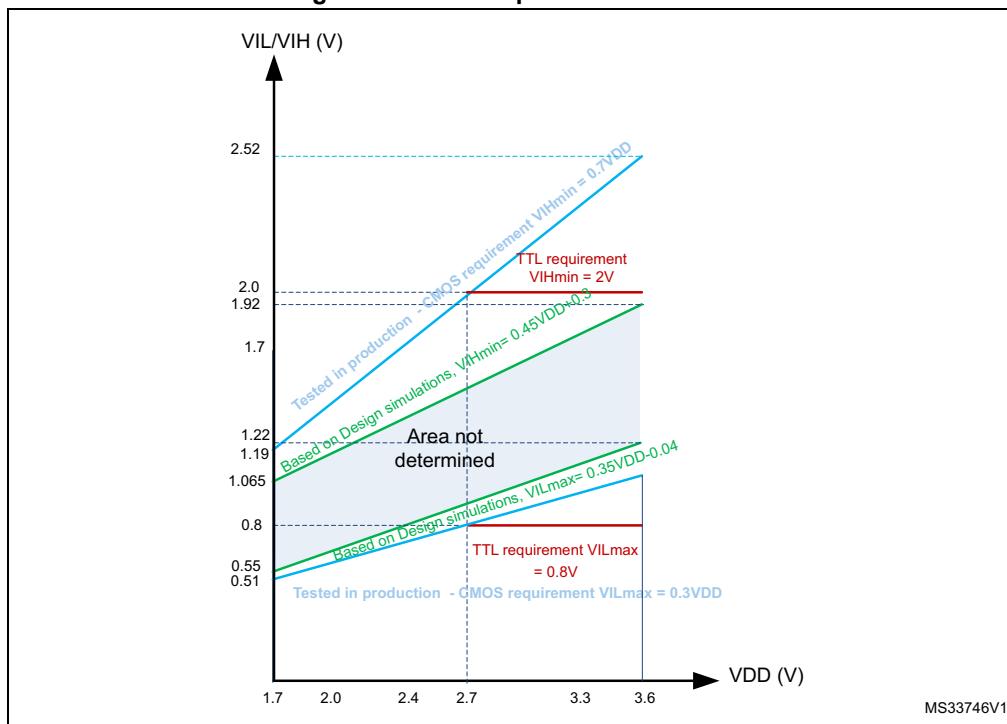
Table 56. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{PU}$	Weak pull-up equivalent resistor <sup>(6)</sup>	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
			7	10	14	
$R_{PD}$	Weak pull-down equivalent resistor <sup>(7)</sup>	$V_{IN} = V_{DD}$	30	40	50	$k\Omega$
			7	10	14	
$C_{IO}^{(8)}$	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 55: I/O current injection susceptibility](#)
5. To sustain a voltage higher than  $VDD + 0.3$  V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 55: I/O current injection susceptibility](#)
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in [Figure 35](#).

Figure 35. FT I/O input characteristics



### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to  $\pm 8$  mA, and sink or source up to  $\pm 20$  mA (with a relaxed  $V_{OL}/V_{OH}$ ) except PC13, PC14, PC15 and PI8 which can sink or source up to  $\pm 3$  mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#). In particular:

- The sum of the currents sourced by all the I/Os on  $V_{DD}$ , plus the maximum Run consumption of the MCU sourced on  $V_{DD}$ , cannot exceed the absolute maximum rating  $\Sigma I_{VDD}$  (see [Table 15](#)).
- The sum of the currents sunk by all the I/Os on  $V_{SS}$  plus the maximum Run consumption of the MCU sunk on  $V_{SS}$  cannot exceed the absolute maximum rating  $\Sigma I_{VSS}$  (see [Table 15](#)).

## Output voltage levels

Unless otherwise specified, the parameters given in [Table 57](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#). All I/Os are CMOS and TTL compliant.

**Table 57. Output voltage characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port <sup>(2)</sup> $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD} - 0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port <sup>(2)</sup> $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$1.3^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD} - 1.3^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD} - 0.4^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(5)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD} - 0.4^{(5)}$	-	

1. The  $I_{IO}$  current sunk by the device must always respect the absolute maximum rating specified in [Table 15](#), and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VSS}$ .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The  $I_{IO}$  current sourced by the device must always respect the absolute maximum rating specified in [Table 15](#) and the sum of  $I_{IO}$  (I/O ports and control pins) must not exceed  $I_{VDD}$ .
4. Based on characterization data.
5. Guaranteed by design.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 36](#) and [Table 58](#), respectively.

Unless otherwise specified, the parameters given in [Table 58](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#).

**Table 58. I/O AC characteristics<sup>(1)(2)</sup>**

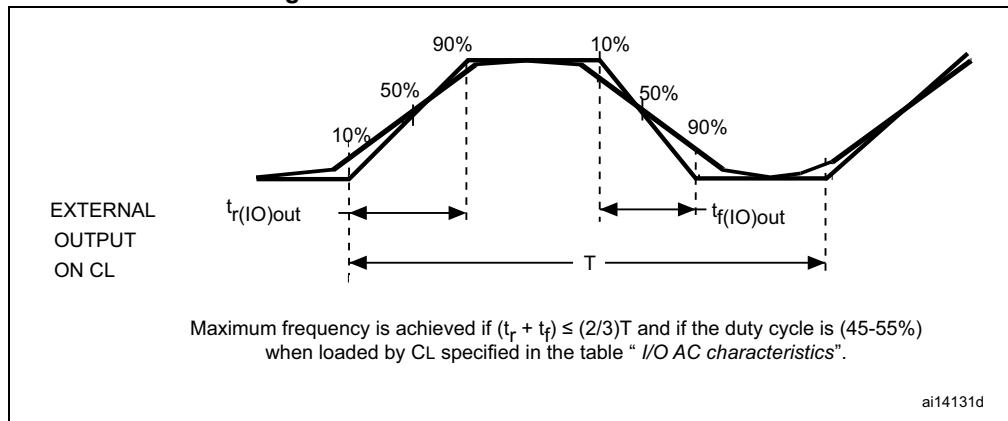
OSPEEDRy [1:0] bit value <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
00	$f_{max(IO)out}$	Maximum frequency <sup>(3)</sup>	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	MHz		
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	2			
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	8			
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	4			
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	3			
	$t_{f(IO)out}/t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.7 \text{ V} \text{ to } 3.6 \text{ V}$	-	-	100	ns		
01	$f_{max(IO)out}$	Maximum frequency <sup>(3)</sup>	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	25	MHz		
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	12.5			
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10			
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	50			
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	20			
	$t_{f(IO)out}/t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	12.5	ns		
10			$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	10			
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	6			
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	20			
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10			
$f_{max(IO)out}$	Maximum frequency <sup>(3)</sup>	$C_L = 40 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	50 <sup>(4)</sup>	MHz			
		$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	100 <sup>(4)</sup>				
		$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	25				
		$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	50				
		$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	42.5				
$t_{f(IO)out}/t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 40 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	6	ns			
		$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4				
		$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10				
		$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	6				

Table 58. I/O AC characteristics<sup>(1)(2)</sup> (continued)

OSPEEDRy [1:0] bit value <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{max(IO)out}$	Maximum frequency <sup>(3)</sup>	$C_L = 30 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	100 <sup>(4)</sup>	MHz
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	50	
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	42.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	180 <sup>(4)</sup>	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	100	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	72.5	
	$t_f(IO)out/t_r(IO)out$	Output high to low level fall time and output low to high level rise time	$C_L = 30 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	ns
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	6	
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	7	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	2.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	3.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	4	
-	tEXTIpw	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx\_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in [Figure 36](#).
4. For maximum frequencies above 50 MHz and  $V_{DD} > 2.4 \text{ V}$ , the compensation cell should be used.

Figure 36. I/O AC characteristics definition



### 6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor,  $R_{PU}$  (see [Table 56: I/O static characteristics](#)).

Unless otherwise specified, the parameters given in [Table 59](#) are derived from tests performed under the ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#).

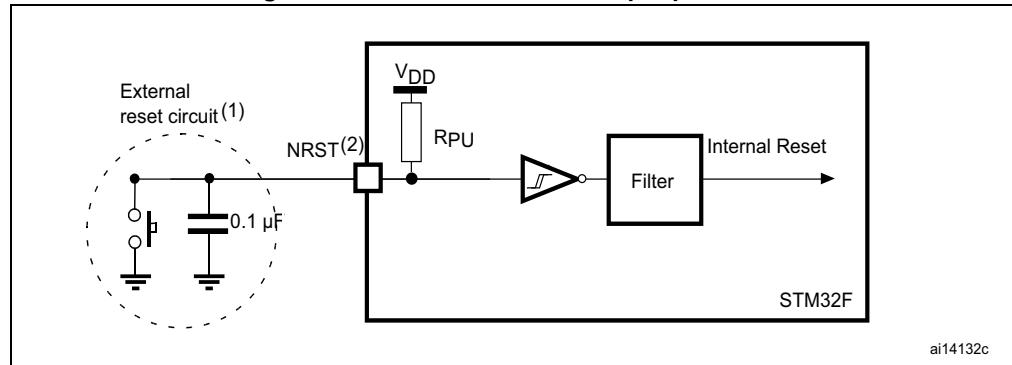
**Table 59. NRST pin characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{PU}$	Weak pull-up equivalent resistor <sup>(1)</sup>	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}^{(2)}$	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}^{(2)}$	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
$T_{NRST\_OUT}$	Generated reset pulse duration	Internal Reset source	20	-	-	μs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

2. Guaranteed by design.

**Figure 37. Recommended NRST pin protection**



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 59](#). Otherwise the reset is not taken into account by the device.

### 6.3.19 TIM timer characteristics

The parameters given in [Table 60](#) are guaranteed by design.

Refer to [Section 6.3.17: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 60. TIMx characteristics<sup>(1)(2)</sup>**

Symbol	Parameter	Conditions <sup>(3)</sup>	Min	Max	Unit
$t_{\text{res(TIM)}}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{\text{TIMxCLK}} = 180 \text{ MHz}$	1	-	$t_{\text{TIMxCLK}}$
		AHB/APBx prescaler>4, $f_{\text{TIMxCLK}} = 90 \text{ MHz}$	1	-	$t_{\text{TIMxCLK}}$
$f_{\text{EXT}}$	Timer external clock frequency on CH1 to CH4	$f_{\text{TIMxCLK}} = 180 \text{ MHz}$	0	$f_{\text{TIMxCLK}}/2$	MHz
			-	16/32	bit
$t_{\text{MAX\_COUNT}}$	Maximum possible count with 32-bit counter		-	$65536 \times 65536$	$t_{\text{TIMxCLK}}$

1. TIMx is used as a general term to refer to the TIM1 to TIM12 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 180 MHz, by setting the TIMPRE bit in the RCC\_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK = 4x PCLKx.

### 6.3.20 Communications interfaces

#### I<sup>2</sup>C interface characteristics

The I<sup>2</sup>C interface meets the timings requirements of the I<sup>2</sup>C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.

The I<sup>2</sup>C timings requirements are guaranteed by design when the I<sup>2</sup>C peripheral is properly configured (refer to RM0090 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V<sub>DD</sub> is disabled, but is still present. Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the I<sup>2</sup>C I/O characteristics.

All I<sup>2</sup>C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

**Table 61. I2C analog filter characteristics<sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
t <sub>AF</sub>	Maximum pulse width of spikes that are suppressed by the analog filter	50 <sup>(2)</sup>	260 <sup>(3)</sup>	ns

1. Guaranteed by design.
2. Spikes with widths below t<sub>AF(min)</sub> are filtered.
3. Spikes with widths above t<sub>AF(max)</sub> are not filtered

### SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 62](#) for the SPI interface are derived from tests performed under the ambient temperature, f<sub>PCLKx</sub> frequency and V<sub>DD</sub> supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5V<sub>DD</sub>

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 62. SPI dynamic characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>SCK</sub> 1/t <sub>c(SCK)</sub>	SPI clock frequency	Master mode, SPI1/4/5/6, 2.7 V≤V <sub>DD</sub> ≤3.6 V	-	-	45	MHz
		Slave mode, SPI1/4/5/6, 2.7 V≤V <sub>DD</sub> ≤3.6 V			45	
		Transmitter/ full-duplex			38 <sup>(2)</sup>	
		Master mode, SPI1/2/3/4/5/6, 1.7 V≤V <sub>DD</sub> ≤3.6 V	-	-	22.5	
		Slave mode, SPI1/2/3/4/5/6, 1.7 V≤V <sub>DD</sub> ≤3.6 V			22.5	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%

Table 62. SPI dynamic characteristics<sup>(1)</sup> (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCKH)}$	SCK high and low time	Master mode, SPI presc = 2, 2.7 V ≤ $V_{DD}$ ≤ 3.6 V	$T_{PCLK} - 0.5$	$T_{PCLK}$	$T_{PCLK} + 0.5$	ns
$t_{w(SCKL)}$		Master mode, SPI presc = 2, 1.7 V ≤ $V_{DD}$ ≤ 3.6 V	$T_{PCLK} - 2$	$T_{PCLK}$	$T_{PCLK} + 2$	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4T_{PCLK}$	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$			
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	ns
$t_{su(SI)}$		Slave mode	0	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	0.5	-	-	
$t_{h(SI)}$		Slave mode	2	-	-	
$t_a(SO)$	Data output access time	Slave mode, SPI presc = 2	0	-	$4T_{PCLK}$	
$t_{dis(SO)}$	Data output disable time	Slave mode, SPI1/4/5/6, 2.7 V ≤ $V_{DD}$ ≤ 3.6 V	0	-	8.5	ns
		Slave mode, SPI1/2/3/4/5/6 and 1.7 V ≤ $V_{DD}$ ≤ 3.6 V	0	-	16.5	
$t_v(SO)$ $t_h(SO)$	Data output valid/hold time	Slave mode (after enable edge), SPI1/4/5/6 and 2.7 V ≤ $V_{DD}$ ≤ 3.6 V	-	11	13	ns
		Slave mode (after enable edge), SPI2/3, 2.7 V ≤ $V_{DD}$ ≤ 3.6 V	-	14	15	
		Slave mode (after enable edge), SPI1/4/5/6, 1.7 V ≤ $V_{DD}$ ≤ 3.6 V	-	15.5	19	
		Slave mode (after enable edge), SPI2/3, 1.7 V ≤ $V_{DD}$ ≤ 3.6 V	-	15.5	17.5	
$t_v(MO)$	Data output valid time	Master mode (after enable edge), SPI1/4/5/6, 2.7 V ≤ $V_{DD}$ ≤ 3.6 V	-	-	2.5	ns
		Master mode (after enable edge), SPI1/2/3/4/5/6, 1.7 V ≤ $V_{DD}$ ≤ 3.6 V	-	-	4.5	
$t_h(MO)$	Data output hold time	Master mode (after enable edge)	0	-	-	

1. Guaranteed by characterization results.

2. Maximum frequency in Slave transmitter mode is determined by the sum of  $t_{v(SO)}$  and  $t_{su(MI)}$  which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having  $t_{su(MI)} = 0$  while Duty(SCK) = 50%

Figure 38. SPI timing diagram - slave mode and CPHA = 0

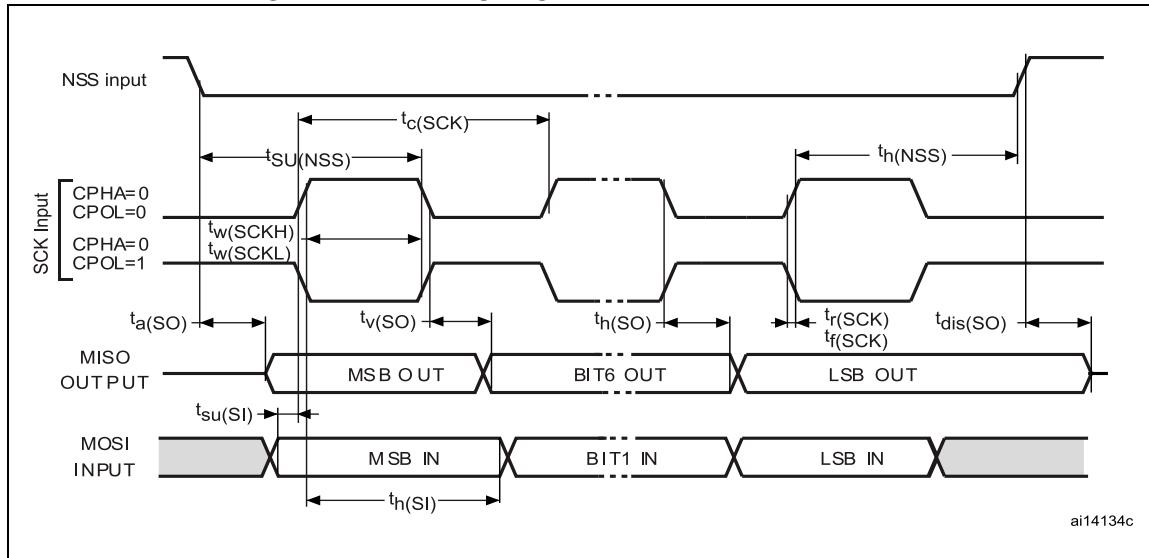


Figure 39. SPI timing diagram - slave mode and CPHA = 1

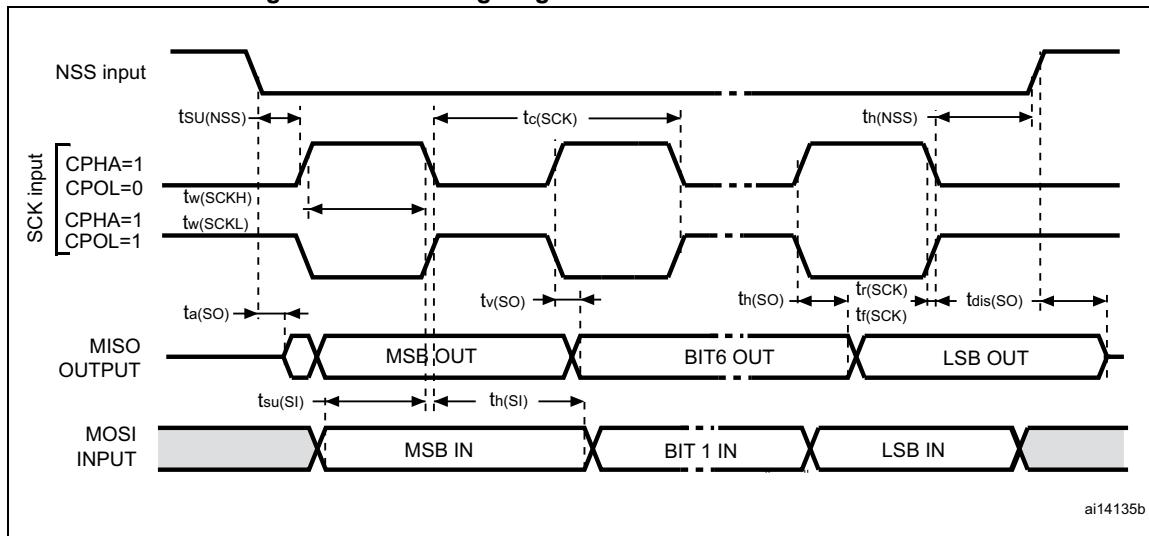
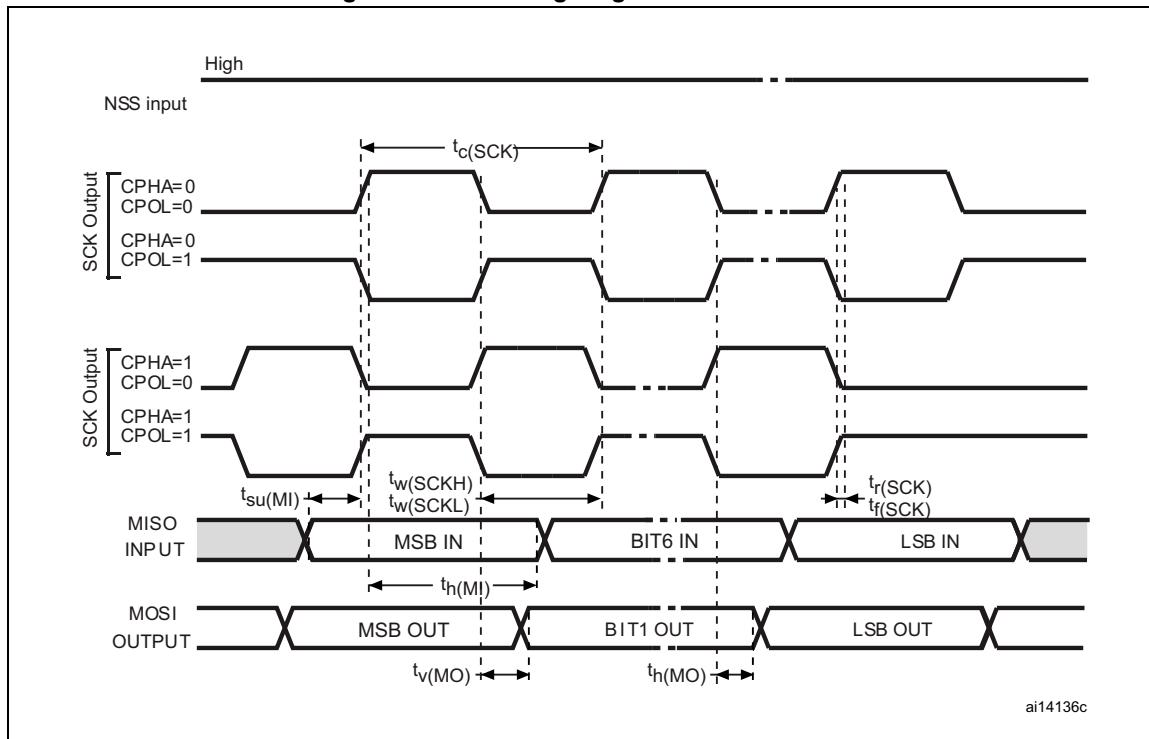


Figure 40. SPI timing diagram - master mode



## I<sup>2</sup>S interface characteristics

Unless otherwise specified, the parameters given in [Table 63](#) for the I<sup>2</sup>S interface are derived from tests performed under the ambient temperature, f<sub>PCLKx</sub> frequency and V<sub>DD</sub> supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5V<sub>DD</sub>

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CK, SD, WS).

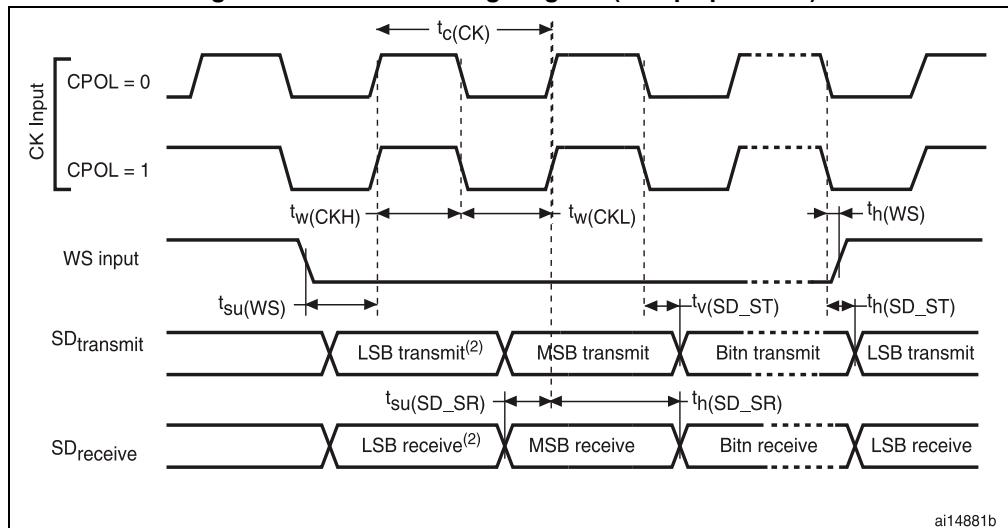
**Table 63. I<sup>2</sup>S dynamic characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
f <sub>MCK</sub>	I <sup>2</sup> S Main clock output	-	256x8K	256xFs <sup>(2)</sup>	MHz
f <sub>CK</sub>	I <sup>2</sup> S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D <sub>CK</sub>	I <sup>2</sup> S clock frequency duty cycle	Slave receiver	30	70	%
t <sub>v(WS)</sub>	WS valid time	Master mode	0	6	ns
t <sub>h(WS)</sub>	WS hold time	Master mode	0	-	
t <sub>su(WS)</sub>	WS setup time	Slave mode	1	-	
t <sub>h(WS)</sub>	WS hold time	Slave mode	0	-	
t <sub>su(SD_MR)</sub>	Data input setup time	Master receiver	7.5	-	
		Slave receiver	2	-	
t <sub>h(SD_MR)</sub>	Data input hold time	Master receiver	0	-	
		Slave receiver	0	-	
t <sub>v(SD_ST)</sub> t <sub>h(SD_ST)</sub>	Data output valid time	Slave transmitter (after enable edge)	-	27	
		Master transmitter (after enable edge)	-	20	
t <sub>h(SD_MT)</sub>	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Guaranteed by characterization results.
2. The maximum value of 256xFs is 45 MHz (APB1 maximum frequency).

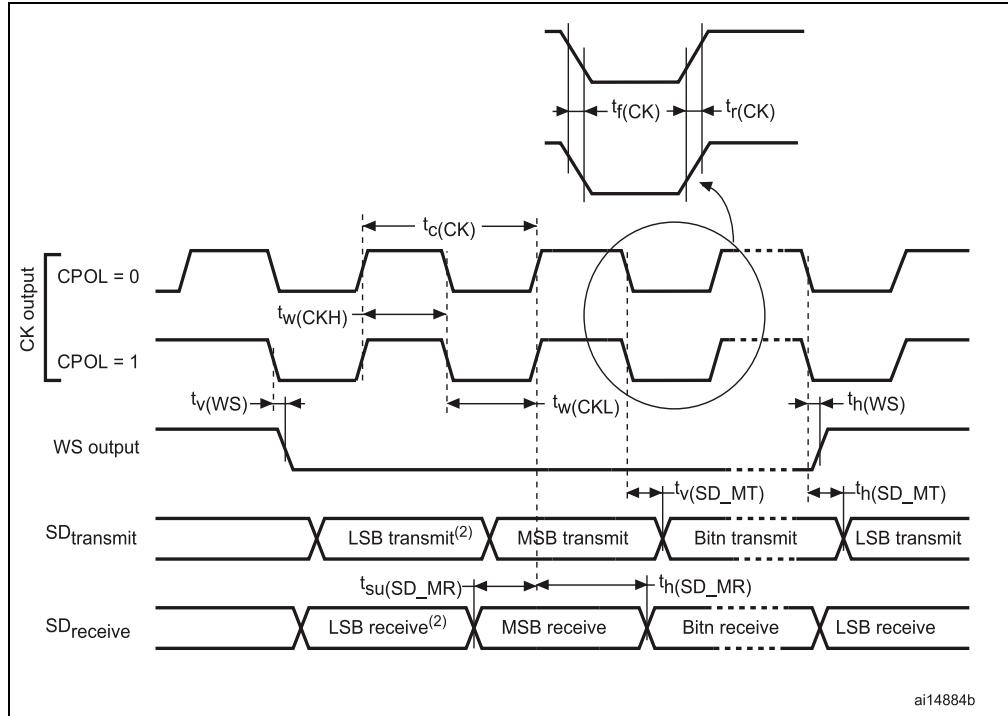
**Note:** Refer to the I<sup>2</sup>S section of RM0090 reference manual for more details on the sampling frequency (F<sub>S</sub>).

f<sub>MCK</sub>, f<sub>CK</sub>, and D<sub>CK</sub> values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D<sub>CK</sub> depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2\*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2\*I2SDIV+ODD). F<sub>S</sub> maximum value is supported for each mode/condition.

Figure 41. I<sup>2</sup>S slave timing diagram (Philips protocol)<sup>(1)</sup>

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1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 42. I<sup>2</sup>S master timing diagram (Philips protocol)<sup>(1)</sup>

ai14884b

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### SAI characteristics

Unless otherwise specified, the parameters given in [Table 64](#) for SAI are derived from tests performed under the ambient temperature,  $f_{PCLKx}$  frequency and VDD supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: 0.5V<sub>DD</sub>

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SCK,SD,WS).

**Table 64. SAI characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{MCKL}$	SAI Main clock output	-	256 x 8K	256xFs <sup>(2)</sup>	MHz
$F_{SCK}$	SAI clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
$D_{SCK}$	SAI clock frequency duty cycle	Slave receiver	30	70	%
$t_{V(FS)}$	FS valid time	Master mode	8	22	ns
$t_{su(FS)}$	FS setup time	Slave mode	2	-	
$t_{h(FS)}$	FS hold time	Master mode	8	-	
		Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	5	-	
$t_{su(SD\_SR)}$		Slave receiver	3	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	22	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	8	-	

1. Guaranteed by characterization results.

2. 256xFs maximum corresponds to 45 MHz (APB2 xmaximum frequency)

Figure 43. SAI master timing waveforms

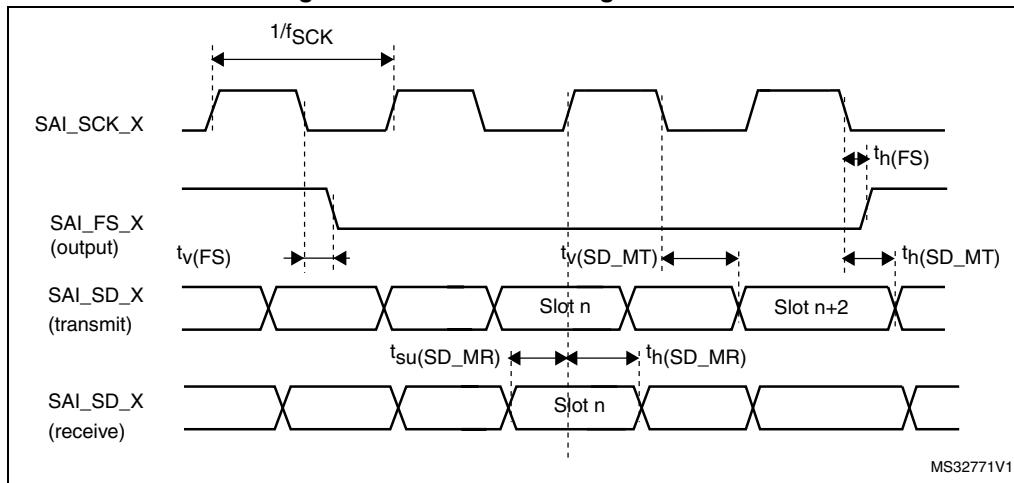
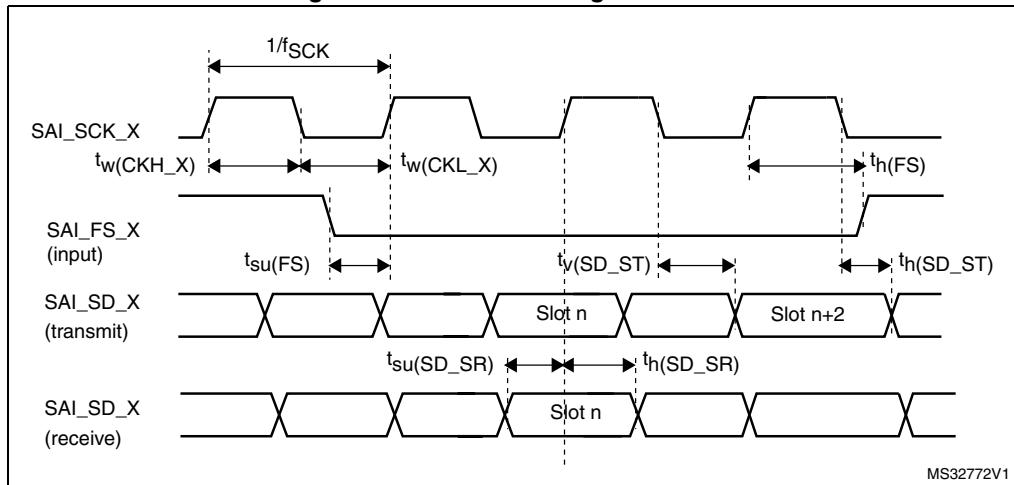


Figure 44. SAI slave timing waveforms



### USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

**Table 65. USB OTG full speed startup time**

Symbol	Parameter	Max	Unit
$t_{STARTUP}^{(1)}$	USB OTG full speed transceiver startup time	1	$\mu s$

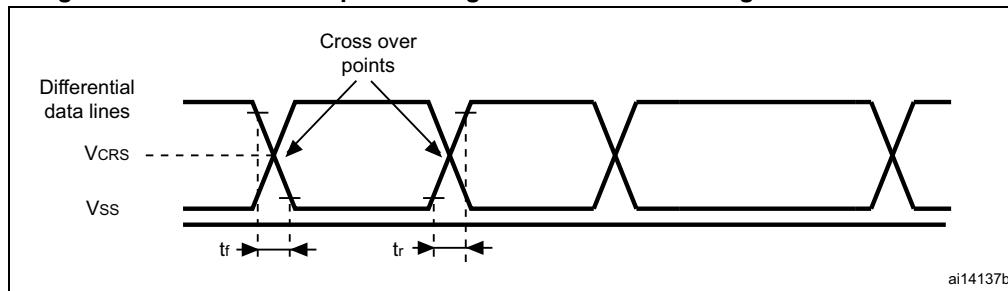
1. Guaranteed by design.

**Table 66. USB OTG full speed DC electrical characteristics**

Symbol	Parameter	Conditions	Min. <sup>(1)</sup>	Typ.	Max. <sup>(1)</sup>	Unit
<b>Input levels</b>	$V_{DD}$	USB OTG full speed transceiver operating voltage	3.0 <sup>(2)</sup>	-	3.6	V
	$V_{DI}^{(3)}$	Differential input sensitivity		0.2	-	-
	$V_{CM}^{(3)}$	Differential common mode range		0.8	-	2.5
	$V_{SE}^{(3)}$	Single ended receiver threshold		1.3	-	2.0
<b>Output levels</b>	$V_{OL}$	Static output level low	$R_L$ of 1.5 k $\Omega$ to 3.6 V <sup>(4)</sup>	-	-	0.3
	$V_{OH}$	Static output level high		2.8	-	3.6
$R_{PD}$	PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	k $\Omega$
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
$R_{PU}$	PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
	PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

- All the voltages are measured from the local ground potential.
- The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V  $V_{DD}$  voltage range.
- Guaranteed by design.
- $R_L$  is the load connected on the USB OTG full speed drivers.

**Note:** When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200  $\mu A$  current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.

**Figure 45. USB OTG full speed timings: definition of data signal rise and fall time****Table 67. USB OTG full speed electrical characteristics<sup>(1)</sup>**

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
$t_r$	Rise time <sup>(2)</sup>	$C_L = 50 \text{ pF}$	4	20	ns
$t_f$	Fall time <sup>(2)</sup>	$C_L = 50 \text{ pF}$	4	20	ns
$t_{rfm}$	Rise/ fall time matching	$t_r/t_f$	90	110	%
$V_{CRS}$	Output signal crossover voltage		1.3	2.0	V
$Z_{DRV}$	Output driver impedance <sup>(3)</sup>	Driving high or low	28	44	$\Omega$

1. Guaranteed by design.

2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

### USB high speed (HS) characteristics

Unless otherwise specified, the parameters given in [Table 70](#) for ULPI are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency summarized in [Table 69](#) and  $V_{DD}$  supply voltage conditions summarized in [Table 68](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10, unless otherwise specified
- Capacitive load  $C = 30 \text{ pF}$ , unless otherwise specified
- Measurement points are done at CMOS levels:  $0.5V_{DD}$ .

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

**Table 68. USB HS DC electrical characteristics**

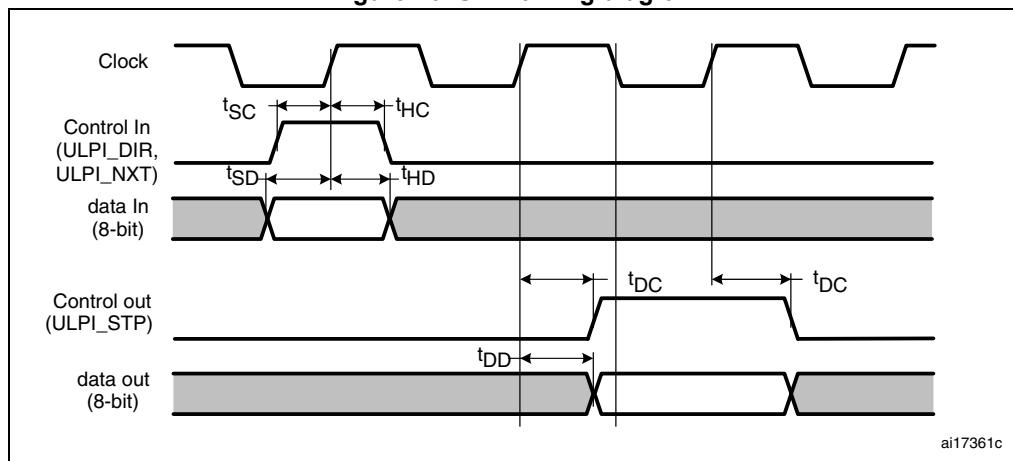
Symbol	Parameter	Min. <sup>(1)</sup>	Max. <sup>(1)</sup>	Unit
Input level	$V_{DD}$	USB OTG HS operating voltage	1.7	3.6

1. All the voltages are measured from the local ground potential.

**Table 69. USB HS clock timing parameters<sup>(1)</sup>**

Symbol	Parameter		Min	Typ	Max	Unit
	$f_{HCLK}$ value to guarantee proper operation of USB HS interface		30	-	-	MHz
$F_{START\_8BIT}$	Frequency (first transition)	8-bit ±10%	54	60	66	MHz
$F_{STEADY}$	Frequency (steady state) ±500 ppm		59.97	60	60.03	MHz
$D_{START\_8BIT}$	Duty cycle (first transition)	8-bit ±10%	40	50	60	%
$D_{STEADY}$	Duty cycle (steady state) ±500 ppm		49.975	50	50.025	%
$t_{STEADY}$	Time to reach the steady state frequency and duty cycle after the first transition		-	-	1.4	ms
$t_{START\_DEV}$	Clock startup time after the de-assertion of SuspendM	Peripheral	-	-	5.6	ms
$t_{START\_HOST}$		Host	-	-	-	
$t_{PREP}$	PHY preparation time after the first transition of the input clock		-	-	-	μs

1. Guaranteed by design.

**Figure 46. ULPI timing diagram**

**Table 70. Dynamic characteristics: USB ULPI<sup>(1)</sup>**

<b>Symbol</b>	<b>Parameter</b>	<b>Conditions</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>	
$t_{SC}$	Control in (ULPI_DIR, ULPI_NXT) setup time		2	-	-		
$t_{HC}$	Control in (ULPI_DIR, ULPI_NXT) hold time		0.5	-	-		
$t_{SD}$	Data in setup time		1.5	-	-		
$t_{HD}$	Data in hold time		2	-	-		
$t_{DC}/t_{DD}$	Data/control output delay	2.7 V < $V_{DD}$ < 3.6 V, $C_L = 15 \text{ pF}$ and OSPEEDRy[1:0] = 11	-	9	9.5	ns	
		2.7 V < $V_{DD}$ < 3.6 V, $C_L = 20 \text{ pF}$ and OSPEEDRy[1:0] = 10	-	12	15		
		1.7 V < $V_{DD}$ < 3.6 V, $C_L = 15 \text{ pF}$ and OSPEEDRy[1:0] = 11	-				

1. Guaranteed by characterization results.

### Ethernet characteristics

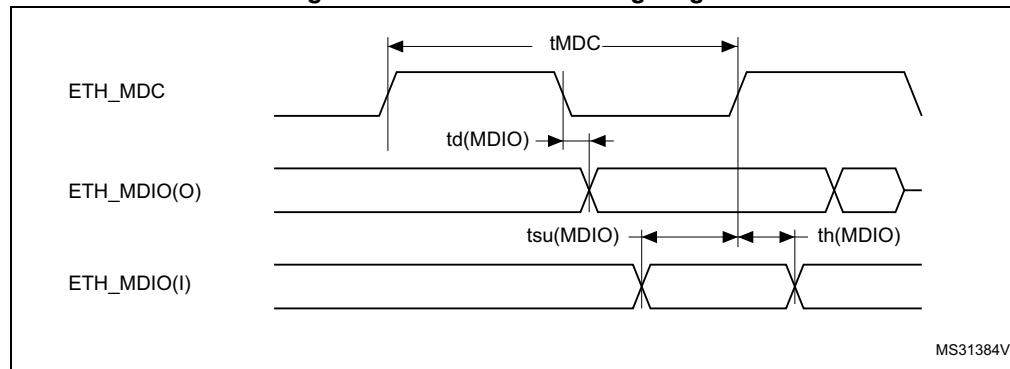
Unless otherwise specified, the parameters given in [Table 71](#), [Table 72](#) and [Table 73](#) for SMI, RMII and MII are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency summarized in [Table 17](#) with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF for  $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$
- Capacitive load C = 20 pF for  $1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$
- Measurement points are done at CMOS levels:  $0.5V_{DD}$ .

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

[Table 71](#) gives the list of Ethernet MAC signals for the SMI (station management interface) and [Figure 47](#) shows the corresponding timing diagram.

**Figure 47. Ethernet SMI timing diagram**



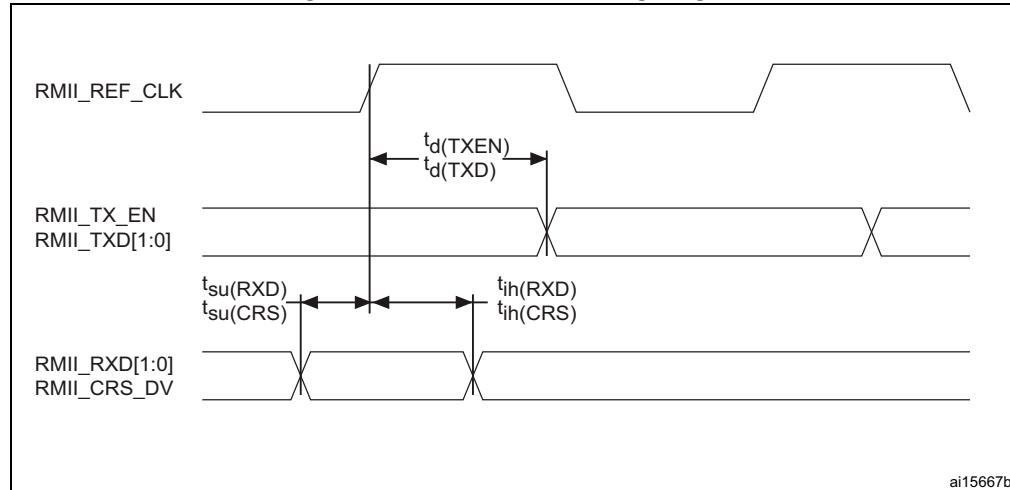
**Table 71. Dynamics characteristics: Ethernet MAC signals for SMI<sup>(1)</sup>**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{MDC}$	MDC cycle time(2.38 MHz)	411	420	425	ns
$T_d(\text{MDIO})$	Write data valid time	6	10	13	
$t_{su}(\text{MDIO})$	Read data setup time	12	-	-	
$t_h(\text{MDIO})$	Read data hold time	0	-	-	

1. Guaranteed by characterization results.

*Table 72* gives the list of Ethernet MAC signals for the RMII and *Figure 48* shows the corresponding timing diagram.

**Figure 48. Ethernet RMII timing diagram**



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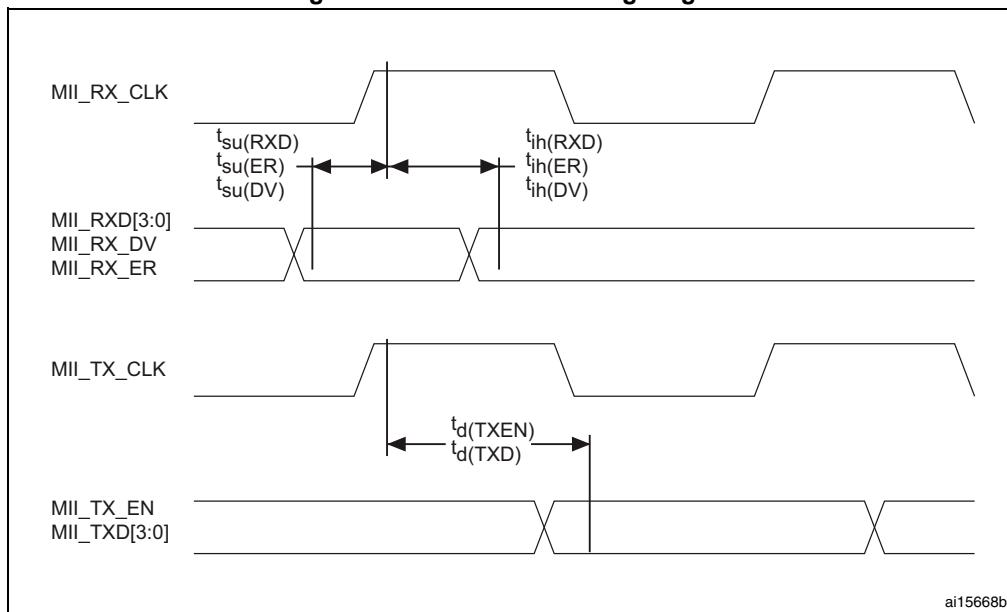
**Table 72. Dynamics characteristics: Ethernet MAC signals for RMII<sup>(1)</sup>**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{su}(RXD)$	Receive data setup time	$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$	1.5	-	-	ns
$t_{ih}(RXD)$	Receive data hold time		0	-	-	
$t_{su}(CRS)$	Carrier sense setup time		1	-	-	
$t_{ih}(CRS)$	Carrier sense hold time		1	-	-	
$t_d(TXEN)$	Transmit enable valid delay time	$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	8	10.5	12	ns
		$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$	8	10.5	14	
$t_d(TXD)$	Transmit data valid delay time	$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	8	11	12.5	
		$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$	8	11	14.5	

1. Guaranteed by characterization results.

*Table 73* gives the list of Ethernet MAC signals for MII and *Figure 48* shows the corresponding timing diagram.

Figure 49. Ethernet MII timing diagram



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Table 73. Dynamics characteristics: Ethernet MAC signals for MII<sup>(1)</sup>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{su}(RXD)$	Receive data setup time	$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$	9	-	-	ns
$t_{ih}(RXD)$	Receive data hold time		10	-	-	
$t_{su}(DV)$	Data valid setup time		9	-	-	
$t_{ih}(DV)$	Data valid hold time		8	-	-	
$t_{su}(ER)$	Error setup time		6	-	-	
$t_{ih}(ER)$	Error hold time		8	-	-	
$t_d(TXEN)$	Transmit enable valid delay time	$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	8	10	14	ns
		$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$	8	10	16	
$t_d(TXD)$	Transmit data valid delay time	$2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$	7.5	10	15	
		$1.71 \text{ V} < V_{DD} < 3.6 \text{ V}$	7.5	10	17	

1. Guaranteed by characterization results.

### CAN (controller area network) interface

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANx\_TX and CANx\_RX).

### 6.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 74](#) are derived from tests performed under the ambient temperature,  $f_{PCLK2}$  frequency and  $V_{DDA}$  supply voltage conditions summarized in [Table 17](#).

**Table 74. ADC characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA}$	Power supply	$V_{DDA} - V_{REF+} < 1.2 \text{ V}$	1.7 <sup>(1)</sup>	-	3.6	V
$V_{REF+}$	Positive reference voltage		1.7 <sup>(1)</sup>	-	$V_{DDA}$	
$V_{REF-}$	Negative reference voltage	-	-	0	-	
$f_{ADC}$	ADC clock frequency	$V_{DDA} = 1.7^{(1)} \text{ to } 2.4 \text{ V}$	0.6	15	18	MHz
		$V_{DDA} = 2.4 \text{ to } 3.6 \text{ V}$	0.6	30	36	MHz
$f_{TRIG}^{(2)}$	External trigger frequency	$f_{ADC} = 30 \text{ MHz}$ , 12-bit resolution	-	-	1764	kHz
			-	-	17	$1/f_{ADC}$
$V_{AIN}$	Conversion voltage range <sup>(3)</sup>		0 ( $V_{SSA}$ or $V_{REF-}$ tied to ground)	-	$V_{REF+}$	V
$R_{AIN}^{(2)}$	External input impedance	See <a href="#">Equation 1</a> for details	-	-	50	kΩ
$R_{ADC}^{(2)(4)}$	Sampling switch resistance		1.5	-	6	kΩ
$C_{ADC}^{(2)}$	Internal sample and hold capacitor		-	4	7	pF
$t_{lat}^{(2)}$	Injection trigger conversion latency	$f_{ADC} = 30 \text{ MHz}$	-	-	0.100	μs
			-	-	3 <sup>(5)</sup>	$1/f_{ADC}$
$t_{latr}^{(2)}$	Regular trigger conversion latency	$f_{ADC} = 30 \text{ MHz}$	-	-	0.067	μs
			-	-	2 <sup>(5)</sup>	$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	$f_{ADC} = 30 \text{ MHz}$	0.100	-	16	μs
			3	-	480	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time		-	2	3	μs
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	$f_{ADC} = 30 \text{ MHz}$ 12-bit resolution	0.50	-	16.40	μs
		$f_{ADC} = 30 \text{ MHz}$ 10-bit resolution	0.43	-	16.34	μs
		$f_{ADC} = 30 \text{ MHz}$ 8-bit resolution	0.37	-	16.27	μs
		$f_{ADC} = 30 \text{ MHz}$ 6-bit resolution	0.30	-	16.20	μs
		9 to 492 ( $t_S$ for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 74. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_S^{(2)}$	Sampling rate ( $f_{ADC} = 30$ MHz, and $t_S = 3$ ADC cycles)	12-bit resolution Single ADC	-	-	2	MspS
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	MspS
		12-bit resolution Interleave Triple ADC mode	-	-	6	MspS
$I_{VREF+}^{(2)}$	ADC $V_{REF}$ DC current consumption in conversion mode		-	300	500	$\mu$ A
$I_{VDDA}^{(2)}$	ADC $V_{DDA}$ DC current consumption in conversion mode		-	1.6	1.8	mA

1.  $V_{DDA}$  minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).
2. Guaranteed by characterization results.
3.  $V_{REF+}$  is internally connected to  $V_{DDA}$  and  $V_{REF-}$  is internally connected to  $V_{SSA}$ .
4.  $R_{ADC}$  maximum value is given for  $V_{DD}=1.7$  V, and minimum value for  $V_{DD}=3.3$  V.
5. For external triggers, a delay of  $1/f_{PCLK2}$  must be added to the latency specified in [Table 74](#).

Equation 1:  $R_{AIN}$  max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB.  $N = 12$  (from 12-bit resolution) and  $k$  is the number of sampling periods defined in the ADC\_SMPR1 register.

Table 75. ADC static accuracy at  $f_{ADC} = 18$  MHz

Symbol	Parameter	Test conditions	Typ	Max <sup>(1)</sup>	Unit
ET	Total unadjusted error	$f_{ADC} = 18$ MHz $V_{DDA} = 1.7$ to $3.6$ V $V_{REF} = 1.7$ to $3.6$ V $V_{DDA} - V_{REF} < 1.2$ V	$\pm 3$	$\pm 4$	LSB
EO	Offset error		$\pm 2$	$\pm 3$	
EG	Gain error		$\pm 1$	$\pm 3$	
ED	Differential linearity error		$\pm 1$	$\pm 2$	
EL	Integral linearity error		$\pm 2$	$\pm 3$	

1. Guaranteed by characterization results.

**Table 76. ADC static accuracy at  $f_{ADC} = 30$  MHz**

Symbol	Parameter	Test conditions	Typ	Max <sup>(1)</sup>	Unit
ET	Total unadjusted error	$f_{ADC} = 30$ MHz, $R_{AIN} < 10$ k $\Omega$ , $V_{DDA} = 2.4$ to $3.6$ V, $V_{REF} = 1.7$ to $3.6$ V, $V_{DDA} - V_{REF} < 1.2$ V	$\pm 2$	$\pm 5$	LSB
EO	Offset error		$\pm 1.5$	$\pm 2.5$	
EG	Gain error		$\pm 1.5$	$\pm 3$	
ED	Differential linearity error		$\pm 1$	$\pm 2$	
EL	Integral linearity error		$\pm 1.5$	$\pm 3$	

1. Guaranteed by characterization results.

**Table 77. ADC static accuracy at  $f_{ADC} = 36$  MHz**

Symbol	Parameter	Test conditions	Typ	Max <sup>(1)</sup>	Unit
ET	Total unadjusted error	$f_{ADC} = 36$ MHz, $V_{DDA} = 2.4$ to $3.6$ V, $V_{REF} = 1.7$ to $3.6$ V $V_{DDA} - V_{REF} < 1.2$ V	$\pm 4$	$\pm 7$	LSB
EO	Offset error		$\pm 2$	$\pm 3$	
EG	Gain error		$\pm 3$	$\pm 6$	
ED	Differential linearity error		$\pm 2$	$\pm 3$	
EL	Integral linearity error		$\pm 3$	$\pm 6$	

1. Guaranteed by characterization results.

**Table 78. ADC dynamic accuracy at  $f_{ADC} = 18$  MHz - limited test conditions<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{ADC} = 18$ MHz $V_{DDA} = V_{REF+} = 1.7$ V Input Frequency = 20 KHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-67	-72	-	

1. Guaranteed by characterization results.

**Table 79. ADC dynamic accuracy at  $f_{ADC} = 36$  MHz - limited test conditions<sup>(1)</sup>**

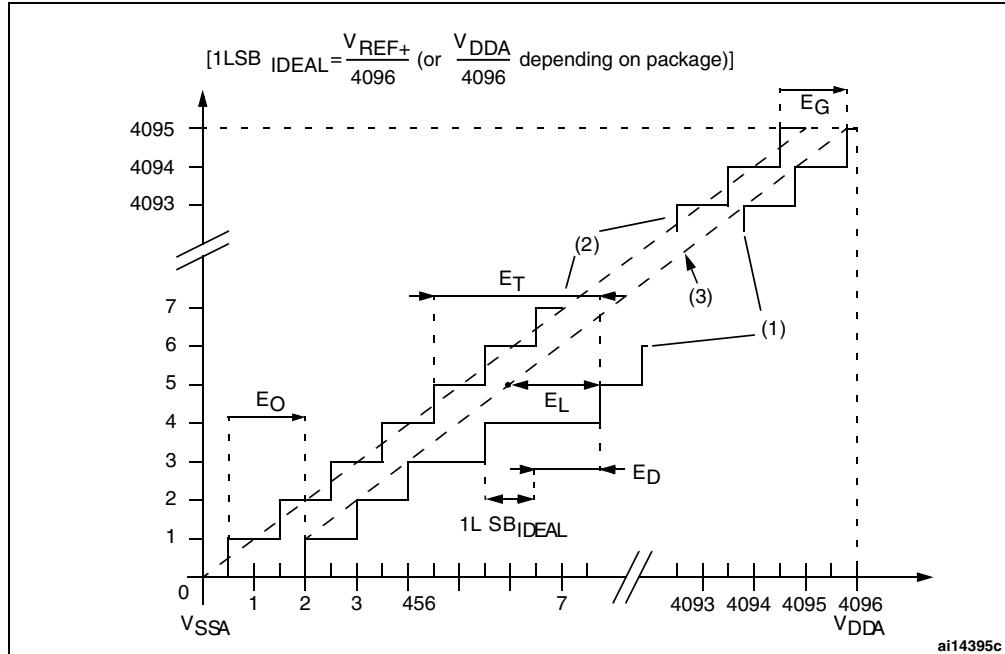
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{ADC} = 36$ MHz $V_{DDA} = V_{REF+} = 3.3$ V Input Frequency = 20 KHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-70	-72	-	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

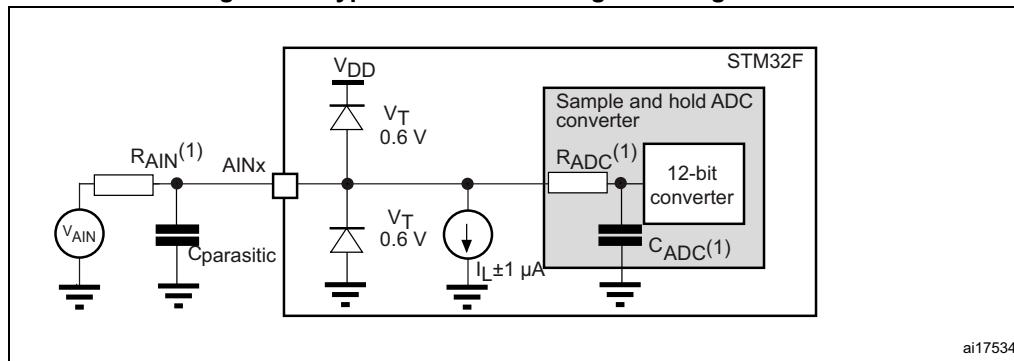
Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in [Section 6.3.17](#) does not affect the ADC accuracy.

**Figure 50. ADC accuracy characteristics**



1. See also [Table 76](#).
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5.  $E_T$  = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.  
 $E_O$  = Offset Error: deviation between the first actual transition and the first ideal one.  
 $E_G$  = Gain Error: deviation between the last ideal transition and the last actual one.  
 $ED$  = Differential Linearity Error: maximum deviation between actual steps and the ideal one.  
 $EL$  = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 51. Typical connection diagram using the ADC



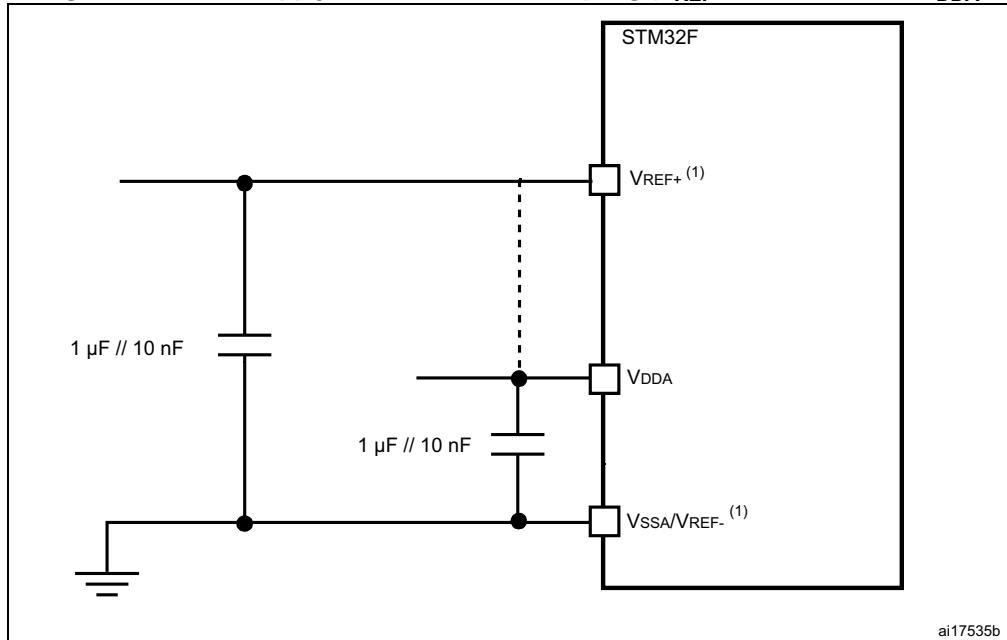
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1. Refer to [Table 74](#) for the values of  $R_{AIN}$ ,  $R_{ADC}$  and  $C_{ADC}$ .
2.  $C_{parasitic}$  represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high  $C_{parasitic}$  value downgrades conversion accuracy. To remedy this,  $f_{ADC}$  should be reduced.

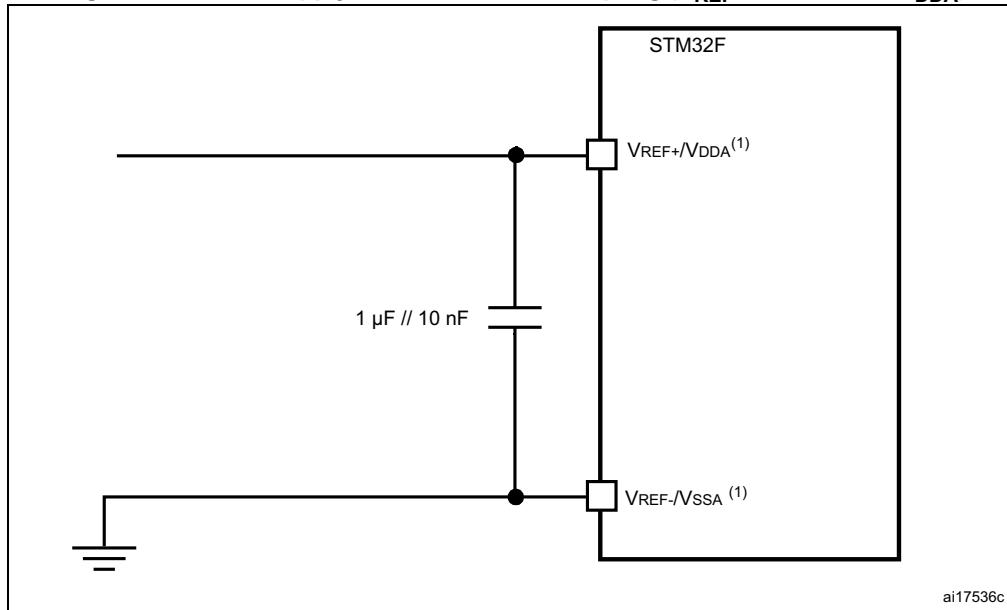
### General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 52](#) or [Figure 53](#), depending on whether  $V_{REF+}$  is connected to  $V_{DDA}$  or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 52. Power supply and reference decoupling ( $V_{REF+}$  not connected to  $V_{DDA}$ )**



1.  $V_{REF+}$  and  $V_{REF-}$  inputs are both available on UFBGA176.  $V_{REF+}$  is also available on LQFP100, LQFP144, and LQFP176. When  $V_{REF+}$  and  $V_{REF-}$  are not available, they are internally connected to  $V_{DDA}$  and  $V_{SSA}$ .

**Figure 53. Power supply and reference decoupling ( $V_{REF+}$  connected to  $V_{DDA}$ )**

1.  $V_{REF+}$  and  $V_{REF-}$  inputs are both available on UFBGA176.  $V_{REF+}$  is also available on LQFP100, LQFP144, and LQFP176. When  $V_{REF+}$  and  $V_{REF-}$  are not available, they are internally connected to  $V_{DDA}$  and  $V_{SSA}$ .

### 6.3.22 Temperature sensor characteristics

**Table 80. Temperature sensor characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	$V_{SENSE}$ linearity with temperature	-	$\pm 1$	$\pm 2$	°C
Avg_Slope <sup>(1)</sup>	Average slope	-	2.5		mV/°C
$V_{25}^{(1)}$	Voltage at 25 °C	-	0.76		V
$t_{START}^{(2)}$	Startup time	-	6	10	μs
$T_{S\_temp}^{(2)}$	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	μs

1. Guaranteed by characterization results.

2. Guaranteed by design.

**Table 81. Temperature sensor calibration values**

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3.3$ V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, $V_{DDA} = 3.3$ V	0x1FFF 7A2E - 0x1FFF 7A2F

### 6.3.23 V<sub>BAT</sub> monitoring characteristics

**Table 82. V<sub>BAT</sub> monitoring characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V <sub>BAT</sub>	-	50	-	KΩ
Q	Ratio on V <sub>BAT</sub> measurement	-	4	-	
Er <sup>(1)</sup>	Error on Q	-1	-	+1	%
T <sub>S_vbat</sub> <sup>(2)(2)</sup>	ADC sampling time when reading the V <sub>BAT</sub> 1 mV accuracy	5	-	-	μs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

### 6.3.24 Reference voltage

The parameters given in [Table 83](#) are derived from tests performed under ambient temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 17](#).

**Table 83. internal reference voltage**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>REFINT</sub>	Internal reference voltage	-40 °C < T <sub>A</sub> < +105 °C	1.18	1.21	1.24	V
T <sub>S_vrefint</sub> <sup>(1)</sup>	ADC sampling time when reading the internal reference voltage		10	-	-	μs
V <sub>RERINT_s</sub> <sup>(2)</sup>	Internal reference voltage spread over the temperature range	V <sub>DD</sub> = 3V ± 10mV	-	3	5	mV
T <sub>Coeff</sub> <sup>(2)</sup>	Temperature coefficient		-	30	50	ppm/°C
t <sub>START</sub> <sup>(2)</sup>	Startup time		-	6	10	μs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production

**Table 84. Internal reference voltage calibration values**

Symbol	Parameter	Memory address
V <sub>REFIN_CAL</sub>	Raw data acquired at temperature of 30 °C V <sub>DDA</sub> = 3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

### 6.3.25 DAC electrical characteristics

Table 85. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
$V_{DDA}$	Analog supply voltage	-	1.7 <sup>(1)</sup>	-	3.6	V	-
$V_{REF+}$	Reference supply voltage	-	1.7 <sup>(1)</sup>	-	3.6	V	$V_{REF+} \leq V_{DDA}$
$V_{SSA}$	Ground	-	0	-	0	V	-
$R_{LOAD}^{(2)}$	Resistive load	DAC output buffer ON	$R_{LOAD}$ connected to $V_{SSA}$	5	-	-	k $\Omega$
			$R_{LOAD}$ connected to $V_{DDA}$	25	-	-	
$R_O^{(2)}$	Impedance output with buffer OFF	-	-	-	15	k $\Omega$	When the buffer is OFF, the Minimum resistive load between DAC_OUT and Vss to have a 1% accuracy is 1.5 M $\Omega$
$C_{LOAD}^{(2)}$	Capacitive load	-	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_O_UT_min <sup>(2)</sup>	Lower DAC_OUT voltage with buffer ON	-	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+} = 3.6$ V and (0x1C7) to (0xE38) at $V_{REF+} = 1.7$ V
DAC_O_UT_max <sup>(2)</sup>	Higher DAC_OUT voltage with buffer ON	-	-	-	$V_{DDA} - 0.2$	V	
DAC_O_UT_min <sup>(2)</sup>	Lower DAC_OUT voltage with buffer OFF	-	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_O_UT_max <sup>(2)</sup>	Higher DAC_OUT voltage with buffer OFF	-	-	-	$V_{REF+} - 1\text{LSB}$	V	
$I_{VREF+}^{(4)}$	DAC DC $V_{REF}$ current consumption in quiescent mode (Standby mode)	-	-	170	240	$\mu\text{A}$	With no load, worst code (0x800) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs
		-	-	50	75	$\mu\text{A}$	With no load, worst code (0xF1C) at $V_{REF+} = 3.6$ V in terms of DC consumption on the inputs

Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
$I_{DDA}^{(4)}$	DAC DC VDDA current consumption in quiescent mode <sup>(3)</sup>	-	-	280	380	µA	With no load, middle code (0x800) on the inputs
		-	-	475	625	µA	With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs
DNL <sup>(4)</sup>	Differential non linearity Difference between two consecutive code-1LSB)	-	-	-	$\pm 0.5$	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	$\pm 2$	LSB	Given for the DAC in 12-bit configuration.
INL <sup>(4)</sup>	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	-	$\pm 1$	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	$\pm 4$	LSB	Given for the DAC in 12-bit configuration.
Offset <sup>(4)</sup>	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$ )	-	-	-	$\pm 10$	mV	Given for the DAC in 12-bit configuration
		-	-	-	$\pm 3$	LSB	Given for the DAC in 10-bit at $V_{REF+}$ = 3.6 V
		-	-	-	$\pm 12$	LSB	Given for the DAC in 12-bit at $V_{REF+}$ = 3.6 V
Gain error <sup>(4)</sup>	Gain error	-	-	-	$\pm 0.5$	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}^{(4)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 4$ LSB)	-	-	3	6	µs	$C_{LOAD} \leq 50 \text{ pF}$ , $R_{LOAD} \geq 5 \text{ k}\Omega$
THD <sup>(4)</sup>	Total Harmonic Distortion Buffer ON	-	-	-	-	dB	$C_{LOAD} \leq 50 \text{ pF}$ , $R_{LOAD} \geq 5 \text{ k}\Omega$
Update rate <sup>(2)</sup>	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	-	1	MS/s	$C_{LOAD} \leq 50 \text{ pF}$ , $R_{LOAD} \geq 5 \text{ k}\Omega$

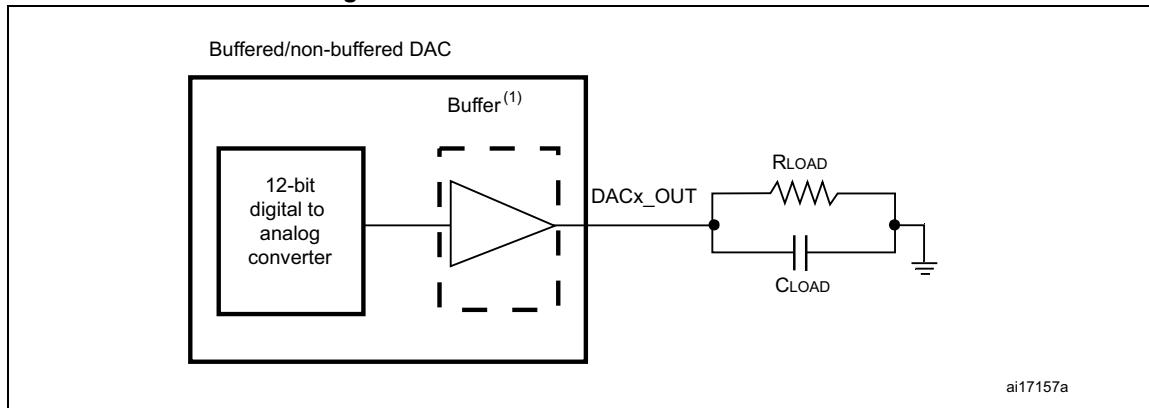
Table 85. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
$t_{WAKEUP}^{(4)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	μs	$C_{LOAD} \leq 50 \text{ pF}$ , $R_{LOAD} \geq 5 \text{ k}\Omega$ input code between lowest and highest possible ones.
PSRR <sub>+</sub> (2)	Power supply rejection ratio (to $V_{DDA}$ ) (static DC measurement)	-	-	-67	-40	dB	No $R_{LOAD}$ , $C_{LOAD} = 50 \text{ pF}$

1.  $V_{DDA}$  minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).

2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization.

Figure 54. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC\_CR register.

### 6.3.26 FMC characteristics

Unless otherwise specified, the parameters given in [Table 86](#) to [Table 101](#) for the FMC interface are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#), with the following configuration:

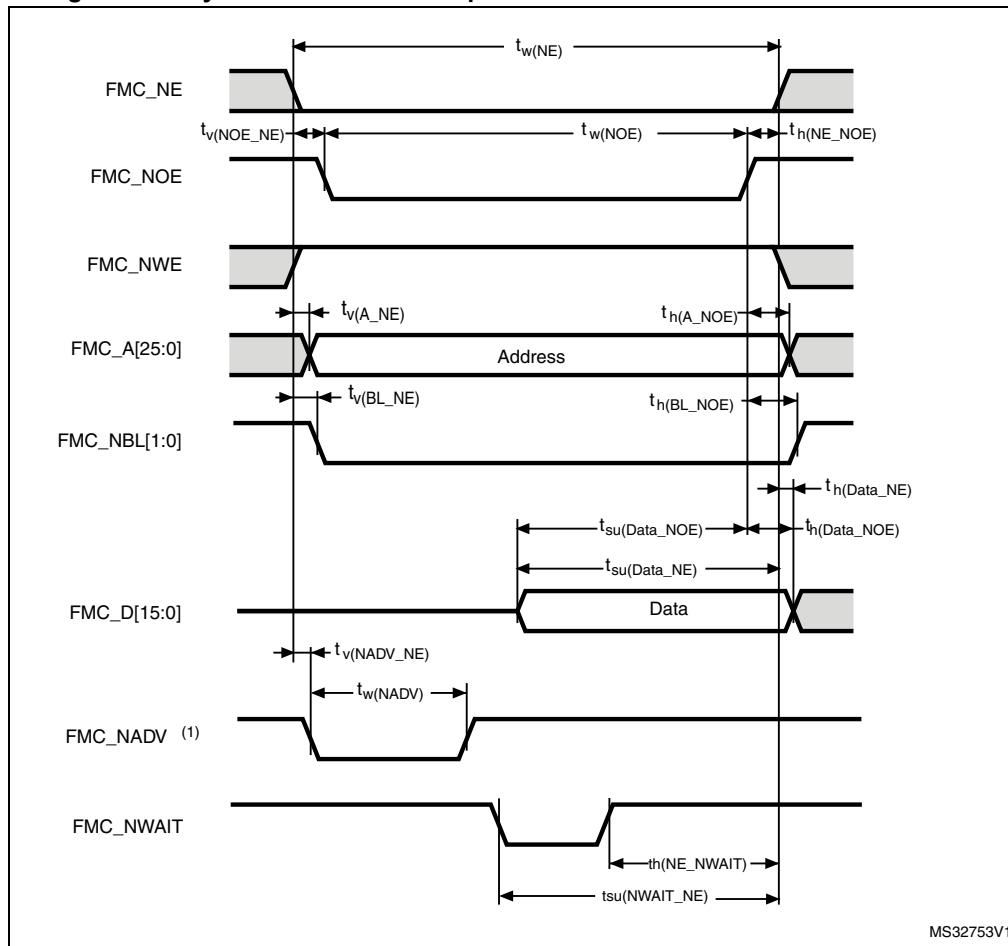
- Output speed is set to OSPEEDRy[1:0] = 10 except at  $V_{DD}$  range 1.7 to 2.1V where OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 $V_{DD}$

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

### Asynchronous waveforms and timings

[Figure 55](#) through [Figure 58](#) represent asynchronous waveforms and [Table 86](#) through [Table 93](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- For SDRAM memories,  $V_{DD}$  ranges from 2.7 to 3.6 V and maximum frequency FMC\_SDCLK = 90 MHz
- For Mobile LPSDR SDRAM memories,  $V_{DD}$  ranges from 1.7 to 1.95 V and maximum frequency FMC\_SDCLK = 84 MHz

**Figure 55. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**

1. Mode 2/B, C and D only. In Mode 1, FMC\_NADV is not used.

**Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK} - 0.5$	$2 T_{HCLK} + 0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	ns
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$	$2T_{HCLK} + 0.5$	ns
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	ns
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 2.5$	-	ns
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	$T_{HCLK} + 2$	-	ns

**Table 86. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings<sup>(1)(2)</sup> (continued)**

Symbol	Parameter	Min	Max	Unit
$t_h(\text{Data\_NOE})$	Data hold time after FMC_NOE high	0	-	ns
$t_h(\text{Data\_NE})$	Data hold time after FMC_NEx high	0	-	ns
$t_v(\text{NADV\_NE})$	FMC_NEx low to FMC_NADV low	-	0	ns
$t_w(\text{NADV})$	FMC_NADV low time	-	$T_{\text{HCLK}} + 1$	ns

1.  $C_L = 30 \text{ pF}$ .

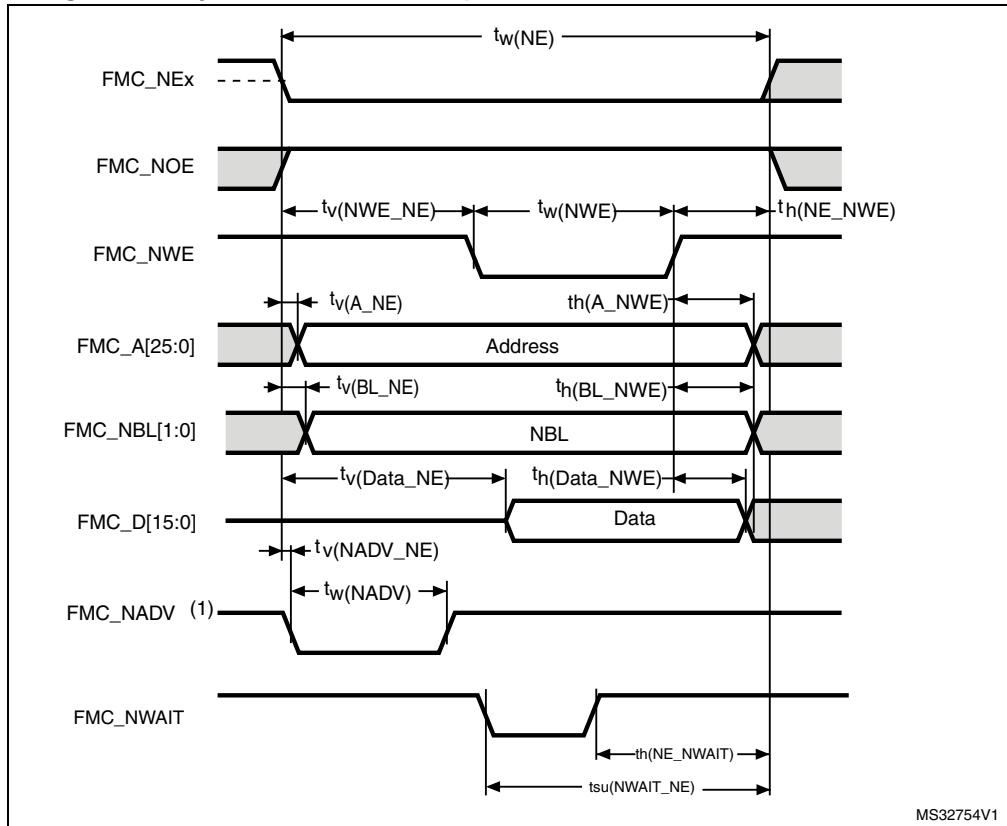
2. Guaranteed by characterization results.

**Table 87. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(\text{NE})$	FMC_NE low time	$7T_{\text{HCLK}} + 0.5$	$7T_{\text{HCLK}} + 1$	ns
$t_w(\text{NOE})$	FMC_NWE low time	$5T_{\text{HCLK}} - 1.5$	$5T_{\text{HCLK}} + 2$	
$t_{su}(\text{NWAIT\_NE})$	FMC_NWAIT valid before FMC_NEx high	$5T_{\text{HCLK}} + 1.5$	-	
$t_h(\text{NE\_NWAIT})$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{\text{HCLK}} + 1$	-	

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

**Figure 56. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**

1. Mode 2/B, C and D only. In Mode 1, FMC\_NADV is not used.

**Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+1$	ns
$t_v(NWE\_NE)$	FMC_NEx low to FMC_NWE low	$T_{HCLK}-0.5$	$T_{HCLK}+0.5$	ns
$t_w(NWE)$	FMC_NWE low time	$T_{HCLK}$	$T_{HCLK}+0.5$	ns
$t_h(NE\_NWE)$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK}+1.5$	-	ns
$t_v(A\_NE)$	FMC_NEx low to FMC_A valid	-	0	ns
$t_h(A\_NWE)$	Address hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_v(BL\_NE)$	FMC_NEx low to FMC_BL valid	-	1.5	ns
$t_h(BL\_NWE)$	FMC_BL hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_v(Data\_NE)$	Data to FMC_NEx low to Data valid	-	$T_{HCLK}+2$	ns
$t_h(Data\_NWE)$	Data hold time after FMC_NWE high	$T_{HCLK}+0.5$	-	ns
$t_v(NADV\_NE)$	FMC_NEx low to FMC_NADV low	-	0.5	ns
$t_w(NADV)$	FMC_NADV low time	-	$T_{HCLK}+0.5$	ns

1.  $C_L = 30 \text{ pF}$ .
2. Guaranteed by characterization results.

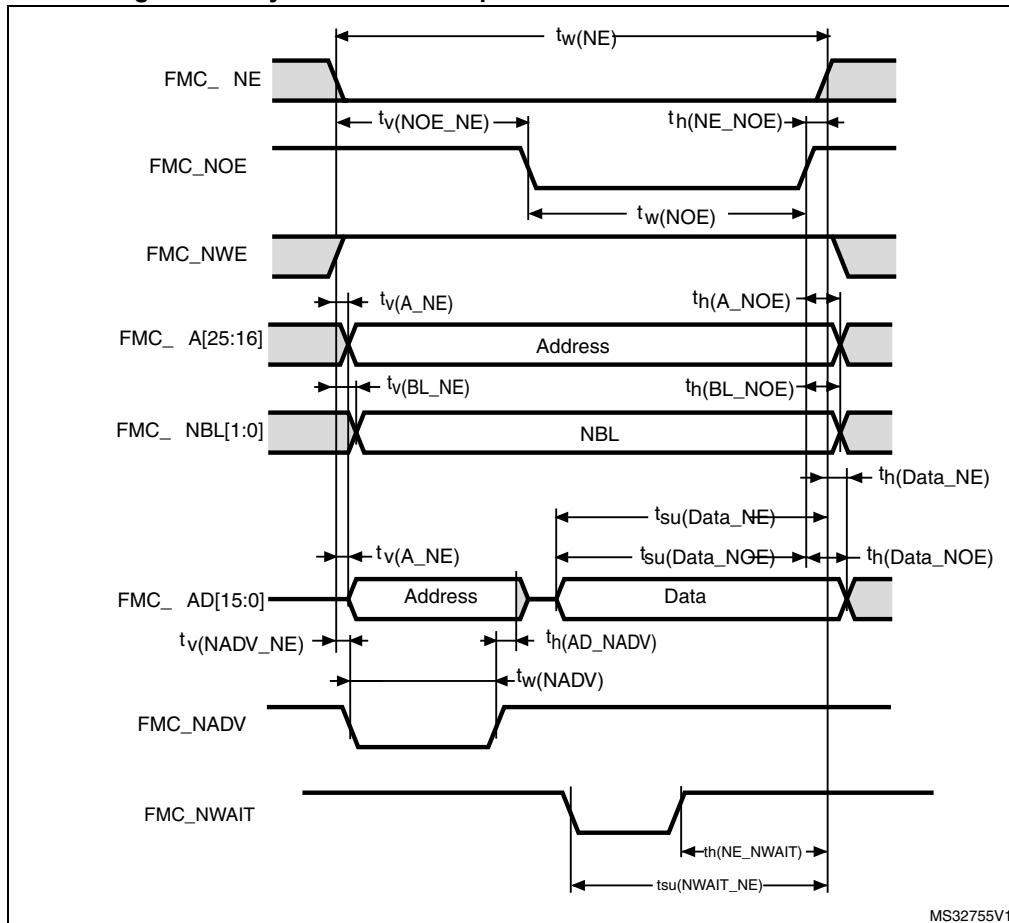
**Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FMC_NE low time	$8T_{HCLK}+1$	$8T_{HCLK}+2$	ns
$t_w(NWE)$	FMC_NWE low time	$6T_{HCLK}-1$	$6T_{HCLK}+2$	ns
$t_{su}(NWAIT\_NE)$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	ns
$t_h(NE\_NWAIT)$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$		ns

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

**Figure 57. Asynchronous multiplexed PSRAM/NOR read waveforms**



**Table 90. Asynchronous multiplexed PSRAM/NOR read timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK} - 1$	$3T_{HCLK} + 0.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK} - 0.5$	$2T_{HCLK}$	ns
$t_{tw(NOE)}$	FMC_NOE low time	$T_{HCLK} - 1$	$T_{HCLK} + 1$	ns
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	1	-	ns
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	ns
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	2	ns
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK} + 0.5$	ns
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	0	-	ns
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK} - 0.5$	-	ns
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK} + 1.5$	-	ns
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK} + 1$	-	ns
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	ns

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

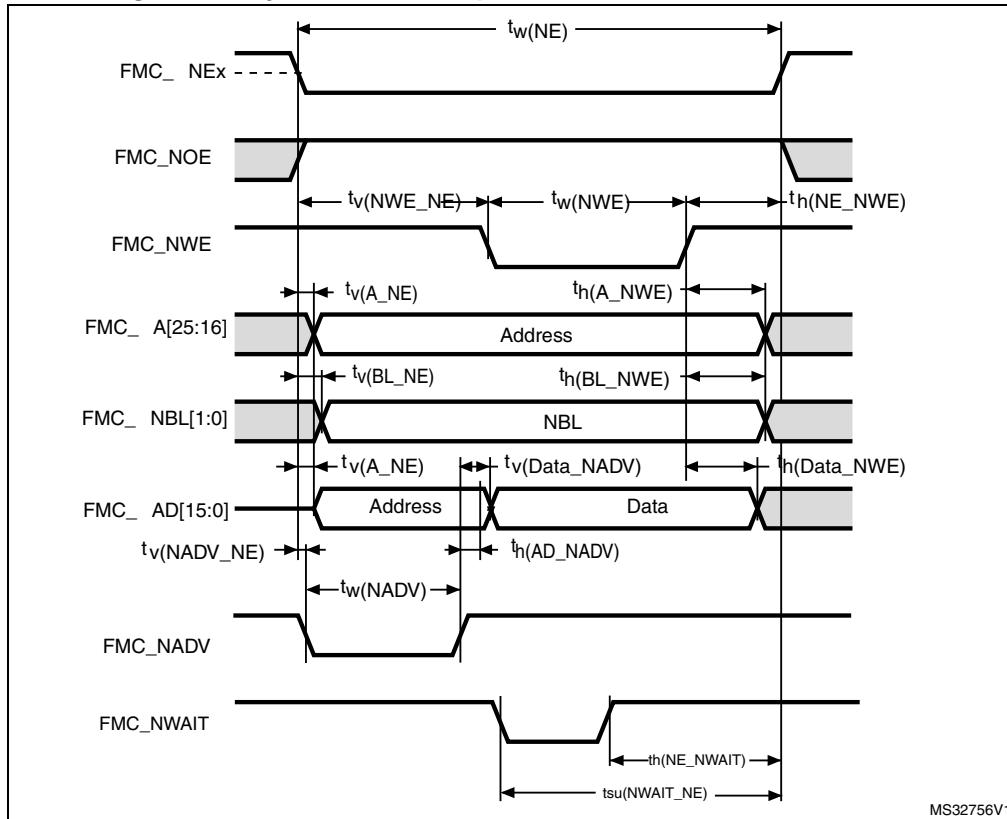
**Table 91. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK} + 0.5$	$8T_{HCLK} + 2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK} - 1$	$5T_{HCLK} + 1.5$	ns
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK} + 1.5$	-	ns
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK} + 1$		ns

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

**Figure 58. Asynchronous multiplexed PSRAM/NOR write waveforms**



**Table 92. Asynchronous multiplexed PSRAM/NOR write timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(NE)$	FMC_NE low time	$4T_{HCLK}$	$4T_{HCLK}+0.5$	ns
$t_v(NWE\_NE)$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK}+0.5$	ns
$t_w(NWE)$	FMC_NWE low time	$2T_{HCLK}$	$2T_{HCLK}+0.5$	ns
$t_h(NE\_NWE)$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK}$	-	ns
$t_v(A\_NE)$	FMC_NEx low to FMC_A valid	-	0	ns
$t_v(NADV\_NE)$	FMC_NEx low to FMC_NADV low	0.5	1	ns
$t_w(NADV)$	FMC_NADV low time	$T_{HCLK} - 0.5$	$T_{HCLK}+ 0.5$	ns
$t_h(AD\_NADV)$	FMC_AD(address) valid hold time after FMC_NADV high)	$T_{HCLK} - 2$	-	ns
$t_h(A\_NWE)$	Address hold time after FMC_NWE high	$T_{HCLK}$	-	ns
$t_h(BL\_NWE)$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 2$	-	ns
$t_v(BL\_NE)$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_v(Data\_NADV)$	FMC_NADV high to Data valid	-	$T_{HCLK} +1.5$	ns
$t_h(Data\_NWE)$	Data hold time after FMC_NWE high	$T_{HCLK} +0.5$	-	ns

$$1. \quad C_L = 30 \text{ pF.}$$

2. Guaranteed by characterization results.

**Table 93. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$	$7T_{HCLK}+2$	ns
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+1.5$	-	ns
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	ns

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

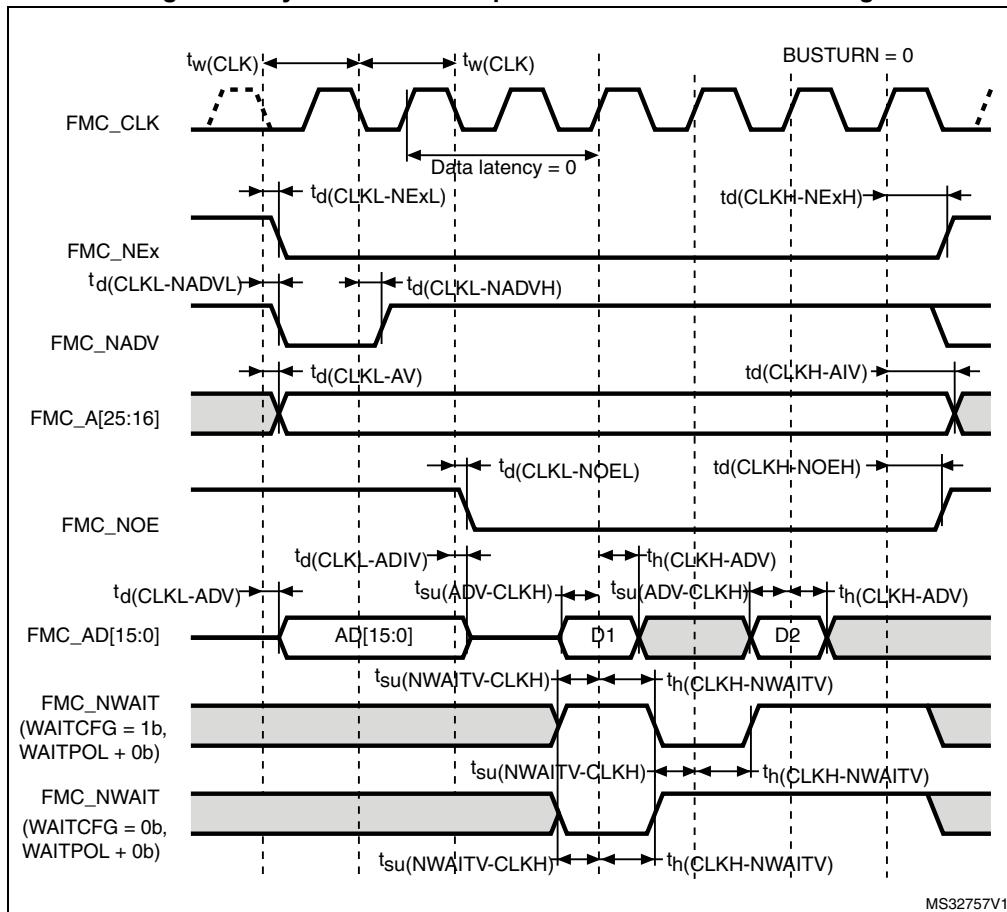
### Synchronous waveforms and timings

*Figure 59* through *Figure 62* represent synchronous waveforms and *Table 94* through *Table 97* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC\_BurstAccessMode\_Enable;
- MemoryType = FMC\_MemoryType\_CRAM;
- WriteBurst = FMC\_WriteBurst\_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F4xx reference manual : RM0090)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the  $T_{HCLK}$  is the HCLK clock period (with maximum FMC\_CLK = 90 MHz).

Figure 59. Synchronous multiplexed NOR/PSRAM read timings

Table 94. Synchronous multiplexed NOR/PSRAM read timings<sup>(1)(2)</sup>

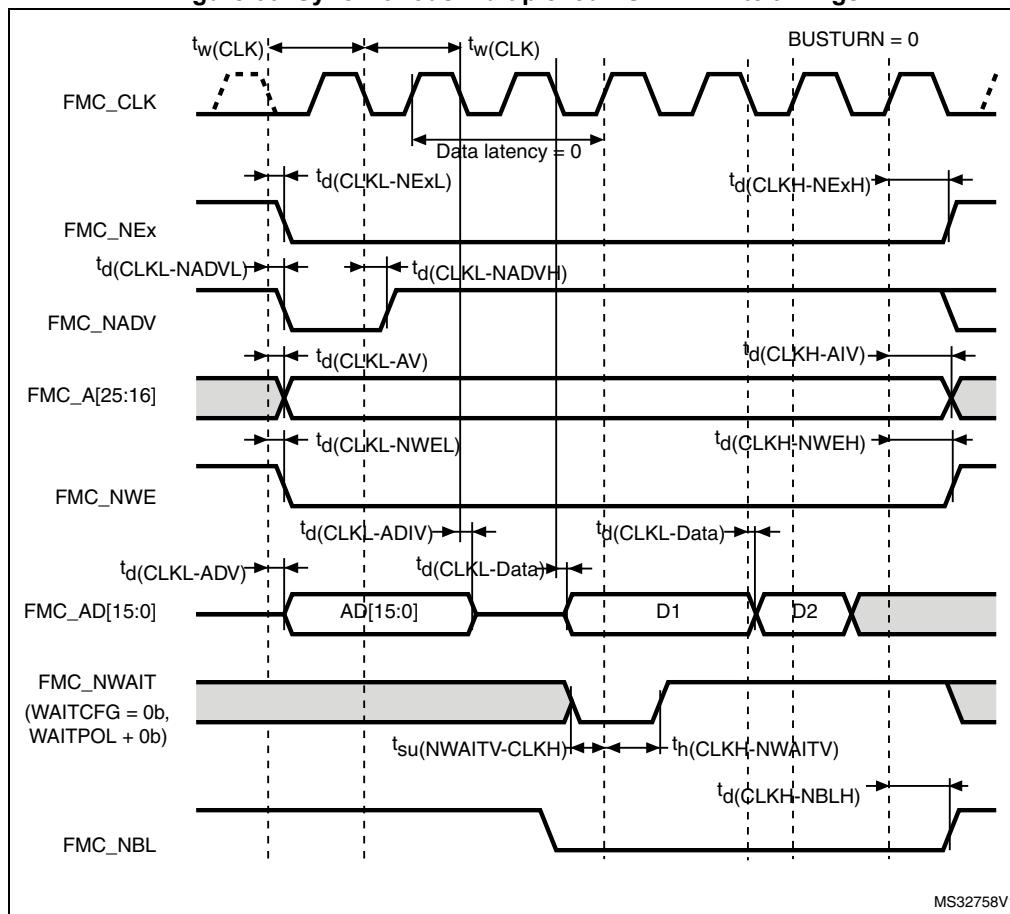
Symbol	Parameter	Min	Max	Unit
$t_w(CLK)$	FMC_CLK period	$2T_{HCLK} - 1$	-	ns
$t_d(CLKL-NExL)$	FMC_CLK low to FMC_NEx low ( $x=0..2$ )	-	0	ns
$t_d(CLKH_NExH)$	FMC_CLK high to FMC_NEx high ( $x= 0..2$ )	$T_{HCLK}$	-	ns
$t_d(CLKL-NADVL)$	FMC_CLK low to FMC_NADV low	-	0	ns
$t_d(CLKL-NADVH)$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_d(CLKL-AV)$	FMC_CLK low to FMC_Ax valid ( $x=16..25$ )	-	0	ns
$t_d(CLKH-AIV)$	FMC_CLK high to FMC_Ax invalid ( $x=16..25$ )	0	-	ns
$t_d(CLKL-NOEL)$	FMC_CLK low to FMC_NOE low	-	$T_{HCLK}+0.5$	ns
$t_d(CLKH-NOEH)$	FMC_CLK high to FMC_NOE high	$T_{HCLK}-0.5$	-	ns
$t_d(CLKL-ADV)$	FMC_CLK low to FMC_AD[15:0] valid	-	0.5	ns
$t_d(CLKL-ADIV)$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	ns

**Table 94. Synchronous multiplexed NOR/PSRAM read timings<sup>(1)(2)</sup> (continued)**

Symbol	Parameter	Min	Max	Unit
$t_{su}(\text{ADV-CLKH})$	FMC_A/D[15:0] valid data before FMC_CLK high	5	-	ns
$t_h(\text{CLKH-ADV})$	FMC_A/D[15:0] valid data after FMC_CLK high	0	-	ns
$t_{su}(\text{NWAIT-CLKH})$	FMC_NWAIT valid before FMC_CLK high	4	-	ns
$t_h(\text{CLKH-NWAIT})$	FMC_NWAIT valid after FMC_CLK high	0	-	ns

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

**Figure 60. Synchronous multiplexed PSRAM write timings**

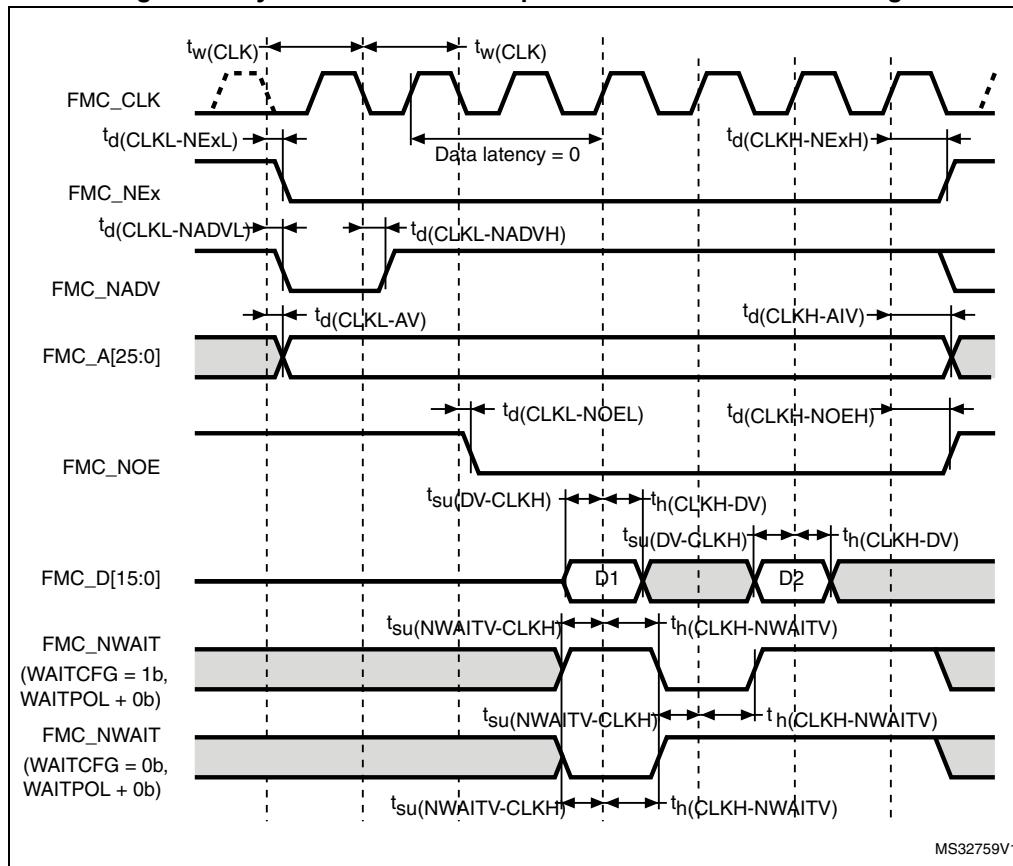
**Table 95. Synchronous multiplexed PSRAM write timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FMC_CLK period, VDD range= 2.7 to 3.6 V	$2T_{\text{HCLK}} - 1$	-	ns
$t_d(\text{CLKL-NExL})$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1.5	ns
$t_d(\text{CLKH-NExH})$	FMC_CLK high to FMC_NEx high (x= 0...2)	$T_{\text{HCLK}}$	-	ns
$t_d(\text{CLKL-NADVL})$	FMC_CLK low to FMC_NADV low	-	0	ns
$t_d(\text{CLKL-NADVH})$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_d(\text{CLKL-AV})$	FMC_CLK low to FMC_Ax valid (x=16...25)	-	0	ns
$t_d(\text{CLKH-AIV})$	FMC_CLK high to FMC_Ax invalid (x=16...25)	$T_{\text{HCLK}}$	-	ns
$t_d(\text{CLKL-NWEL})$	FMC_CLK low to FMC_NWE low	-	0	ns
$t_d(\text{CLKH-NWEH})$	FMC_CLK high to FMC_NWE high	$T_{\text{HCLK}} - 0.5$	-	ns
$t_d(\text{CLKL-ADV})$	FMC_CLK low to FMC_AD[15:0] valid	-	3	ns
$t_d(\text{CLKL-ADIV})$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	ns
$t_d(\text{CLKL-DATA})$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	ns
$t_d(\text{CLKL-NBLL})$	FMC_CLK low to FMC_NBL low	0	-	ns
$t_d(\text{CLKH-NBLH})$	FMC_CLK high to FMC_NBL high	$T_{\text{HCLK}} - 0.5$	-	ns
$t_{su}(\text{NWAIT-CLKH})$	FMC_NWAIT valid before FMC_CLK high	4	-	ns
$t_h(\text{CLKH-NWAIT})$	FMC_NWAIT valid after FMC_CLK high	0	-	ns

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

Figure 61. Synchronous non-multiplexed NOR/PSRAM read timings

Table 96. Synchronous non-multiplexed NOR/PSRAM read timings<sup>(1)(2)</sup>

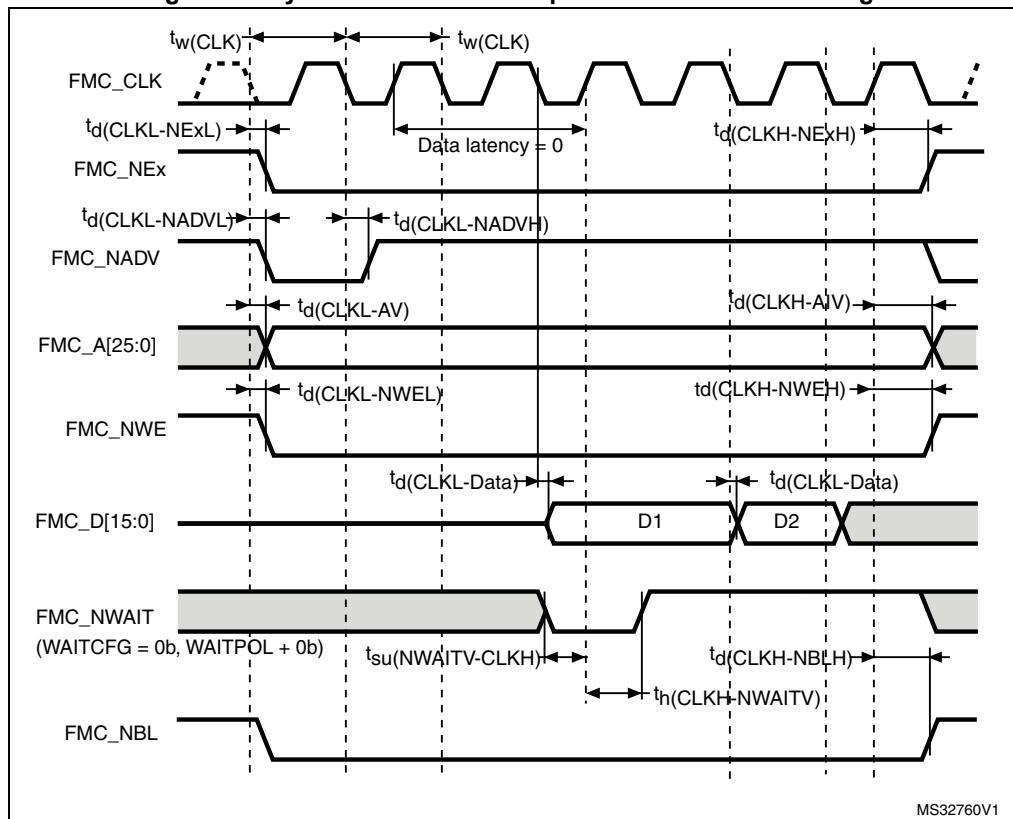
Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FMC_CLK period	$2T_{\text{HCLK}} - 1$	-	ns
$t_{(\text{CLKL}-\text{NExL})}$	FMC_CLK low to FMC_NEx low ( $x=0..2$ )	-	0.5	ns
$t_{d(\text{CLKH}-\text{NExH})}$	FMC_CLK high to FMC_NEx high ( $x= 0..2$ )	$T_{\text{HCLK}}$	-	ns
$t_{d(\text{CLKL}-\text{NADV})}$	FMC_CLK low to FMC_NADV low	-	0	ns
$t_{d(\text{CLKL}-\text{NADVH})}$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_{d(\text{CLKL}-\text{AV})}$	FMC_CLK low to FMC_Ax valid ( $x=16..25$ )	-	0	ns
$t_{d(\text{CLKH}-\text{AIV})}$	FMC_CLK high to FMC_Ax invalid ( $x=16..25$ )	$T_{\text{HCLK}} - 0.5$	-	ns
$t_{d(\text{CLKL}-\text{NOEL})}$	FMC_CLK low to FMC_NOE low	-	$T_{\text{HCLK}}+2$	ns
$t_{d(\text{CLKH}-\text{NOEH})}$	FMC_CLK high to FMC_NOE high	$T_{\text{HCLK}} - 0.5$	-	ns
$t_{su(\text{DV}-\text{CLKH})}$	FMC_D[15:0] valid data before FMC_CLK high	5	-	ns

**Table 96. Synchronous non-multiplexed NOR/PSRAM read timings<sup>(1)(2)</sup> (continued)**

Symbol	Parameter	Min	Max	Unit
$t_h(CLKH-DV)$	FMC_D[15:0] valid data after FMC_CLK high	0	-	ns
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4		
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	0		

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

**Figure 62. Synchronous non-multiplexed PSRAM write timings****Table 97. Synchronous non-multiplexed PSRAM write timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{HCLK} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low ( $x=0..2$ )	-	0.5	ns
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high ( $x=0..2$ )	$T_{HCLK}$	-	ns
$t_{d(CLKL-NADV)}$	FMC_CLK low to FMC_NADV low	-	0	ns
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid ( $x=16..25$ )	-	0	ns

**Table 97. Synchronous non-multiplexed PSRAM write timings<sup>(1)(2)</sup> (continued)**

Symbol	Parameter	Min	Max	Unit
$t_d(CLKH-AIV)$	FMC_CLK high to FMC_Ax invalid (x=16...25)	0	-	ns
$t_d(CLKL-NWEL)$	FMC_CLK low to FMC_NWE low	-	0	ns
$t_d(CLKH-NWEH)$	FMC_CLK high to FMC_NWE high	$T_{HCLK}-0.5$	-	ns
$t_d(CLKL-Data)$	FMC_D[15:0] valid data after FMC_CLK low	-	2.5	ns
$t_d(CLKL-NBLL)$	FMC_CLK low to FMC_NBL low	0	-	ns
$t_d(CLKH-NBLH)$	FMC_CLK high to FMC_NBL high	$T_{HCLK}-0.5$	-	ns
$t_{su}(NWAIT-CLKH)$	FMC_NWAIT valid before FMC_CLK high	4		
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	0		

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

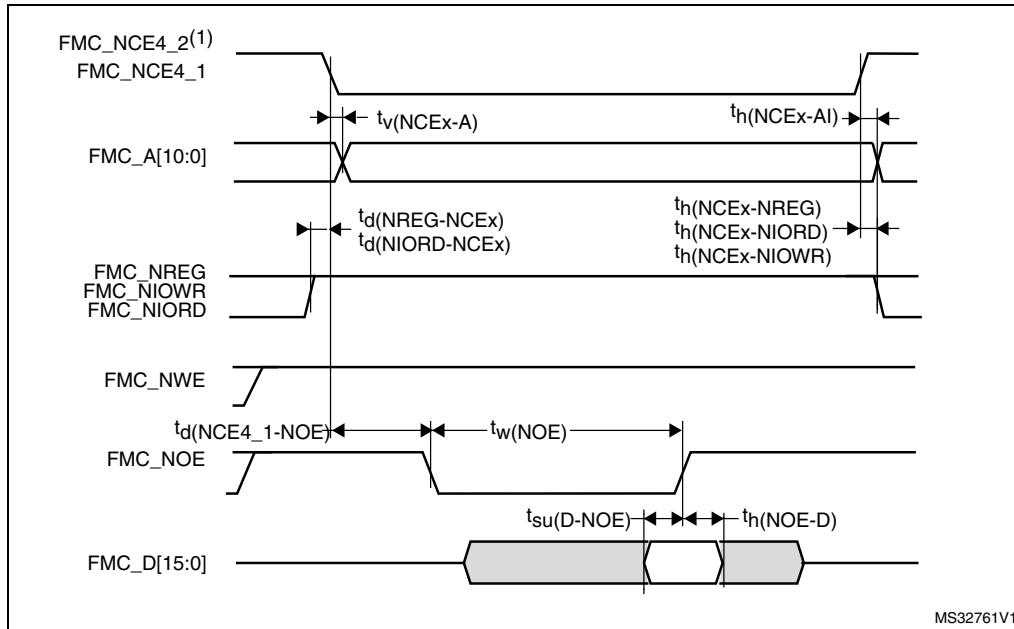
### PC Card/CompactFlash controller waveforms and timings

*Figure 63* through *Figure 68* represent synchronous waveforms, and *Table 98* and *Table 99* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC\_SetupTime = 0x04;
- COM.FMC\_WaitSetupTime = 0x07;
- COM.FMC\_HoldSetupTime = 0x04;
- COM.FMC\_HiZSetupTime = 0x00;
- ATT.FMC\_SetupTime = 0x04;
- ATT.FMC\_WaitSetupTime = 0x07;
- ATT.FMC\_HoldSetupTime = 0x04;
- ATT.FMC\_HiZSetupTime = 0x00;
- IO.FMC\_SetupTime = 0x04;
- IO.FMC\_WaitSetupTime = 0x07;
- IO.FMC\_HoldSetupTime = 0x04;
- IO.FMC\_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

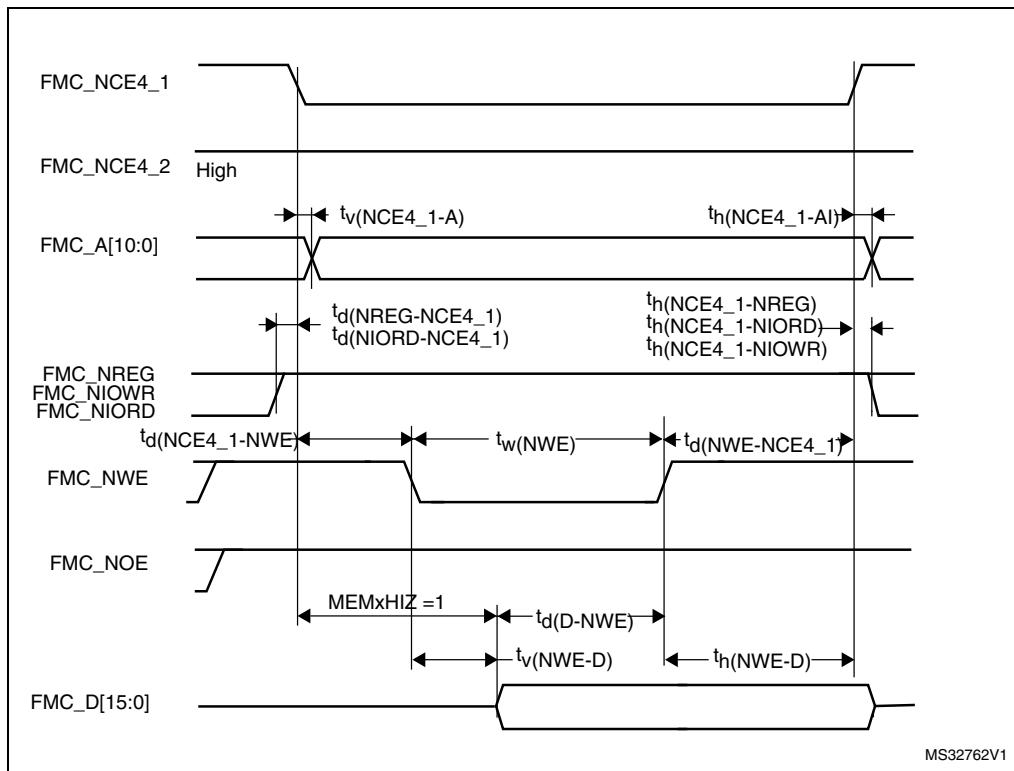
In all timing tables, the  $T_{HCLK}$  is the HCLK clock period.

**Figure 63. PC Card/CompactFlash controller waveforms for common memory read access**

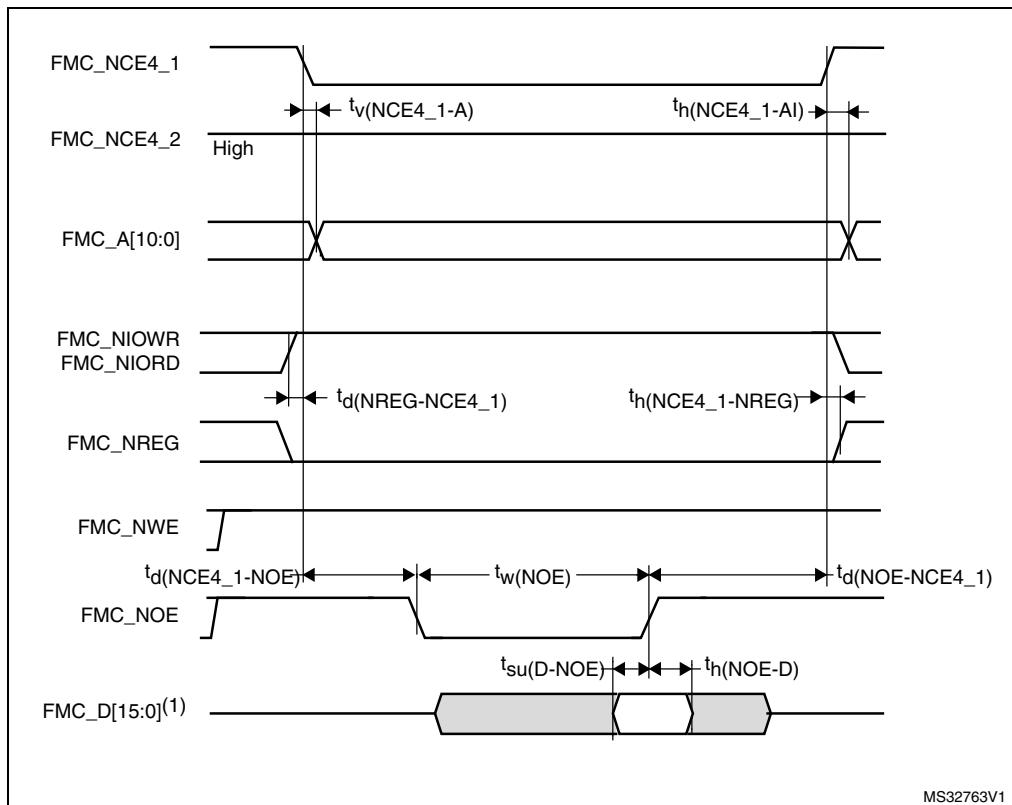


1. FMC\_NCE4\_2 remains high (inactive during 8-bit access).

**Figure 64. PC Card/CompactFlash controller waveforms for common memory write access**

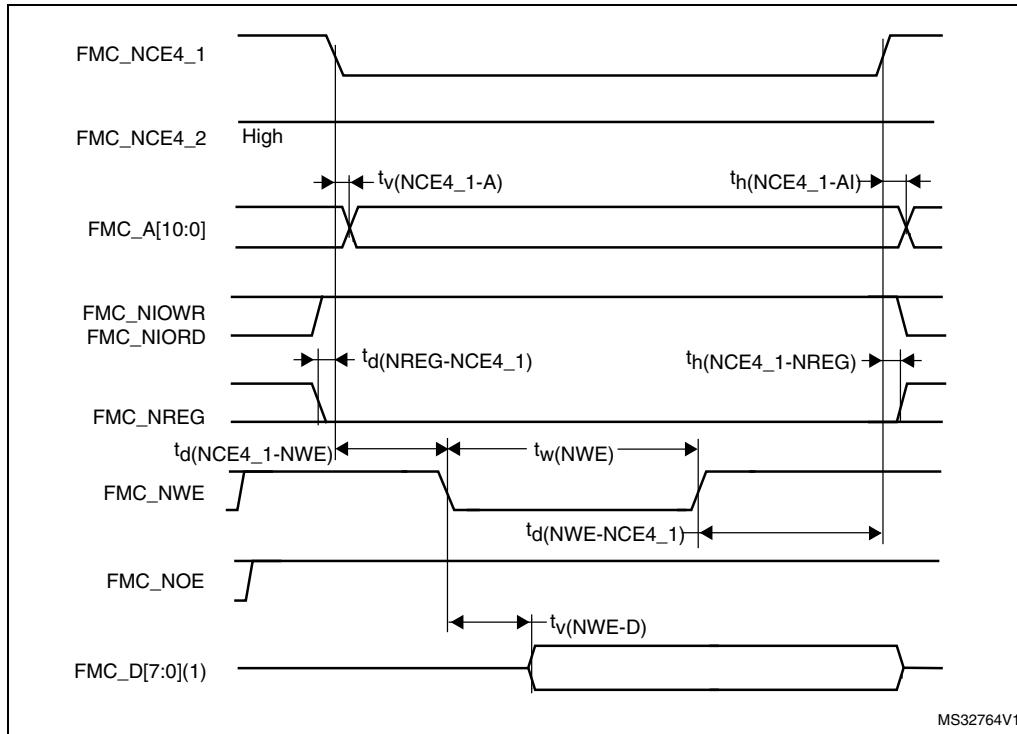


**Figure 65. PC Card/CompactFlash controller waveforms for attribute memory read access**



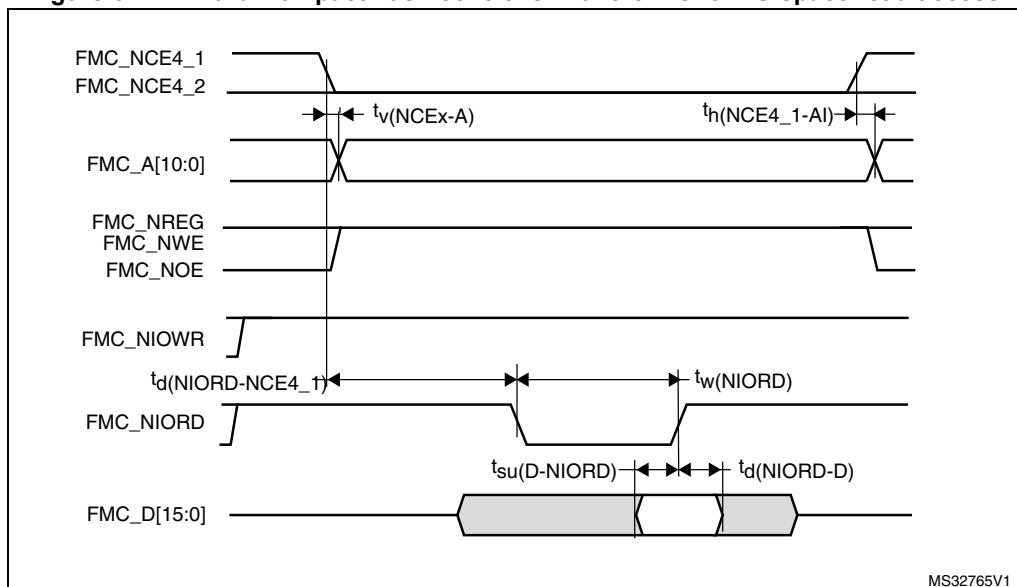
- Only data bits 0...7 are read (bits 8...15 are disregarded).

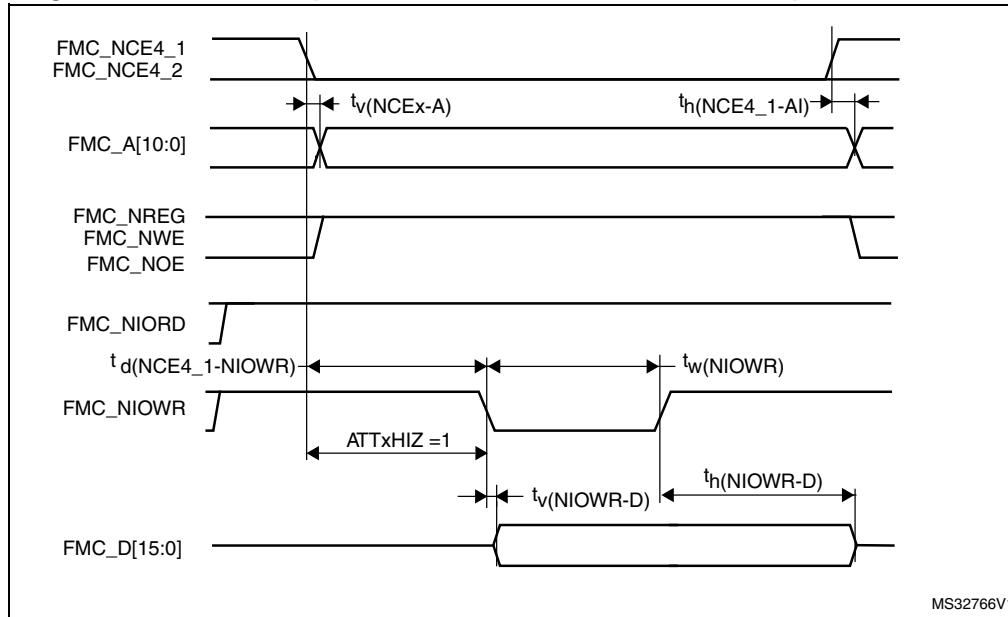
**Figure 66. PC Card/CompactFlash controller waveforms for attribute memory write access**



- Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

**Figure 67. PC Card/CompactFlash controller waveforms for I/O space read access**



**Figure 68. PC Card/CompactFlash controller waveforms for I/O space write access****Table 98. Switching characteristics for PC Card/CF read and write cycles in attribute/common space<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_v(\text{NCEx-A})$	FMC_NCEx low to FMC_Ay valid	-	0	ns
$t_h(\text{NCEx\_AI})$	FMC_NCEx high to FMC_Ax invalid	0	-	ns
$t_d(\text{NREG-NCEx})$	FMC_NCEx low to FMC_NREG valid	-	1	ns
$t_h(\text{NCEx-NREG})$	FMC_NCEx high to FMC_NREG invalid	$T_{\text{HCLK}} - 2$	-	ns
$t_d(\text{NCEx-NWE})$	FMC_NCEx low to FMC_NWE low	-	$5T_{\text{HCLK}}$	ns
$t_w(\text{NWE})$	FMC_NWE low width	$8T_{\text{HCLK}} - 0.5$	$8T_{\text{HCLK}} + 0.5$	ns
$t_d(\text{NWE-NCEx})$	FMC_NWE high to FMC_NCEx high	$5T_{\text{HCLK}} + 1$	-	ns
$t_v(\text{NWE-D})$	FMC_NWE low to FMC_D[15:0] valid	-	0	ns
$t_h(\text{NWE-D})$	FMC_NWE high to FMC_D[15:0] invalid	$9T_{\text{HCLK}} - 0.5$	-	ns
$t_d(\text{D-NWE})$	FMC_D[15:0] valid before FMC_NWE high	$13T_{\text{HCLK}} - 3$	-	ns
$t_d(\text{NCEx-NOE})$	FMC_NCEx low to FMC_NOE low	-	$5T_{\text{HCLK}}$	ns
$t_w(\text{NOE})$	FMC_NOE low width	$8 T_{\text{HCLK}} - 0.5$	$8 T_{\text{HCLK}} + 0.5$	ns
$t_d(\text{NOE-NCEx})$	FMC_NOE high to FMC_NCEx high	$5T_{\text{HCLK}} - 1$	-	ns
$t_{su}(\text{D-NOE})$	FMC_D[15:0] valid data before FMC_NOE high	$T_{\text{HCLK}}$	-	ns
$t_h(\text{NOE-D})$	FMC_NOE high to FMC_D[15:0] invalid	0	-	ns

1.  $C_L = 30 \text{ pF}$ .

2. Guaranteed by characterization results.

**Table 99. Switching characteristics for PC Card/CF read and write cycles  
in I/O space<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
tw(NIOWR)	FMC_NIOWR low width	$8T_{HCLK} - 0.5$	-	ns
tv(NIOWR-D)	FMC_NIOWR low to FMC_D[15:0] valid	-	0	ns
th(NIOWR-D)	FMC_NIOWR high to FMC_D[15:0] invalid	$9T_{HCLK} - 2$	-	ns
td(NCE4_1-NIOWR)	FMC_NCE4_1 low to FMC_NIOWR valid	-	$5T_{HCLK}$	ns
th(NCEx-NIOWR)	FMC_NCEx high to FMC_NIOWR invalid	$5T_{HCLK}$	-	ns
td(NIORD-NCEx)	FMC_NCEx low to FMC_NIORD valid	-	$5T_{HCLK}$	ns
th(NCEx-NIORD)	FMC_NCEx high to FMC_NIORD valid	$6T_{HCLK} + 2$	-	ns
tw(NIORD)	FMC_NIORD low width	$8T_{HCLK} - 0.5$	$8T_{HCLK} + 0.5$	ns
tsu(D-NIORD)	FMC_D[15:0] valid before FMC_NIORD high	$T_{HCLK}$	-	ns
td(NIORD-D)	FMC_D[15:0] valid after FMC_NIORD high	0	-	ns

1.  $C_L = 30 \text{ pF}$ .

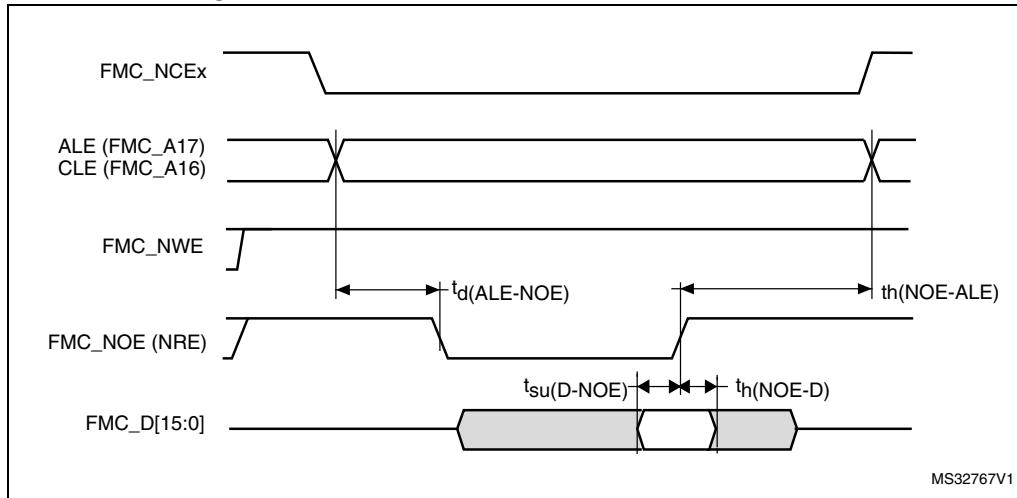
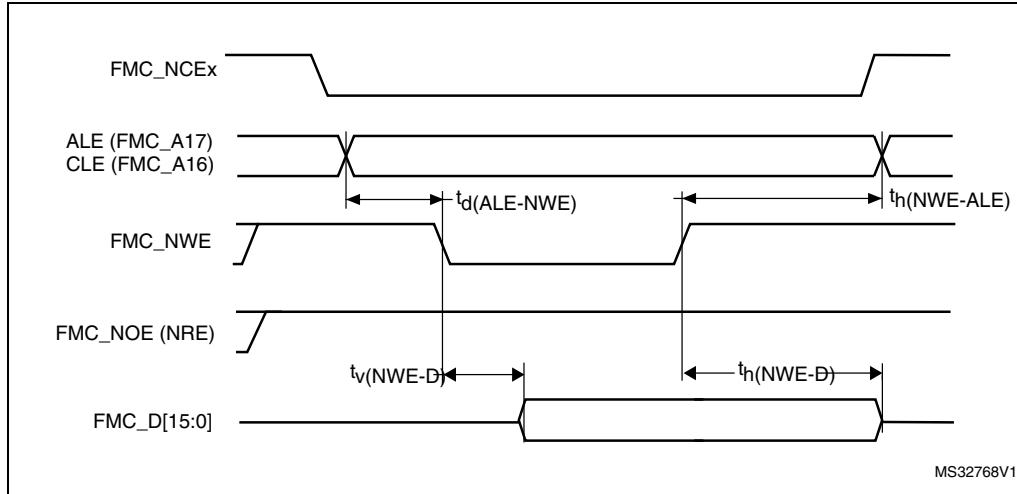
2. Guaranteed by characterization results.

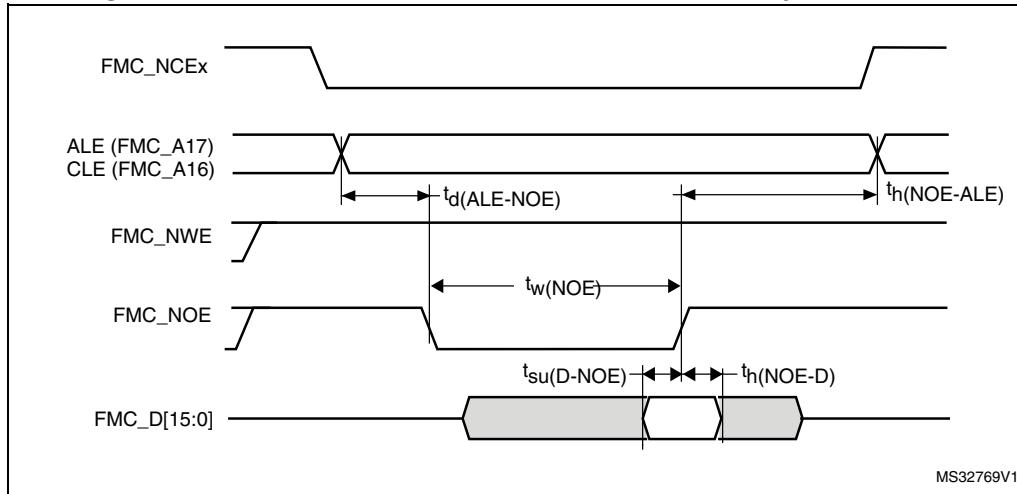
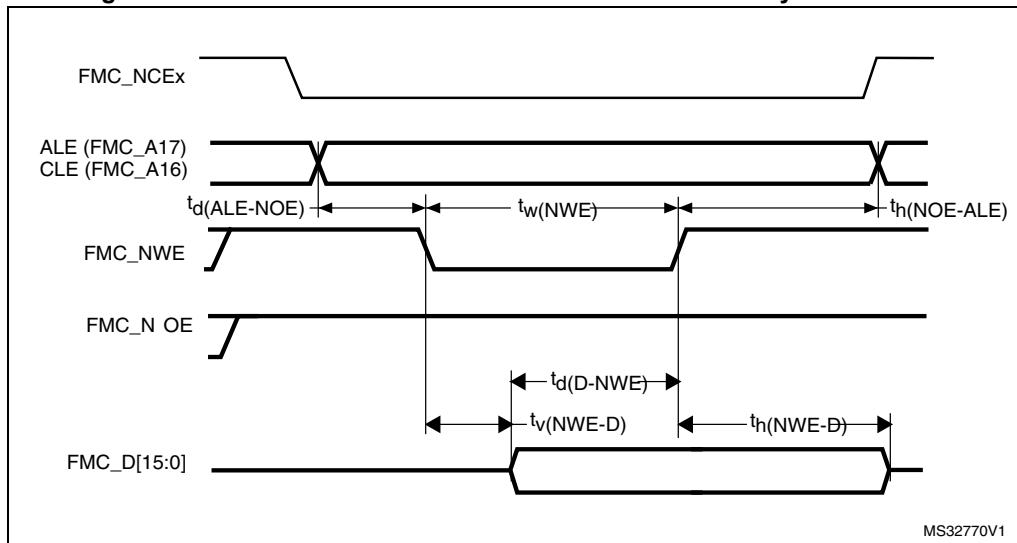
### NAND controller waveforms and timings

*Figure 69* through *Figure 72* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC\_SetupTime = 0x01;
- COM.FMC\_WaitSetupTime = 0x03;
- COM.FMC\_HoldSetupTime = 0x02;
- COM.FMC\_HiZSetupTime = 0x01;
- ATT.FMC\_SetupTime = 0x01;
- ATT.FMC\_WaitSetupTime = 0x03;
- ATT.FMC\_HoldSetupTime = 0x02;
- ATT.FMC\_HiZSetupTime = 0x01;
- Bank = FMC\_Bank\_NAND;
- MemoryDataWidth = FMC\_MemoryDataWidth\_16b;
- ECC = FMC\_ECC\_Enable;
- ECCPageSize = FMC\_ECCPageSize\_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the  $T_{HCLK}$  is the HCLK clock period.

**Figure 69. NAND controller waveforms for read access****Figure 70. NAND controller waveforms for write access**

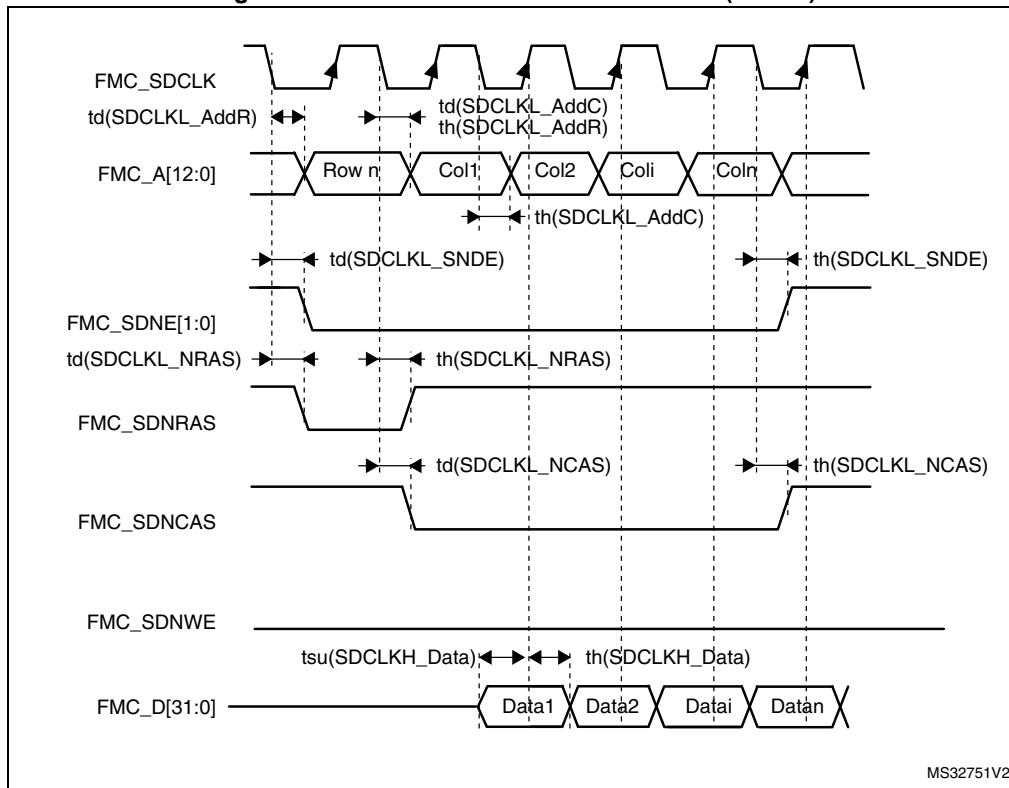
**Figure 71. NAND controller waveforms for common memory read access****Figure 72. NAND controller waveforms for common memory write access****Table 100. Switching characteristics for NAND Flash read cycles<sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(\text{NOE})$	FMC_NOE low width	$4T_{\text{HCLK}} - 0.5$	$4T_{\text{HCLK}} + 0.5$	ns
$t_{su}(\text{D-NOE})$	FMC_D[15-0] valid data before FMC_NOE high	9	-	ns
$t_h(\text{NOE-D})$	FMC_D[15-0] valid data after FMC_NOE high	0	-	ns
$t_d(\text{ALE-NOE})$	FMC_ALE valid before FMC_NOE low	-	$3T_{\text{HCLK}} - 0.5$	ns
$t_h(\text{NOE-ALE})$	FMC_NWE high to FMC_ALE invalid	$3T_{\text{HCLK}} - 2$	-	ns

1.  $C_L = 30 \text{ pF}$ .

**Table 101. Switching characteristics for NAND Flash write cycles<sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(NWE)$	FMC_NWE low width	$4T_{HCLK}$	$4T_{HCLK}+1$	ns
$t_v(NWE-D)$	FMC_NWE low to FMC_D[15-0] valid	0	-	ns
$t_h(NWE-D)$	FMC_NWE high to FMC_D[15-0] invalid	$3T_{HCLK}-1$	-	ns
$t_d(D-NWE)$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}-3$	-	ns
$t_d(ALE-NWE)$	FMC_ALE valid before FMC_NWE low	-	$3T_{HCLK}-0.5$	ns
$t_h(NWE-ALE)$	FMC_NWE high to FMC_ALE invalid	$3T_{HCLK}-1$	-	ns

1.  $C_L = 30 \text{ pF}$ .**SDRAM waveforms and timings****Figure 73. SDRAM read access waveforms (CL = 1)**

MS32751V2

**Table 102. SDRAM read timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{HCLK}} - 0.5$	$2T_{\text{HCLK}} + 0.5$	ns
$t_{su}(\text{SDCLKH\_Data})$	Data input setup time	2	-	
$t_h(\text{SDCLKH\_Data})$	Data input hold time	0	-	
$t_d(\text{SDCLKL\_Add})$	Address valid time	-	1.5	
$t_d(\text{SDCLKL\_SDNE})$	Chip select valid time	-	0.5	
$t_h(\text{SDCLKL\_SDNE})$	Chip select hold time	0	-	
$t_d(\text{SDCLKL\_SDNRAS})$	SDNRAS valid time	-	0.5	
$t_h(\text{SDCLKL\_SDNRAS})$	SDNRAS hold time	0	-	
$t_d(\text{SDCLKL\_SDNCAS})$	SDNCAS valid time	-	0.5	
$t_h(\text{SDCLKL\_SDNCAS})$	SDNCAS hold time	0	-	

1. CL = 30 pF on data and address lines. CL=15pF on FMC\_SDCLK.

2. Guaranteed by characterization results.

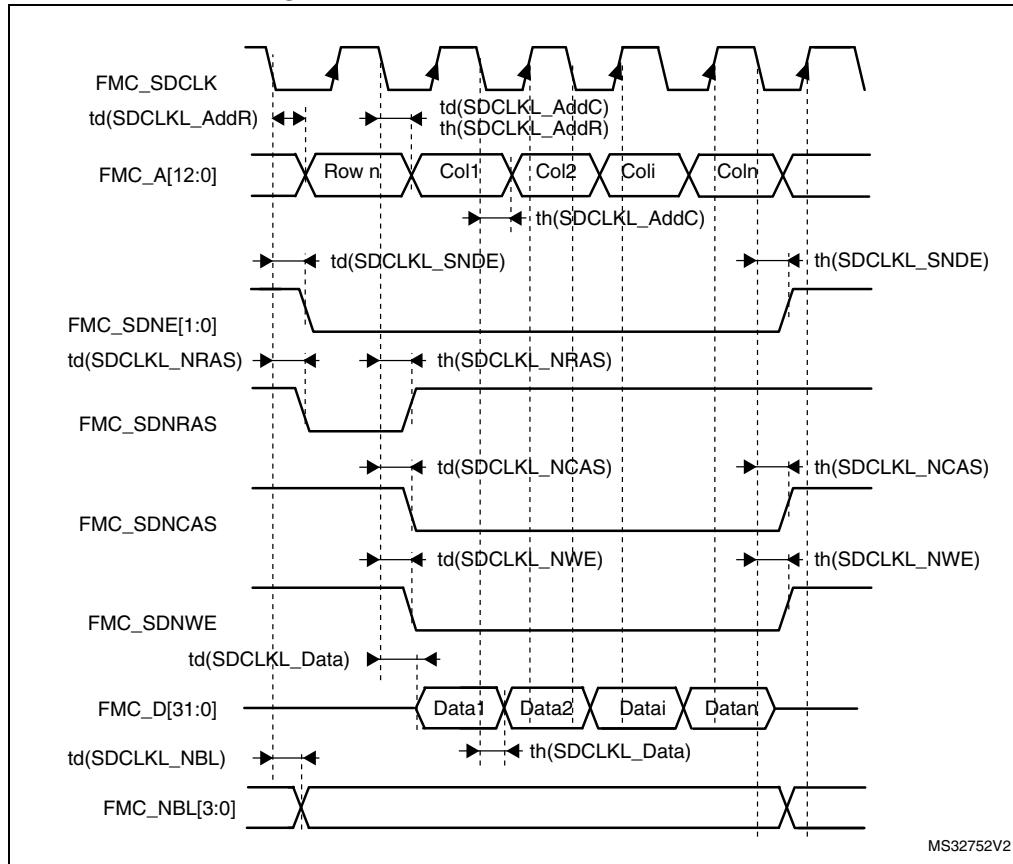
**Table 103. LPDDR SDRAM read timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{HCLK}} - 0.5$	$2T_{\text{HCLK}} + 0.5$	ns
$t_{su}(\text{SDCLKH\_Data})$	Data input setup time	2.5	-	
$t_h(\text{SDCLKH\_Data})$	Data input hold time	0	-	
$t_d(\text{SDCLKL\_Add})$	Address valid time	-	1	
$t_d(\text{SDCLKL\_SDNE})$	Chip select valid time	-	1	
$t_h(\text{SDCLKL\_SDNE})$	Chip select hold time	1	-	
$t_d(\text{SDCLKL\_SDNRAS})$	SDNRAS valid time	-	1	
$t_h(\text{SDCLKL\_SDNRAS})$	SDNRAS hold time	1	-	
$t_d(\text{SDCLKL\_SDNCAS})$	SDNCAS valid time	-	1	
$t_h(\text{SDCLKL\_SDNCAS})$	SDNCAS hold time	1	-	

1. CL = 10 pF.

2. Guaranteed by characterization results.

Figure 74. SDRAM write access waveforms



MS32752V2

**Table 104. SDRAM write timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{HCLK}} - 0.5$	$2T_{\text{HCLK}} + 0.5$	ns
$t_d(\text{SDCLKL\_Data})$	Data output valid time	-	3.5	
$t_h(\text{SDCLKL\_Data})$	Data output hold time	0	-	
$t_d(\text{SDCLKL\_Add})$	Address valid time	-	1.5	
$t_d(\text{SDCLKL\_SDNWE})$	SDNWE valid time	-	1	
$t_h(\text{SDCLKL\_SDNWE})$	SDNWE hold time	0	-	
$t_d(\text{SDCLKL\_SDNE})$	Chip select valid time	-	0.5	
$t_h(\text{SDCLKL\_SDNE})$	Chip select hold time	0	-	
$t_d(\text{SDCLKL\_SDNRAS})$	SDNRAS valid time	-	2	
$t_h(\text{SDCLKL\_SDNRAS})$	SDNRAS hold time	0	-	
$t_d(\text{SDCLKL\_SDNCAS})$	SDNCAS valid time	-	0.5	
$t_d(\text{SDCLKL\_SDNCAS})$	SDNCAS hold time	0	-	
$t_d(\text{SDCLKL\_NBL})$	NBL valid time	-	0.5	
$t_h(\text{SDCLKL\_NBL})$	NBL output time	0	-	

1. CL = 30 pF on data and address lines. CL=15pF on FMC\_SDCLK.

2. Guaranteed by characterization results.

**Table 105. LPDDR SDRAM write timings<sup>(1)(2)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{HCLK}} - 0.5$	$2T_{\text{HCLK}} + 0.5$	ns
$t_d(\text{SDCLKL\_Data})$	Data output valid time	-	5	
$t_h(\text{SDCLKL\_Data})$	Data output hold time	2	-	
$t_d(\text{SDCLKL\_Add})$	Address valid time	-	2.8	
$t_d(\text{SDCLKL\_SDNWE})$	SDNWE valid time	-	2	
$t_h(\text{SDCLKL\_SDNWE})$	SDNWE hold time	1	-	
$t_d(\text{SDCLKL\_SDNE})$	Chip select valid time	-	1.5	
$t_h(\text{SDCLKL\_SDNE})$	Chip select hold time	1	-	
$t_d(\text{SDCLKL\_SDNRAS})$	SDNRAS valid time	-	1.5	
$t_h(\text{SDCLKL\_SDNRAS})$	SDNRAS hold time	1.5	-	
$t_d(\text{SDCLKL\_SDNCAS})$	SDNCAS valid time	-	1.5	
$t_d(\text{SDCLKL\_SDNCAS})$	SDNCAS hold time	1.5	-	
$t_d(\text{SDCLKL\_NBL})$	NBL valid time	-	1.5	
$t_h(\text{SDCLKL\_NBL})$	NBL output time	1.5	-	

1. CL = 10 pF.

2. Guaranteed by characterization results.

### 6.3.27 Camera interface (DCMI) timing specifications

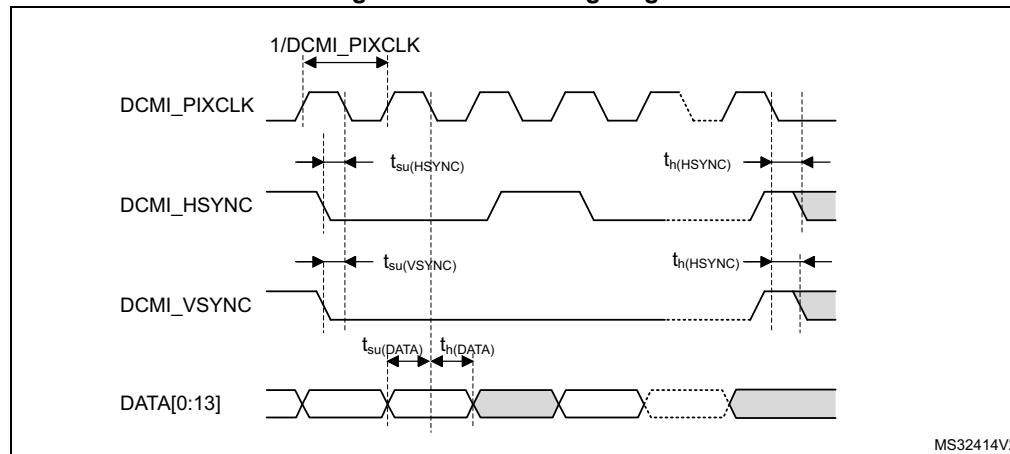
Unless otherwise specified, the parameters given in [Table 106](#) for DCMI are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency and  $V_{DD}$  supply voltage summarized in [Table 17](#), with the following configuration:

- DCMI\_PIXCLK polarity: falling
- DCMI\_VSYNC and DCMI\_HSYNC polarity: high
- Data formats: 14 bits

**Table 106. DCMI characteristics**

Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/ $f_{HCLK}$	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D <sub>Pixel</sub>	Pixel clock input duty cycle	30	70	%
t <sub>su</sub> (DATA)	Data input setup time	2	-	ns
t <sub>h</sub> (DATA)	Data input hold time	2.5	-	
t <sub>su</sub> (HSYNC) t <sub>su</sub> (VSYNC)	DCMI_HSYNC/DCMI_VSYNC input setup time	0.5	-	
t <sub>h</sub> (HSYNC) t <sub>h</sub> (VSYNC)	DCMI_HSYNC/DCMI_VSYNC input hold time	1	-	

**Figure 75. DCMI timing diagram**



### 6.3.28 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in [Table 107](#) for LCD-TFT are derived from tests performed under the ambient temperature,  $f_{HCLK}$  frequency and VDD supply voltage summarized in [Table 17](#), with the following configuration:

- LCD\_CLK polarity: high
- LCD\_DE polarity : low
- LCD\_VSYNC and LCD\_HSYNC polarity: high
- Pixel formats: 24 bits

**Table 107. LTDC characteristics**

Symbol	Parameter	Min	Max	Unit	
$f_{CLK}$	LTDC clock output frequency	-	83	MHz	
$D_{CLK}$	LTDC clock output duty cycle	45	55	%	
$t_w(CLKH)$ $t_w(CLKL)$	Clock High time, low time	$t_w(CLK)/2 - 0.5$	$t_w(CLK)/2 + 0.5$	ns	
$t_v(DATA)$	Data output valid time	-	3.5		
$t_h(DATA)$	Data output hold time	1.5	-		
$t_v(HSYNC)$	HSYNC/VSYNC/DE output valid time	-	2.5		
$t_v(VSYNC)$					
$t_v(DE)$					
$t_h(HSYNC)$	HSYNC/VSYNC/DE output hold time	2	-		
$t_h(VSYNC)$					
$t_h(DE)$					

Figure 76. LCD-TFT horizontal timing diagram

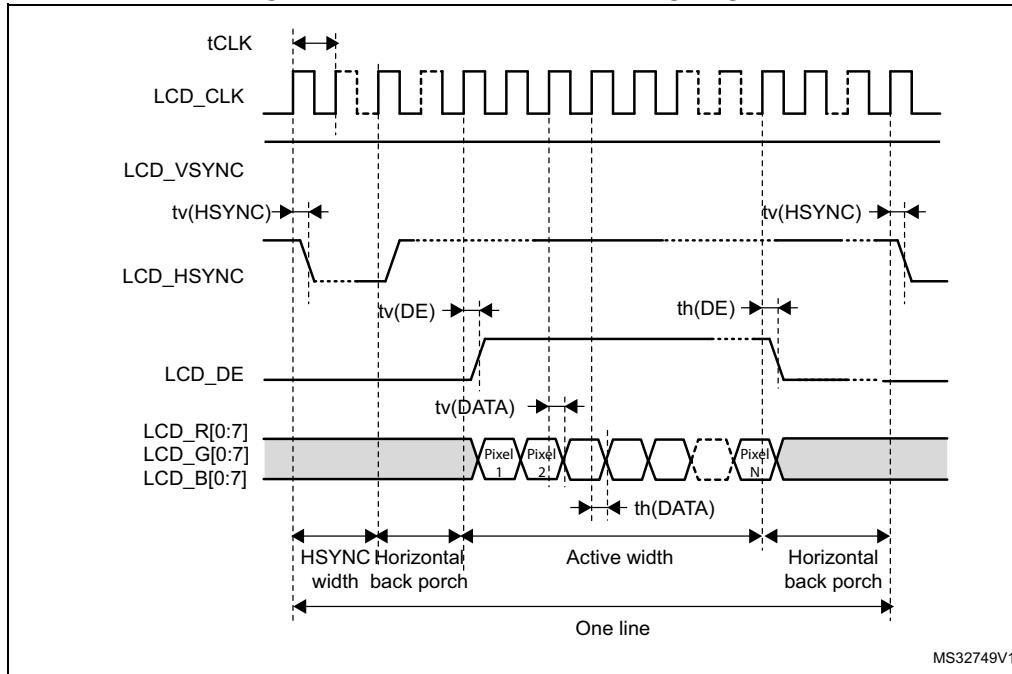
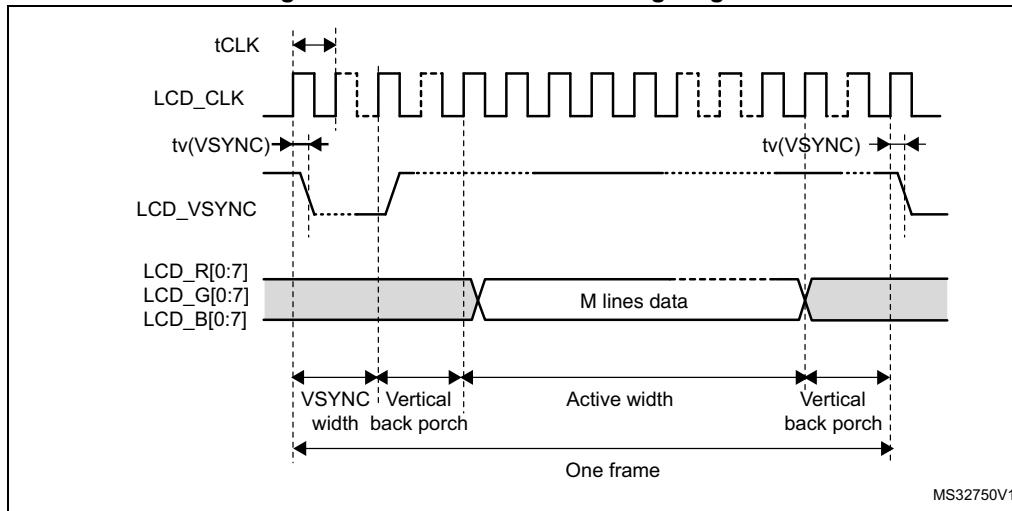


Figure 77. LCD-TFT vertical timing diagram



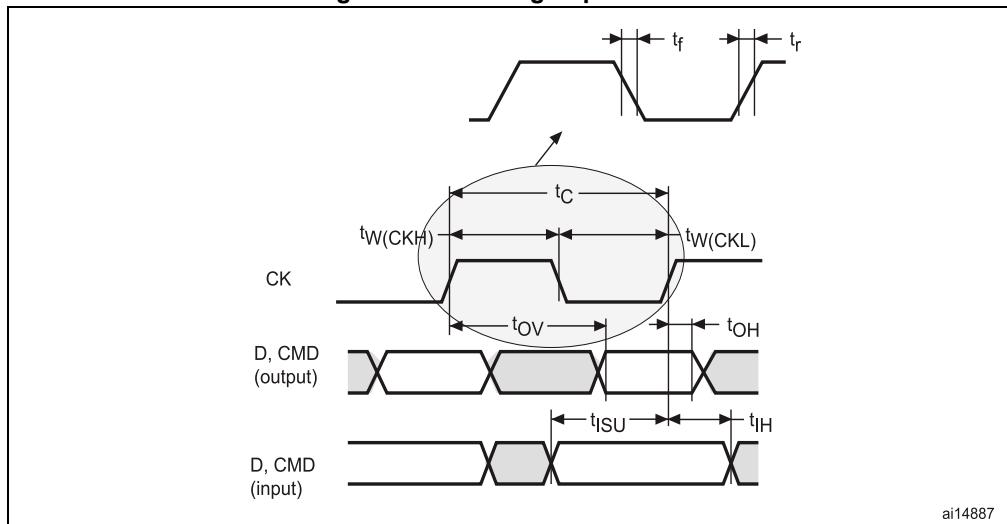
### 6.3.29 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 108](#) for the SDIO/MMC interface are derived from tests performed under the ambient temperature,  $f_{PCLK2}$  frequency and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#), with the following configuration:

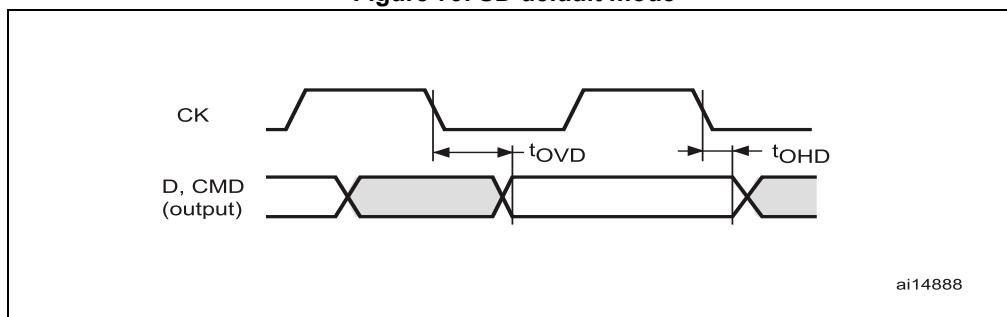
- Output speed is set to OSPEEDR[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 $V_{DD}$

Refer to [Section 6.3.17: I/O port characteristics](#) for more details on the input/output characteristics.

**Figure 78. SDIO high-speed mode**



**Figure 79. SD default mode**



**Table 108. Dynamic characteristics: SD / MMC characteristics<sup>(1)(2)</sup>**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>PP</sub>	Clock frequency in data transfer mode		0		48	MHz
-	SDIO_CK/fPCLK2 frequency ratio		-	-	8/3	-
t <sub>W(CKL)</sub>	Clock low time	f <sub>PP</sub> =48 MHz	8.5	9	-	ns
t <sub>W(CKH)</sub>	Clock high time	f <sub>PP</sub> =48 MHz	8.3	10	-	
<b>CMD, D inputs (referenced to CK) in MMC and SD HS mode</b>						
t <sub>ISU</sub>	Input setup time HS	f <sub>PP</sub> =48 MHz	3.5	-	-	ns
t <sub>IH</sub>	Input hold time HS	f <sub>PP</sub> =48 MHz	0	-	-	
<b>CMD, D outputs (referenced to CK) in MMC and SD HS mode</b>						
t <sub>OV</sub>	Output valid time HS	f <sub>PP</sub> =48 MHz	-	4.5	7	ns
t <sub>OH</sub>	Output hold time HS	f <sub>PP</sub> =48 MHz	3	-	-	
<b>CMD, D inputs (referenced to CK) in SD default mode</b>						
t <sub>ISUD</sub>	Input setup time SD	f <sub>PP</sub> =24 MHz	1.5	-	-	ns
t <sub>IHD</sub>	Input hold time SD	f <sub>PP</sub> =24 MHz	0.5	-	-	
<b>CMD, D outputs (referenced to CK) in SD default mode</b>						
t <sub>OVD</sub>	Output valid default time SD	f <sub>PP</sub> =24 MHz	-	4.5	6.5	ns
t <sub>OHD</sub>	Output hold default time SD	f <sub>PP</sub> =24 MHz	3.5	-	-	

1. Guaranteed by characterization results.

2. V<sub>DD</sub> = 2.7 to 3.6 V.

### 6.3.30 RTC characteristics

**Table 109. RTC characteristics**

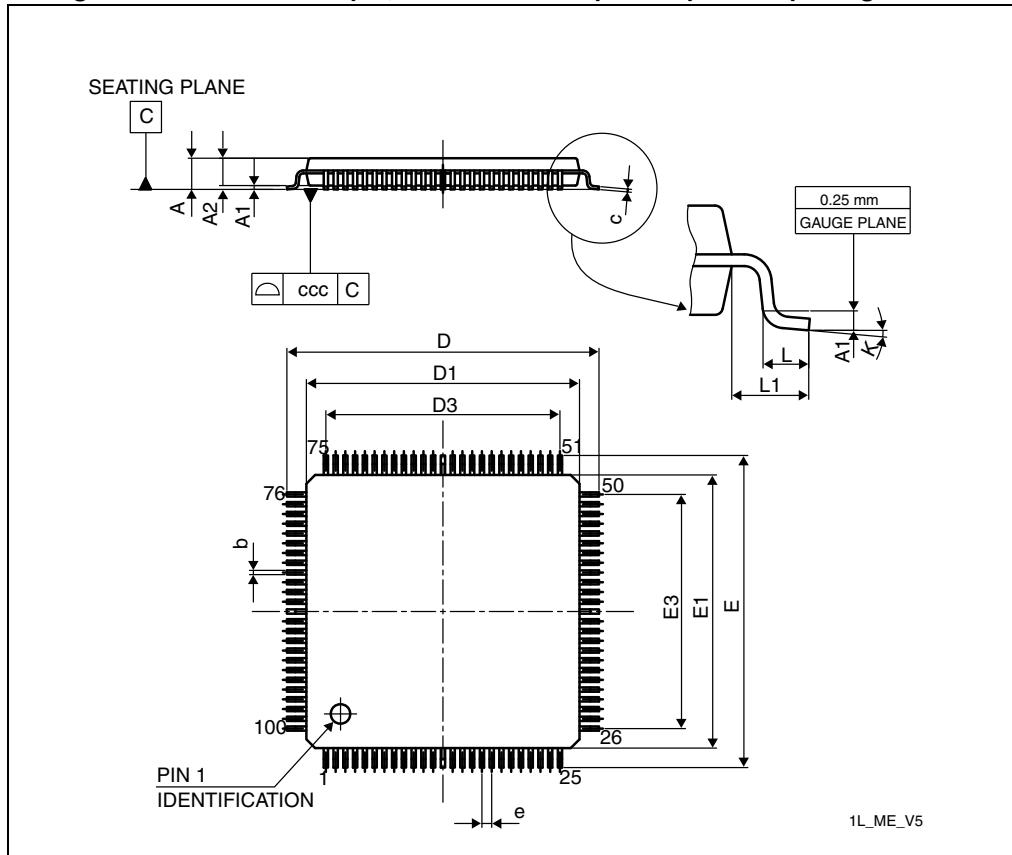
Symbol	Parameter	Conditions	Min	Max
-	f <sub>PCLK1</sub> /RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).  
ECOPACK® is an ST trademark.

### 7.1 LQFP100 package information

Figure 80. LQFP100 -100-pin, 14 x 14 mm low-profile quad flat package outline



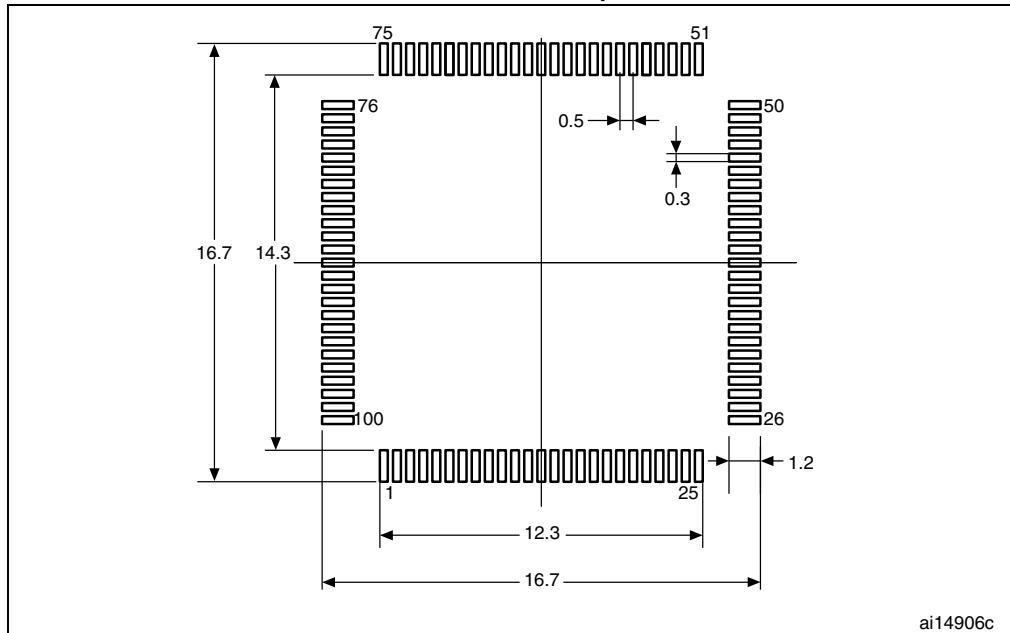
1. Drawing is not to scale.

**Table 110. LQPF100 100-pin, 14 x 14 mm low-profile quad flat package mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 81. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint**



1. Dimensions are expressed in millimeters.

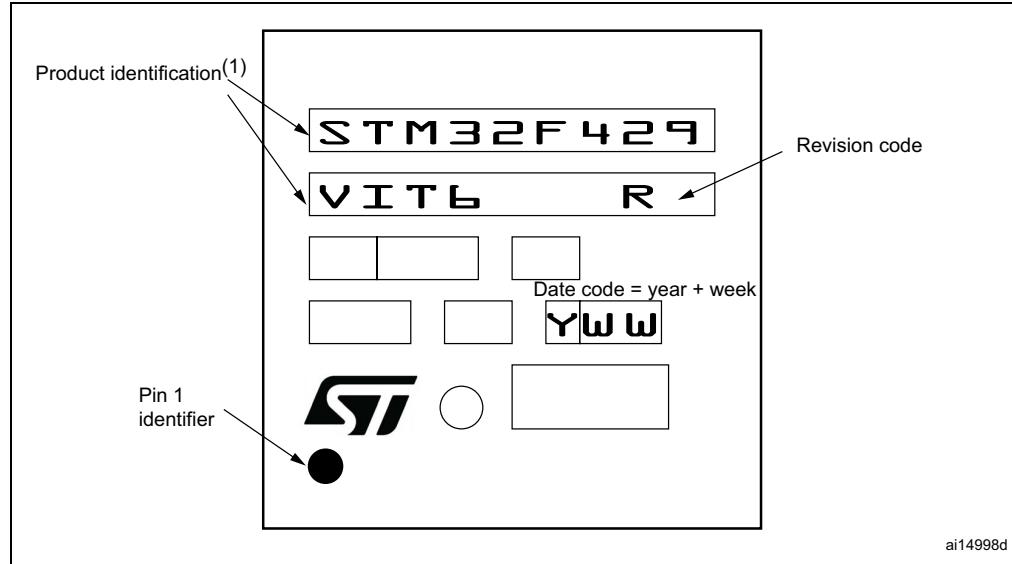
ai14906c

### Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on assembly location, are not indicated below.

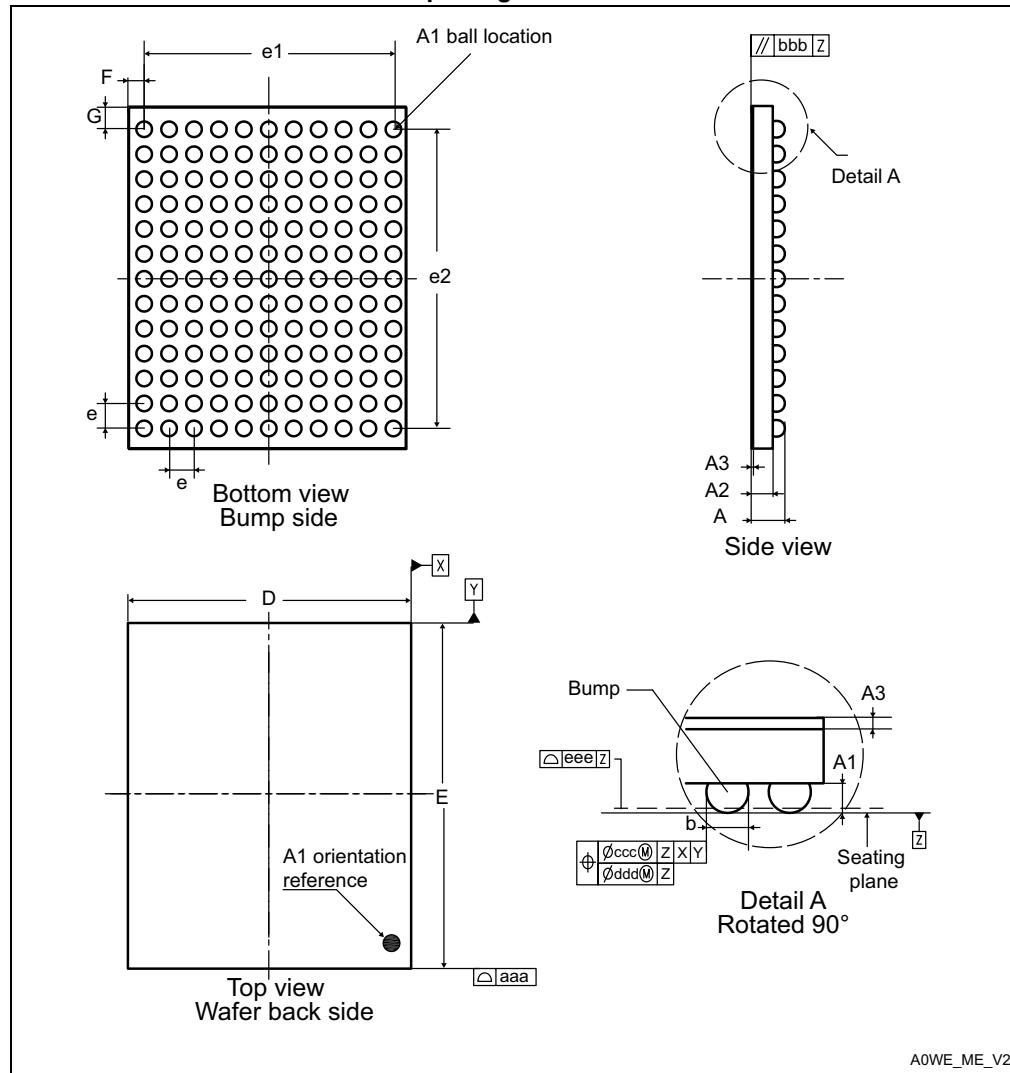
Figure 82. LQFP100 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.2 WLCSP143 package information

**Figure 83. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline**



1. Drawing is not to scale.

**Table 111. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data**

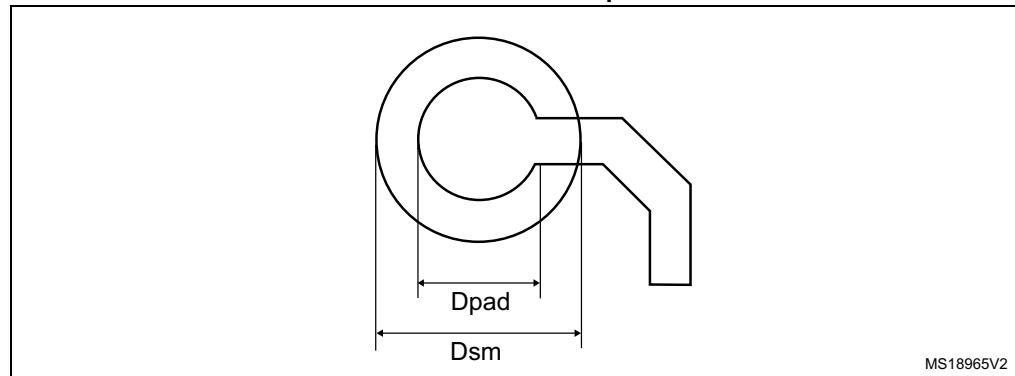
Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	0.155	0.175	0.195	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 <sup>(2)</sup>	-	0.025	-	-	0.0010	-
b <sup>(3)</sup>	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	4.486	4.521	4.556	0.1766	0.1780	0.1794
E	5.512	5.547	5.582	0.2170	0.2184	0.2198
e	-	0.400	-	-	0.0157	-
e1	-	4.000	-	-	0.1575	-
e2	-	4.800	-	-	0.1890	-
F	-	0.2605	-	-	0.0103	-
G	-	0.3735	-	-	0.0147	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating.

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

**Figure 84. WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint**



MS18965V2

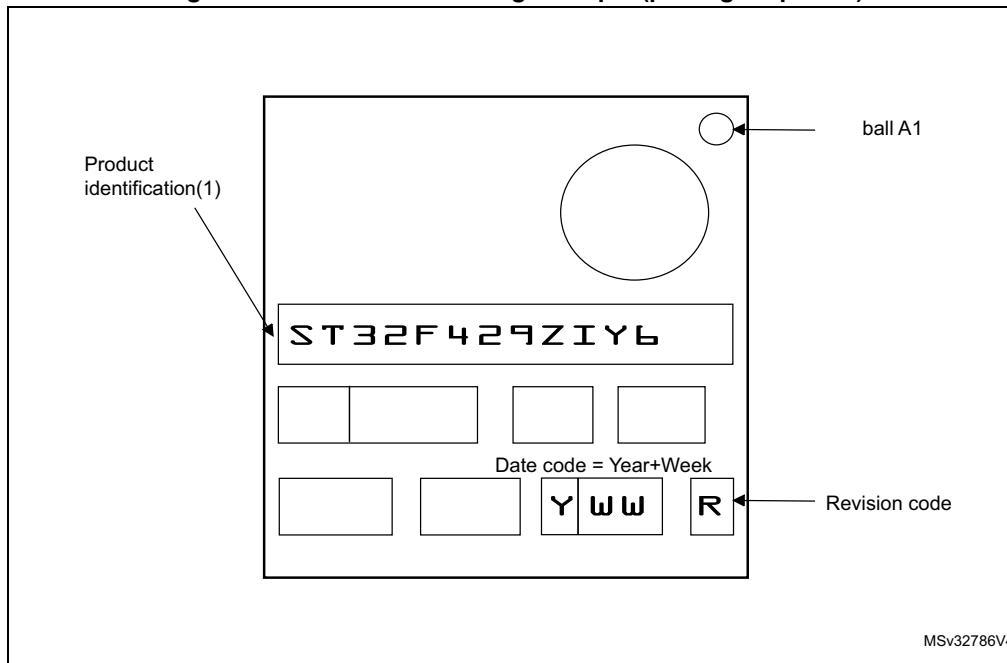
**Table 112. WLCSP143 recommended PCB design rules (0.4 mm pitch)**

Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular)
	220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

**Device marking for WLCSP143**

The following figure gives an example of topside marking orientation versus ball A 1 identifier location.

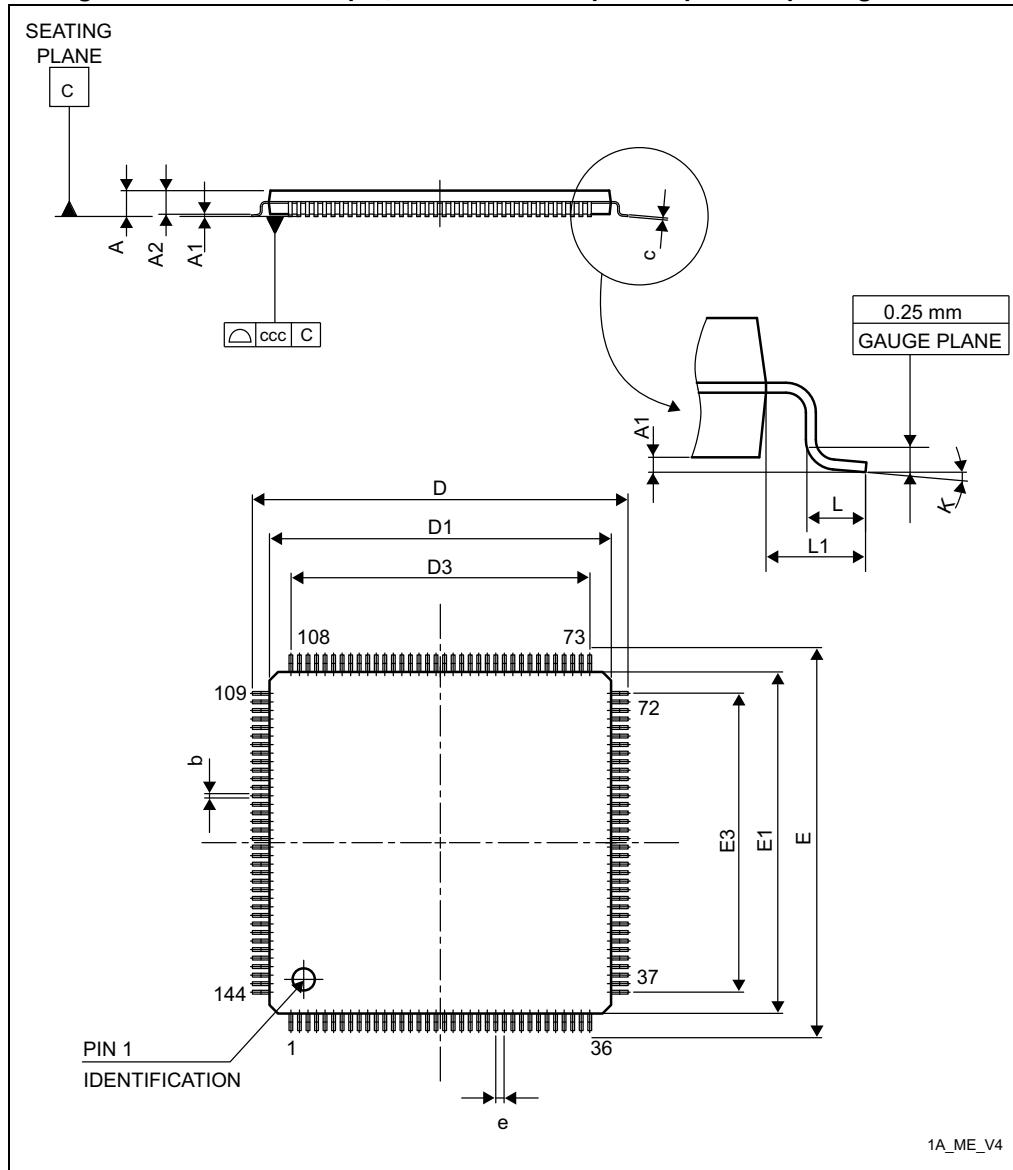
Other optional marking or inset/upset marks, which depend on assembly location, are not indicated below.

**Figure 85. WLCSP143 marking example (package top view)**

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.3 LQFP144 package information

Figure 86. LQFP144-144-pin, 20 x 20 mm low-profile quad flat package outline



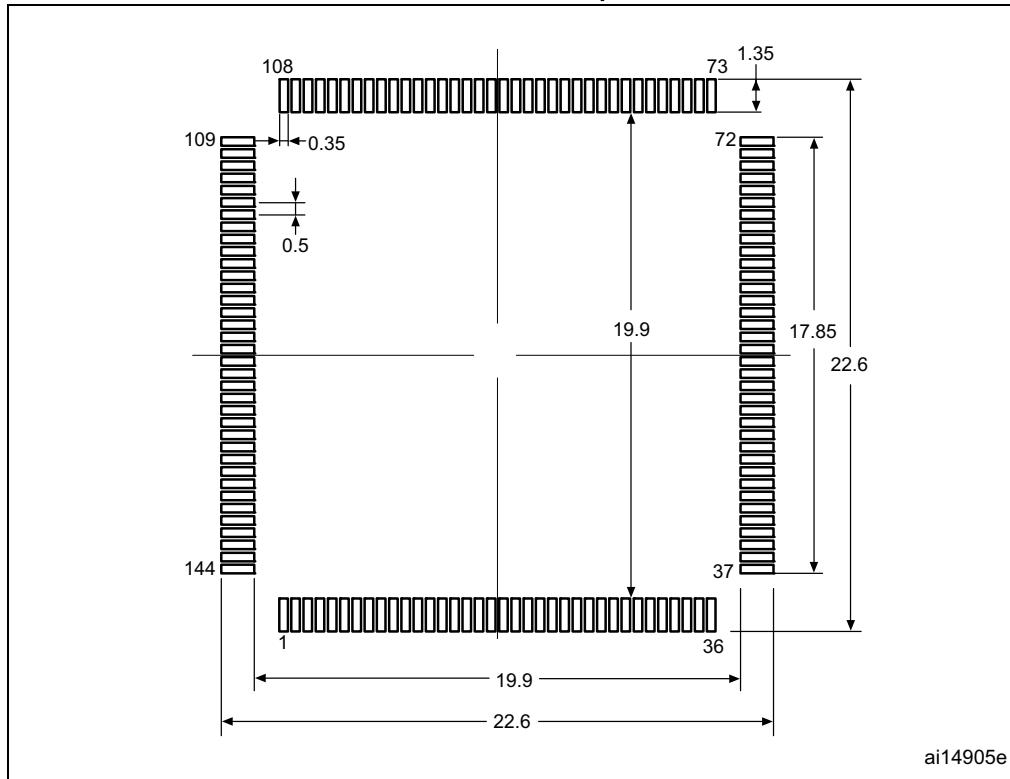
1. Drawing is not to scale.

**Table 113. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 87. LQPF144- 144-pin,20 x 20 mm low-profile quad flat package  
recommended footprint**



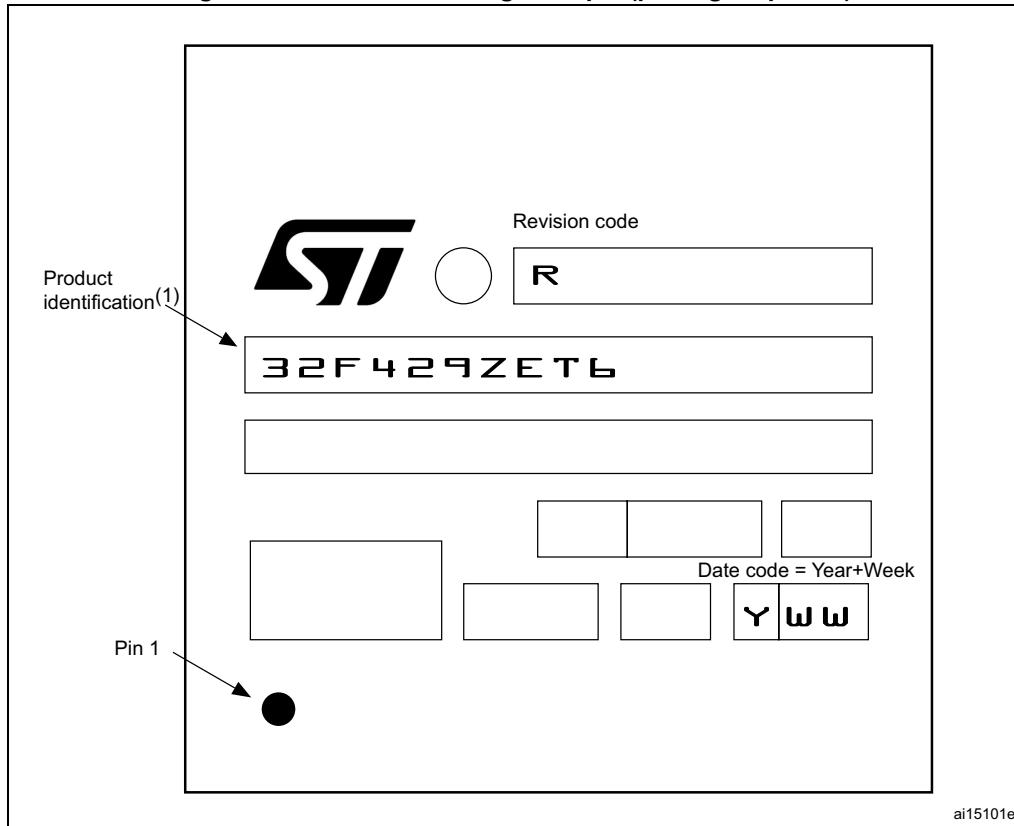
1. Dimensions are expressed in millimeters.

### Device marking for LQFP144

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on assembly location, are not indicated below.

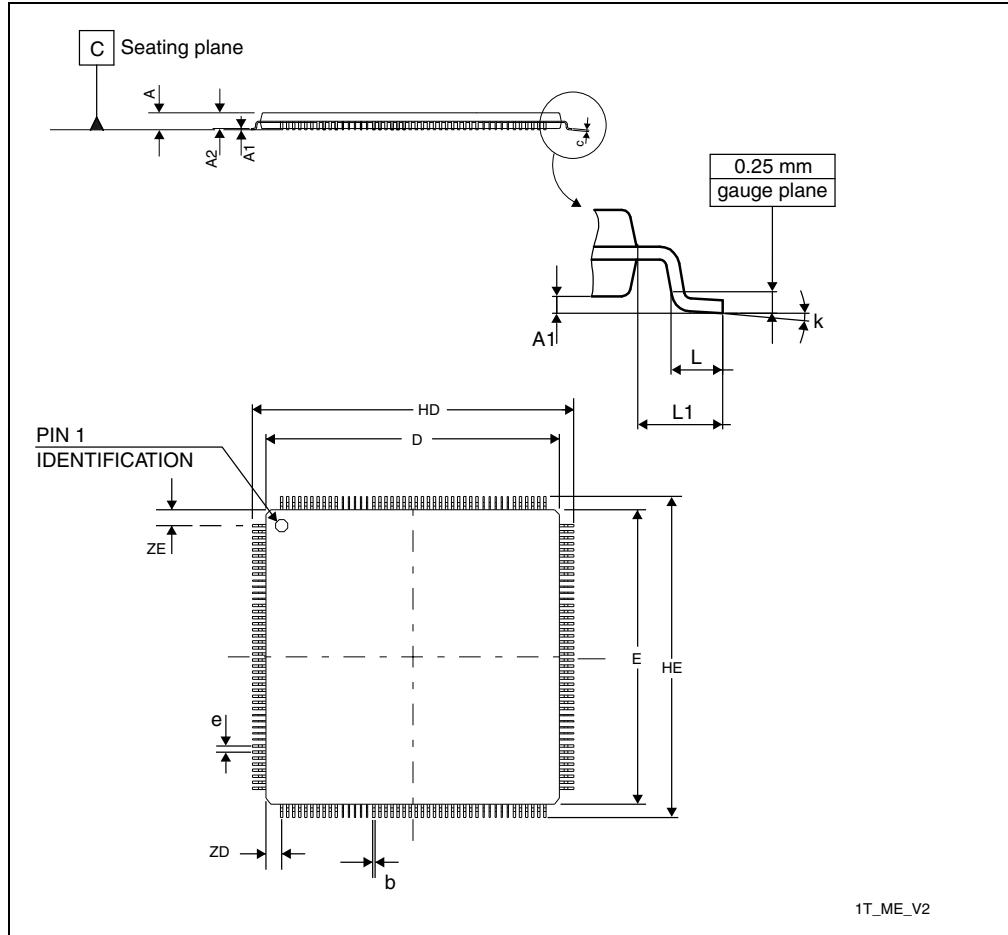
Figure 88. LQFP144 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.4 LQFP176 package information

**Figure 89. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package outline**



1. Drawing is not to scale.

**Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488
HD	25.900	-	26.100	1.0197	-	1.0276

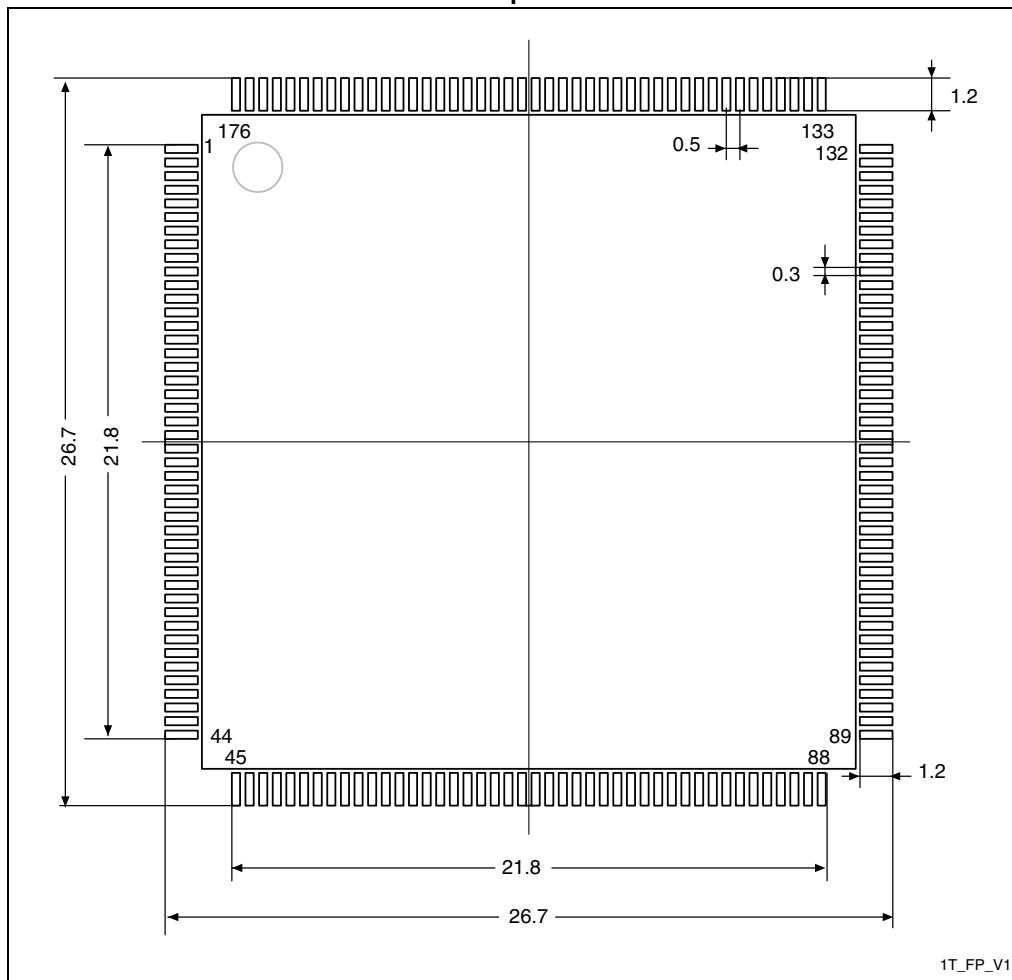
**Table 114. LQFP176 - 176-pin, 24 x 24 mm low-profile quad flat package  
mechanical data (continued)**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L <sup>(2)</sup>	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

**Figure 90. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint**



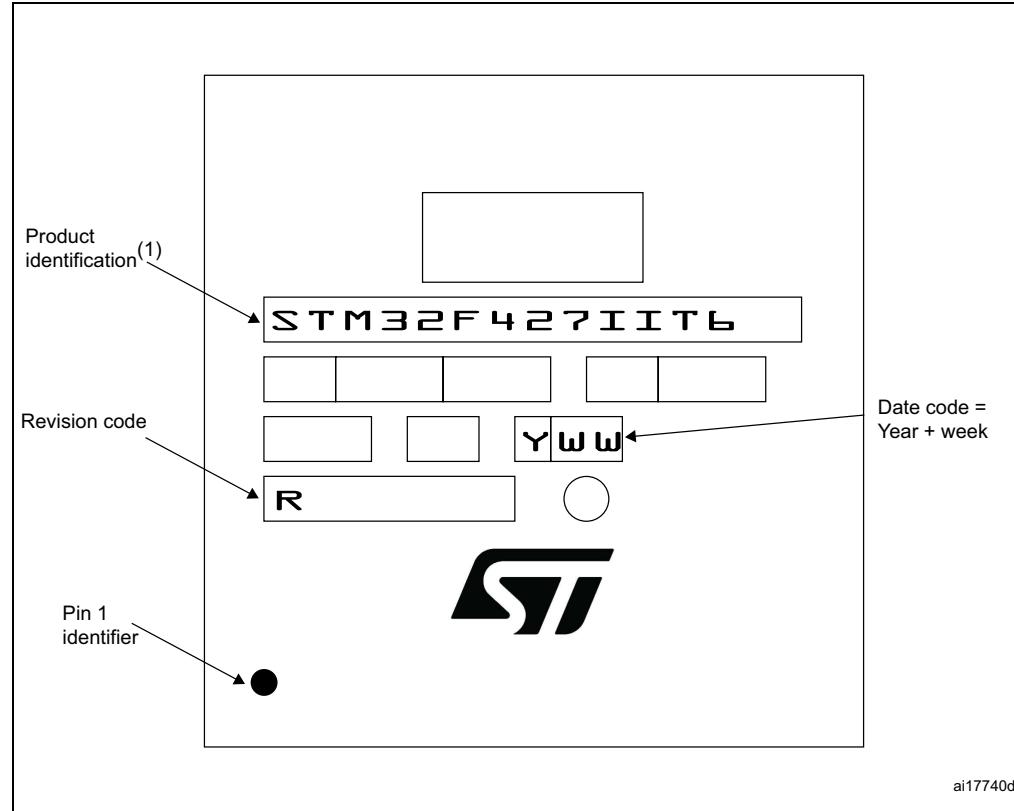
1. Dimensions are expressed in millimeters.

### Device marking for LQFP176

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on assembly location, are not indicated below.

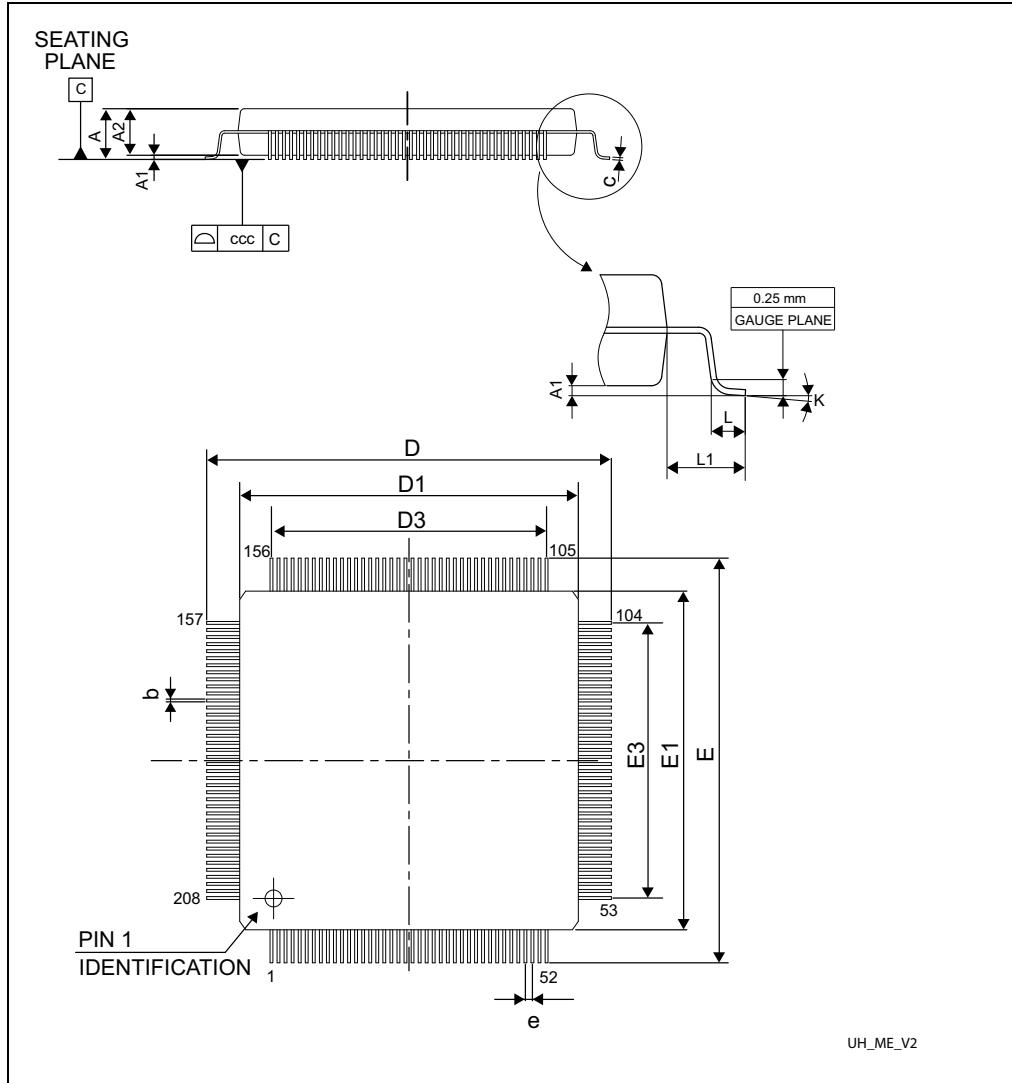
Figure 91. LQFP176 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.5 LQFP208 package information

**Figure 92. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline**



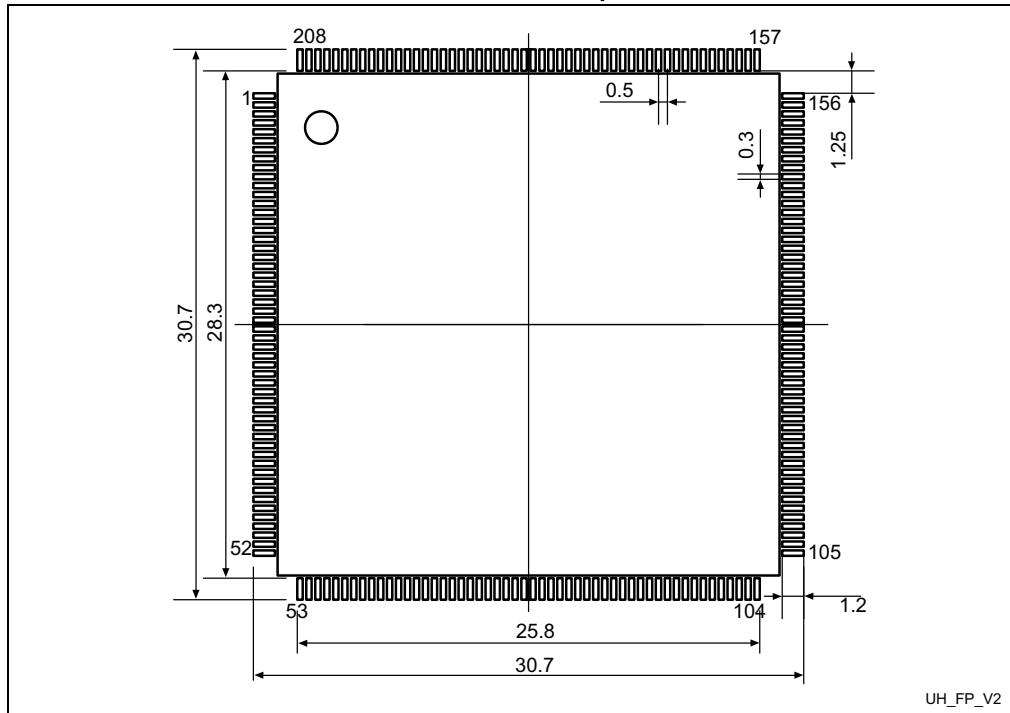
1. Drawing is not to scale.

**Table 115. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	--	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1732	1.1811	1.1890
D1	27.800	28.000	28.200	1.0945	1.1024	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1732	1.1811	1.1890
E1	27.800	28.000	28.200	1.0945	1.1024	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7.0°	0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 93. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package  
recommended footprint



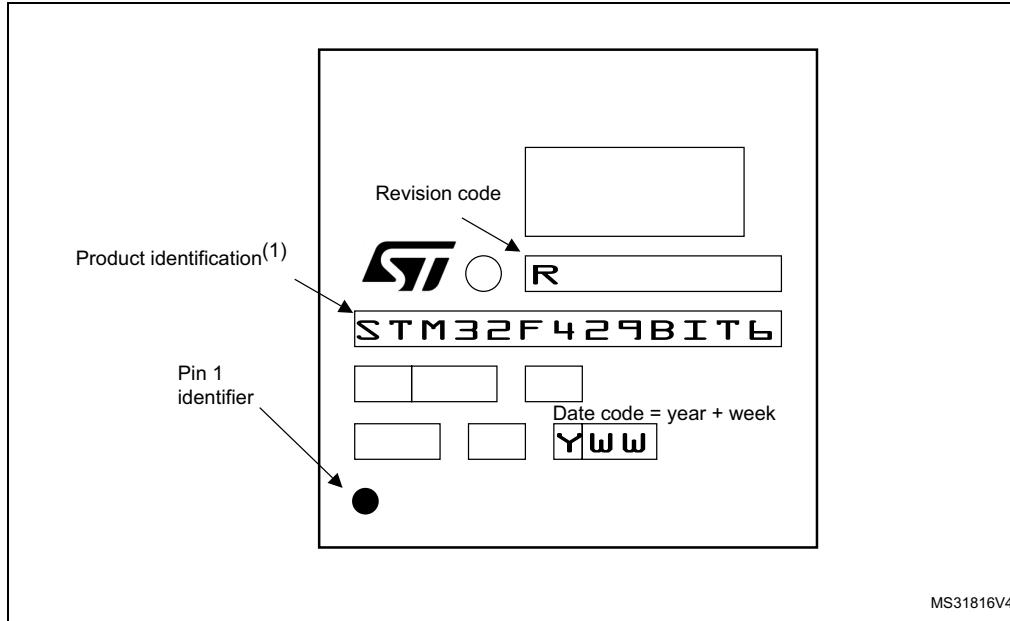
1. Dimensions are expressed in millimeters.

### Device marking for LQFP208

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on assembly location, are not indicated below.

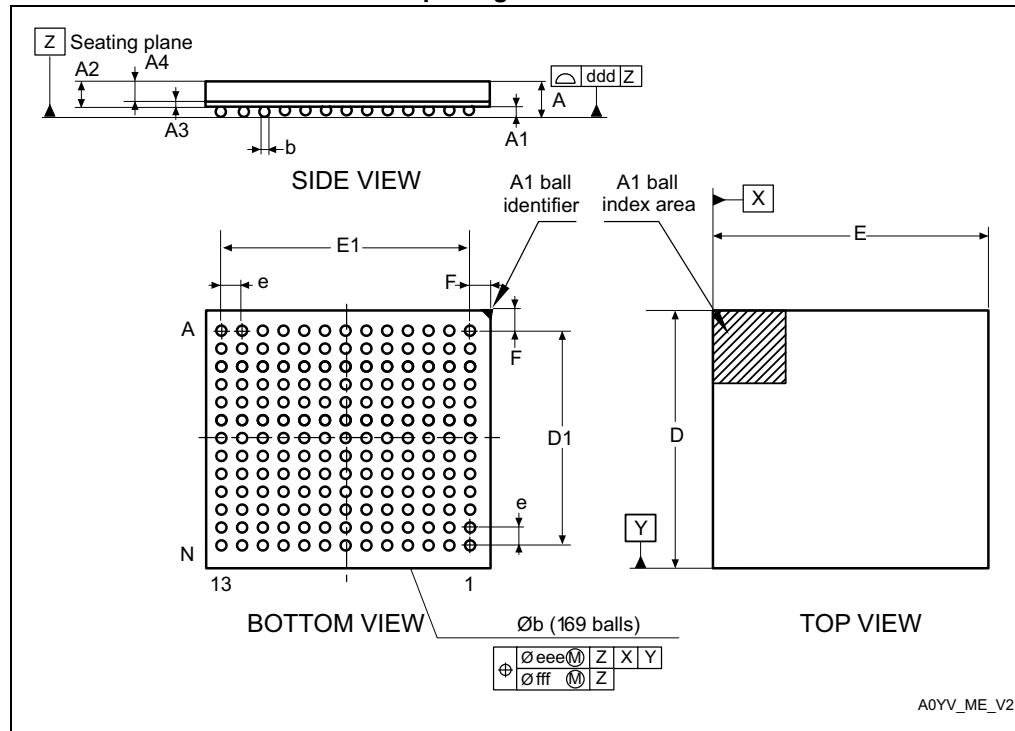
Figure 94. LQFP208 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.6 UFBGA169 package information

**Figure 95.** UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

**Table 116.** UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

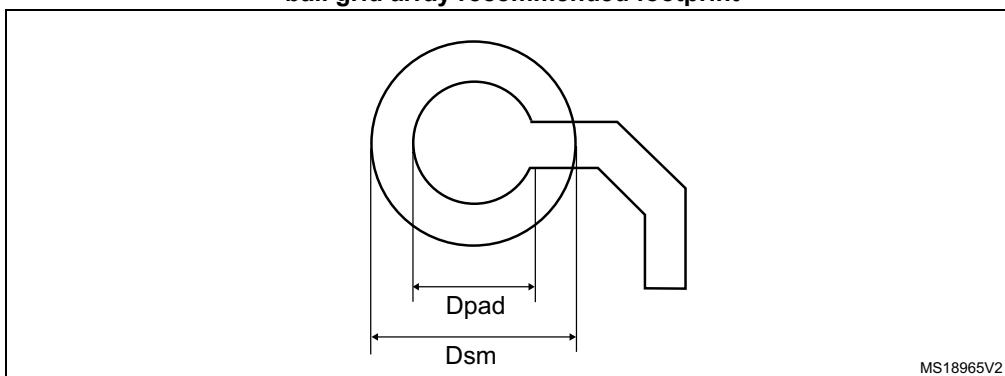
Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-

**Table 116. UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 96. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint**



**Table 117. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

**Note:** Non-solder mask defined (NSMD) pads are recommended.

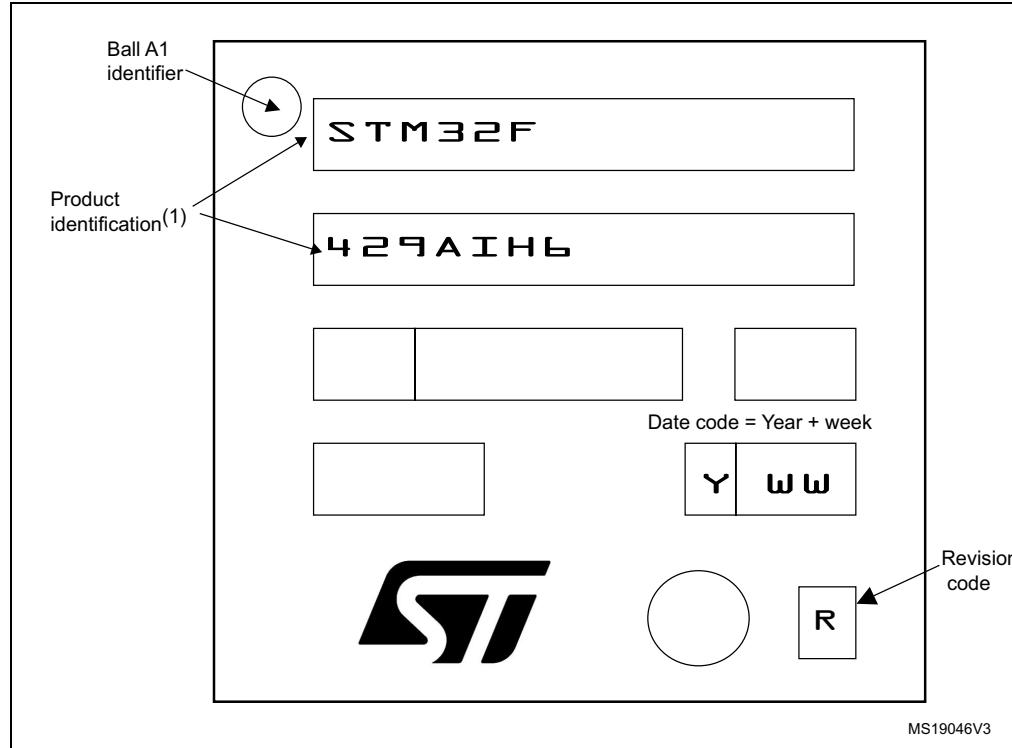
4 to 6 mils solder paste screen printing process.

### Device marking for UFBGA169

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depend on assembly location, are not indicated below.

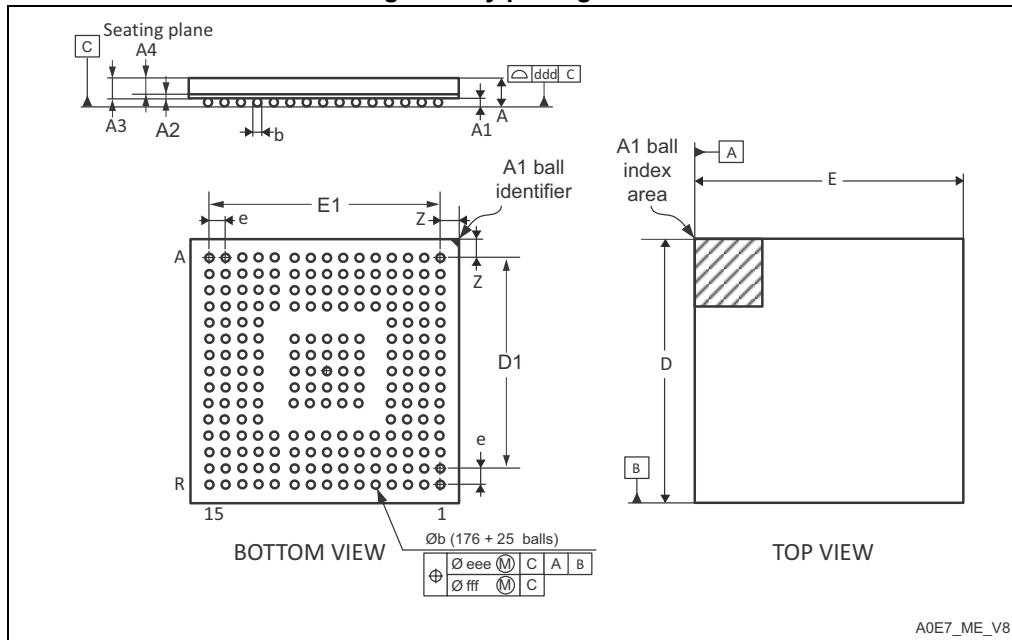
Figure 97. UFBGA169 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.7 UFBGA176+25 package information

**Figure 98. UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline**



1. Drawing is not to scale.

**Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data**

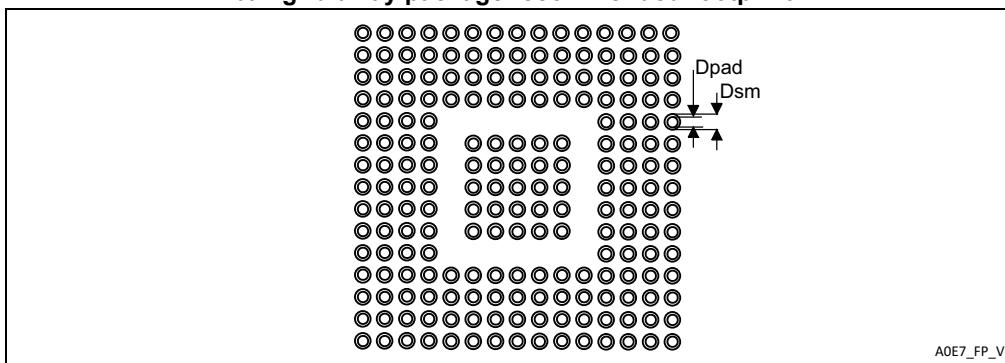
Symbol	millimeters			inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

**Table 118. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)**

<b>Symbol</b>	<b>millimeters</b>			<b>inches<sup>(1)</sup></b>		
	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 99. UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint**



**Table 119. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)**

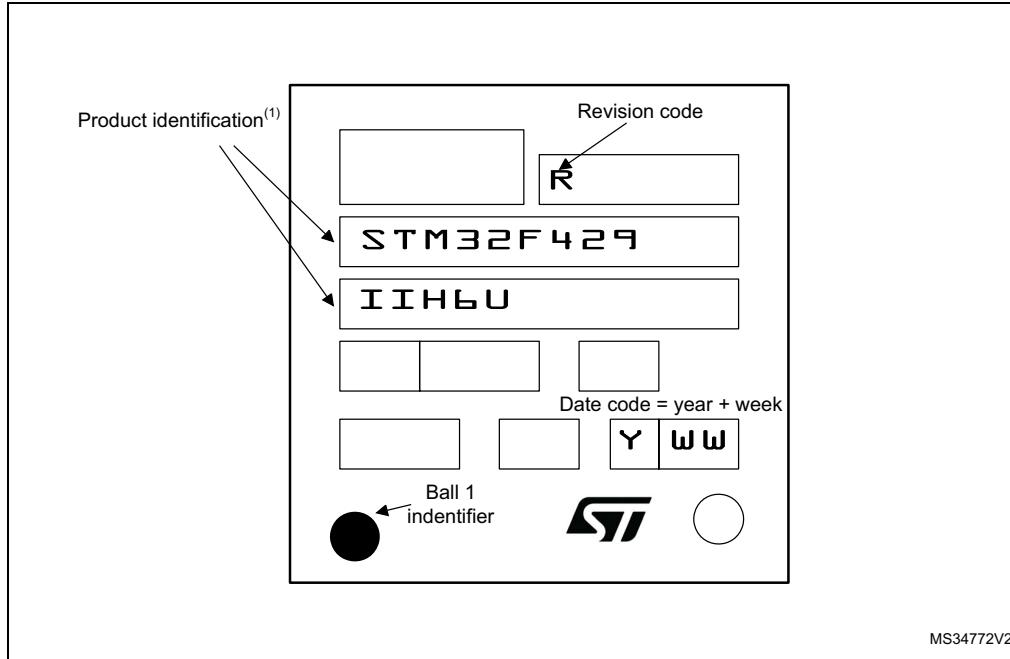
<b>Dimension</b>	<b>Recommended values</b>
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

**Device marking for UFBGA176+25**

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depend on assembly location, are not indicated below.

Figure 100. UFBGA176+25 marking example (package top view)

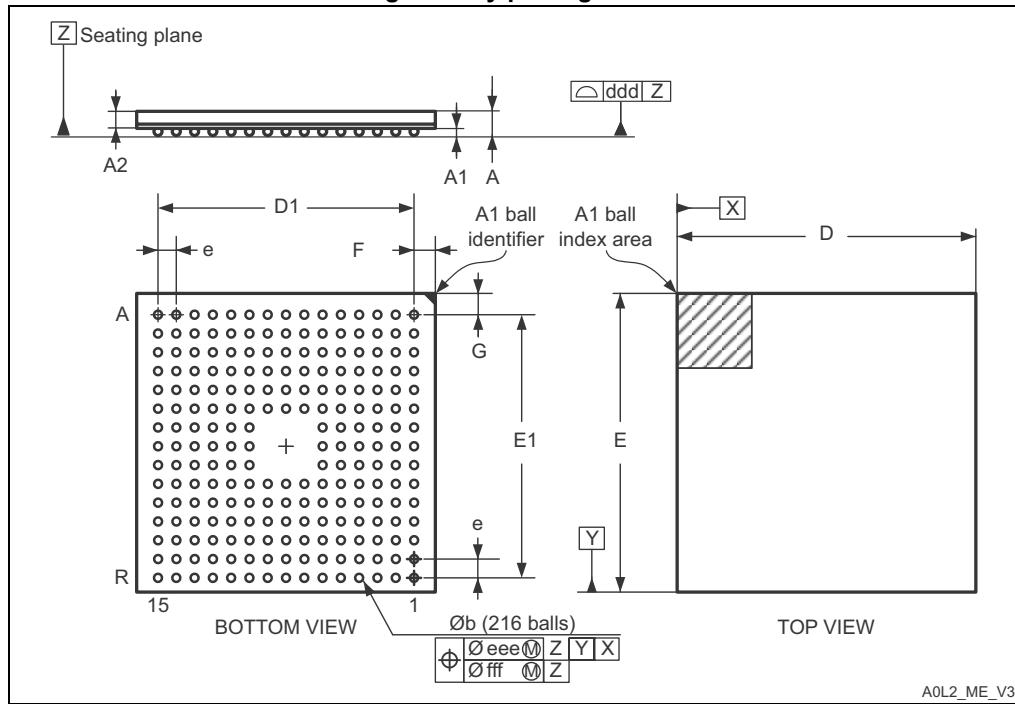


MS34772V2

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.8 TFBGA216 package information

**Figure 101. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline**



1. Drawing is not to scale.

**Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5118	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5118	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039

**Table 120. TFBGA216 - 216 ball 13 × 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data (continued)**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

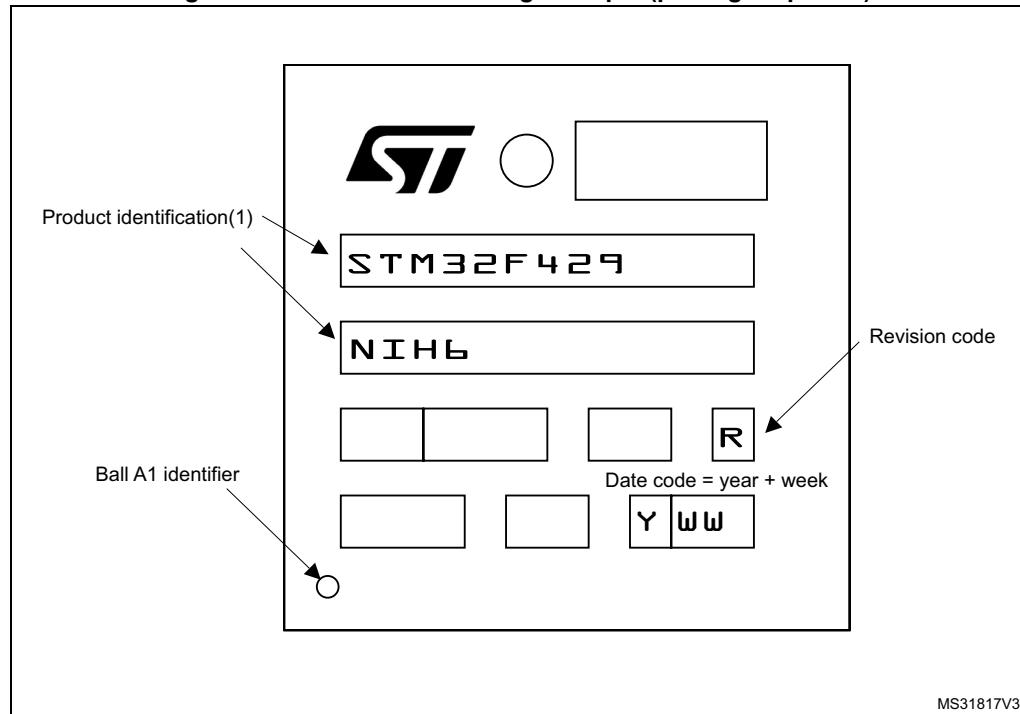
1. Values in inches are converted from mm and rounded to 4 decimal digits.

### Device marking for TFBGA176

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which depend on assembly location, are not indicated below.

**Figure 102. TFBGA176 marking example (package top view)**



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.9 Thermal characteristics

The maximum chip-junction temperature,  $T_J$  max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$  max is the maximum ambient temperature in °C,
- $\Theta_{JA}$  is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$  max is the sum of  $P_{INT}$  max and  $P_{I/O}$  max ( $P_D$  max =  $P_{INT}$  max +  $P_{I/O}$  max),
- $P_{INT}$  max is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$  max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual  $V_{OL}$  /  $I_{OL}$  and  $V_{OH}$  /  $I_{OH}$  of the I/Os at low and high level in the application.

Table 121. Package thermal characteristics

Symbol	Parameter	Value	Unit
$\Theta_{JA}$	<b>Thermal resistance junction-ambient</b> LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	°C/W
	<b>Thermal resistance junction-ambient</b> WLCSP143	31.2	
	<b>Thermal resistance junction-ambient</b> LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	<b>Thermal resistance junction-ambient</b> LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	<b>Thermal resistance junction-ambient</b> LQFP208 - 28 × 28 mm / 0.5 mm pitch	19	
	<b>Thermal resistance junction-ambient</b> UFBGA169 - 7 × 7mm / 0.5 mm pitch	52	
	<b>Thermal resistance junction-ambient</b> UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	
	<b>Thermal resistance junction-ambient</b> TFBGA216 - 13 × 13 mm / 0.8 mm pitch	29	

### Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from [www.jedec.org](http://www.jedec.org).

## 8 Part numbering

**Table 122. Ordering information scheme**

Example:	STM32	F	429	V	I	T	6	xxx
<b>Device family</b>								
STM32 = Arm-based 32-bit microcontroller								
<b>Product type</b>								
F = general-purpose								
<b>Device subfamily</b>								
427= STM32F427xx, USB OTG FS/HS, camera interface, Ethernet								
429= STM32F429xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT								
<b>Pin count</b>								
V = 100 pins								
Z = 143 and 144 pins								
A = 169 pins								
I = 176 pins								
B = 208 pins								
N = 216 pins								
<b>Flash memory size</b>								
E = 512 Kbytes of Flash memory								
G = 1024 Kbytes of Flash memory								
I = 2048 Kbytes of Flash memory								
<b>Package</b>								
T = LQFP								
H = BGA								
Y = WLCSP								
<b>Temperature range</b>								
6 = Industrial temperature range, -40 to 85 °C.								
7 = Industrial temperature range, -40 to 105 °C.								
<b>Options</b>								
xxx = programmed parts								
TR = tape and reel								

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

## Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V<sub>BAT</sub> functionality is no more available and V<sub>BAT</sub> pin should be connected to V<sub>DD</sub>.
- The over-drive mode is not supported.

### A.1 Operating conditions

**Table 123. Limitations depending on the operating power supply range**

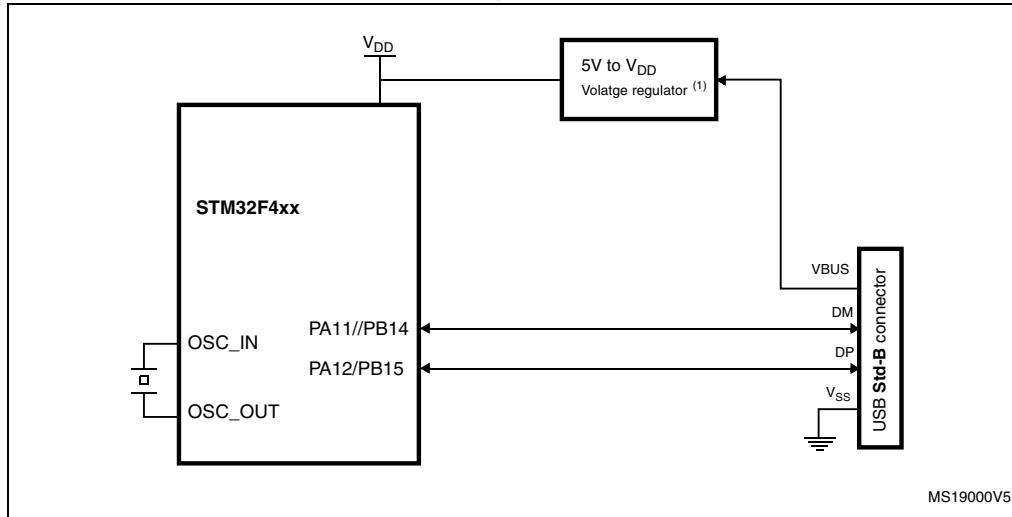
Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ( $f_{Flashmax}$ )	Maximum Flash memory access frequency with wait states <sup>(1)(2)</sup>	I/O operation	Possible Flash memory operations
V <sub>DD</sub> = 1.7 to 2.1 V <sup>(3)</sup>	Conversion time up to 1.2 Msps	20 MHz <sup>(4)</sup>	168 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V<sub>DD</sub>/V<sub>DDA</sub> minimum value of 1.7 V, with the use of an external power supply supervisor (refer to [Section 3.17.1: Internal reset ON](#)).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.

## Appendix B Application block diagrams

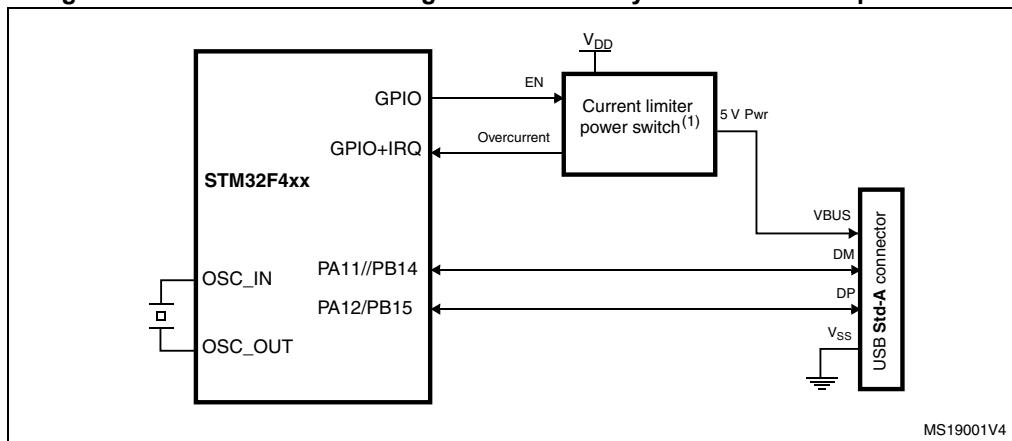
### B.1 USB OTG full speed (FS) interface solutions

**Figure 103. USB controller configured as peripheral-only and used in Full speed mode**

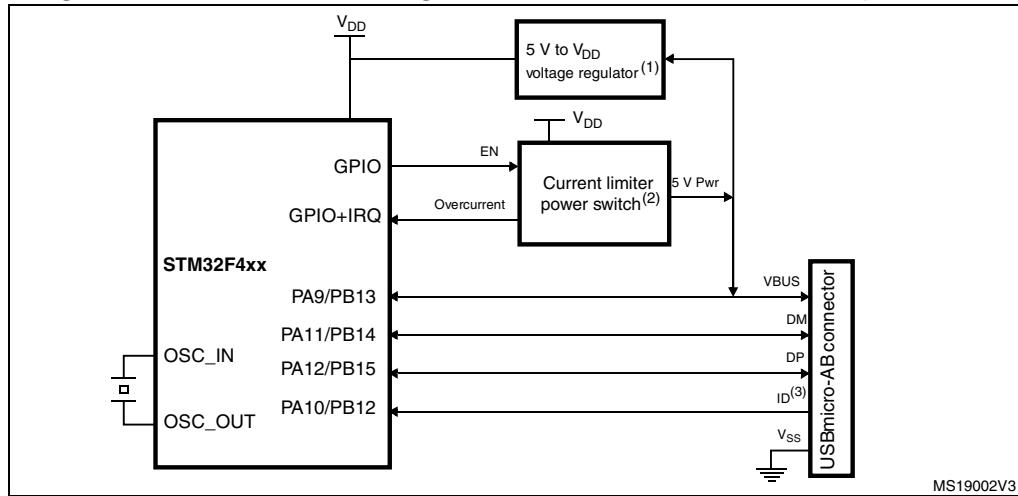


1. External voltage regulator only needed when building a V<sub>BUS</sub> powered device.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

**Figure 104. USB controller configured as host-only and used in full speed mode**



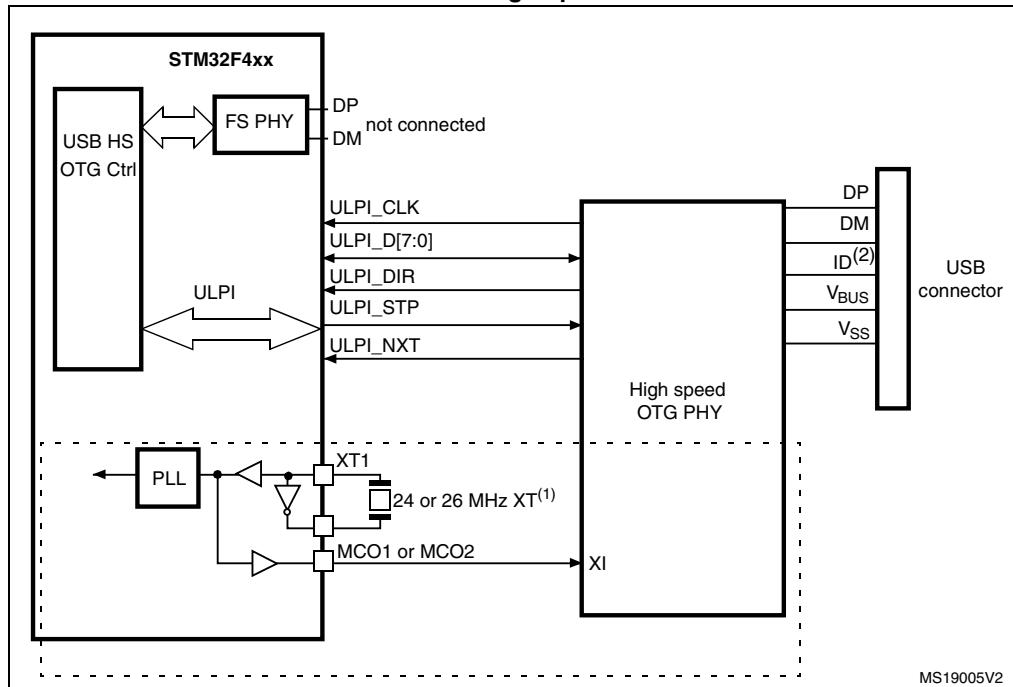
1. The current limiter is required only if the application has to support a V<sub>BUS</sub> powered device. A basic power switch can be used if 5 V are available on the application board.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

**Figure 105. USB controller configured in dual mode and used in full speed mode**

1. External voltage regulator only needed when building a  $V_{BUS}$  powered device.
2. The current limiter is required only if the application has to support a  $V_{BUS}$  powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

## B.2 USB OTG high speed (HS) interface solutions

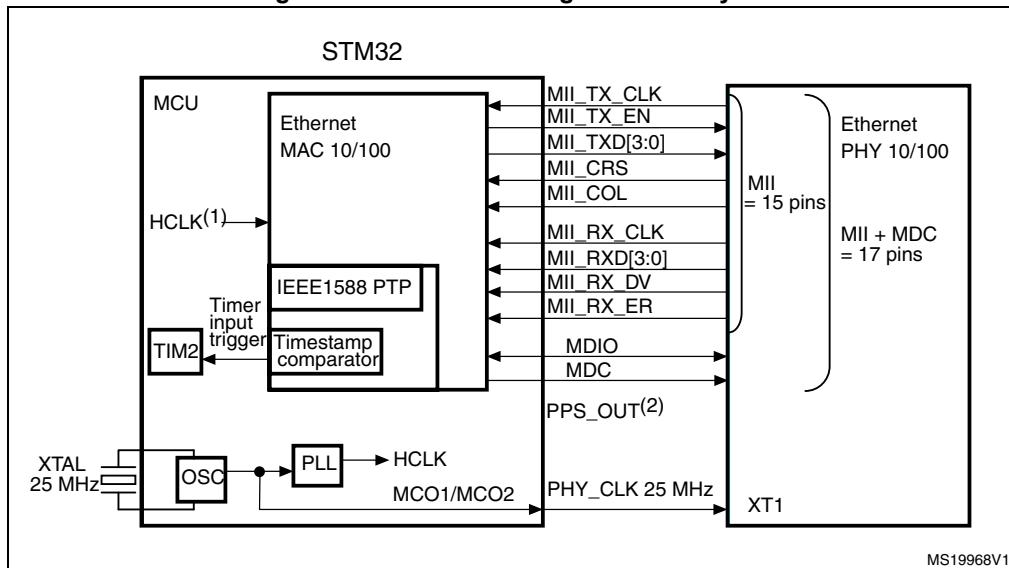
**Figure 106. USB controller configured as peripheral, host, or dual-mode and used in high speed mode**



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F42x with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.

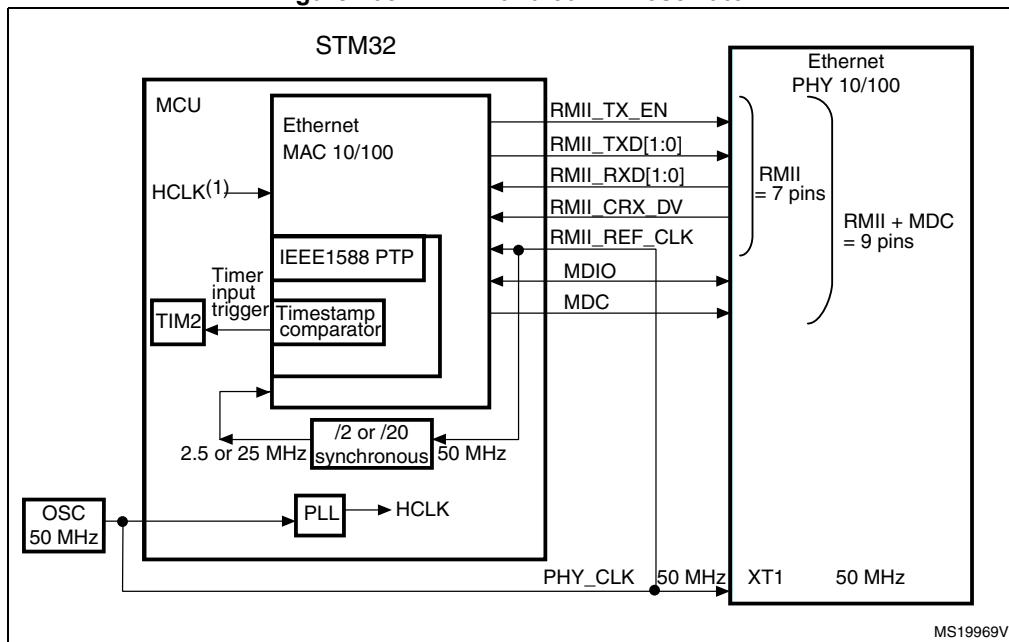
### B.3 Ethernet interface solutions

Figure 107. MII mode using a 25 MHz crystal



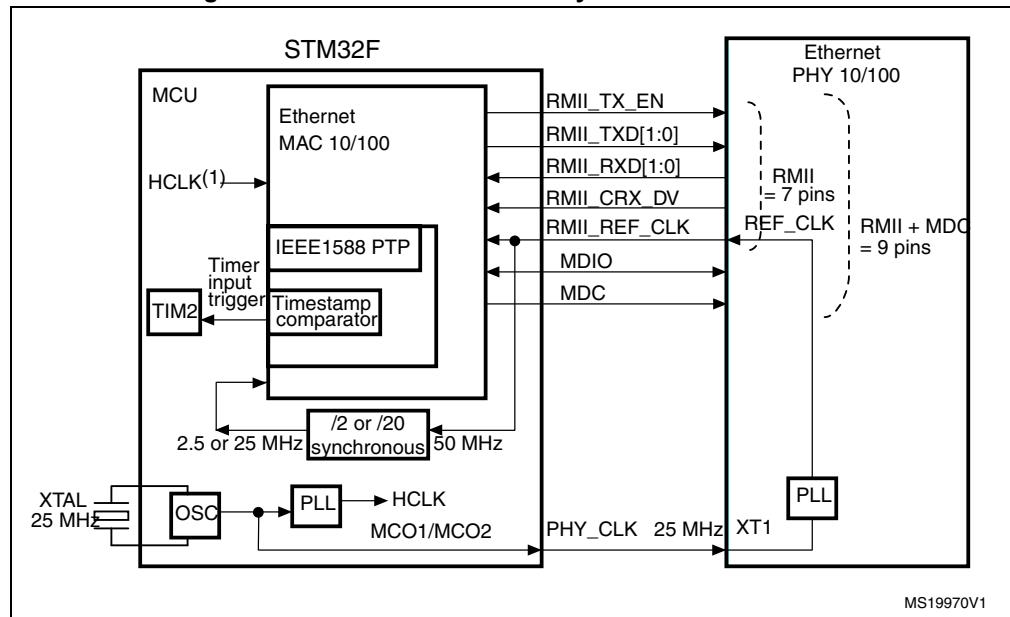
1.  $f_{HCLK}$  must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP optional signal.

Figure 108. RMII with a 50 MHz oscillator



1.  $f_{HCLK}$  must be greater than 25 MHz.

Figure 109. RMII with a 25 MHz crystal and PHY with PLL



1.  $f_{HCLK}$  must be greater than 25 MHz.
2. The 25 MHz (PHY\_CLK) must be derived directly from the HSE oscillator, before the PLL block.

## 9 Revision history

**Table 124. Document revision history**

Date	Revision	Changes
19-Mar-2013	1	<p>Initial release.</p>
10-Sep-2013	2	<p>Added STM32F429xx part numbers and related informations.  <b>STM32F427xx part numbers:</b>  Replaced FSMC by FMC added Chrom-ART Accelerator and SAI interface.  Increased core, timer, GPIOs, SPI maximum frequencies  Updated <a href="#">Figure 8</a>.Updated <a href="#">Figure 9</a>.  Removed note in <a href="#">Section 1: Standby mode</a>.  Updated <a href="#">Figure 18</a>.  Updated <a href="#">Table 10: STM32F427xx and STM32F429xx pin and ball definitions</a> and <a href="#">Table 12: STM32F427xx and STM32F429xx alternate function mapping..</a>  Modified <a href="#">Figure 19: Memory map</a>.  Updated <a href="#">Table 17: General operating conditions</a>, <a href="#">Table 18: Limitations depending on the operating power supply range</a>. Removed note 1 in <a href="#">Table 22: reset and power control block characteristics</a>. Added <a href="#">Table 23: Over-drive switching characteristics</a>.  Updated <a href="#">Section 2: Typical and maximum current consumption</a>, <a href="#">Table 34: Switching output I/O current consumption</a>, <a href="#">Table 35: Peripheral current consumption</a> and <a href="#">Section 3: On-chip peripheral current consumption</a>.  Updated <a href="#">Table 36: Low-power mode wakeup timings</a>.  Modified <a href="#">Section 4: High-speed external user clock generated from an external source</a>, <a href="#">Section 5: Low-speed external user clock generated from an external source</a>, and <a href="#">Section 6.3.10: Internal clock source characteristics</a>.  Updated <a href="#">Table 43: Main PLL characteristics</a> and <a href="#">Table 45: PLL/SAI (audio and LCD-TFT PLL) characteristics</a>.  Updated <a href="#">Table 52: EMI characteristics</a>.  Updated <a href="#">Table 57: Output voltage characteristics</a> and <a href="#">Table 58: I/O AC characteristics</a>.  Updated <a href="#">Table 60: TIMx characteristics</a>, <a href="#">Table 61: I<sup>2</sup>C characteristics</a>, <a href="#">Table 62: SPI dynamic characteristics</a>, <a href="#">Section 7: SAI characteristics</a>.  Updated <a href="#">Table 102: SDRAM read timings</a> and <a href="#">Table 104: SDRAM write timings</a>.</p>

**Table 124. Document revision history**

Date	Revision	Changes
24-Jan-2014	3	<p>Added STM32F429xE part numbers featuring 512 Mbytes of Flash memory and UFBGA169 package.</p> <p>Added LPSDR SDRAM.</p> <p>Changed INTN into INTR in <a href="#">Figure 4: STM32F427xx and STM32F429xx block diagram</a>.</p> <p>Added note 4 in <a href="#">Table 2: STM32F427xx and STM32F429xx features and peripheral counts</a>.</p> <p>Updated <a href="#">Section 3.15: Boot modes</a>.</p> <p>Updated for PA4 and PA5 in <a href="#">Table 10: STM32F427xx and STM32F429xx pin and ball definitions</a>.</p> <p>Added <math>V_{IN}</math> for BOOT0 pins in <a href="#">Table 14: Voltage characteristics</a>.</p> <p>Updated Note 6., added Note 1., and updated maximum <math>V_{IN}</math> for B pins in <a href="#">Table 17: General operating conditions</a>.</p> <p>Updated maximum Flash memory access frequency with wait states for <math>V_{DD} = 1.8</math> to 2.1 V in <a href="#">Table 18: Limitations depending on the operating power supply range</a>.</p> <p>Updated <a href="#">Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM</a> and <a href="#">Table 25: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)</a>.</p> <p>Updated <a href="#">Table 30: Typical current consumption in Run mode, code with data processing running from Flash memory or RAM, regulator ON (ART accelerator enabled except prefetch), VDD=1.7 V</a>, <a href="#">Table 31: Typical current consumption in Run mode, code with data processing running from Flash memory, regulator OFF (ART accelerator enabled except prefetch)</a>, and <a href="#">Table 32: Typical current consumption in Sleep mode, regulator ON, VDD=1.7 V</a>.</p> <p>Updated <a href="#">Table 57: Output voltage characteristics</a>.</p> <p>Updated <a href="#">Table 58: I/O AC characteristics</a>. Added <a href="#">Figure 35</a>.</p> <p>Updated <math>t_{h(SDA)}</math>, <math>t_r(SDA)</math> and <math>t_r(SCL)</math> and added <math>t_{SP}</math> in <a href="#">Table 61: I<sup>2</sup>C characteristics</a>.</p> <p>Updated <math>f_{SCK}</math> in <a href="#">Table 62: SPI dynamic characteristics</a>.</p> <p>Updated <a href="#">Table 70: Dynamic characteristics: USB ULPI</a>.</p> <p>Updated <a href="#">Section 6.3.26: FMC characteristics</a> conditions. Updated <a href="#">Figure 73: SDRAM read access waveforms (CL = 1)</a> and <a href="#">Figure 74: SDRAM write access waveforms</a>. Added <a href="#">Table 103: LPSDR SDRAM read timings</a> and <a href="#">Table 105: LPSDR SDRAM write timings</a>. Updated <a href="#">Table 102: SDRAM read timings</a> and <a href="#">Table 104: SDRAM write timings</a> and added note 2.<a href="#">Table 108: Dynamic characteristics: SD / MMC characteristics</a>.</p>

**Table 124. Document revision history**

Date	Revision	Changes
24-Apr-2014	4	<p>In the whole document, minimum supply voltage changed to 1.7 V when external power supply supervisor is used.</p> <p>Added DCMI_VSYNC alternate function on PG9 and updated note 6. in <a href="#">Table 10: STM32F427xx and STM32F429xx pin and ball definitions</a> and <a href="#">Table 12: STM32F427xx and STM32F429xx alternate function mapping</a>. Added note 2.<a href="#">below Figure 16: STM32F42x UFBGA169 ballout</a>.</p> <p>Changed SVGA (800x600) into XGA1024x768) on cover page and in <a href="#">Section 3.10: LCD-TFT controller (available only on STM32F429xx)</a>.</p> <p>Updated <a href="#">Section 3.18.2: Regulator OFF</a>.</p> <p>Updated signal corresponding to pin L5 in <a href="#">Figure 12: STM32F42x WLCSP143 ballout</a>.</p> <p>Added ACC<sub>HSE</sub> in <a href="#">Table 39: HSE 4-26 MHz oscillator characteristics</a> and ACC<sub>LSE</sub> in <a href="#">Table 40: LSE oscillator characteristics (f<sub>LSE</sub> = 32.768 kHz)</a>.</p> <p>Updated <a href="#">Table 53: ESD absolute maximum ratings</a>.</p> <p>Updated V<sub>IH</sub> in <a href="#">Table 56: I/O static characteristics</a>. Added condition V<sub>DD</sub>&gt;1.7 V in <a href="#">Table 58: I/O AC characteristics</a>.</p> <p>Updated conditions in <a href="#">Table 62: SPI dynamic characteristics</a>.</p> <p>Added Z<sub>DRV</sub> in <a href="#">Table 67: USB OTG full speed electrical characteristics</a></p> <p>Removed note 3 in <a href="#">Table 80: Temperature sensor characteristics</a>.</p> <p>Added <a href="#">Figure 82: LQFP100 marking example (package top view)</a>, <a href="#">Figure 85: WLCSP143 marking example (package top view)</a>, <a href="#">Figure 88: LQFP144 marking example (package top view)</a>, <a href="#">Figure 91: LQFP176 marking (package top view)</a>, <a href="#">Figure 94: LQFP208 marking example (package top view)</a>, <a href="#">Figure 97: UFBGA169 marking example (package top view)</a> and <a href="#">Figure 100: UFBGA176+25 marking example (package top view)</a>.</p> <p>Added <a href="#">Appendix A: Recommendations when using internal reset OFF</a>.</p> <p>Removed Internal reset OFF hardware connection appendix.</p>

**Table 124. Document revision history**

Date	Revision	Changes
19-Feb-2015	5	<p>Update SPI/IS2 in <a href="#">Table 2: STM32F427xx and STM32F429xx features and peripheral counts</a>.</p> <p>Updated LQFP208 in <a href="#">Table 4: Regulator ON/OFF and internal reset ON/OFF availability</a>.</p> <p>Updated <a href="#">Figure 19: Memory map</a>.</p> <p>Changed PLS[2:0]=101 (falling edge) maximum value in <a href="#">Table 22: reset and power control block characteristics</a>.</p> <p>Updated current consumption with all peripherals disabled in <a href="#">Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM</a>. Updated note 1. in <a href="#">Table 28: Typical and maximum current consumptions in Standby mode</a>.</p> <p>Updated <math>t_{WSTOP}</math> in <a href="#">Table 36: Low-power mode wakeup timings</a>.</p> <p>Updated ESD standards and <a href="#">Table 53: ESD absolute maximum ratings</a>.</p> <p>Updated <a href="#">Table 56: I/O static characteristics</a>.</p> <p><b>Section : I2C interface characteristics:</b> updated section introduction, removed Table <a href="#">I2C characteristics</a>, Figure <a href="#">I2C bus AC waveforms and measurement circuit</a> and Table <a href="#">SCL frequency</a>; added <a href="#">Table 61: I2C analog filter characteristics</a>.</p> <p>Updated measurement conditions in <a href="#">Table 62: SPI dynamic characteristics</a>.</p> <p>Updated <a href="#">Figure 51: Typical connection diagram using the ADC</a>.</p> <p>Updated <a href="#">Section : Device marking for LQFP100</a>.</p> <p>Updated <a href="#">Figure 83: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package outline</a> and <a href="#">Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data</a>; added <a href="#">Figure 84: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale recommended footprint</a> and <a href="#">Table 112: WLCSP143 recommended PCB design rules (0.4 mm pitch)</a>. Updated <a href="#">Figure 85: WLCSP143 marking example (package top view)</a> and related note. Updated <a href="#">Section : Device marking for WLCSP143</a>.</p> <p>Updated <a href="#">Section : Device marking for LQFP144</a>.</p> <p>Updated <a href="#">Section : Device marking for LQFP176</a>.</p> <p>Updated <a href="#">Figure 92: LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline</a>; Updated <a href="#">Section : Device marking for LQFP208</a>.</p> <p>Modified UFBGA169 pitch, updated <a href="#">Figure 95: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package outline</a> and <a href="#">Table 116: UFBGA169 - 169-ball 7 x 7 mm 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data</a>; updated <a href="#">Section : Device marking for LQFP208</a>.</p> <p>updated <a href="#">Section : Device marking for UFBGA169</a>, <a href="#">Section : Device marking for UFBGA176+25</a> and <a href="#">Section : Device marking for TFBGA176</a>.</p> <p>Updated Z pin count in <a href="#">Table 122: Ordering information scheme</a>.</p>

**Table 124. Document revision history**

Date	Revision	Changes
17-Sep-2015	6	<p>Updated notes related to the minimum and maximum values guaranteed by design, characterization or test in production.</p> <p>Updated <math>I_{DD\_STOP\_UDM}</math> in <a href="#">Table 27: Typical and maximum current consumptions in Stop mode</a>.</p> <p>Removed note related to tests in production in <a href="#">Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM</a> and <a href="#">Table 26: Typical and maximum current consumption in Sleep mode</a>.</p> <p>Updated <a href="#">Table 41: HSI oscillator characteristics</a>. <a href="#">Figure 31</a> renamed <a href="#">ACCHSI accuracy versus temperature</a> and updated.</p> <p>Updated <a href="#">Figure 38: SPI timing diagram - slave mode and CPHA = 0</a>.</p> <p>Updated <a href="#">Section : Ethernet characteristics</a>.</p> <p>Updated <a href="#">Table 43: Main PLL characteristics</a>, <a href="#">Table 44: PLLI2S (audio PLL) characteristics</a> and <a href="#">Table 45: PLLISAI (audio and LCD-TFT PLL) characteristics</a>.</p> <p>Removed note 1 in <a href="#">Table 75: ADC static accuracy at fADC = 18 MHz</a>, <a href="#">Table 76: ADC static accuracy at fADC = 30 MHz</a> and <a href="#">Table 77: ADC static accuracy at fADC = 36 MHz</a>.</p> <p>Updated <math>t_d(SDCLKL\_Data)</math> and <math>t_h(SDCLKL\_Data)</math> in <a href="#">Table 104: SDRAM write timings</a>.</p> <p>Added <a href="#">Figure 96: UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint</a> and <a href="#">Table 117: UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)</a>.</p> <p>Added <a href="#">Figure 99: UFBGA176+25-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint</a> and <a href="#">Table 119: UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)</a>.</p>
30-Nov-2015	7	<p>Updated <math> V_{SSX} - V_{SSL} </math> in <a href="#">Table 14: Voltage characteristics</a> to add <math>V_{REF-}</math>.</p> <p>Updated <math>t_d(TXEN)</math> and <math>t_d(TXD)</math> minimum value in <a href="#">Table 72: Dynamics characteristics: Ethernet MAC signals for RMII</a> and <a href="#">Table 73: Dynamics characteristics: Ethernet MAC signals for MII</a>.</p> <p>Added <math>V_{REF-}</math> in <a href="#">Table 74: ADC characteristics</a>.</p> <p>Added A1 minimum and maximum values in <a href="#">Table 111: WLCSP143 - 143-ball, 4.521x 5.547 mm, 0.4 mm pitch wafer level chip scale package mechanical data</a>. Updated <a href="#">Figure 86: LQFP144-144-pin, 20 x 20 mm low-profile quad flat package outline</a>.</p> <p>Updated <a href="#">Figure 98: UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline</a> and <a href="#">Table 118: UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data</a>. Updated <a href="#">Figure 101: TFBGA216 - 216 ball 13 x 13 mm 0.8 mm pitch thin fine pitch ball grid array package outline</a> and <a href="#">Table 120: TFBGA216 - 216 ball 13 x 13 mm 0.8 mm pitch thin fine pitch ball grid array package mechanical data</a>.</p>
21-Jan-2016	8	<p>Updated <a href="#">Figure 22: Power supply scheme</a>.</p> <p>Added <math>t_d(TXD)</math> values corresponding to <math>1.71 \text{ V} &lt; V_{DD} &lt; 3.6 \text{ V}</math> in <a href="#">Table 72: Dynamics characteristics: Ethernet MAC signals for RMII</a>.</p>

Table 124. Document revision history

Date	Revision	Changes
18-Jul-2016	9	<p>Updated <a href="#">Figure 1: Compatible board design STM32F10xx/STM32F2xx/STM32F4xx for LQFP100 package</a>.</p> <p>Added mission profile compliance with JEDEC JESD47 in <a href="#">Section 6.2: Absolute maximum ratings</a>.</p> <p>Changed <a href="#">Figure 31 HSI deviation versus temperature to ACCHSI versus temperature</a>.</p> <p>Updated <math>R_{LOAD}</math> in <a href="#">Table 85: DAC characteristics</a>.</p> <p>Added note 2. related to the position of the 0.1 <math>\mu</math>F capacitor below <a href="#">Figure 37: Recommended NRST pin protection</a>.</p> <p>Updated <a href="#">Figure 40: SPI timing diagram - master mode</a>.</p> <p>Added reference to optional marking or inset/upset marks in all package device marking sections. Updated <a href="#">Figure 85: WL CSP143 marking example (package top view)</a>, <a href="#">Figure 88: LQFP144 marking example (package top view)</a>, <a href="#">Figure 91: LQFP176 marking (package top view)</a>, <a href="#">Figure 94: LQFP208 marking example (package top view)</a>.</p> <p>Updated <a href="#">Figure 98: UFBGA176+25 - ball 10 x 10 mm, 0.65 mm pitch ultra thin fine pitch ball grid array package outline</a> and <a href="#">Table 118: UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array mechanical data</a>.</p>
19-Jan-2018	10	<p>Updated Arm wordmark and added Arm logo in <a href="#">Section 2: Description</a>.</p> <p>Updated LDC-TFT feature on cover page.</p> <p>Updated <a href="#">Table 24: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM</a> and <a href="#">Table 26: Typical and maximum current consumption in Sleep mode</a>.</p> <p><math>R_{ADC}</math> minimum value added in <a href="#">Table 74: ADC characteristics</a>.</p> <p>LTDC clock output frequency changed to 83 MHz in <a href="#">Table 107: LTDC characteristics</a>.</p>

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