Dahua Feng

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Education

School of Electronics Engineering and Computer Science, Peking University 2020.9 - Present
Major in Information and Computing Sciences

- **GPA:** 3.618/4.000

Research Experience

Research Assistant for Prof. Zhi Yang 2022.3 - 2023.1
School of Computer Science, Peking University

- Prof. Zhi Yang now works as an associate professor at School of Computer Science of Peking University. Our project is on efficient parallel systems for large-scale data analytic, specifically on the compiler for deep neural networks.
- Our project focuses on the schedule of the ops and resources allocation to get more speedup for the computation of neural networks. Primarily, we try to use a kind of genetic algorithm based on BFS and dynamic programming to schedule the ops. Currently, we mainly focus on the resources allocation based on some existed schedulers.
- I learnt about the latest achievements in this field and some basic instruments about the research including TVM, IOS, Ansor, Rammer and Roller, and did reports on them respectively.
- I analyzed part of the source code of Roller which is about its construction policy, and part of the source code of TVM which is about the time evaluation. Also, I did reports on them respectively.
- I gathered and read some papers on neural networks and summarized the structures of them, so as to provide the benchmarks for our project.
- I read the related part of source code of IOS and added the functionality of resources allocation for it. I analyzed the results and compared the performances between them.

Skills

Programming Languages & Softwares: C, C++, Python, LaTeX, Markdown, Linux
Languages: Mandarin (native), English (CET-6: 579/710)

Coursework

Introduction to Computer Systems

- This course is from the course in CMU with the same name, and in this course I completed seven labs (except the proxy lab) which are similar to those in CMU. Among them the shell lab and malloc lab have the heaviest workload.
- In the shell lab, I am required to complete a tiny shell, which can support some basic jobs management, which is related to processes management and signals. Here is my code of this lab.
- In the malloc lab, I am required to complete a malloc function, and the utility and throughput should both reach the standard. Here is my code of this lab.

Operating System

- In this course, I completed the labs of MIT6.S081 except the last one, networking.
- These labs are based on a naive operating system structure xv6, requiring me to improve and perfect it by implementing many functionalities such as the lazy alloction, COW, mmap and so on step by step.

Computer Networks

- In this course, I completed four labs for the application layer, the transport layer, the network layer and the data link layer respectively. The lab for the transport layer has the heaviest workload.
- In this lab, I am required to complete a kind of reliable transport like TCP but based on the UDP socket. I have to implement a function in the sender that can divide a long message into some short data grams and send them to another socket reliably and a function in the receiver to receive and dispose the data grams properly. Here is the code of this lab.

Computer Architectures

- In this course, I completed six labs using gem5 simulator. These labs are about the CPU, cache, branch predictor and so on. The work of these labs includes data collection and analysis, coding and writing paper summaries. The last two labs have the heaviest workload relatively.
- In these two labs, I am required to read a paper, write a brief summary for it, reproduce the key idea of it and evaluate my own implementation. One paper is on the branch prediction, and the other is on the cache prefetching. Here are the two papers:
  Jiménez, Daniel A. and Calvin Lin. "Dynamic branch prediction with perceptrons." *Proceedings HPCA Seventh International Symposium on High-Performance Computer Architecture* (2001): 197-206.

  Khan, Samira Manabi et al. "Sampling Dead Block Prediction for Last-Level Caches." *2010 43rd Annual IEEE/ACM International Symposium on Microarchitecture* (2010): 175-186.