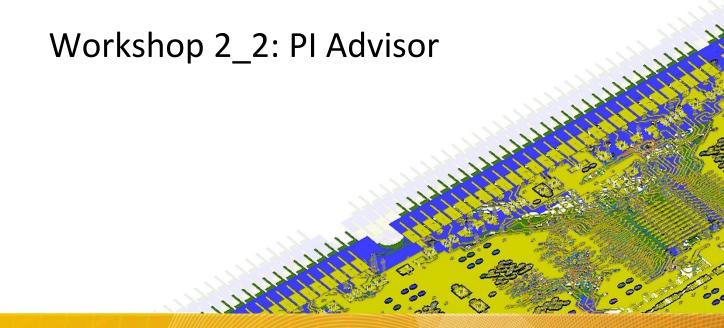


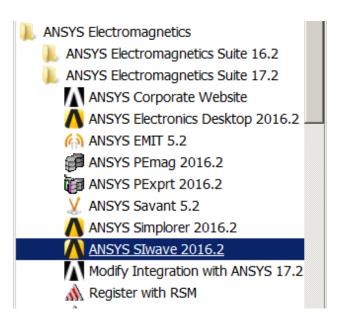
Slwave for Power Integrity Analysis



Opening or Importing a Project

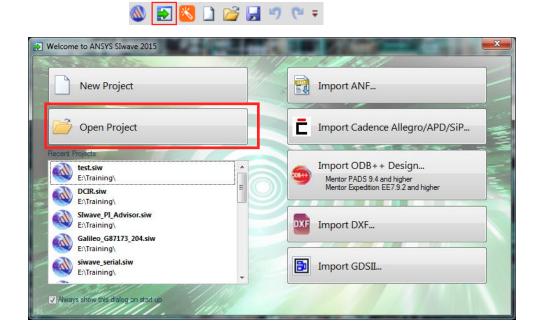
Starting Slwave

- To launch SIwave, click the Microsoft Start Button > ALL Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 17.2.
- Select the ANSYS SIwave 2016 executable.



Open a Slwave Project

- Select the Open Project button
 - Browse for the file: **Pl.siw**,
 - Click the Open button

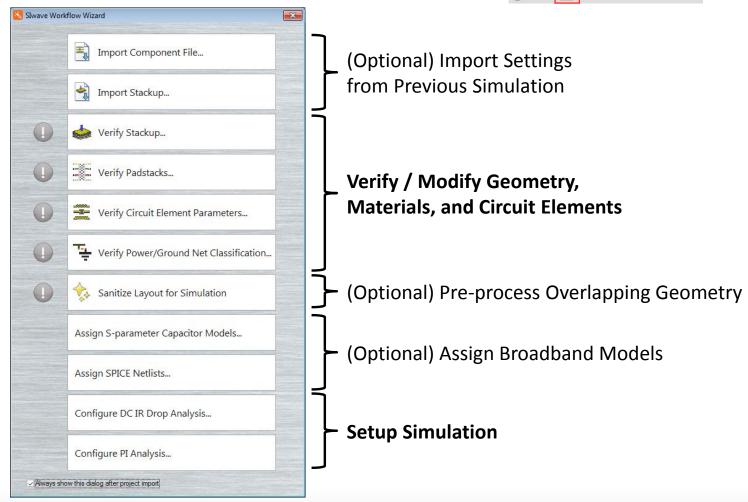




Slwave Workflow Wizard Dialogue

Opening the Workflow Wizard

• In the Common Functions menu, choose the **SIwave Workflow Wizard Dialogue**.



Verify Stackup

Color

Name

Type

Apply

Material

As Is

As Is

DIELECTRIC

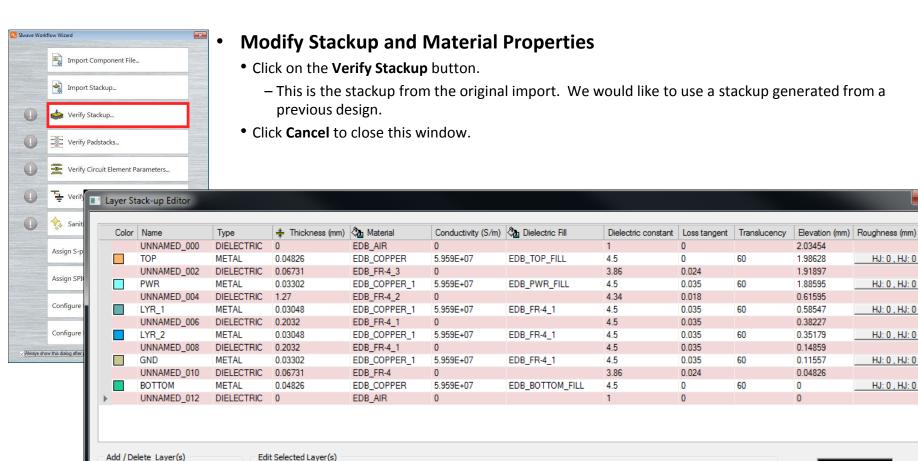
Add Above Selected Layer

Add Below Selected Laver

Delete Selected Layers

DIELECTRIC ▼

4



Edit Material Properties

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Dielectric Fill

Translucency

As Is

Thickness

Roughness

Units mm

Update

Update

Update

Update

HJ: 0, HJ: 0

HJ: 0 , HJ: 0

HJ: 0 , HJ: 0

HJ: 0, HJ: 0

HJ: 0, HJ: 0

HJ: 0, HJ: 0

Cancel

Update

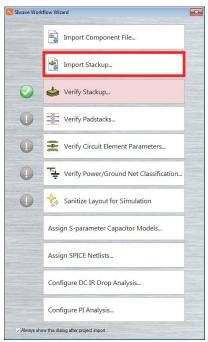
Update

Update

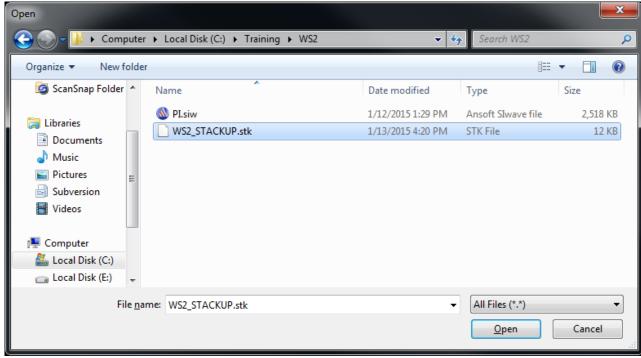
Update

mm

Import Stackup



- Importing a Stackup from a Previous Design
 - Click the **Import Stackup** button.
 - Locate WS2_STACKUP.stk in the same directory as Pl.siw.
 - Click **Open** to apply the stackup.

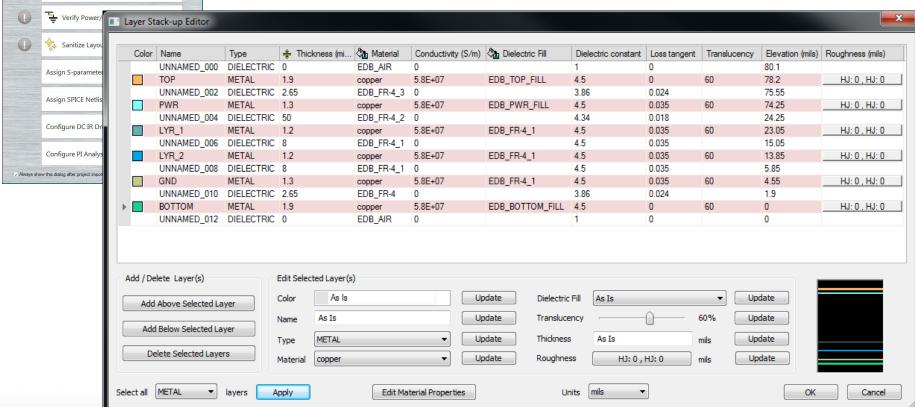


Verify Stackup

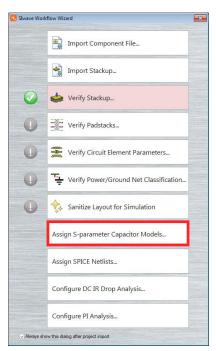


6

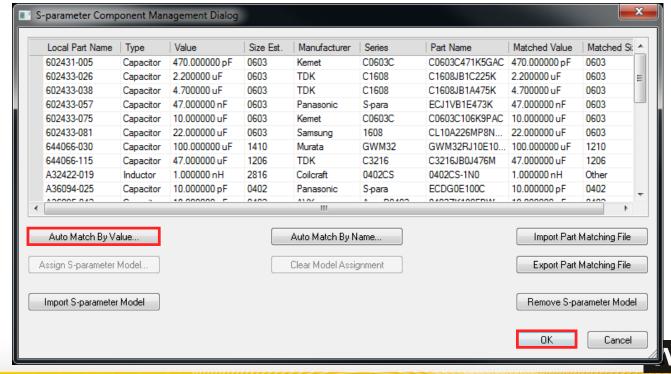
- Verify Imported Stackup
 - Click on the **Verify Stackup** button once again.
 - Importing the stackup from the last step has modified the material for metal layers. Importing the stackup can modify any and all parameters in this window.
 - Verify that copper is assigned to all of the metal layers.
 - Click Cancel to close this window.



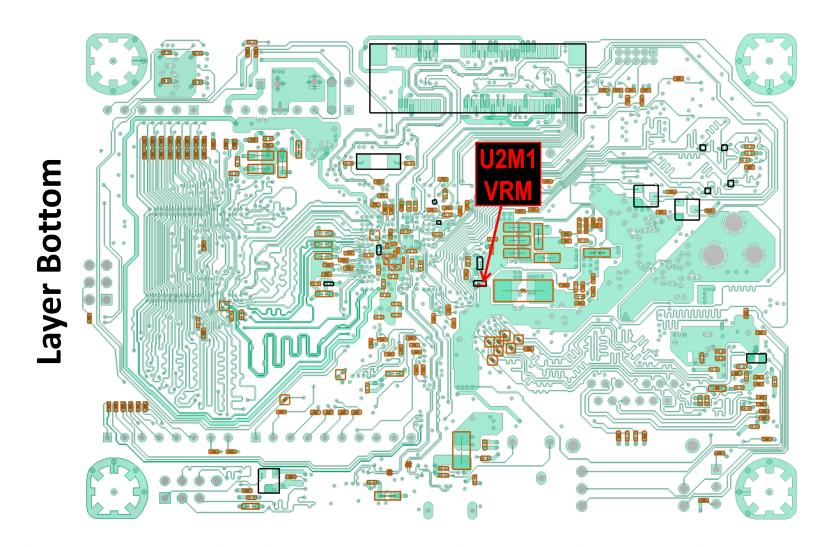
Assign S-parameter Capacitor (and Inductor) Models



- Assigning Broadband Models to Capacitor Locations
 - For this exercise, we will assume that the Padstacks, Circuit Elements, and Power/Ground Net Classification has been handled properly during import.
 - Click on the Assign S-parameter Capacitor Models button.
 - Click Auto Match By Value.
 - The auto-match function looks at the original capacitance value and the estimated size and attempts to choose a suitable part from Slwave's vendor library. The vendor library includes over 20,000 capacitor and inductor models directly from 12 of the major vendors.
 - Click **OK** to commit changes.



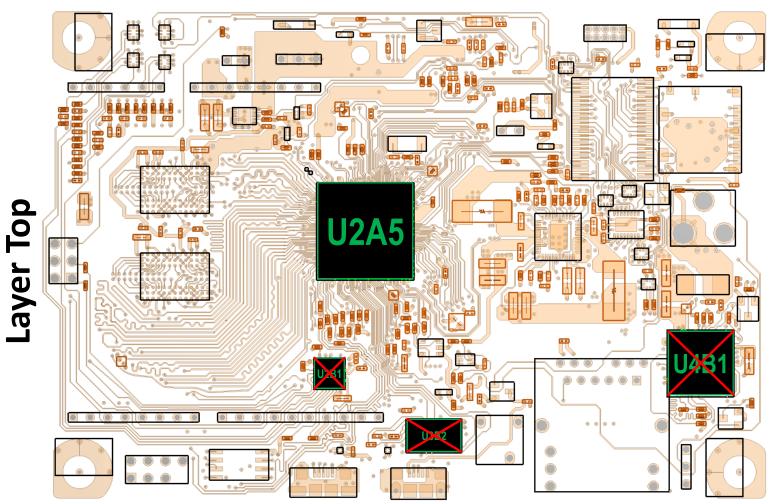
PI Simulation Ports





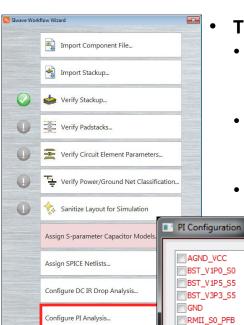
PI Simulation Ports

Single active device to simplify simulation results.



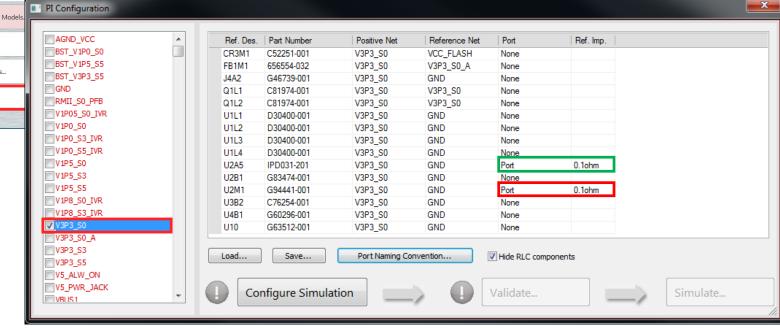


Configure PI Analysis

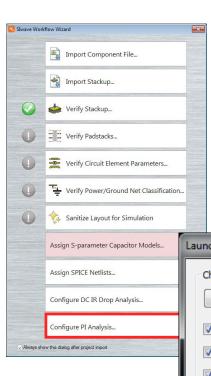


Always show this dialog after project import

- Table Driven Schematic
 - Place a check mark next to net V3P3_S0.
 - This displays any active devices connected to this net.
 - Check and uncheck **Hide RLC components** to see passive devices.
 - Assign a Port to U2A5 and U2M1.
 - This was chosen only for simplification. It is possible to create ports for any and all components.
 - The default reference impedance is 0.10hm to resolve very small impedances.
 - Click **Configure Simulation**.



Validation Check



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Validation Check

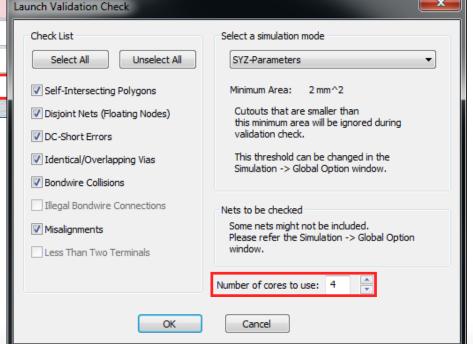
- The validation check analyzes the entire setup to ensure it is ready for simulation.
- Increase the **Number of cores to use** for this validation step by pressing the up button.
- Click **OK** to start the validation check.

Validation Check Results

The Validation Check can automatically repair certain geometry problems such as disjoint nets and

overlapping vias.

Press OK to close this window and apply any Auto Fix.



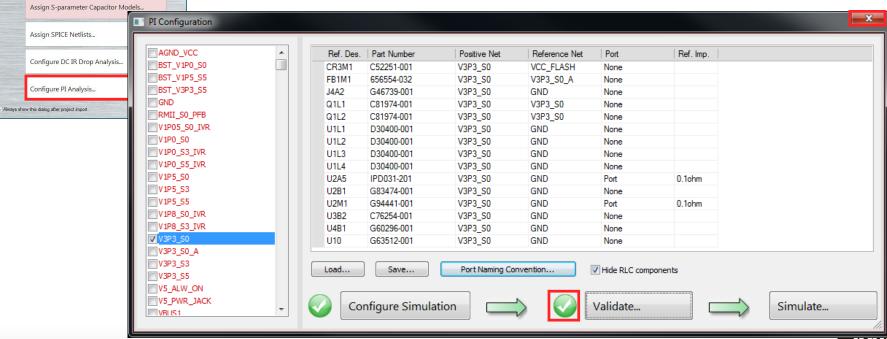
Validation Check Results Errors Self-Intersecting Polygons: - Circular Loops: Auto Fix - Others: Point-Connections: 0 Auto Fix Disjoint Nets: DC-shorted Errors: Identical/Overlapping Vias: 0 Auto Fix Traces-Inside-Traces Errors: 0 Auto Fix Collisions of Bondwires: Illegal Connections of Bondwires: Identical Bondwires: 0 Auto Fix Reversed Bondwires: 0 Auto Fix Floating Nodes: 0 Auto Fix Zero Via Plating: Nets With Less Than 2 Terminals: Warnings 1 Auto Fix Misalignments (Planes/Traces/Vias): Bondwires Misaligned With Die Pads: 0 Auto Fix Pins Shared By Multiple Pin Groups: 0 Auto Fix OK Cancel

Configure PI Analysis, cont.



Simulation

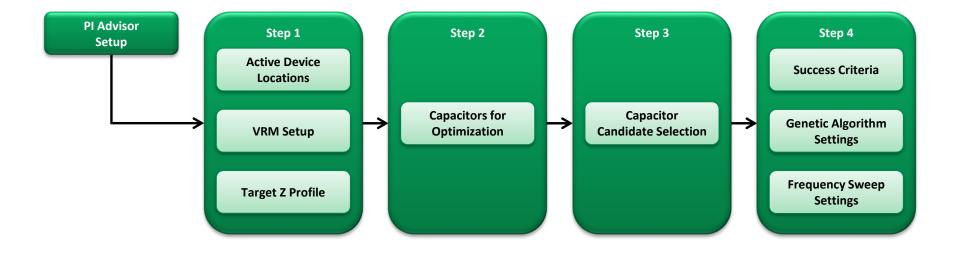
- The check mark next to validation check will continue to display as a warning sign until it detects zero warnings or errors. Warnings will not stop simulation progress, but errors most likely will.
- (Optional) Run the validation check again to get a green check mark next to the Validate button.
- At this point, it is possible to run the SYZ sweep to obtain S-parameters. The results obtained here can be exported in touchstone or Full Wave SPICE formats and run in a circuit simulation. This exercise, however, is geared towards optimizing capacitor selection.
- Click the X in the upper right hand corner to close this window.
- Both the PI Configuration and SIwave Workflow Wizard windows will close.



NVSYS

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PI Advisor Workflow Diagram

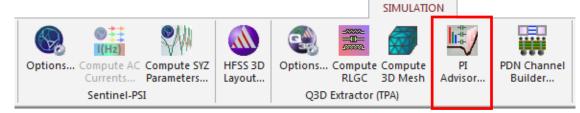




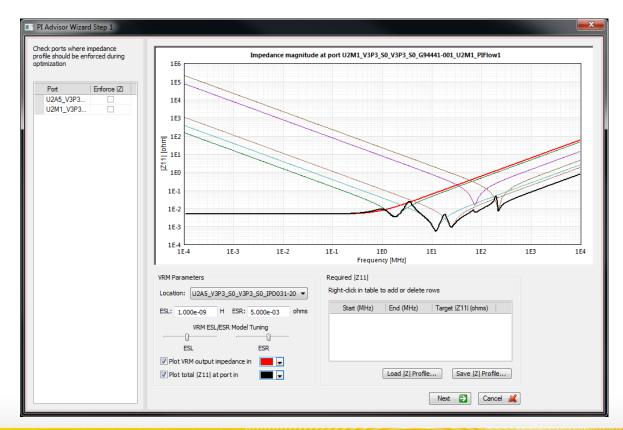
Launching PI Advisor

Starting PI Advisor

- Click on the **Simulation** menu tab.
- Click the PI Advisor button to start PI Advisor.

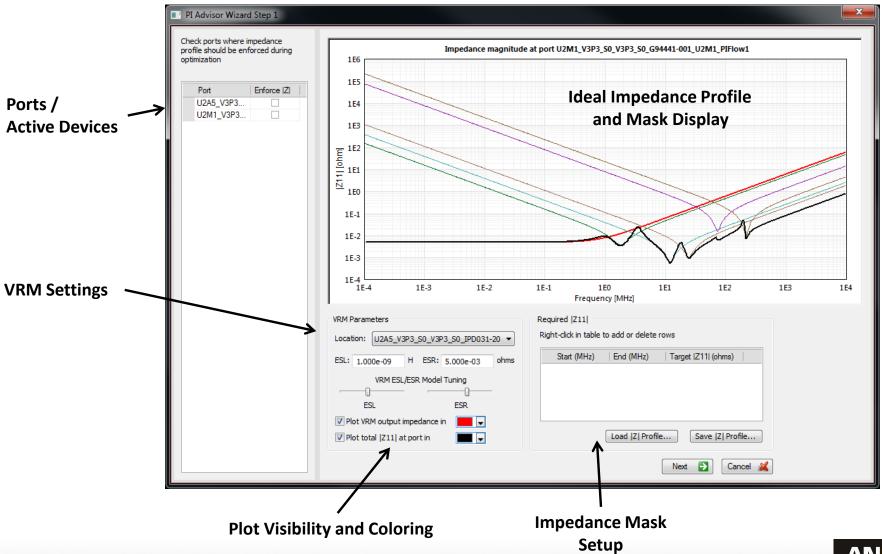


• This will put you into the first step of PI Advisor.





PI Advisor: Step 1



Choose Ports / Active Devices to Optimize

- Click the Enforce |Z| check box next to V3P3_S0_IPD031-201_U2A5_PIFlow1.
 - This is indicated by the ▶ graphic next to the port name
- Do not check the box for U2M1.

VRM Setup

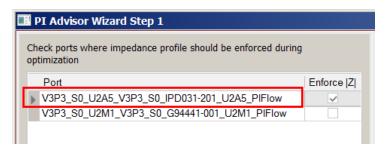
16

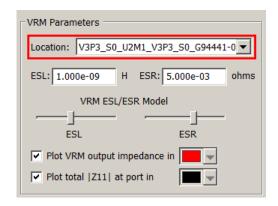
- Change the Location of the VRM to U2M1.
 - ESL and ESR can be modified to match the VRM parameters.
 - The graph will update indicating the shift in impedance.

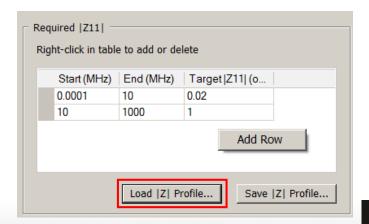
Impedance Mask Setup

- Click the Load |Z| Profile button.
- Choose the **Z_target.zprof** file and click **OK**.
- Alternatively, it is possible to right-click and add rows.
- Click the Next button to proceed to Step 2.







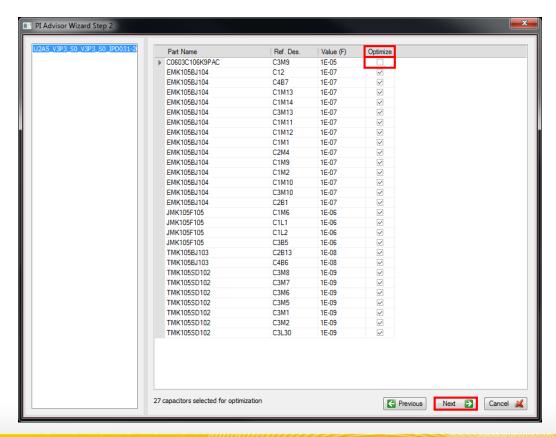




PI Advisor: Step 2

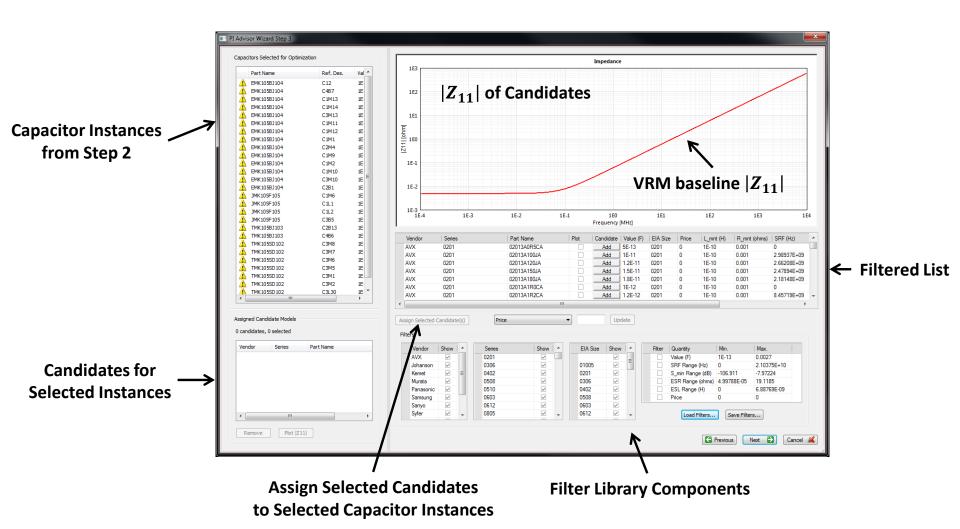
Choosing Capacitors to Optimize

- Click on the **Optimize** column header to place a check mark next to all capacitor instances.
- Uncheck the Optimize check box next to Reference Designator C3M9.
 - This is a 0603 part that we do not want to optimize. The remainder are 0402 parts.
- Click the **Next** button to proceed to Step 3.



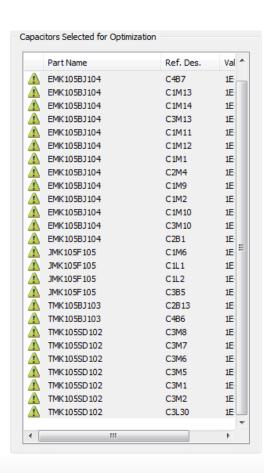


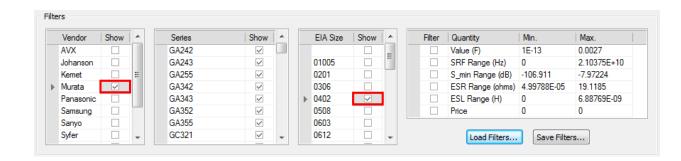
PI Advisor: Step 3



Potential Candidate Filter

- Select only Murata as a Vendor
- Select only **0402** for the **EIA Size**



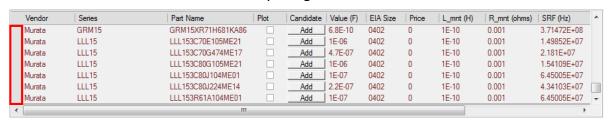


Select Capacitor Instances

Select all Capacitor Instances by using Shift+Click or Ctrl+Click. The warning icon indicates
that there are no candidates assigned to the capacitor instances.

Select Candidates

Select all filtered candidate instances by using Shift+Click or Ctrl+Click in the row indicator.



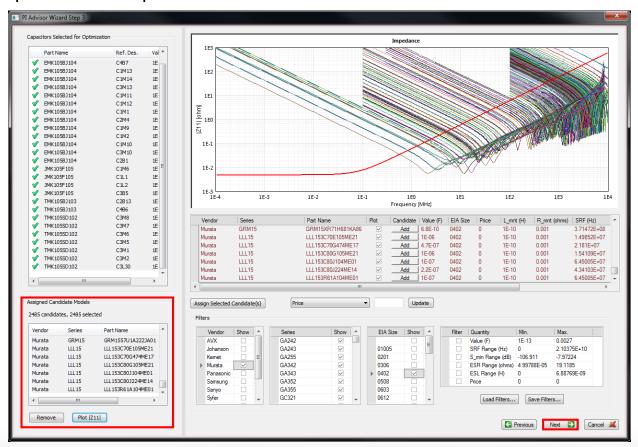
Assign Selected Candidate(s)

 Click the Assign Selected Candidates button with both Capacitor Instances and Selected Candidates to populated the Assigned Candidate Models.



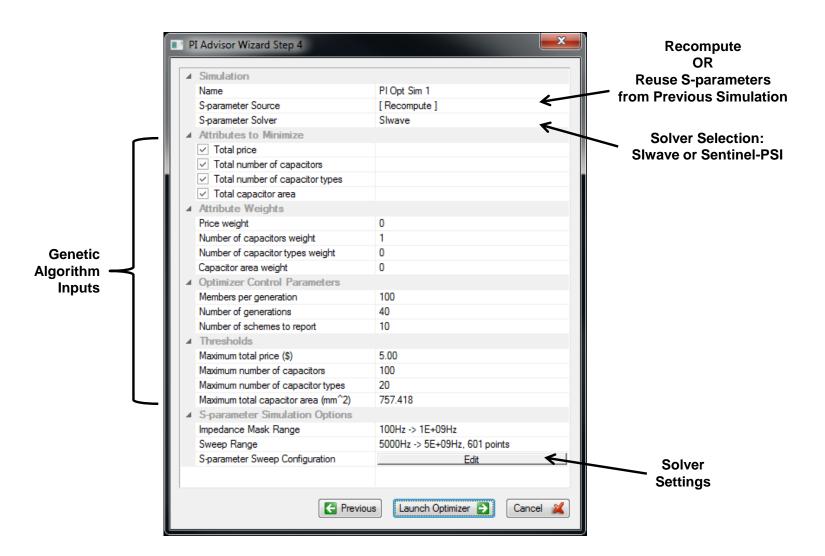
Plot Assigned Candidate Models

- Select all of the Assigned Candidate Models by using Shift+Click or Ctrl+Click.
- Click the **Plot |Z11|** button to display the candidate model profiles. Your display should now appear similar to the graphic below.
- Click **Next** to proceed to Step 4.





PI Advisor: Step 4



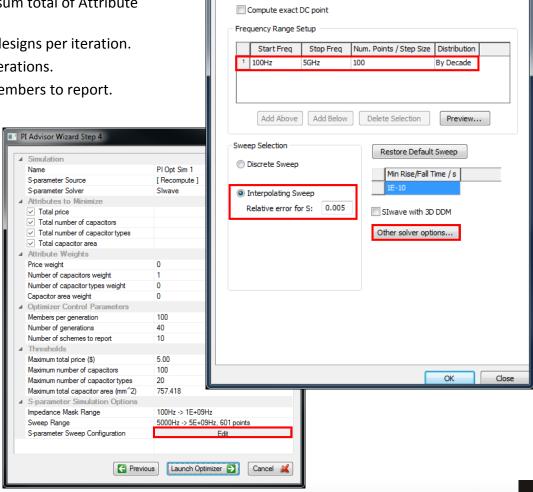


Genetic Algorithm Settings

- The default settings for the genetic algorithm attempts to reduce the number of capacitors as the goal. The sum total of Attribute Weights should add up to 1.
- Members per generation: Number of trial designs per iteration.
- Number of generations: Total number of iterations.
- Number of schemes to report: Subset of members to report.

SYZ Sweep Settings

- Click the Edit button.
- Set the following Sweep Definition:
 - Start Frequency: 100Hz
 - Stop Frequency: **5GHz**
 - Num. Points / Step Size: 100
 - Distribution: By Decade
- Set the Sweep Selection to:
 - Interpolating Sweep
 - Relative error for S: 0.005
- Click Other solver options...



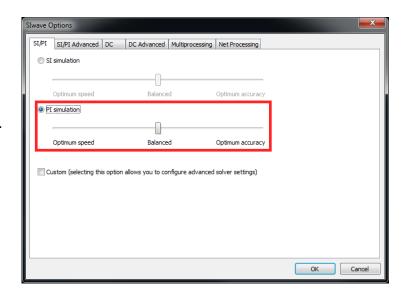
PI Advisor Solution Frequency Range

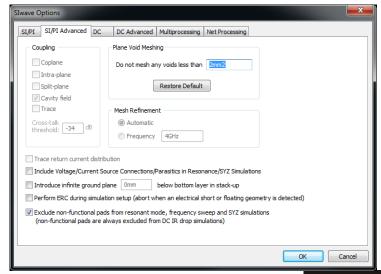
Sweep

SIwave Options

- SI/PI tab
 - Choose Balanced
 - The slider bar allows you to choose between three predefined settings.
 To see what settings are changed, move the slider bar to different positions and click on the SI/PI Advanced tab.

- SI/PI Advanced tab
 - Note that we are only solving for cavity fields for this balanced PI simulation and Automatic Mesh Refinement is turned on.





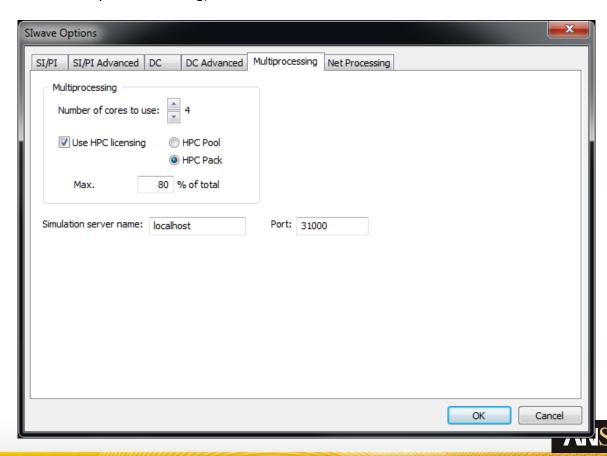


Multiprocessing (High Performance Computing, HPC)

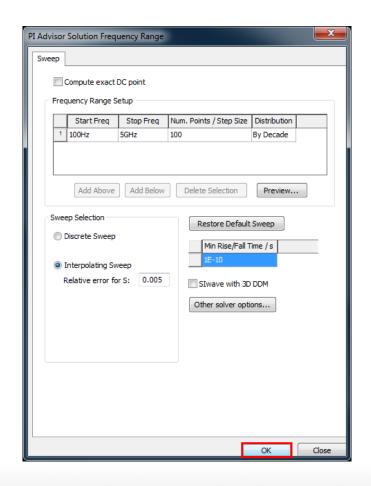
- For a PI simulation, HPC can distribute the solver across multiple cores.
- Click on the **Multiprocessing** tab.
- Ensure the following options are set:
 - Number of cores to use: **Max** (increase until it stops incrementing)
 - Use HPC Licensing: Enable
 - HPC Pack: Selected

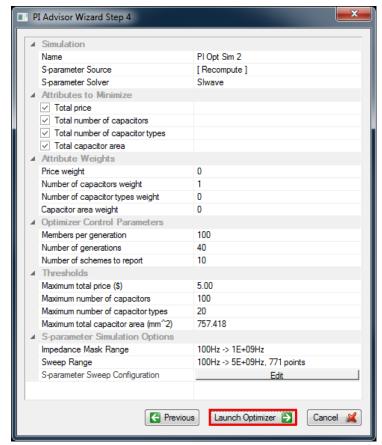
24

- Max: 80% of total RAM
- Click **OK** to close this window.



- Genetic Algorithm and SYZ Sweep Settings, cont.
 - Click **OK** to apply the S-parameter sweep settings.
 - Click Launch Optimizer to begin the PI Advisor simulation.





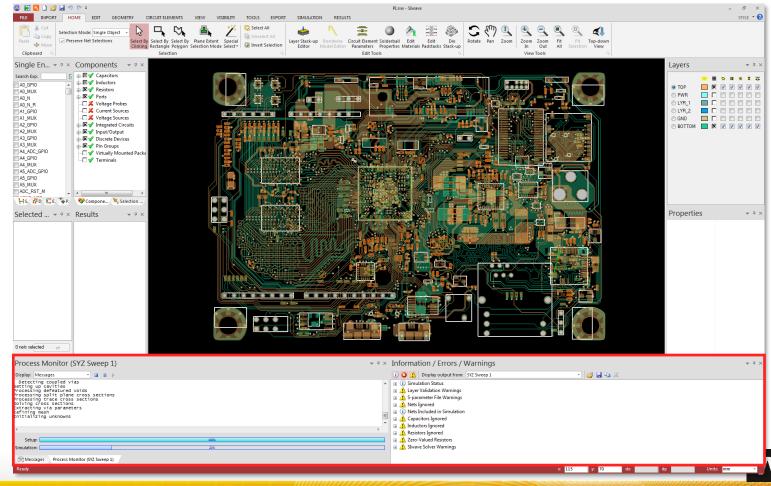


SYZ Sweep and PI Advisor Simulation Status

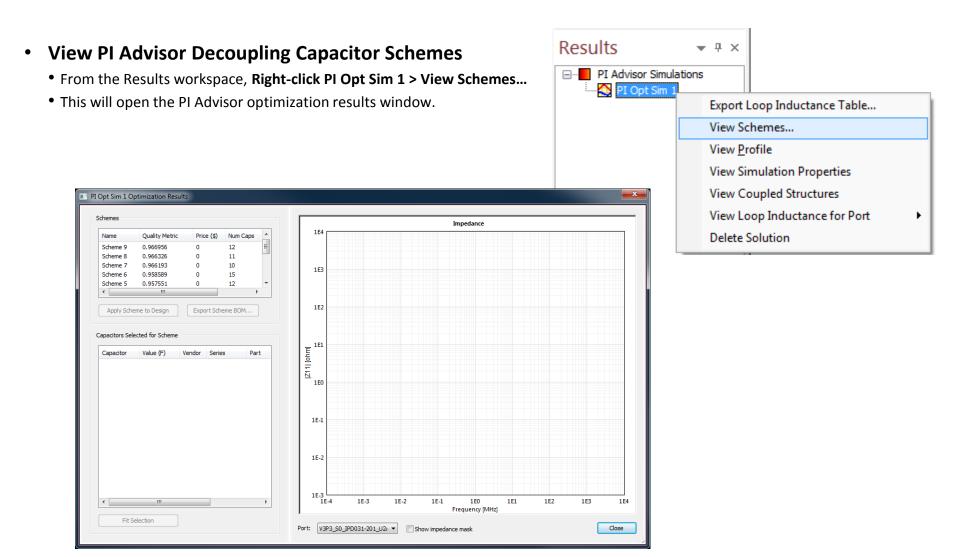
Process Monitor and Information / Errors / Warnings

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- The process monitor shows the simulation status and steps taken by the solver.
- Information / Errors / Warnings alerts you to any potential issues that may arise during the solution process.



PI Advisor Results

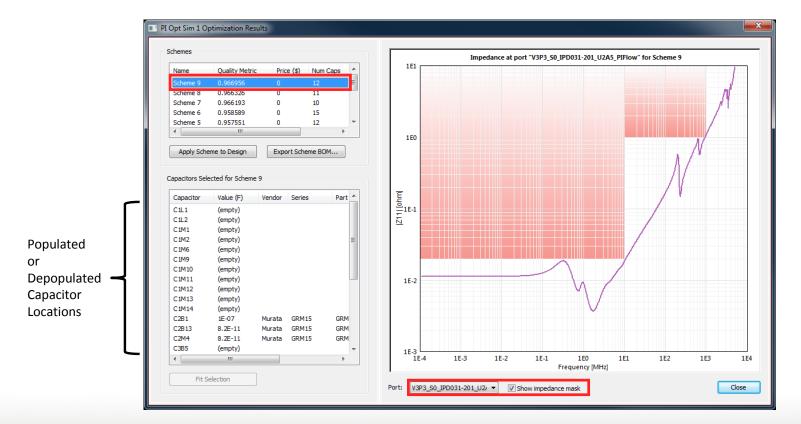




PI Advisor Results

Viewing Results

- The results window displays ten capacitor selections that come the closest to the specified criteria and the corresponding |Z11|.
- Each Scheme is able to be applied back to the project or exported as a Bill of Materials (BOM) change.
- Select **Scheme 9** from the Schemes window.
- Click the **Show impedance mask** check box.
- If multiple Active Devices were specified, the Port field would enable selection of those ports.

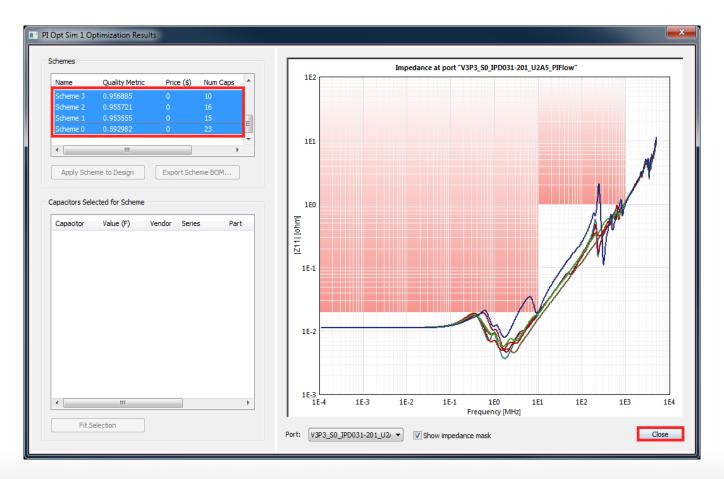




PI Advisor Results, cont.

Viewing Results

- Selecting multiple lines accumulates |Z11| for all available schemes.
- Click **Close** to close the PI Advisor Results window.





PI Advisor Results

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Plotting and Exporting Loop Inductance

- From the Results workspace, Right-click PI Opt Sim 1 > View Loop Inductance for Port > V3P3_S0_OPD031-201_U2A5_PIFlow
- This plot shows the loop inductance to each capacitor as seen from the selected active device. The inverse relationship of this loop inductance shows that lower values can contribute to higher frequency resonances. This inductance value is the geometry portion of the loop inductance not inclusive of ESL from a placed capacitor ($L_{geometry}$).
- A text file of these loop inductances can be exported from the results option **Export Loop Inductance Table**.

