PC104-DAC06

User's Manual

MEASUREMENT COMPUTING™

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1.0 INTRODUCTION

The PC104-DAC06 is a six-channel analog output board. The analog outputs are dual-DAC AD7237s with each output buffered. The PC104-DAC06 is compatible with the CIO-DAC16 but has only six channels. Software designed for the DAC16 and DDA-06 will operate the analog outputs correctly.

The analog outputs are controlled by writing a digital control word (two bytes) to the DAC's control register. The control register is double buffered so the DAC's output is not updated until both bytes (first low byte, then high byte) have been written to the register.

The analog outputs may also be set for simultaneous update in groups of two, four or all six. Analog outputs are grouped as 0&1, 2&3, 4&5. By selecting XFER on the jumper below the DAC, each pair may be set for simultaneous update.

When a DAC pair is set for simultaneous update, writing new digital values to the DAC's control register does not cause an update of the DAC's voltage output. Update of the output occurs only after a READ from the board's valid addresses (any address base + 0 through base + 11).

In this way, the PC104-DAC06 may be set to hold new values until all channels are loaded, then update any two, four or all six channels simultaneously. This is a very useful feature for multi-axis motor control.

The PC104-DAC06 has six sets of gain jumpers, one base address switch and three simultaneous update jumpers.

2.0 SOFTWARE INSTALLATION

The board has a variety of switches and jumpers to set before installing the board in your computer. By far the simplest way to configure your board is to use the *Insta*Cal™ program provided as part of your software package. *Insta*Cal™ will show you all available options, how to configure the various switches and jumpers to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically know the exact configuration of the board.

Please refer to the *Software Installation Manual* regarding the installation and operation of *Insta*Cal™. The following hard copy information is provided as a matter

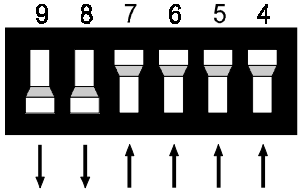
of completeness, and will allow you to set the hardware configuration of the board if you do not have immediate access to *Insta*Cal™ and/or your computer.

3.0 HARDWARE INSTALLATION

Several switch and jumper settings must be made before the PC104-DAC06 is installed into the computer. There are six jumper blocks for setting the gain of each channel, a simultaneous update jumper for each pair of channels and a base address switch.

3.1 BASE ADDRESS

The switches on your base address switch are set at the factory to address 300 hex (768 decimal) as shown in Figure 3-1. Unless there is already a board in your system using address 300h (768 decimal), we suggest leaving the switches as they are set at the factory..



SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20
A4	10

BASE ADDRESS SWITCH - Address 300H shown here.

Figure 3-1. Base Address Switches

Certain address are used by the PC, others are free and may be used by the PC104-DAC06 and other expansion boards.

Table 3-1. PC I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

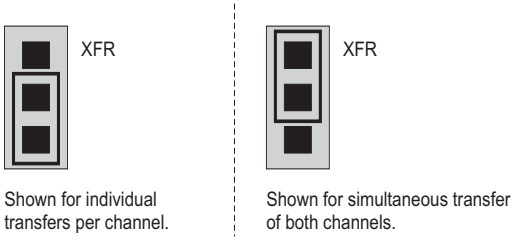
The PC104-DAC06 BASE switch may be set for address in the range of 000-3F0 so it should not be hard to find a free address area for your PC104-DAC06. Once again, if you are not using IBM prototype cards or some other board which occupies these addresses, then 300-31Fh are free to use. Address not specifically listed, such as 390-39Fh, are free.

3.2 SIMULTANEOUS UPDATE JUMPER

The analog outputs can be jumpered so that new output data is held until two, four, or six DACs have been loaded with new digital data. Then, as a group, those that are jumpered for simultaneous outputs will have that new data sent to the voltage outputs. Simultaneous update occurs whenever any addresses BASE + 0 through BASE + 11 are read.

The analog output chips are dual DACs. A single jumper sets both DACs on a single chip to be either simultaneous TRANSFER or individual UPDATE.

Figure 3-2 shows the jumper block in each configuration. Place the jumper on the two pins closest to the word XFER for simultaneous transfer.



SIMULTANEOUS TRANSFER JUMPERS - One per pair of channels.

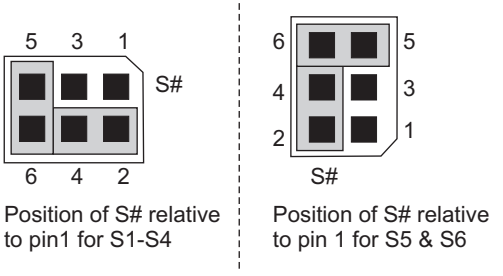
Figure 3-2. Simultaneous Transfer Jumpers

Jumper #	**DAC Controlled**
J1	DAC 0 & 1
J2	DAC 2 & 3
J3	DAC 4 & 5

3.3 ANALOG OUTPUT RANGE JUMPER

The analog output voltage range of each channel can be set via a six pin jumper block. The switches are located on the board near the DACs they control and are labeled S1 through S6. The number corresponds to the DAC under control + 1.

Set the jumpers for an individual channel using Figure 3-3 to orient the jumper block pin 1, and Table 3-2 below to select the range.



JUMPERS SHOWN +/-5v RANGE

Figure 3-3. Range Jumpers

Table 3-2. Range Select Jumpers

Jump Pins	**Range**
2-4, 3-5	+/-10V
2-4, 5-6	+/-5V
1-2, 3-5	0 to 10V
1-2, 5-6	0 to 5V

3.4 OUTPUT TRANSFER FUNCTIONS

To program a DAC, you must select the output you desire in volts, then apply a transfer function to that value. The transfer function for CODE = output is:

The UNIPOLAR transfer function of the DAC is:
FSV / 4096 * CODE = OutV or CODE = OutV / FSV * 4096

For Example:
If the range is 0 to 5V and you desire a 2V output:
CODE = 2/5 * 4096 = 1638

The BIPOLAR transfer function for the DAC is:
FSV/4096 * CODE – .5 * FSV or CODE = (OutV + .5 * FSV) / FSV * 4096

For example:
If the range is set to ±10 and you desire a −7V output:
CODE = (−7V + .5 * 20) / 20 * 4096=614.

3.5 CABLING

Several cabling and screw termination options are available.

C40FF-2	2 foot (and longer) ribbon cable with 40-pin connectors.
CIO-MINI40	Simple, 40-position 4"X4" screw terminal board.
C40-37F-2	2 foot ribbon cable maps 40-pin to 37-pin D connector.
CIO-MINI37	Simple, 40-position 4"X4" screw terminal board.
CIO-TERMINAL	Full featured 4"X16" screw terminal board with prototype and interface circuitry.

3.6 SIGNAL CONNECTIONS

The analog outputs are two-wire hookups; a signal, labeled D/A # OUT on the connector diagram below, and a Low Level Ground (LLGND). The low level ground

is an analog ground and is the ground reference which should be used for all analog hookups.

Possible analog output ranges are:

Bipolar Ranges	±10V	±5V
and		
Unipolar Ranges	0 to 10V	0 to 5V

Each of the DAC06 outputs are individually buffered through an OP-27 operational amplifier (OP-AMP). The OP-27s are socketted so that if one fails it can be replaced in the field. The OP-27 for each channel is located adjacent to the calibration potentiometers for that channel.

At the full rated output swing of ±10V, each channel is capable of sinking or sourcing ±5 mA. That means a load of 2KΩ can be connected to each channel.

If load resistance is raised from 2KΩ up to 10 MegΩ or more, the output load on the DAC decreases. Any load resistor greater than 2KΩ is acceptable.

As the load resistance decreases, the output load increases. The OP-27 responds by producing a lower output voltage. If your DAC06 will not produce the output voltage specified by the code and range combination, check the load with an ohmmeter.

Under normal circumstances you will not damage the OP-27 by connecting the output to ground. If your connection results in a failure of the OP-27, chances are there was some potential at the connecting point in addition to a load at ground or between 0 and 2K ohms. Explore the point with a DVM before reconnecting the DAC06 (and after replacing the OP-27 of course). Connect the negative lead of the DVM to any LLGND pin of the DAC06.

3.7 CONNECTOR DIAGRAM

The connector is a male, 40-pin header type connector (Figure 3-4).

The connector accepts female 40 pin connectors, such as those on the C40FF-2, a two- foot cable with connectors or, for compatibility with the CIO-DAC series, a BP40-37 adapter (Figure 3-5) may be used along with a C37FF-2 cable.

If frequent changes to signal connections or signal conditioning are required, please refer to the information on the CIO-TERMINAL, CIO-SPADE50, CIO-MINI40 and CIO-MINI37 (if using a BP40-37 adapter) screw terminal boards.

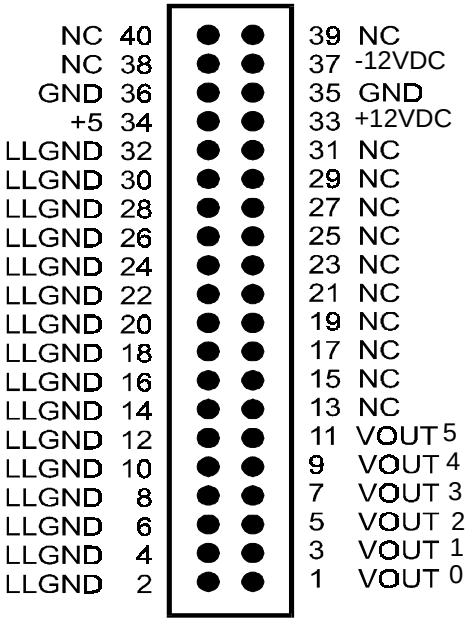


Figure 3-4. Board Connector

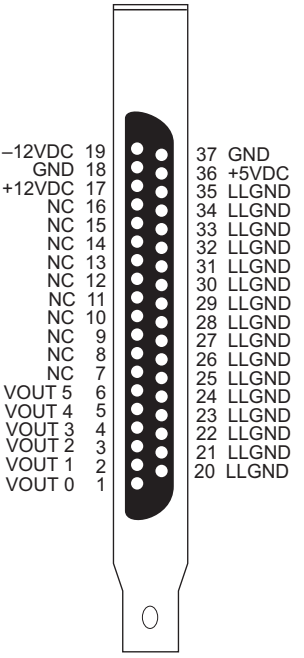


Figure 3-5 Cable BP40-37 Pin-Out

4.0 CONTROL & DATA REGISTERS

All control and data is read/written with simple I/O read and write signals. No interrupt or DMA control software is required. Hence, the board's functions are easy to control directly from BASIC, C or PASCAL.

The PC104-DAC06 has 12 analog output registers. There are two for each channel, one for the lower eight bits and one for the upper four bits.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

A register is easy to read and write to. The register descriptions all follow the format:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Where the numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the bit weights in table 2-1 apply:

Table 2-1. Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a byte.
The method of programming required to set/read bits from bytes is beyond the scope of this manual.

In summary form, the registers and their function are listed in Table 2-2. Each register has eight bits which constitute a byte of data or eight individual bit functions.

Each DAC has two 8-bit registers which are used to control it. The first register contains the least-significant eight bits of D/A code. Write to it first.

7	6	5	4	3	2	1	0
D5	D6	D7	D8	D9	D10	D11	D12 LSB

The second register contains the most significant four bits of D/A code. Write to it last. A write to this register will update the output of the D/A with all 12 bits of the D/A code contained in the two registers. If the XFER jumper is set for the DAC, no update will occur until a read of any one of the DAC registers is executed. Upon a read, all DACs set for simultaneous transfer (XFER jumper set) will update together.

7	6	5	4	3	2	1	0
X	X	X	X	D1 MSB	D2	D3	D4

The DAC06 contains 12 registers. Two registers control one D/A output. These register functions are identical to the CIO-DAC series registers except that there are only 12 of them.

Table 2-2. Board Registers

ADDRESS	WRITE FUNCTION	READ FUNCTION
BASE + 0	D/A 0 Least Significant Byte	Initiate simultaneous up
BASE + 1	D/A 0 Most Significant Nibble	Initiate simultaneous up
BASE + 2	D/A 1 Least Significant Byte	Initiate simultaneous up
BASE + 3	D/A 1 Most Significant Nibble	Initiate simultaneous up
BASE + 4	D/A 2 Least Significant Byte	Initiate simultaneous up
BASE + 5	D/A 2 Most Significant Nibble	Initiate simultaneous up
BASE + 6	D/A 3 Least Significant Byte	Initiate simultaneous up
BASE + 7	D/A 3 Most Significant Nibble	Initiate simultaneous up
BASE + 8	D/A 4 Least Significant Byte	Initiate simultaneous up
BASE + 9	D/A 4 Most Significant Nibble	Initiate simultaneous up
BASE + 10	D/A 5 Least Significant Byte	Initiate simultaneous up
BASE + 11	D/A 5 Most Significant Nibble	Initiate simultaneous up
BASE + 12 to 15	None	None

5.0 SPECIFICATIONS

Power consumption

Icc: +5V quiescent	130 mA typical, 180 mA max
Icc: +12V quiescent	50 mA typical, 75 mA max
Icc: −12V quiescent	30 mA typical, 45 mA max

Analog Output section

D/A converter type	AD7237
Resolution	12 bits
Number of channels	6
Ranges	±10V, ±5V, 0 to 10V, 0 to 5V each channel individually jumper selectable
D/A pacing	Software
Data transfer	Software polled
Throughput	125 kHz typical (PC-dependent)
Offset error	Adjustable to zero
Gain error	Adjustable to zero
Integral non-linearity	±0.5 LSB
Differential non-linearity	±0.5 LSB
Monotonicity	Guaranteed over temperature range
Gain drift	160 ppm/°C
Zero drift	150 ppm/°C
Current Drive	±5 mA min
Short circuit current	±40 mA
Output resistance	0.1ohms
Slew rate	1.7V/µs
Miscellaneous	Double buffered input latches Update DACs individually or simultaneously (jumper selectable by DAC pairs) DAC output state on power-up and reset undefined

Environmental

Operating temperature range	0 to 70°C
Storage temperature range	−40 to 100°C
Humidity	0 to 90% non-condensing

EC Declaration of Conformity

We, Measurement Computing Corporation, declare under sole responsibility that the product:

PC104-DAC06	
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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