MSI-P402/P404

PC/104 QUADRATURE DECODER/COUNTER CARD

PC/104 Embedded
Industrial Analog I/O Series

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I. DESCRIPTION

The MSI-P402/P404 is a 32-bit quadrature decoder PC/104 card designed for monitoring up to 8 quadrature encoder inputs used in monitoring shaft positions and rotations for machine control and robotic applications. Each channel provides a 32-bit binary up/down counter with selectable 1X, 2X or 4X decoding using an Agilent HCTL-2032 decoder IC. This device provides a digital noise filter network, decoding logic, a 32-bit counter, and a 32-bit latched output. In addition, the MSI-P404 provides index inputs for encoders that have indexing. A card outline is shown in Figure 1.

Inputs from quadrature encoders are applied to input connector J1 that requires a frequency and a reference signal input for each channel in use. For the MSI-P404, index inputs are applied to connector J2. Input signals are TTL levels. The clock employed for processing the input signals is selectable from SYSCLK (6 to 8.33 MHz, depending on the processor card

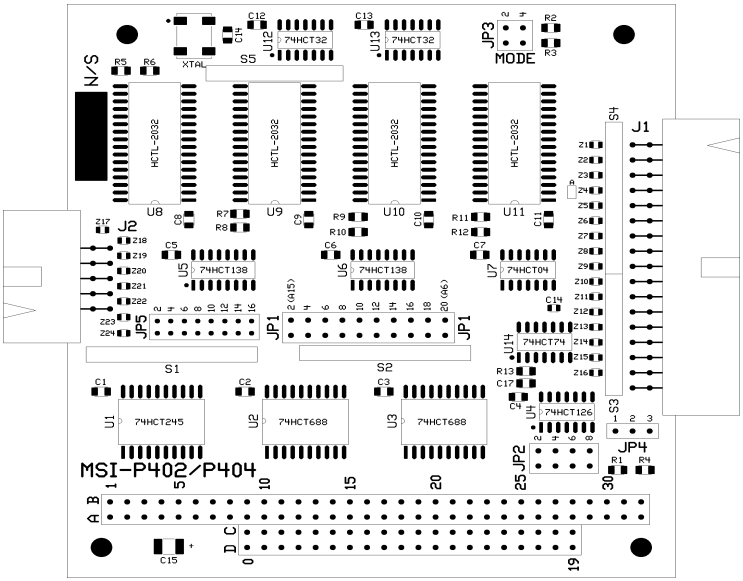

Figure 1. Outline of MSI-P402/P404 Card.

used, or OSC at 14.318 MHz) of the PC/104 bus. As an option, clock oscillators from 2 to 33 MHz are available.

In addition to the frequency (CHA_0 thru CHA_7) and reference (CHB_0 thru CHB_7) quadrature inputs, +5V and GND connections are provided on the input connector for supplying power to the encoder of each channel. Surge protectors are provided on each all quadrature inputs and index inputs to protect against damage due to voltage surges in noisy environments.

The maximum frequency that can be applied to either a frequency or reference input is

$$f_{max} = CLK/7$$

Therefore, for CLK = 8.33 MHz, f_{max} = 1.19 MHz and for CLK = 14.318 MHz, f_{max} = 2.045 MHz.

Each channel has a 32-bit up/down counter and an output latch. When a frequency input (CHA_x, x = 0 to 7) leads a reference input (CHB_x, x = 0 to 7), nominally by 90 degrees, the counter counts up. Conversely, when the reference input leads the frequency input, nominally by 90 degrees, the counter counts down. Counts range from 0 to FFFFFFFF hexadecimal (0 to 4,294,967,295 decimal). Data reads require four Byte I/O reads to acquire the 32-bit count of each channel. Roll-over occurs for 0-to-FFFFFFFF and FFFFFFFF-to-0 count transitions. These transitions are OR'ed together for use with interrupts IRQ3 thru IRQ9. The monitoring software must account for the roll-over events. A software reset is provided for each channel that sets the count to 0. The card is an 8-bit stackthrough unit that requires +5V from the PC/104 bus.

For the MSI-P404, and index input will reset the count for the channel to zero when an index pulse occurs if the channel is not disabled using option jumpers on JP5.

II. CARD CONFIGURATIONS

A. Card Address Selection

The I/O-mapped card address is set by installing appropriate jumpers on JP1, pins 1 thru 20. An uninstalled jumper for a given address bit sets the bit to 1 (true) and an installed jumper sets the bit to 0 (false). Addresses A6 thru A15 are jumper selectable for defining the ***base address*** of the card from 0000H to FFC0H on integral 40H boundaries, where H denotes a hexadecimal number. To assign a base address of 300H, for example, install all jumpers except JP1-15,16 (A8) and JP1-13,14 (A9).

B. Clock Source Selection

The clock source for the HCTL-2032 decoders is selectable by inserting the appropriate jumper on JP4 as follows:

JP4-1,2 PC/104 BUS SYSCLK (Approx. 8 MHz)

JP4-2,3 PC/104 BUS OSC (14.318 MHz) *

* Factory Default setting.

Note: An optional clock from 1 to 33 MHz is available.

C. Count Mode Selection

The HCTL-2032 decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of one, two or four (1X, 2X, 4X decoding) depending on the resolution mode. When using an encoder for motion sensing, the user benefits from the selectable resolution by being able to provide better system control. The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the integral position counter. The 4x decoder mode

will output a count signal for every state transition (count up and count down). The 2x/1x decoder will output a count signal at respective state transition, depending on the counting direction. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down.

The count mode for the HCTL-2032 decoders is selectable as 1X, 2X or 4X counting. Insert the appropriate jumpers on JP3 as follows:

None 1X Decoding (Default)

JP3-1,3 2X Decoding

JP3-2,4 4X Decoding

D. Interrupt (IRQ3 thru IRQ7, IRQ9) Selection

The HCTL-2032 decoders have 32-bit count registers and interrupt processing for rollover is usually not be necessary. In cases where counts exceed 32 bits interrupt processing for rollover can be used. Outputs RO-0 thru RO_7 are OR'd together to generate a single interrupt signal in the event of an overflow or an underflow of any of the HTCL-2032 decoders. This signal is available on JP2-8 for wirewrap routing to the desired IRQx (where x = 3, 4, 5, 6, 7 or 9), as shown in the schematics of Appendix A. When a rollover occurs, the interrupt is latched by U14 and remains valid until the latch is reset by performing an I/O read at ***base address + 20H.*** This must be performed in software by the user's interrupt handler. In addition, the eight channels of the HCTL-2032 decoders must be read to determine the device that has overflowed. A 1 KOhm pull-down resistor is provided on JP2-6 for use in avoiding a floating interrupt line when no interrupt request is present.

E. 32-Bit Counter Registers

Eight input channels, denoted as CH0 thru CH7, correspond to inputs CHA_0 and CHB_0 thru CHA_7 and CHB_7,

respectively. The I/O addresses are given in Table 1. Count data is obtained by performing consecutive I/O reads at these addresses. The resulting channel count is

Count = Low Byte + 256 x 2nd Byte + 65,536 x 3rd Byte
+ 16,777,216 x High Byte

Table 1. Input Addresses of MSI-P402 Count Registers.

Channel	Low Byte of Count* 3rd Byte of Count*	2nd Byte of Count* High Byte of Count*
CH0	base address base address+2	base address+1 base address+3
CH1	base address+4 base address+6	base address+5 base address+7
CH2	base address+8 base address+AH	base address+9 base address+BH
CH3	base address+CH base address+1EH	base address+DH base address+FH
CH4	base address+10H base address+12H	base address+11H base address+13H
CH5	base address+14H base address+16H	base address+15H base address+17H
CH6	base address+18H base address+1AH	base address+19H base address+1BH
CH7	base address+1CH base address+1EH	base address+1DH base address+1FH

* *Offsets from the base address are in hexadecimal notation.*

F. Resetting the Counter Registers

The counts contained in all registers (high to low bytes) can be reset to zero by performing a write of any value to the reset addresses of Table 2. This is a very useful function in many applications. At power-on, it is recommended that all channels be reset to zero performing a dummy write to each reset channel address of Table 2.

Table 2. Reset Addresses of MSI-P402 Count Registers.

Channel	Reset Address *
CH0	base address
CH1	base address + 1
CH2	base address + 2
CH3	base address + 3
CH4	base address + 4
CH5	base address + 5
CH6	base address + 6
CH7	base address + 7

** Offsets from the base address are in hexadecimal notation.*

G. Quadrature Input Connector Pin Assignments

The input connections for the quadrature inputs are provided by J1. Also available are +5V and ground connections for powering the user's quadrature encoders. The pinouts for J1 are given in Table 3.

Table 3. Quadrature Input Connector J1.

Pin No.	Signal	Pin No.	Signal
1	CHA_0	2	+5V
3	CHB_0	4	GND
5	CHA_1	6	+5V
7	CHB_1	8	GND
9	CHA_2	10	+5V
11	CHB_2	12	GND
13	CHA_3	14	+5V
15	CHB_3	16	GND
17	CHA_4	18	+5V
19	CHB_4	20	GND
21	CHA_5	22	+5V
23	CHB_5	24	GND
25	CHA_6	26	+5V
27	CHB_6	28	GND
29	CHA_7	30	+5V
31	CHB_7	32	GND
33	N/C	34	N/C

H. Index Inputs of the MSI-P404

The input connections for the index inputs are provided by J2. The pinouts for J1 are given in Table 3. A pulse generated by the quadrature encoder will reset the the count of the channel to which it is connected.

Any channel can be disabled by inserting the appropriate jumper on JP5, as shown in Table 5. A jumper that is inserted will ground the index input of the encoder. If this is not desired, simply do not connect the index input to J2. All index inputs have 10KOhm pull-up resistors. **Any input that is not connected to J2 must be disabled using JP5 so that the quadrature input channel will count.**

Table 4. Index Input Connector J2.

Pin No.	Signal	Pin No.	Signal
1	CH 7 INDEX	2	CH 6 INDEX
3	CH 5 INDEX	4	CH 4 INDEX
5	GND	6	GND
7	CH 3 INDEX	8	CH 2 INDEX
9	CH 1 INDEX	10	CH 0 INDEX

Table 5. Index Disable Jumpers of JP5.

Jumper	Function	Jumper	Function
1-2	CH 7 Disable	3-4	CH 6 Disable
5-6	CH 5 Disable	7-8	CH 4 Disable
9-10	CH 3 Disable	11-12	CH 2 Disable
13-14	CH 1 Disable	15-16	CH 0 Disable

III. SPECIFICATIONS

PC/104

8-bit, stackthrough

Quadrature Encoder and Index Inputs (Index for MSI-P404 only)

No. of Channels 2, 4, 6 or 8

Freq & Ref (Quadrature inputs for each channel)

Low level 1.5V Max.*
High Level 3.5V Min.*
Input Impedance 10 KΩ *
Surge Supression Varistors on each input

* Note: 10K pull-up on all inputs.

Input Frequency

f_{max} = CLK/7

f_{max} = 1.19 MHz for CLK = 8.33 MHz

f_{max} = 2.045 MHz for CLK = 14.318 MHz

Address Selection, Interrupt, Count Mode, and Clock Selection Jumpers (JP1 thru JP4)

Base Address Selection for A6 thru A15
Interrupts IRQ3 thru IRQ7 and IRQ9
Count Mode 1X, 2X, and 4X
Clock Selection SYSCLK or OSC of PC104 BUS

0.025" square posts, 0.1" grid

Index Input Disable Jumpers (JP5 of MSI-P404)

0.020" square posts, 2 mm grid

Input Connector (J1)

Quadrature Inputs, +5V and GND

One (1) 3M 303XX-5002
or equivalent.

XX = 10, 2 channels.
XX = 16, 4 channels.
XX = 26, 6 channels.
XX = 34, 8 channels.

Input Connector (J2)

Index Inputs

One (1) 3M 30310-5002 or equivalent.

Electrical & Environmental

+5V @ 2 mA/Channel typical
-40° to 85° C

Models

MSI-P402 - X, X = no. of channels (2, 4, 6, 8)

MSI-P404 - X, X = no. of channels (2, 4, 6, 8).

APPENDIX A

MSI-P402/P404 Circuit Diagram

Schematic Diagrams of the MSI-P402/P404

1) P404-1.sch - Schematic sheet 1 of 3.

See p404-1.pdf

2) P404-2.sch - Schematic sheet 2 of 3.

See p404-2.pdf

3) P404-2.sch - Schematic sheet 3 of 3.

See p404-3.pdf

APPENDIX B

HCTL-2032 Data Sheet