Dai-Rong Wu

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SPICE Modeling | PDK Development | EDA Workflow Automation | CAD Tool automation | Python • Cadence SKILL • Tcl • Perl

CAREER SUMMARY

SPICE modeling and PDK development engineer with 7+ years of experience at leading semiconductor companies (Infineon, Siemens EDA, UMC). Expert in advanced device modeling (BSIM4, BSIM-Bulk, HiSIM-HV), PDK/iPDK development, and EDA workflow automation. Proven track record of reducing project cycles, enhancing QA efficiency, and leading cross-functional teams. Seeking to leverage technical skills in the U.S.-based semiconductor or EDA role.

SKILLS

- **Modeling:** SPICE Models (BSIM4, BSIM-Bulk, HiSIM-HV), Reliability Modeling, RF modeling
- **PDK/iPDK**: PCell Design, Callbacks Development, Netlisting
- **Workflow:** SVN, Git (version control), Jira (issue tracking), Confluence (documentation)
- **EDA Tools**: Cadence Virtuoso, Siemens Tanner/Calibre, Keysight ICCAP/MBP, ProPlus, Sentaurus TCAD
- **Programming**: Python, Cadence SKILL, C++, Verilog, Tcl, Perl, Shell
- **Semiconductor Knowledge**: CMOS, High-Voltage Devices, Device Characterization

JOB EXPERIENCE

Infineon Technologies, Neubiberg, Germany – *Staff Engineer* *September 2023 - present*

- Performed on-wafer measurements to extract the characteristics of power devices, developed and validated SPICE models (**BSIM4, BSIM-Bulk, HiSIM-HV**) across multiple simulators (Spectre, HSPICE, and in-house simulator).
- Led SPT9U technology modeling projects, managing test chip planning and cross-functional collaboration.

Siemens EDA, Hsinchu, Taiwan – *Software Engineer* *March 2020 - Aug 2023*

- Developed PDK and iPDK in Tanner tools for **5+ foundries and 10+ process nodes**, including front-end functionalities such as **callbacks** and **netlisting procedures**, as well as back-end functionalities such as **PCell** development based on Cadence SKILL or Python.

United Microelectronics Corporation, Hsinchu, Taiwan – *Senior Engineer* *January 2018 - Mar 2020*

- Built and validated SPICE models for MOSFETs, diodes, varactors, resistors, and RF devices
- Contributed to model methodology development, QA flow, and model characterization documentation.

Key PROJECTS

Automated QA Workflow – Infineon Technologies

- Developed a fully automated QA workflow that generates testbenches, netlists and output reports directly from Virtuoso, reducing model QA cycle from **3 days to 1.5 hours**.

Auto-Centering Tool for SPICE Model Parameter Extraction – Infineon Technologies

- Built a GUI-based auto-centering tool that leverages ML-based regression to fit SPICE parameters to device target specs, reducing model centering time from **1.5 days to 1 hour**, significantly accelerating the cycle.

TSMC iPDK Development – Siemens EDA

- Led development on the conversion of TSMC PDK to iPDK(interoperable PDK), ensuring seamless integration with Siemens EDA Tanner, cutting development time by **50%** through optimized workflow.

EDUCATION

National Chiao Tung University, Hsinchu, Taiwan – *M.S. in Electronics* September 2015 - Aug 2017

First Author Publications:

- Crosstalk between single-photon avalanche diodes in a 0.18 μm high-voltage CMOS process. Journal of Lightwave Technology.
- Time-Correlated Crosstalk Measurements Between CMOS Single-Photon Avalanche Diodes. In: 2018 International Conference on OMN.

National Taiwan Normal University, Taipei, Taiwan – *B.S. in Physics* September 2011 - June 2015

LANGUAGES

- Mandarin (Native), Taiwanese (Native), English (Fluent), German (Elementary)

WORK AUTHORIZATION

- **U.S. Green Card in Progress**: EB-2 National Interest Waiver(NIW) I-140 approved, awaiting priority date.
- **Current Status:** Requires H-1B or L-1 sponsorship to begin employment.