



# *Leading University*

## **Lab Report 2**

**Course code: CSE-4113**

**Course Title: VLSI**

### **Submitted To**

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## Experiment No.2:

### Title: Design of 2\*1 MUX and 4\*1 MUX using LTSPICE software

**Abstract:** Multiplexer is a circuit that has maximum of  $2^n$  data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. In 2:1 multiplexer we have two inputs and one select inputs on other hand 4:1 multiplexer have four inputs and two select inputs and consisting one output.

Since there are 'n' selection lines, there will be  $2^n$  possible combinations of zeros and ones. So, each combination will select only one data input. In MUX We implement this circuit using Inverters, AND gates & OR gate.

**Introduction:** The main objectives of the experiment is to study the gate logic behaviour of different multiplexer circuits as follows:

- i. 2\*1 MUX
- ii. 4\*1 MUX

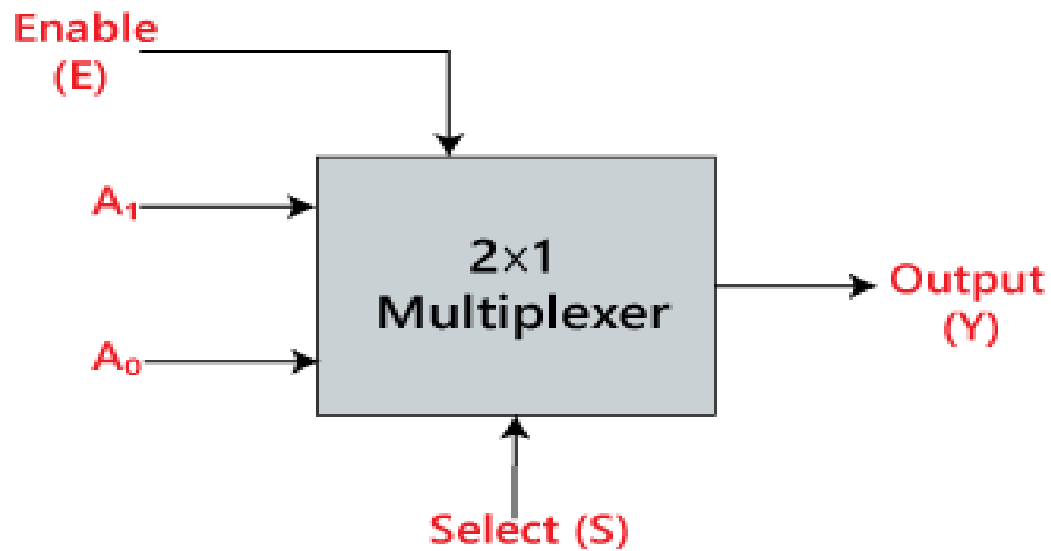
### Theory and Methodology:

- i. **2\*1 MUX:** In  $2 \times 1$  multiplexer, there are only **two inputs**, i.e.,  $A_0$  and  $A_1$ , 1 selection line, i.e.,  $S_0$  and single outputs, i.e.,  $Y$ . On the basis of the combination of inputs which are present at the selection line  $S^0$ , one of these 2 inputs will be connected to the output.

Truth table:

S	D <sub>1</sub>	D <sub>0</sub>	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

**Block Diagram:**

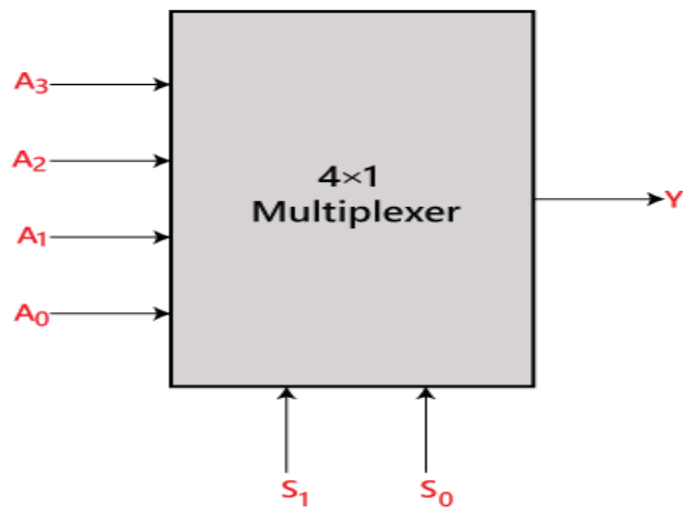


ii. **4\*1 MUX:** A 4-to-1 multiplexer consists **four data input lines as D0 to D3**, **two select lines as S0 and S1** and **a single output line Y**. The select lines S0 and S1 select one of the four input lines to connect the output line.

**Truth Table:**

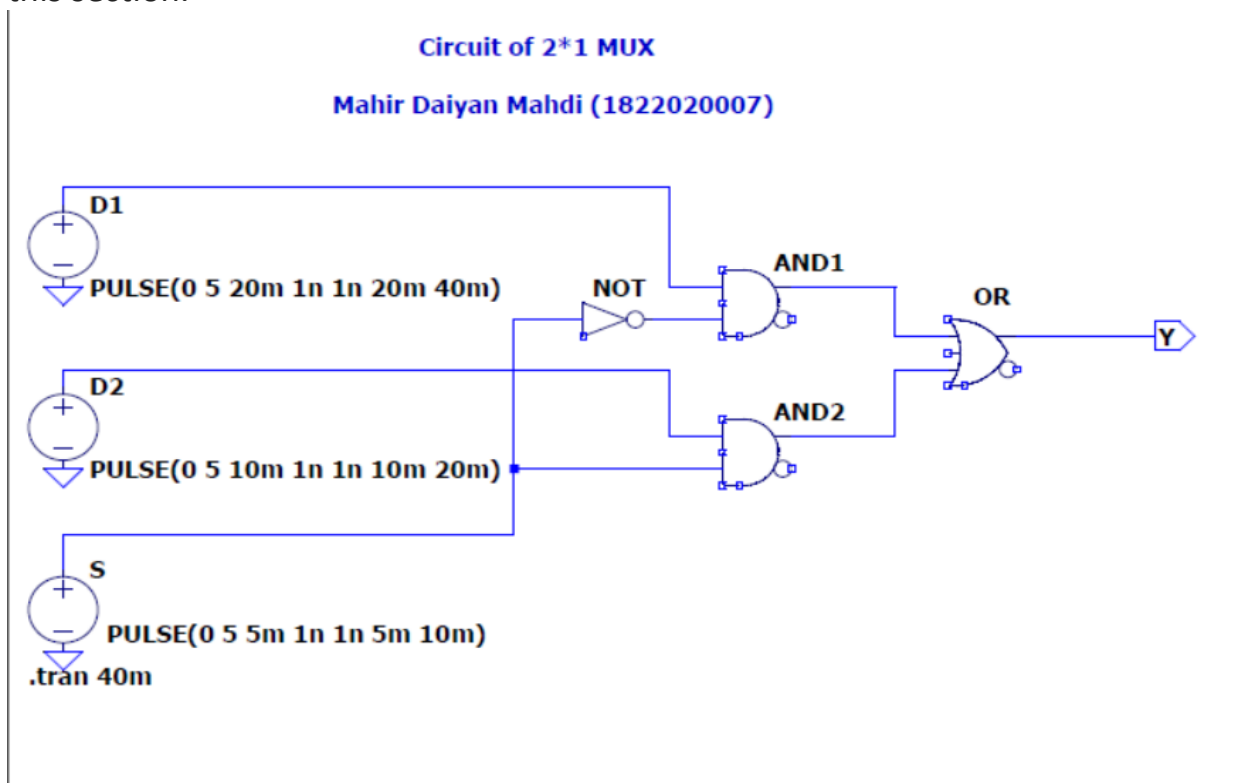
S0	S1	A	B	C	D	Y
0	0	A	0	0	0	A
0	1	0	B	0	0	B
1	0	0	0	C	0	C
1	1	0	0	0	D	D

**Block diagram:**



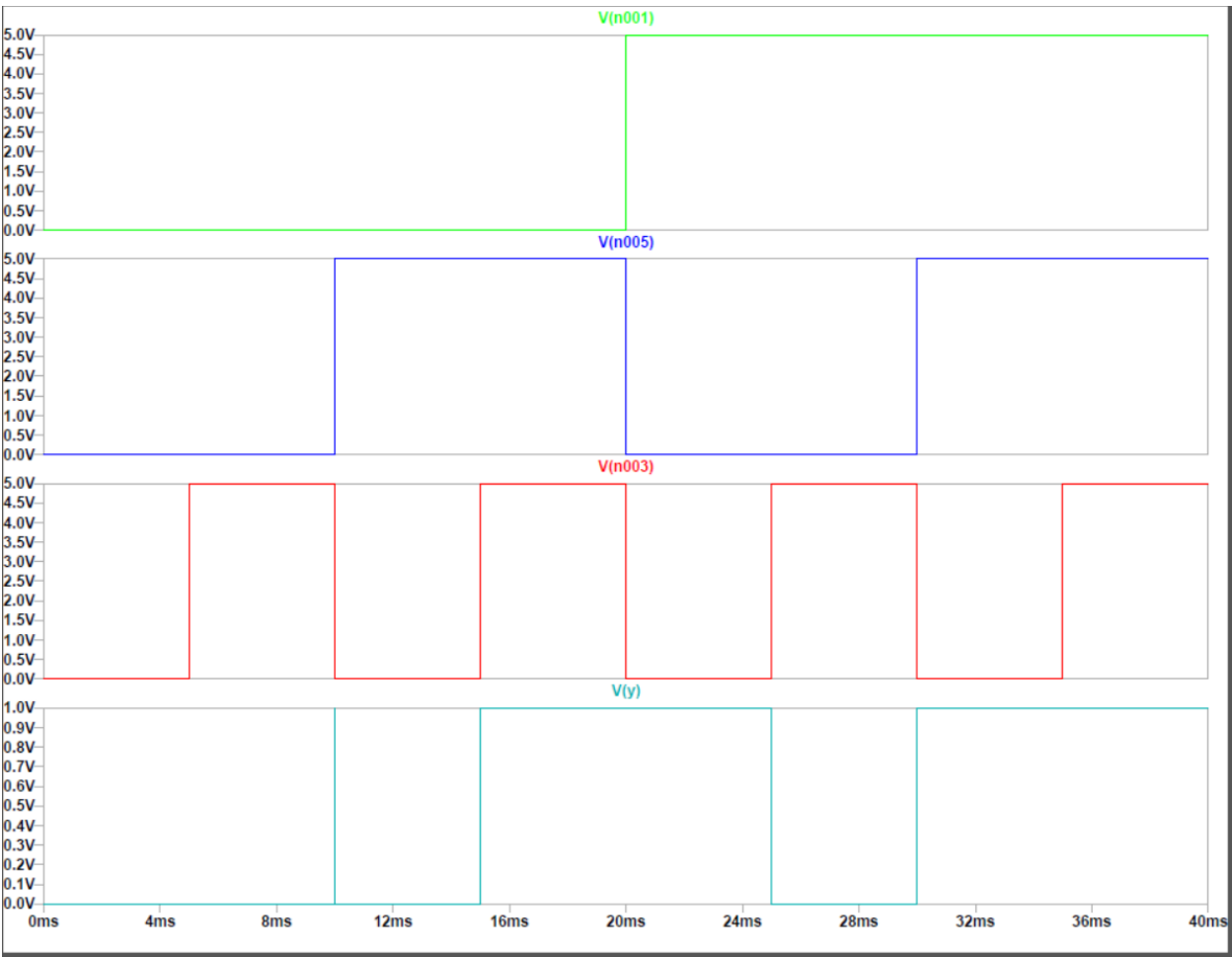
**Software:** LTSPICE XVII

**Circuit diagram:** Providing the schematic circuit diagram from LTSPICE software in this section.



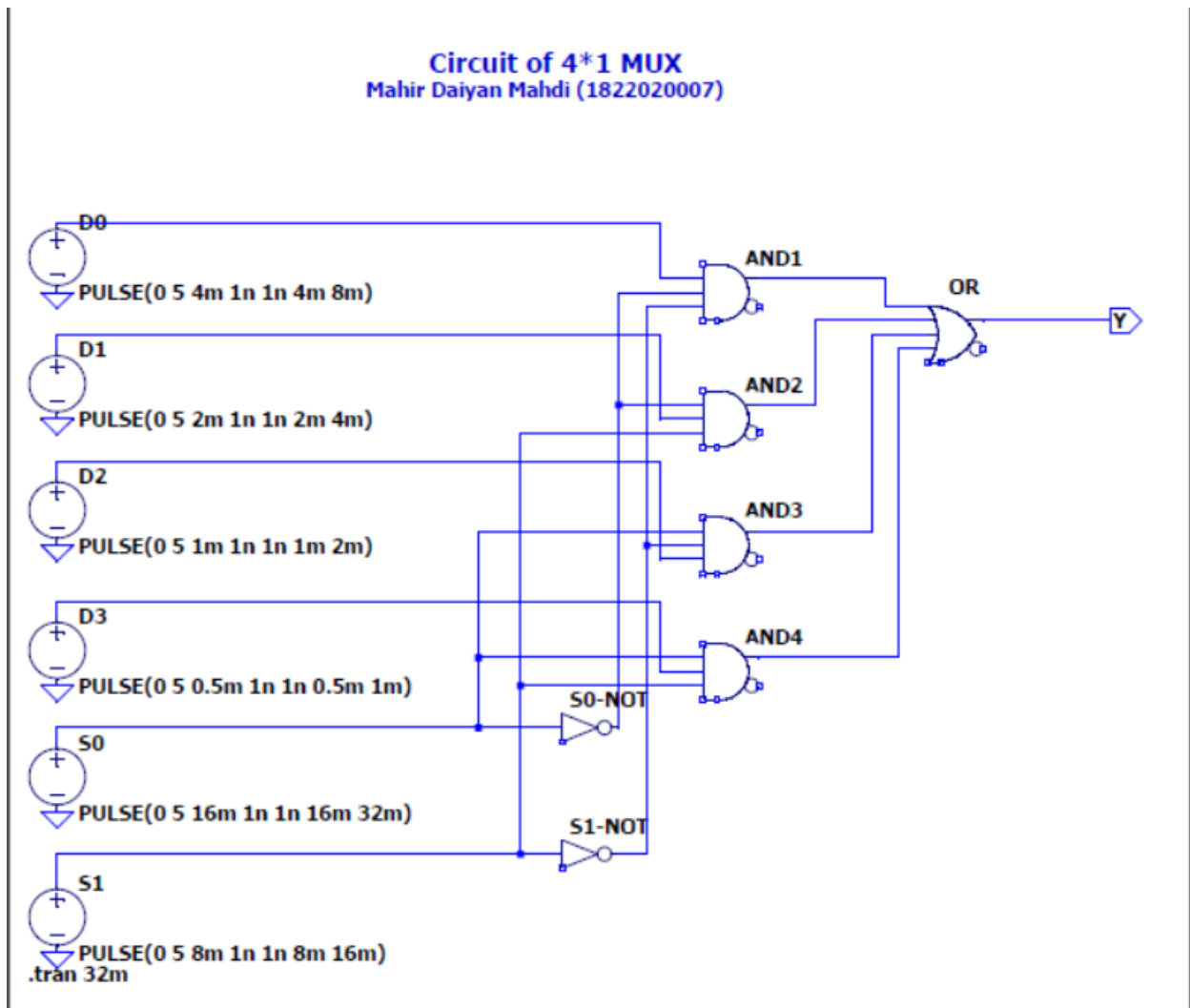
**FIG-01- Schematic diagram of 2\*1 MUX circuit**

**Simulation Result:**



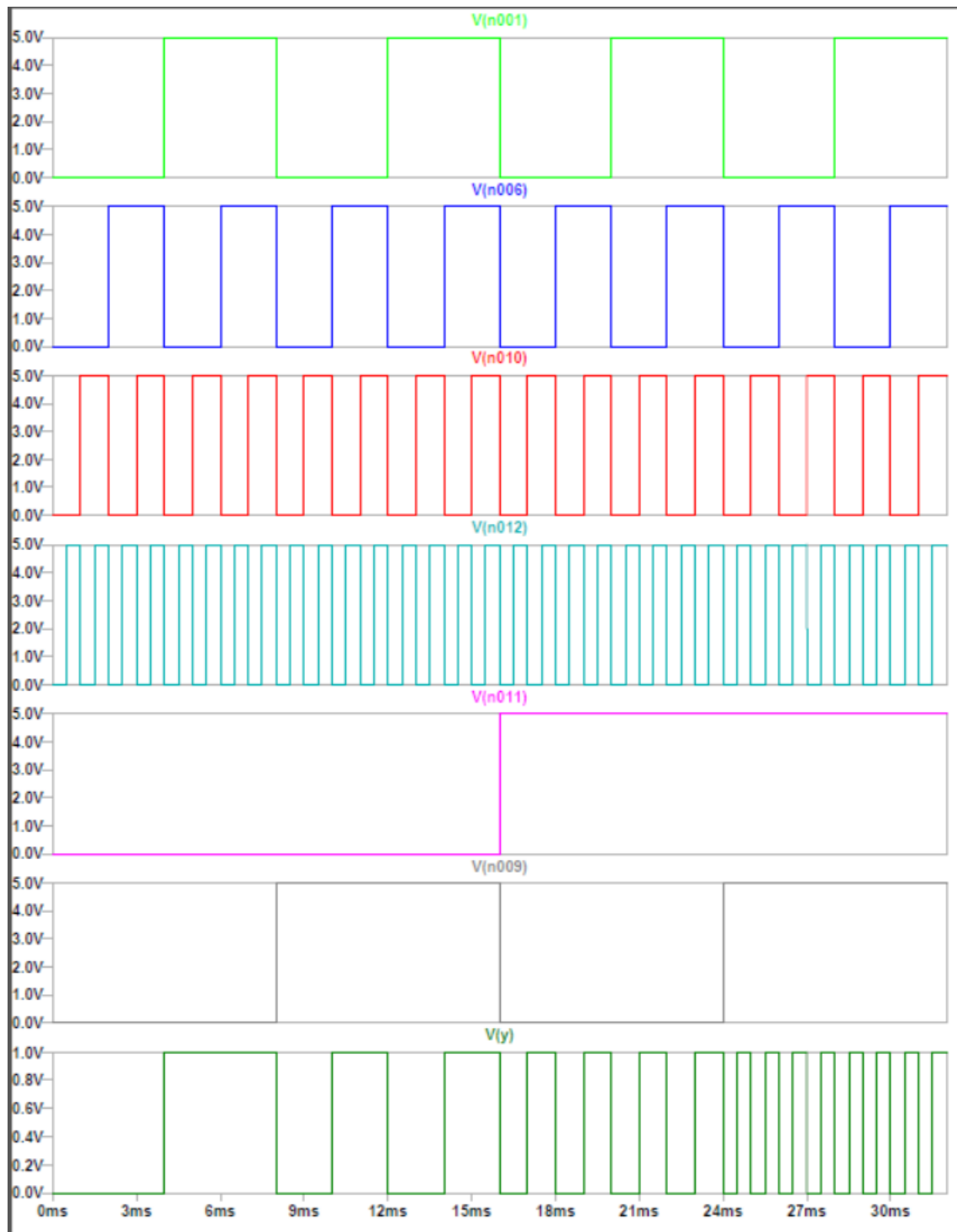
**FIG-02- Simulation result of 2\*1 MUX**

### Circuit diagram of 4\*1 MUX:



**FIG-03- Schematic diagram of 4\*1 MUX circuit**

## Simulation Result:



**FIG-04-Simulation result of 4\*1 MUX**

### **Discussion and Conclusion :**

In this entire experiment I had faced so much troubles specially in 4\*1 MUX just because of the circuit, it was too big and too much complex to draw for me. And also I got some confusion when I saw its simulation graph first time. Its takes most of the time. After all this troubles finally I solved the experiment.