1. 题目1

增加io口:

```
wire [31:0] pc, inst, aluout, memout, out_port0, out_port1, out_port2;
    wire [31:0] in_port0, in_port1, in_port2;
```

增加in_port2,out_port2

sys_clk_counter:

```
module sys_clk_counter (
  input   sys_clk_in,
  input   sys_rst_n,
  output  [31:0] count
);

  // 内部计数器信号
  reg [31:0] internal_count;

  always @(posedge sys_clk_in or negedge sys_rst_n) begin
    if (~sys_rst_n) begin

      internal_count <= 32'b0;
    end else begin

      internal_count <= internal_count + 1;
    end
  end

  // 输出计数器值
  assign count = internal_count;

endmodule
```

```
sys_clk_counter in2(
    .sys_clk_in(sys_clk_in),
    .sys_rst_n(sys_rst_n),
    .count(in_port2)
    );
```

例化

```
module sc_computer_main (
    resetn, clock, imem_clock, dmem_clock, pc, inst, aluout, memout,
    out_port0, out_port1, out_port2, in_port0, in_port1, in_port2);

  input resetn, clock, imem_clock, dmem_clock;
  input [31:0] in_port0, in_port1, in_port2;
  output [31:0] pc, inst, aluout, memout;
  output [31:0] out_port0, out_port1, out_port2;
```

```
module sc_datamem (resetn,
    addr, datain, dataout, we, clock, dmem_clock,
    out_port0, out_port1, out_port2, in_port0, in_port1, in_port2);

  input  [31:0]  addr;
  input  [31:0]  datain;
  input [31:0] in_port0, in_port1, in_port2;
  input          we, clock, dmem_clock, resetn;

  output [31:0]  dataout;
  output [31:0] out_port0, out_port1, out_port2;
  wire [31:0] io_read_data;

  wire write_enable;
  wire [31:0] dataout;
  wire [31:0] mem_dataout;
  wire write_data_enable;
  wire write_io_enable;

   //control signal for write dram or IO space
  assign         write_enable = we & ~clock;
```

在sc_computer_main,sc_datamem增加接口

```
display display(
  .clk(sys_clk_in),
  .reset(sys_rst_n),
  .s({{8'b10000111},HEX4b5,HEX4b4,HEX4b3,HEX4b2,HEX4b1,HEX4b0}),
  .seg0(seg_data_0_pin),
  .seg1(seg_data_1_pin),
  .ans(seg_cs_pin)
    );
```

显示学号

汇编程序：

```
lui x10, 0
ori x4, x10, 0
addi x25, x0, 1
addi x26, x0, 2
addi x27, x0, 3
addi x28, x0, 4
sw x25, 0(x4)
sw x26, 4(x4)
sw x27, 8(x4)
sw x28, 12(x4)
addi x5, x0, 4
call:
jal sum
sw x12, 0(x4)
lw x19, 0(x4)
sub x18, x19, x12
addi x5, x0, 3
loop2:
addi x5, x5, -1
ori x18, x5, -1
xori x18, x18, 1365
addi x19, x0, -1
andi x20, x19, -1
or x16, x20, x19
xor x18, x20, x19
and x17, x20, x16
beq x5, x0, shift
j loop2
shift:
addi x5, x0, -1
slli x18, x5, 15
slli x18, x18, 16
srai x18, x18, 16
srli x18, x18, 15
// 以下六条指令，前面三条指令用于设置端口地址寄存器，后面实现端口值的读取与写入
addi x11, x0, 128
addi x12, x0, 132
```

addi x13, x0, 136

lw x20, 0(x13)

lw x21, 0(x11)

sw x21, 0(x11)

sw x18, 0(x12)

sw x20, 0(x13)

fi:

j fi

sum:

add x18, x0, x0

loop:

lw x19, 0(x4)

addi x4, x4, 4

add x18, x18, x19

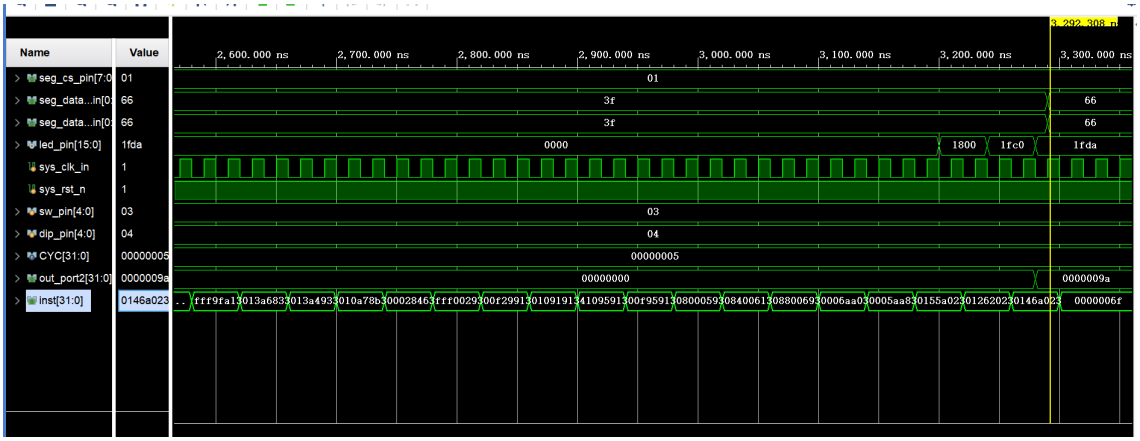
addi x5, x5, -1

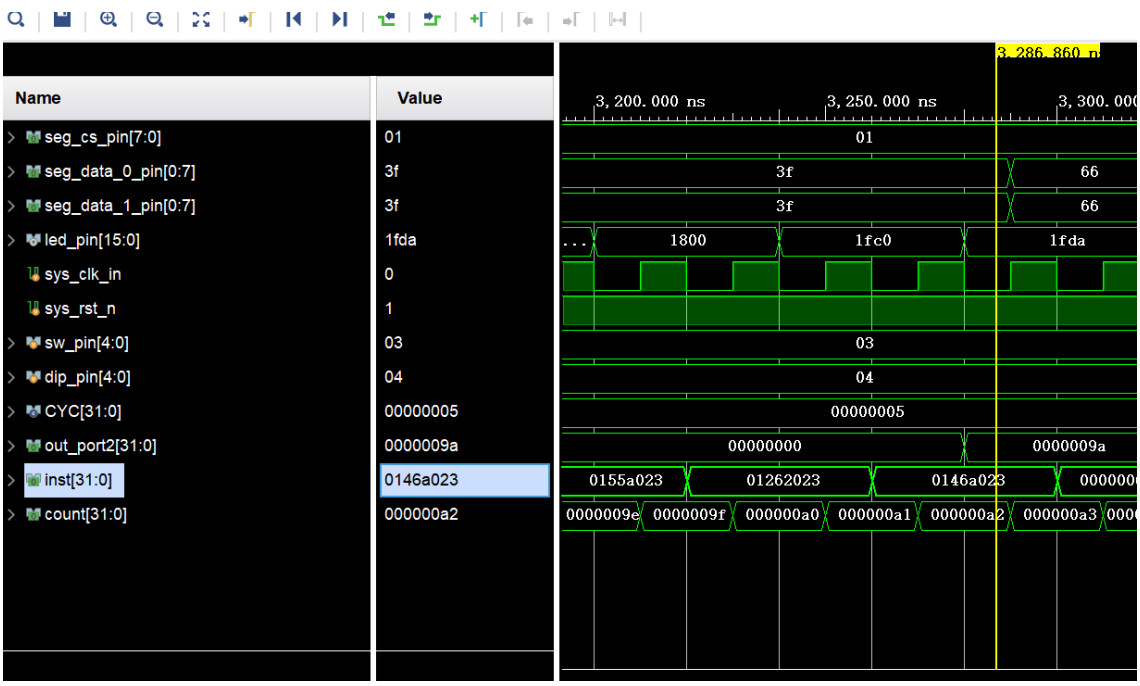
bne x5, x0, loop

slli x12, x18, 0

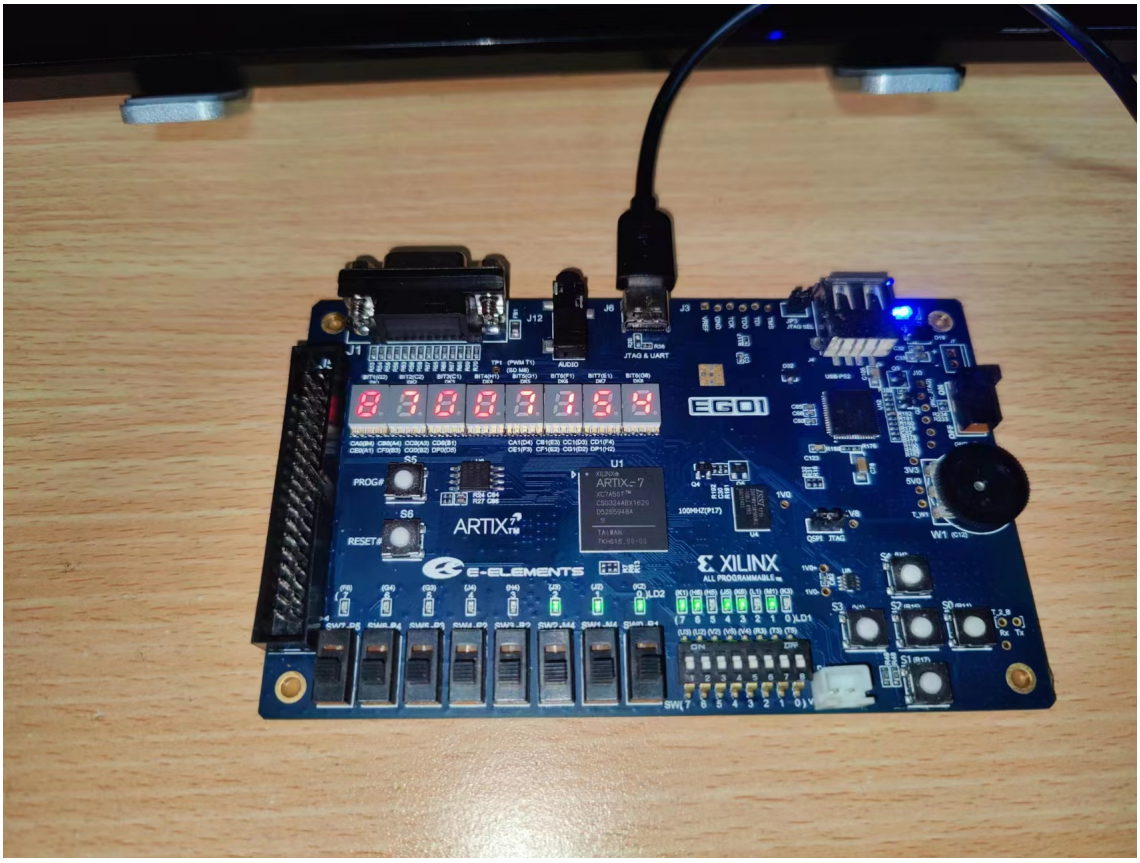
jr ra

仿真：





板上验证：



仿真结果计数器值为9a，转换为十进制就是9*16+10=154，其中最低两位对应位板上最低两位，因此两者结果相符。板上最高两位为学号87，次低两位为71，对应x18最后两位十进制数71.

读取时钟周期计数器值, 未执行该指令对应的时钟周期为76，执行后对应的时钟周期应该是 77, 因此对应正确的计数器的值应该是位 154

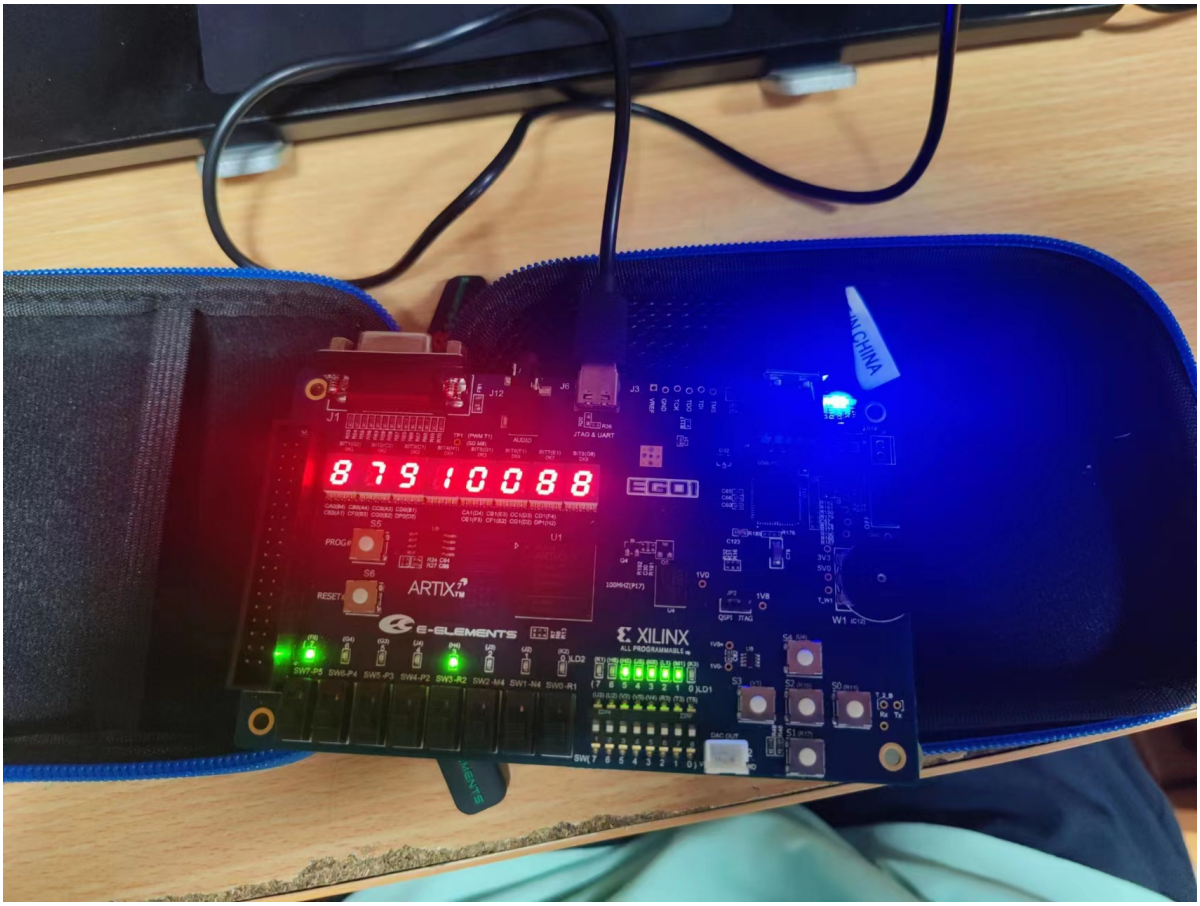
题目二

根据学号修改ram的coe：

```
memory_initialization_radix=16;
memory_initialization_vector=
00000052 ,00000010, 00000030 ,00000091, 00000000 ,00000087 ,00000078, 00000000, 00000019, 00000003, 00000001, 00000025;

```

板级验证：



汇编程序：直接用原有指令实现

```
main:
    addi x11 x0 128 // 初始化
    addi x12 x0 132
    addi x13 x0 136
    addi x4 x0 0 //从前往后依次比较，x4存储的是目前比较到的指针
    lw x15 0(x4)
    lw x16 0(x4)
    addi x8 x0 15 //计数器
    j l
ed:
    lw x20 0 x13  // 存到x20
    sw x20 0 x13
fi:
    j fi
l2:
    beq x8 x0 ed //计数器到0时退出循环
    lw x14 4(x4) //取下一个数
```

```
    add x16 x16 x14 // 更新x16
    addi x4 x4 4 //向后移动指针
    addi x8 x8 -1 //计数器-1
    sw x16 0 x12 //存到x12
    j l2
l2set:
    addi x8 x0 15 //计数器复位
    addi x4 x0 0 //指针复位
    j l2
l:
    beq x8 x0 l2set //计数器到0时退出循环
    lw x14 4(x4) //取下一个数
    add x15 x15 x14//更新x15
    addi x4 x4 4 //向后移动指针
    addi x8 x8 -1  //计数器-1
    sw x15 0 x11 //存到x11
    j l
```

Ripes 验证

Source code

```
.data
v: .4byte 0x52,0x10,0x30,0x91,0x00,0x87
.4byte 0x78,0x00,0x19,0x03,0x01,0x25
.text
main:
    addi x11 x0 128
    addi x12 x0 132
    addi x13 x0 136
    addi x4 x0 0
    lw x15 0(x4)
    lw x16 0(x4)
    addi x8 x0 15
    j l
ed:
    lw x20 0 x13
    sw x20 0 x13
fi:
    j fi
l2:
    beq x8 x0 ed
    lw x14 4(x4)
    add x16 x16 x14
    addi x4 x4 4
    addi x8 x8 -1
    sw x16 0 x12
    j l2
l2set:
    addi x8 x0 15
    addi x4 x0 0
    j l2
l:
    beq x8 x0 l2set
    lw x14 4(x4)
    add x15 x15 x14
    addi x4 x4 4
    addi x8 x8 -1
    sw x15 0 x11
    j l
```

执行后存储空间

Address	Word	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Name
0x0000000000000098	X	X	X	X	X	X	X	X	X	.text
0x0000000000000090	X	X	X	X	X	X	X	X	X	.data
0x0000000000000088	0x000000000…	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	.bss
0x0000000000000080	0x1ca5fd081…	0x08	0xfd	0xa5	0x1c	0x08	0xfd	0xa5	0x1c	
0x0000000000000078	X	X	X	X	X	X	X	X	X	
0x0000000000000070	0x000000000…	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	
0x0000000000000068	0xfe9ff06f0…	0x23	0xa0	0xf5	0x00	0x6f	0xf0	0x9f	0xfe	
0x0000000000000060	0xfff404130…	0x13	0x02	0x42	0x00	0x13	0x04	0xf4	0xff	
0x0000000000000058	0x00e787b30…	0x03	0x27	0x42	0x00	0xb3	0x87	0xe7	0x00	
0x0000000000000050	0xfe040ae3f…	0x6f	0xf0	0xdf	0xfd	0xe3	0x0a	0x04	0xfe	
0x0000000000000048	0x000002130…	0x13	0x04	0xf0	0x00	0x13	0x02	0x00	0x00	
0x0000000000000040	0xfe9ff06f0…	0x23	0x20	0x06	0x01	0x6f	0xf0	0x9f	0xfe	
0x0000000000000038	0xfff404130…	0x13	0x02	0x42	0x00	0x13	0x04	0xf4	0xff	
0x0000000000000030	0x00e808330…	0x03	0x27	0x42	0x00	0x33	0x08	0xe8	0x00	
0x0000000000000028	0xfe040ae30…	0x6f	0x00	0x00	0x00	0xe3	0x0a	0x04	0xfe	
0x0000000000000020	0x0006aa030…	0x03	0xaa	0x06	0x00	0x03	0xaa	0x06	0x00	
0x0000000000000018	0x0380006f0…	0x13	0x04	0xf0	0x00	0x6f	0x00	0x80	0x03	
0x0000000000000010	0x000228030…	0x83	0x27	0x02	0x00	0x03	0x28	0x02	0x00	
0x0000000000000008	0x000002130…	0x93	0x06	0x80	0x08	0x13	0x02	0x00	0x00	
0x0000000000000000	0x084006130…	0x93	0x05	0x00	0x08	0x13	0x06	0x40	0x08	
–	–	–	–	–	–	–	–	–	–	
–	–	–	–	–	–	–	–	–	–	
–	–	–	–	–	–	–	–	–	–	
–	–	–	–	–	–	–	–	–	–	

两个12轮循环，共触发7次赋值，总时钟周期数为94，计数器的值应为 2 × 94 = 188，因此显示88。