**Report for Lab 0**

**一、2-4译码器**

**//源代码**

module decoder2\_4(in, out);

input [1:0] in;

output reg [3:0] out;

always @(\*)

begin

case(in)

2'b00: out=4'b0001;

2'b01: out=4'b0010;

2'b10: out=4'b0100;

2'b11: out=8'b1000;

endcase

end

endmodule

**仿真截图：**

**//testbench代码**

module decoder\_tb();

wire[3:0] out;

reg[1:0] in;

initial begin

#100 in = 2'b00;

#100 in = 2'b01;

#100 in = 2'b10;

#100 in = 2'b11;

#100 $stop;

end

decoder2\_4 d(.in(in),.out(out));

endmodule

****

**二、模18计数器**

**// add.v源代码**

module add(

input rstn,

input clk,

output [4:0] cnt);

reg [4:0] cnt\_temp ;

always@(posedge clk or negedge rstn) begin

if(!rstn) begin

cnt\_temp <= 5'b00000; //当rstn 0 -> 1，cnt置零

end

else begin

if(cnt\_temp == 5'b10001) begin // 当计数器到17（二进制10001），归零

cnt\_temp <= 5'b00000;

end

else

begin

cnt\_temp <= cnt\_temp + 5'b00001; //正常计数

end

end

end

assign cnt = cnt\_temp;

endmodule

**//tb.v代码**

module add\_tb();

wire[4:0] cnt;

add U(.clk(clk), .cnt(cnt),.rstn(rstn));

reg clk,rstn;

parameter clk\_period = 10;

initial begin

rstn = 0;

clk = 0;

#50 rstn = 1;

forever

#(clk\_period/2) clk = ~clk;

end

endmodule

**仿真截图：**

