**Lab 1 实验报告**

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1. 实验目的
2. 实验平台和材料
3. 实验任务

module alu (a,b,aluc,s,z);

input [31:0] a,b;

input [3:0] aluc;

output [31:0] s;

output z;

wire z;

wire [31:0] s;

assign s = (aluc == 4'b0000)? a + b:

(aluc == 4'b1000)? a - b:

(aluc == 4'b0111)? a && b:

(aluc == 4'b0110)? a || b:

(aluc == 4'b0100)? a ^ b:

(aluc == 4'b0010)? b :

(aluc == 4'b0001)? a << b:

(aluc == 4'b0101)? a >> b:

(aluc == 4'b1101)? a >>> b:

0;

assign z = (s == 0);

endmodule

    `timescale 1ns / 1ps

    module alu\_test\_top(

        input sys\_rst\_n, //globle reset,active low,

        input sys\_clk\_in, //board system clock,100MHz

        input [4:0] sw\_pin,//sw\_pin4 to sw\_pin0

        input [4:0] dip\_pin,//dip\_pin4 to dip\_pin0

        output [7:0] seg\_data\_0\_pin,

        output [7:0] seg\_data\_1\_pin,

        output [7:0] seg\_cs\_pin,

        output [0:15] led\_pin

         );

    wire clock\_1s,zero;

    wire [31:0] aluout;

    wire[31:0] alub = {27'b0,sw\_pin[4:0]};

    wire [3:0] aluc = dip\_pin[3:0];

    //instantiate clk\_div

    clk\_div div(

        .clkin(sys\_clk\_in),

        .clkout(clock\_1s)

    );

    //instantiate alu

    alu alu(

        .a(8'h00000005),

        .b(alub),

        .aluc(aluc),

        .s(aluout),

        .z(zero)

    );

    //instantiate display

    display display(

      .clk(sys\_clk\_in),

      .reset(sys\_rst\_n),

      .s(aluout),

      .seg0(seg\_data\_0\_pin),

      .seg1(seg\_data\_1\_pin),

      .ans(seg\_cs\_pin)

    );

    endmodule

1. 实验结果
2. 总结

