上 海 交 通 大 学 试 卷（B 卷）

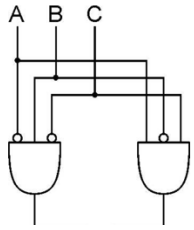
（ 2022 至 2023 学年 第 1 学期 ）

班级号_____ 学号_____ 姓名 _____

课程名称 _____计算机组成_____ 成绩 _____

I. Single choice (20')

1. When ABC=010, the output of the circuit in the figure is (from left to right) ( ).



A. 00 B. 01 C. 10 D. 11

2. Assuming that the word length of the machine is 64 bits and the storage capacity is 128MB. If it is addressed by word, the number of addressable units is ( ).

A. 8M B. 16M C. 32M D. 64M

3. In the 8086 CPU, assuming DS=1300H, SS=2400H, BX=1370H, SI=2600H, DI=5210H, BP=3600H, AX=1024H, after executing the following instructions, which of the corresponding physical addresses and values are correct? ( )

A. MOV [129H], AH; physical address: 1429H; value : 10H
B. MOV [BX], AL ; physical address: 25370H; value : 24H
C. MOV [BP]+48, AX; physical address: 27648; value : 24H
D MOV [SI]+38, AX; physical address: 15639; value : 24H

4. Assuming that a sub instruction is executed, the states of the CF and SF flag registers after calculating 5394H-777FH are ( ) respectively.

A.0,0 B. 0,1 C. 1,0 D. 1,1

5. Which of the following 8086 assembly statements is wrong? ( )

A.MOV AX，CX B.XOR AX, CX C.ADD 10,SUM D.DIV 10

6. In 8086 processor, when executing INT instruction, NMI and INTR interrupts are generated at the same time, so the CPU detects interrupt requests in the following order: ( )

A. NMI、INT instruction、INTR B．NMI、INTR、INT instruction

C. INTR、INT instruction、NMI D．INT instruction、NMI、INTR

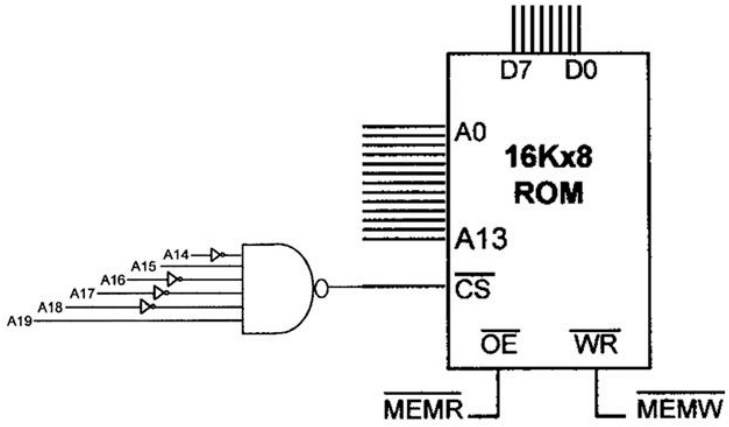
7. If the content of the register is 10100100, the code is ( ) of -92.

A. original code B. two's complement C. one's complement D. BCD code

8. Which of the following declarations defines a 32-bit variable? ( )

A．DB B.DW C.DD D.DQ

9. The address range of the following memory chip is ( ).



A. 88000H~8BFFFH B. 74000H~77FFH C. 8800H~8BFFH D. 7400H~77FFH

10. To keep the higher 4 bit unchanged of the register and change all the lower 4 bits to 1, we need to use instruction ( ).

A. AND AL, 0F0H B. AND AL, 0FH

C. OR AL, 0F0H D. OR AL, 0FH

11. Which of the following statements about the basic idea of Von Neumann Architecture is wrong? ( )

A. The functions of the program are realized through the execution of instructions by the CPU.

B. Instructions and data are represented by binary numbers, and there is no difference in form.

C. The instruction is accessed by address, and the data is directly given in the instruction.

D. Before the program is executed, the instructions and data need to be stored in the memory in advance.

12. Among various I/O methods, the interrupt method is characterized by ( ).

A. CPU and peripherals work serially, data transmission and the main program work serially.

B. CPU and peripherals work in parallel, data transmission and the main program work serially.

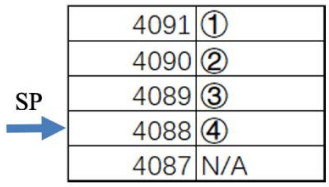
C. CPU and peripherals work serially, data transmission and the main program work in parallel.

D. CPU and peripherals work in parallel, data transmission and the main program work in parallel.

13. Suppose SS=2300H, SP=1500H. After the 8086 CPU executes 3 times of PUSH AX and 1 time of PUSH BX, the values of SS and SP are ( ) respectively.

A. 2300H:14F8H B. 2300H:14FCH C. 22FCH:1500H D. 22F8H:1500H

14. After the ret instruction of a certain function is called, the returned CS:IP is 00ACH:3090H. Before calling the ret instruction, the content of the stack in the figure below is ( ).



A.①00 ②AC ③30 ④90
B.①30 ②90 ③00 ④AC
C.①AC ②00 ③90 ④30
D.①90 ②30 ③AC ④00

15. When the 8086 CPU executes IN AL, 24H instructions, the states of the external pins $\overline{RD}$, M/$\overline{IO}$, $\overline{WR}$ are ( ) respectively.

A. 0,0,0 B. 0,0,1 C. 1,0,0 D. 1,1,1

16. In 8086 interrupt vector table, if 34H, FEH, 00H and F0H are stored sequentially from address 0003CH to higher address, the interrupt type and the entry address of the interrupt service program are ( ).

A. 0FH，F000H：FE34H B. 0FH，00F0H：34FEH
C. 0EH，34FEH：00F0H D. 0EH，F000H：FE34H

17. Which jump instruction uses CF for condition judgment? ( )

①JC ②JAE ③JGE ④JBE
A. ① ② B. ① ② ③
C. ① ② ④ D. ② ③ ④

18. For this assembly code, the value of AX after executing ① and ② are respectively ( ).

MOV AX, 7100H
SUB AX, 8000H ;①
ADC AX,1H ;②
A. 100H, 101H B. 100H, 102H C. F100H, F101H D. F100H, F102H

19. If the control number of 8253 is 0B2H, then the counter and mode are respectively ( ).

A. 2,1 B. 2,3 C. 3,0 D. 1,2

20. Which of the following descriptions of DMA is wrong? ( )

A. DMA transfer is hardware operation: it transfers data from memory to device or from device to memory.
B. For keyboard and mouse data input, DMA is more efficient than interrupt-driven I/O.
C. Data transmission stage of DMA is CPU-free.
D. DMA needs to use interrupt processing.

II. Fill in Blanks (20’)

1. In 8086 systems, assume that SS:SP is 2000H:1000H and AX=1234H, after executing PUSH AX, byte 12H and byte 34H are stored at physical address _____and _____, respectively.

2. Different types of memory form a _____in a computer system, which can obtain a tradeoff between data access performance and cost because_____

_____.

3. In asynchronous serial communication, baud factor refers to _____, which is set to _____.

4. In 8086 systems, “INT 21H” can be used to call the ISR of DOS, which _____(can/cannot) be masked; the entrance address of the ISR is stored at physical address _____H；before entering the ISR, IF of 8086 is cleared, which means _____; when returning from the ISR, the IRET instruction is used, what is the difference between IRET and RETF? _____

_____.

5. Modern CPUs support instruction pipeline technique. A _____(CISC/RISC) instruction set design can better suit instruction pipeline. The 8086 is a _____(CISC/RISC) CPU, which integrates two components, i.e., _____and_____, respectively, forming a _____-stage instruction pipeline. These two components can work simultaneously because_____.

6. An 8-bit number 0FFH in 2’s complement represents integer _____.

7. 8259 is used to manage interrupts in 8086 systems. Which are the two factors that determine whether an interrupt request IR issued from some device can make 8259 issue an effective INT signal to the CPU? _____

_____and_____. The purpose of an EOI command of 8259 is to

_____.

III. Answer Questions (25’)

1. Answer the following questions about (4’)

1) Briefly describe the advantages and disadvantages of the two address decoding methods (i.e., absolute and linear select) for I/O ports (one for each).

2) Briefly describe the interrupt response process.

2. Use several 512K×8-bit memory chip(s) to form a 4M×32-bit memory chip. The memory is addressed by byte. Answer the following questions: (9’)

1) How many 512K×8-bit memory chips are needed? (1’)

2) What are the number of the data lines and that of the address lines of this 4M×32-bit memory chip? (2’)

3) Describe the function of each address line of this 4M×32-bit memory chip. (3’)

4) Is a decoder required to form the 4M×32-bit memory chip? If needed, draw the circuit of the decoder, and label the input address lines. If not, please explain the reason. (3’)

3. Given the C/C++ code below, answer the questions.(12’)

```
int factorial(int n)
{
   if(n <= 1)
   {
      return 1;
   }
   return n * factorial(n - 1);
}
```

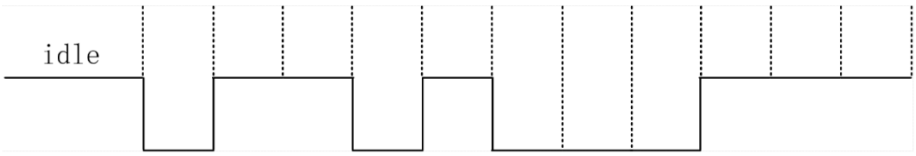
1) Write the non-recursive C/C++ form of the above recursive code. (3’)

2) Convert recursive and non-recursive code to assembly code. (6’)

3) Compare the performance of recursive and non-recursive method and explain the reason. (3’)

IV. Applications (35’)

1. A computer exchanges data with another one via asynchronous serial communication using 7-bit characters, 1 parity bit, 1 stop bit, and the baud factor is 16. Given the following figure which depicts a transmitted character, please answer all requirements. (7’)

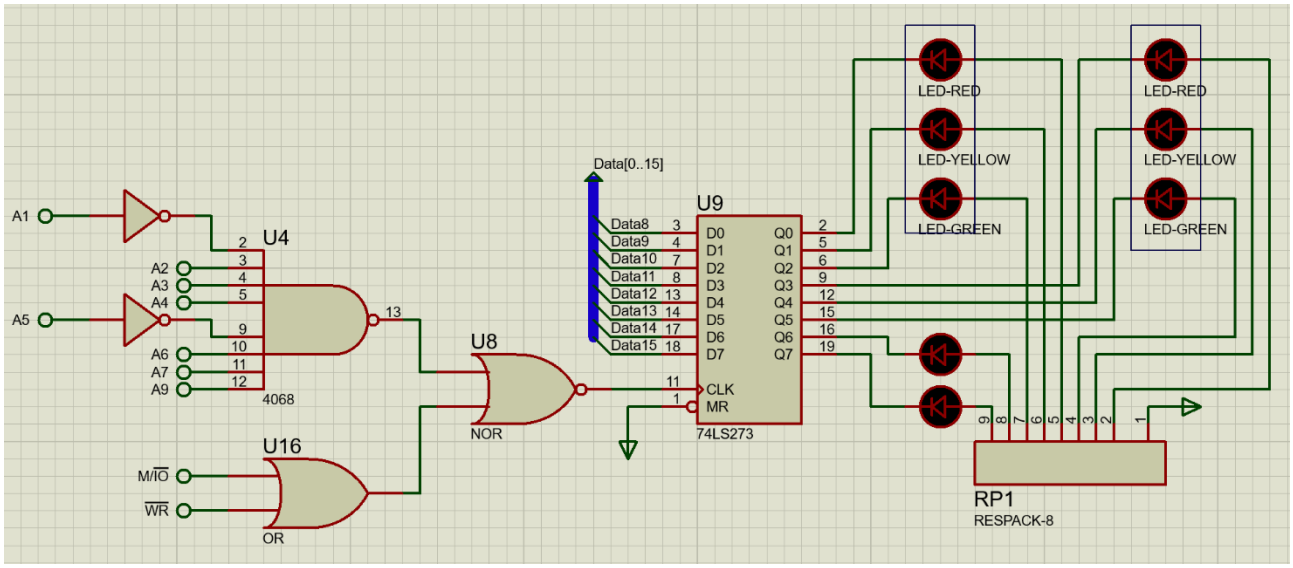


1) Mark the start bit and the stop bit respectively on the figure. (2’)
2) What is the transmitted character? (2’)

3) Odd parity or even parity? (1’)

4) If symbol rate is 9600 bauds, what is the bit rate? (2’)

2. 8086 is executing the following instructions which send the data stored in the memory at a specific address to an output port. Assume that DS=1000H, and byte 81H, 82H, and 83H are stored at 11000H, 11001H, and 11002H, respectively. Please answer the following requirements. (9’)



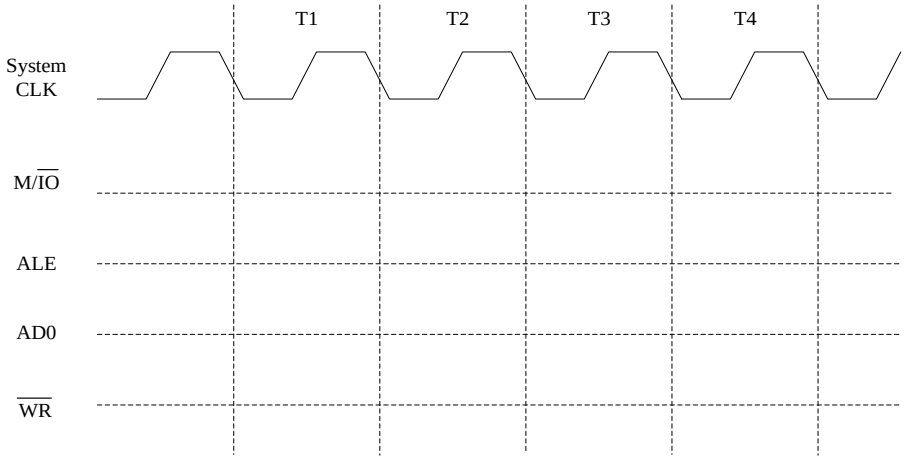

```
MOV AX, [1001H]    ;①
MOV DX, _______H   ;②
OUT DX, AL         ;③
MOV AL, AH
```

```
OUT DX, AL
```

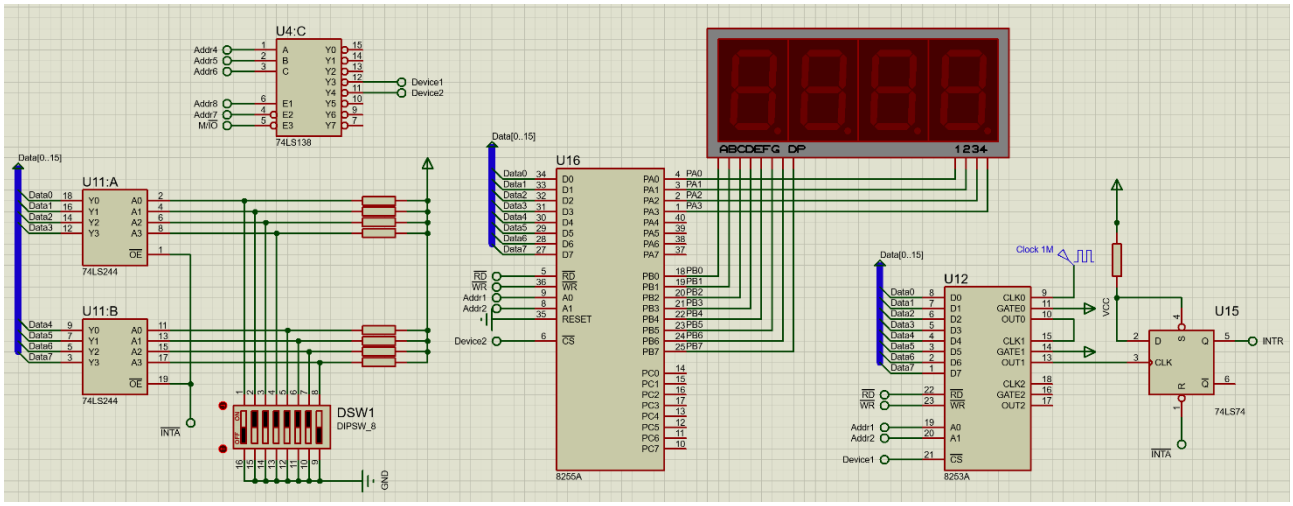
1) How many bus cycles would the instruction at ① take? Please give detailed explanation on each bus cycle including how CPU coordinates the address bus, the control bus and the data bus to obtain a piece of data from the memory. (4’)

2) The port number at ② is _____H. (1’)

3) Please draw the following signals when executing the instruction at ③. (4’)



3. The following schematic shows a timer application, where the OUT1 of 8253 generates an interrupt request on every 1 second, making the timer count down by 1 second until the timer meets terminal count 0. The current count is displayed on the 4-digit LED tubes with the format MM.SS, where MM is the left minutes and SS is the left seconds. Assume that the initial count is 10.00. Please finish the following program. (19’)



1) Identify the port numbers of 8253 and 8255 (all unused system address lines take the value of 0) (3')

```
; 8253
L8253T0         EQU     _______H    ; Timer0's port number
L8253T1         EQU     _______H    ; Timer1's port number
L8253CS         EQU     _______H    ; 8253 Control Register's port number
; 8255
L8255PA         EQU     _______H    ; Port A's port number
L8255PB         EQU     _______H    ; Port B's port number
L8255CS         EQU     _______H    ; 8255 Control Register's port number
```

2) Data segment definition (2')

```
; SEGTAB is the code for displaying "0-F" on 7-Segment Tube
  SEGTAB    DB 3FH ;
            DB 06H ;
            DB 5BH ;          a a a
            DB 4FH ;        f       b
            DB 66H ;        f       b
            DB 6DH ;        f       b
            DB 7DH ;          g g g
            DB 07H ;        e       c
            DB 7FH ;        e       c
            DB 6FH ;        e       c
            DB 77H ;          d d d    h h h
            DB 7CH ; ----------------------------------
            DB 39H ;      b7 b6 b5 b4 b3 b2 b1 b0
            DB 5EH ;      DP  g  f  e  d  c  b  a
            DB 79H ;
```

```
            DB 31H ;
; SEGTAB1 is the code for displaying "0.-F." (2')
  SEGTAB1   DB ___H, ___H, ___H, ___H, 0E6H, 0EDH, 0FDH, 87H
            DB 0FFH, 0EFH, 0F7H, 0FCH, 0B9H, 0DEH, 0F9H, 0B1H
; Any other variables that your code needs
```

3) Initialization of 8253 (2')

```
INIT8253 PROC
; Set the mode and the initial count for Timer0


; Set the mode and the initial count for Timer1



RET
INIT8253 ENDP
```

4) Initialization of 8255 (1')

```
INIT8255 PROC
  ; Init 8255 in Mode x, L8255PA xPUT, L8255PB xPUT


  RET
INIT8255 ENDP
```

5) Identify the interrupt type; set up the IVT; and complete the ISR (5')

```
IRQNum      EQU    _______H   ; INT type (1')

INT_INIT    PROC   FAR    ; set up the IVT (2')
  CLI           ; Disable interrupt
  MOV AX, 0
  MOV ES, AX    ; To set up the interrupt vector table
  ; Put your code from here
```

```
  RET
INT_INIT ENDP

MYIRQ   PROC FAR  ; complete the ISR (2')
  ; Put your code here



  ; 中断返回

MYIRQ   ENDP
```

6) Display control using 8255 (6')

```
DISPLAY8255 PROC
  ; Put your code here
```

```
  RET
DISPLAY8255 ENDP
```