Q1.

Top file

```
module top(
input clk_100M,
input switch,
output [3:0] anode,
output [7:0] cathode
   );

wire clk_5M,clk_1K,clk_1, clk_2;

clk_wiz_0 clk_gen(.clk_in1(clk_100M), .clk_out1(clk_5M));

//1K
clk_div #(12) u1( .clk_in(clk_5M) , .clk_out(clk_1K));
//1Hz
clk_div #(22) u2( .clk_in(clk_5M) , .clk_out(clk_1));

wire [3:0] count;

counter c1(.clk(clk_1), .count(count));

seven_segment u10(.clk(clk_1K), .COUNT(count), .anode(anode), .cathode(cathode));


endmodule
```

Q2.

TOP FILE

```
module top(
input clk_100M,
input switch,
output [3:0] anode,
output [7:0] cathode
   );

wire clk_5M,clk_1K,clk_1, clk_2;

clk_wiz_0 clk_gen(.clk_in1(clk_100M), .clk_out1(clk_5M));

//1K
```

```
clk_div #(12) u1( .clk_in(clk_5M) , .clk_out(clk_1K));
//1Hz
clk_div #(22) u2( .clk_in(clk_5M) , .clk_out(clk_1));
//2Hz
clk_div #(21) u3( .clk_in(clk_5M) , .clk_out(clk_2));

wire [3:0] count;
reg CLK;
always @(*)
begin
   case(switch)
      1'b0: CLK=clk_1;
      1'b1: CLK=clk_2;
      default:  CLK=clk_1;
   endcase
end
counter c1(.clk(CLK), .count(count));

seven_segment u10(.clk(clk_1K), .COUNT(count), .anode(anode), .cathode(cathode));


endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 21.09.2019 13:09:29
// Design Name:
// Module Name: clk_div
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

module clk_div
   #(
      parameter divide_by = 19
    )
    ( input clk_in,
    output clk_out );
    reg [divide_by-1:0] count = 0 ;

    always @ (posedge clk_in)
    begin
      count = count+1 ;
    end

    assign clk_out = count[divide_by-1] ;

endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 21.09.2019 13:16:22
// Design Name:
// Module Name: counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module counter(
input clk,
output [3:0] count

   );

reg [3:0] count_temp=4'd1;

always @(posedge clk)
begin
   if(count_temp==4'd8)
      count_temp=4'd1;
   else
      count_temp=count_temp+1;
end


assign count=count_temp;

endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 21.09.2019 13:27:31
// Design Name:
// Module Name: seven_segment
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module seven_segment(
input clk,
input [3:0] COUNT,
output [3:0] anode,
output [7:0] cathode
   );


reg [6:0] cathode_temp= 7'b1111111;
reg [3:0] anode_temp= 4'b1110;
reg [1:0] count=2'b00;

always @(posedge clk)
   begin
      count=count+1;
   end


always @(*)
   begin
     case(count)
     2'b00:
     begin
         case(COUNT)
            4'd4 : cathode_temp = 7'b0011100; //to display 4
            4'd5 : cathode_temp = 7'b1100010; //to display 8
```

```
            default : cathode_temp = 7'b1111111;
          endcase

         anode_temp = 4'b1110;
        end

       2'b01:
       begin
          case(COUNT)
            4'd3 : cathode_temp = 7'b0011100; //to display 3
            4'd6 : cathode_temp = 7'b1100010; //to display 6
            default : cathode_temp = 7'b1111111;
          endcase

         anode_temp = 4'b1101;
        end

       2'b10:
       begin
        case(COUNT)
            4'd2 : cathode_temp = 7'b0011100; //to display 0
            4'd7 : cathode_temp = 7'b1100010; //to display 1
            default : cathode_temp = 7'b1111111;
         endcase

         anode_temp = 4'b1011;
        end

       2'b11:
       begin
        case(COUNT)
            4'd1 : cathode_temp = 7'b0011100; //to display 0
            4'd8 : cathode_temp = 7'b1100010; //to display 1
            default : cathode_temp = 7'b1111111;
         endcase

         anode_temp = 4'b0111;
        end
      endcase
     end

    assign anode = anode_temp;
    assign cathode = {cathode_temp, 1'b1};


endmodule
```

CONSTRAINTS FILE (Q1, Q2)

```
set_property PACKAGE_PIN W5 [get_ports clk_100M]

        set_property IOSTANDARD LVCMOS33 [get_ports clk_100M]

set_property PACKAGE_PIN V17 [get_ports {switch}]
        set_property IOSTANDARD LVCMOS33 [get_ports {switch}]


set_property PACKAGE_PIN U2 [get_ports {anode[0]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {anode[0]}]
set_property PACKAGE_PIN U4 [get_ports {anode[1]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {anode[1]}]
set_property PACKAGE_PIN V4 [get_ports {anode[2]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {anode[2]}]
set_property PACKAGE_PIN W4 [get_ports {anode[3]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {anode[3]}]

set_property PACKAGE_PIN W7 [get_ports {cathode[7]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[7]}]
set_property PACKAGE_PIN W6 [get_ports {cathode[6]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[6]}]
set_property PACKAGE_PIN U8 [get_ports {cathode[5]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[5]}]
set_property PACKAGE_PIN V8 [get_ports {cathode[4]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[4]}]
set_property PACKAGE_PIN U5 [get_ports {cathode[3]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[3]}]
set_property PACKAGE_PIN V5 [get_ports {cathode[2]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[2]}]
set_property PACKAGE_PIN U7 [get_ports {cathode[1]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[1]}]
set_property PACKAGE_PIN V7 [get_ports {cathode[0]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[0]}]
```

Q3 (all files)

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 21.09.2019 12:46:56
// Design Name:
// Module Name: top
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module top(
input clk_100M,
input switch,
output anode1,
output [6:0] cathode1,
output [3:0] anode,
output [7:0] cathode
   );

wire clk_5M,clk_1K,clk_1, clk_2;

clk_wiz_0 clk_gen(.clk_in1(clk_100M), .clk_out1(clk_5M));

//1K
clk_div #(12) u1( .clk_in(clk_5M) , .clk_out(clk_1K));
//1Hz
clk_div #(22) u2( .clk_in(clk_5M) , .clk_out(clk_1));
//2Hz
clk_div #(21) u3( .clk_in(clk_5M) , .clk_out(clk_2));

wire [3:0] count;
```

```
reg CLK;
always @(*)
begin
   case(switch)
      1'b0: CLK=clk_1;
      1'b1: CLK=clk_2;
      default:  CLK=clk_1;
   endcase
end
counter c1(.clk(CLK), .count(count));


seven_segment u10(.clk(clk_1K), .COUNT(count), .anode(anode), .cathode(cathode));
seven_PMOD p10(.clk(clk_1K), .COUNT(count), .anode(anode1), .cathode(cathode1));


endmodule




`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 21.09.2019 13:09:29
// Design Name:
// Module Name: clk_div
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

module clk_div
   #(
      parameter divide_by = 19
    )
    ( input clk_in,
    output clk_out );
```

```
    reg [divide_by-1:0] count = 0 ;

    always @ (posedge clk_in)
    begin
      count = count+1 ;
    end

    assign clk_out = count[divide_by-1] ;

endmodule



`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 21.09.2019 13:16:22
// Design Name:
// Module Name: counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module counter(
input clk,
output [3:0] count

   );

reg [3:0] count_temp=4'd1;

always @(posedge clk)
begin
   if(count_temp==4'd12)
      count_temp=4'd1;
   else
```

```
      count_temp=count_temp+1;
end


assign count=count_temp;

endmodule




`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 21.09.2019 13:27:31
// Design Name:
// Module Name: seven_segment
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module seven_segment(
input clk,
input [3:0] COUNT,
output [3:0] anode,
output [7:0] cathode
   );


reg [6:0] cathode_temp= 7'b1111111;
reg [3:0] anode_temp= 4'b1110;
reg [1:0] count=2'b00;

always @(posedge clk)
   begin
      count=count+1;
```

```
    end


always @(*)
    begin
      case(count)
      2'b00:
      begin
          case(COUNT)
             4'd4 : cathode_temp = 7'b0011100; //to display 4
             4'd9 : cathode_temp = 7'b1100010; //to display 8
             default : cathode_temp = 7'b1111111;
         endcase

        anode_temp = 4'b1110;
       end

      2'b01:
      begin
          case(COUNT)
             4'd3 : cathode_temp = 7'b0011100; //to display 3
             4'd10 : cathode_temp = 7'b1100010; //to display 6
             default : cathode_temp = 7'b1111111;
          endcase

        anode_temp = 4'b1101;
       end

      2'b10:
      begin
        case(COUNT)
             4'd2 : cathode_temp = 7'b0011100; //to display 0
             4'd11 : cathode_temp = 7'b1100010; //to display 1
             default : cathode_temp = 7'b1111111;
         endcase

        anode_temp = 4'b1011;
       end

      2'b11:
      begin
        case(COUNT)
             4'd1 : cathode_temp = 7'b0011100; //to display 0
             4'd12 : cathode_temp = 7'b1100010; //to display 1
             default : cathode_temp = 7'b1111111;
        endcase

        anode_temp = 4'b0111;
```

```
        end
      endcase
     end

    assign anode = anode_temp;
    assign cathode = {cathode_temp, 1'b1};


endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 21.09.2019 15:05:10
// Design Name:
// Module Name: seven_PMOD
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module seven_PMOD(

   input clk,
input [3:0] COUNT,
output anode,
output [6:0] cathode
   );
```

```
reg [6:0] cathode_temp= 7'b0000000;
reg anode_temp= 1'b0;
reg  count=0;

always @(posedge clk)
   begin
      count=count+1;
   end


always @(*)
   begin
     case(count)
     1'b0:
     begin
         case(COUNT)
            4'd5 : cathode_temp = 7'b1100011; //to display 4
            4'd8 : cathode_temp = 7'b0011101; //to display 8
            default : cathode_temp = 7'b0000000;
        endcase

        anode_temp = 1'b1;
       end

      1'b1:
      begin
          case(COUNT)
            4'd6 : cathode_temp = 7'b1100011; //to display 3
            4'd7 : cathode_temp = 7'b0011101; //to display 6
            default : cathode_temp = 7'b0000000;
          endcase

        anode_temp = 1'b0;
       end

     endcase
    end

    assign anode = anode_temp;
    assign cathode = {cathode_temp+1'b1};


endmodule
```

```
set_property PACKAGE_PIN W5 [get_ports clk_100M]

        set_property IOSTANDARD LVCMOS33 [get_ports clk_100M]

set_property PACKAGE_PIN V17 [get_ports {switch}]
        set_property IOSTANDARD LVCMOS33 [get_ports {switch}]


set_property PACKAGE_PIN U2 [get_ports {anode[0]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {anode[0]}]
set_property PACKAGE_PIN U4 [get_ports {anode[1]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {anode[1]}]
set_property PACKAGE_PIN V4 [get_ports {anode[2]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {anode[2]}]
set_property PACKAGE_PIN W4 [get_ports {anode[3]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {anode[3]}]

set_property PACKAGE_PIN W7 [get_ports {cathode[7]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[7]}]
set_property PACKAGE_PIN W6 [get_ports {cathode[6]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[6]}]
set_property PACKAGE_PIN U8 [get_ports {cathode[5]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[5]}]
set_property PACKAGE_PIN V8 [get_ports {cathode[4]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[4]}]
set_property PACKAGE_PIN U5 [get_ports {cathode[3]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[3]}]
set_property PACKAGE_PIN V5 [get_ports {cathode[2]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[2]}]
set_property PACKAGE_PIN U7 [get_ports {cathode[1]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[1]}]
set_property PACKAGE_PIN V7 [get_ports {cathode[0]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cathode[0]}]




set_property PACKAGE_PIN A14 [get_ports {cathode1[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[0]}]
set_property PACKAGE_PIN A16 [get_ports {cathode1[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[1]}]
set_property PACKAGE_PIN B15 [get_ports {cathode1[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[2]}]
set_property PACKAGE_PIN B16 [get_ports {cathode1[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[3]}]
set_property PACKAGE_PIN K17 [get_ports {cathode1[4]}]
```

```
        set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[4]}]
set_property PACKAGE_PIN M18 [get_ports {cathode1[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[5]}]
set_property PACKAGE_PIN N17 [get_ports {cathode1[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[6]}]


set_property PACKAGE_PIN P18 [get_ports {anode1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {anode1}]
```