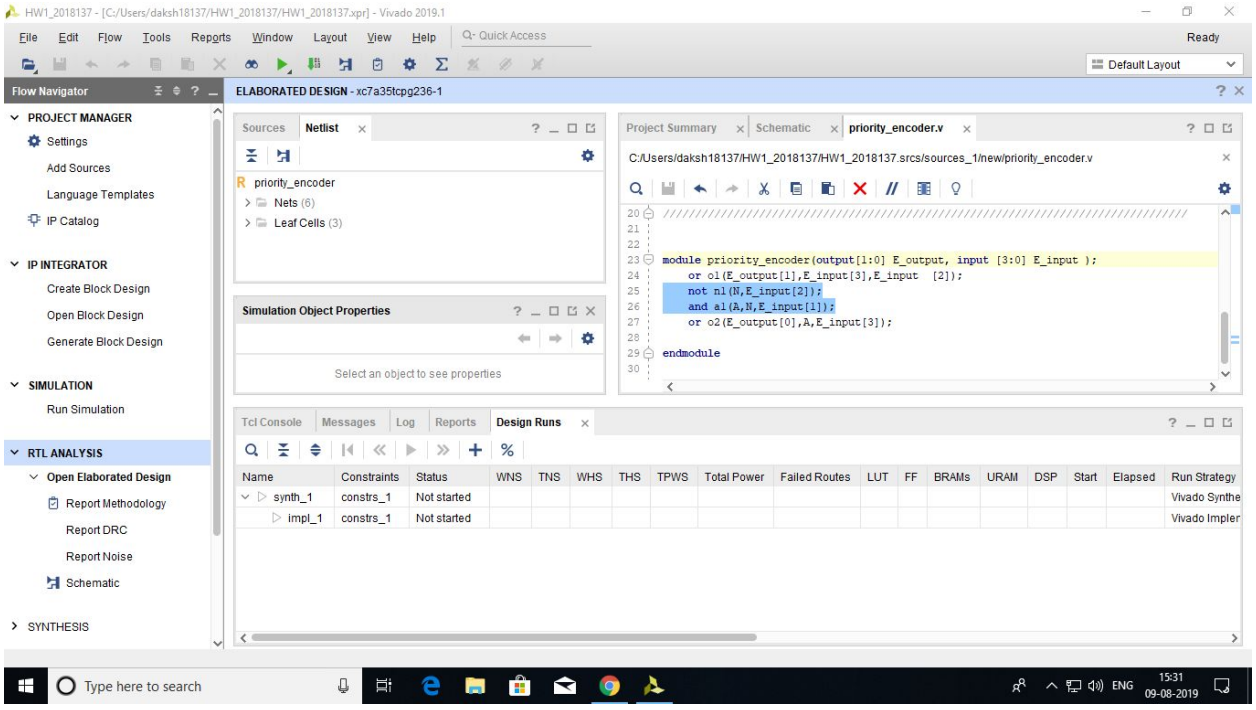
HW1 ELD

PRIORITY ENCODER 4:2

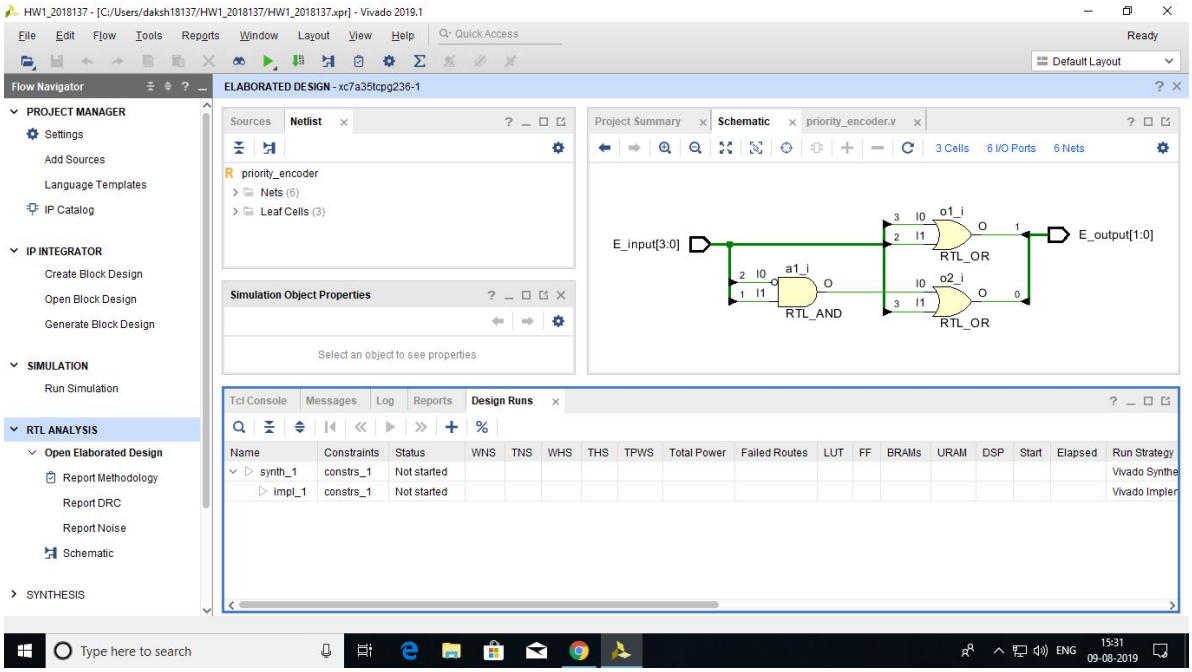
Daksh Thapar 2018137 (grp 2)

Verilog code

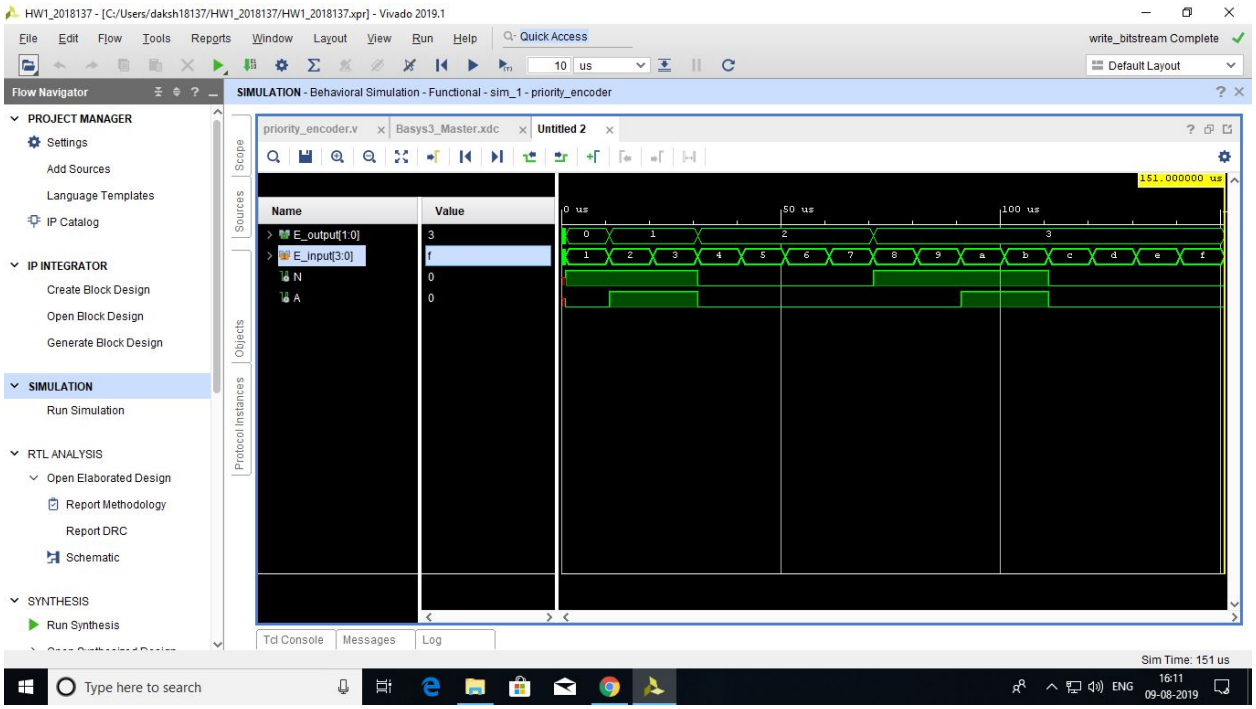
```
module priority_encoder(output[1:0] E_output, input [3:0] E_input );
    or o1(E_output[1],E_input[3],E_input  [2]);
    not n1(N,E_input[2]);
    and a1(A,N,E_input[1]);
    or o2(E_output[0],A,E_input[3]);
endmodule
```



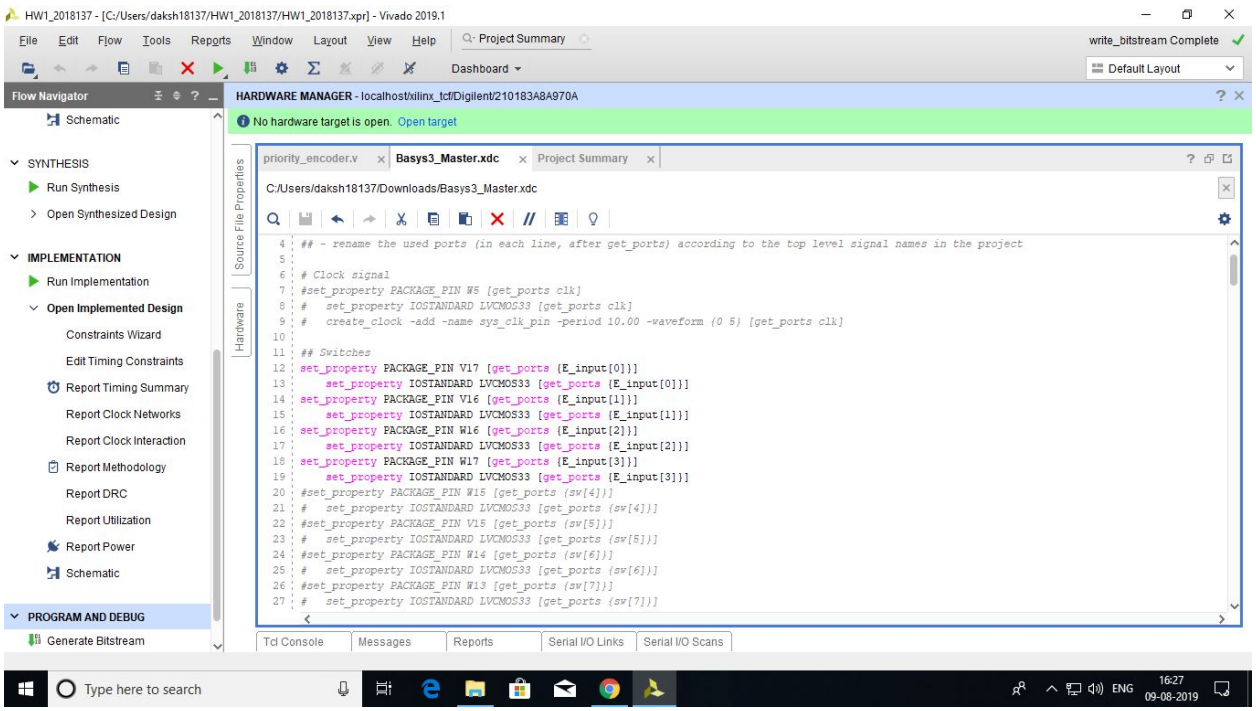
Elaborated Design after RTL analysis



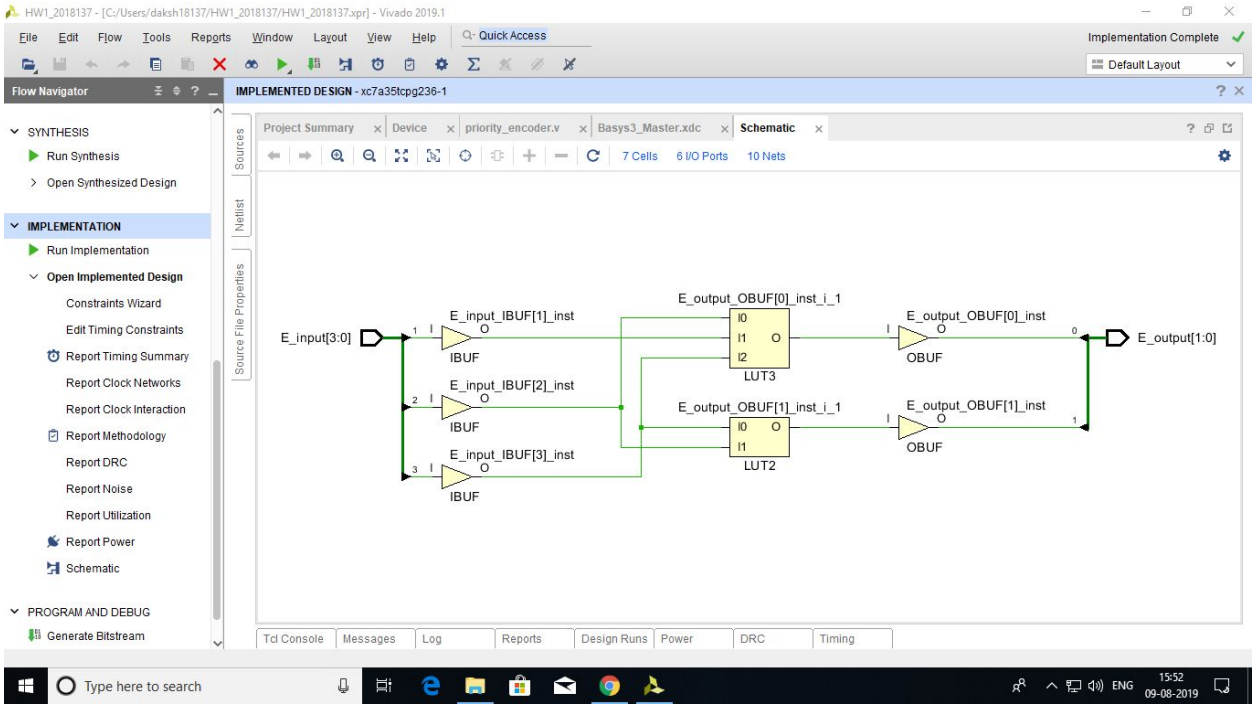
Output waveform for all possible inputs



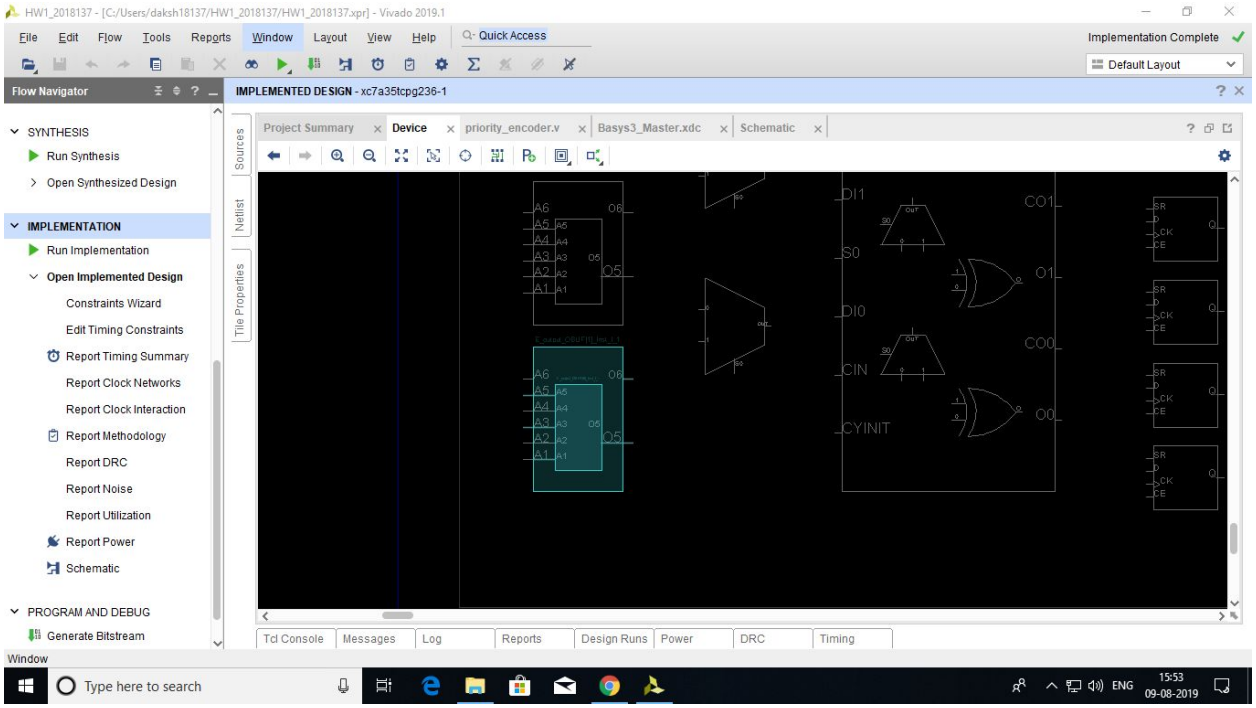
Constraint- file uploaded



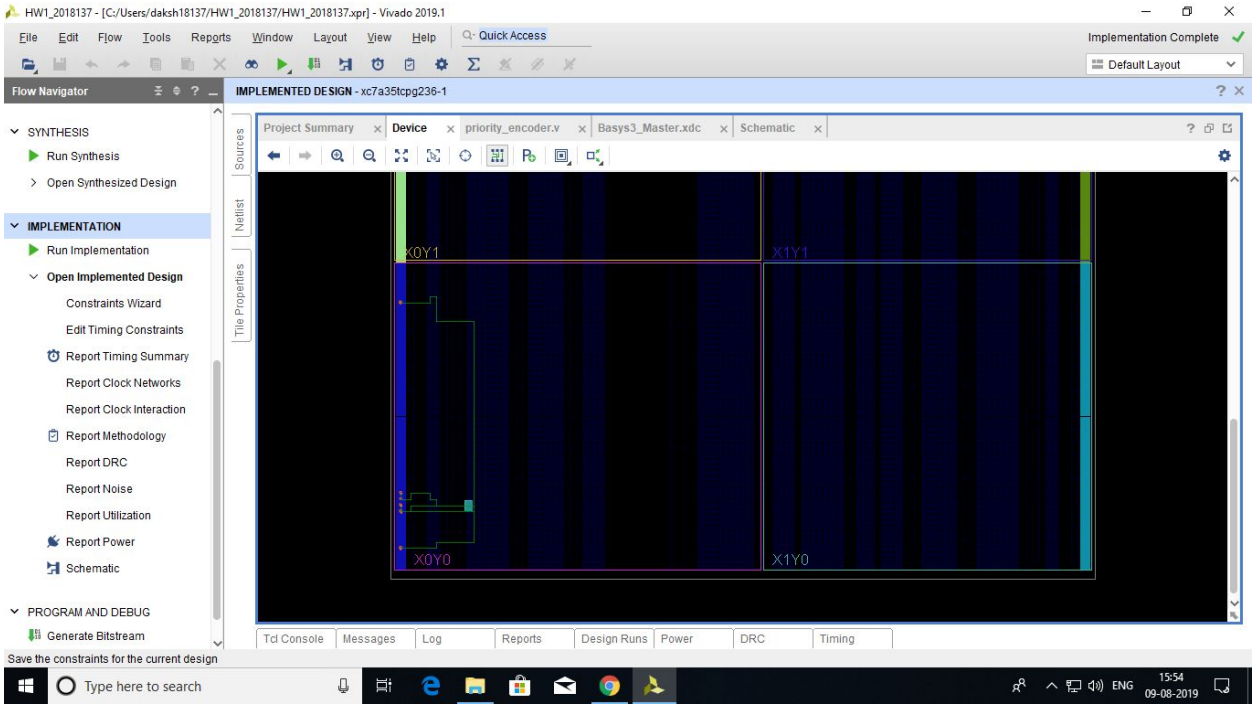
Design after Synthesis

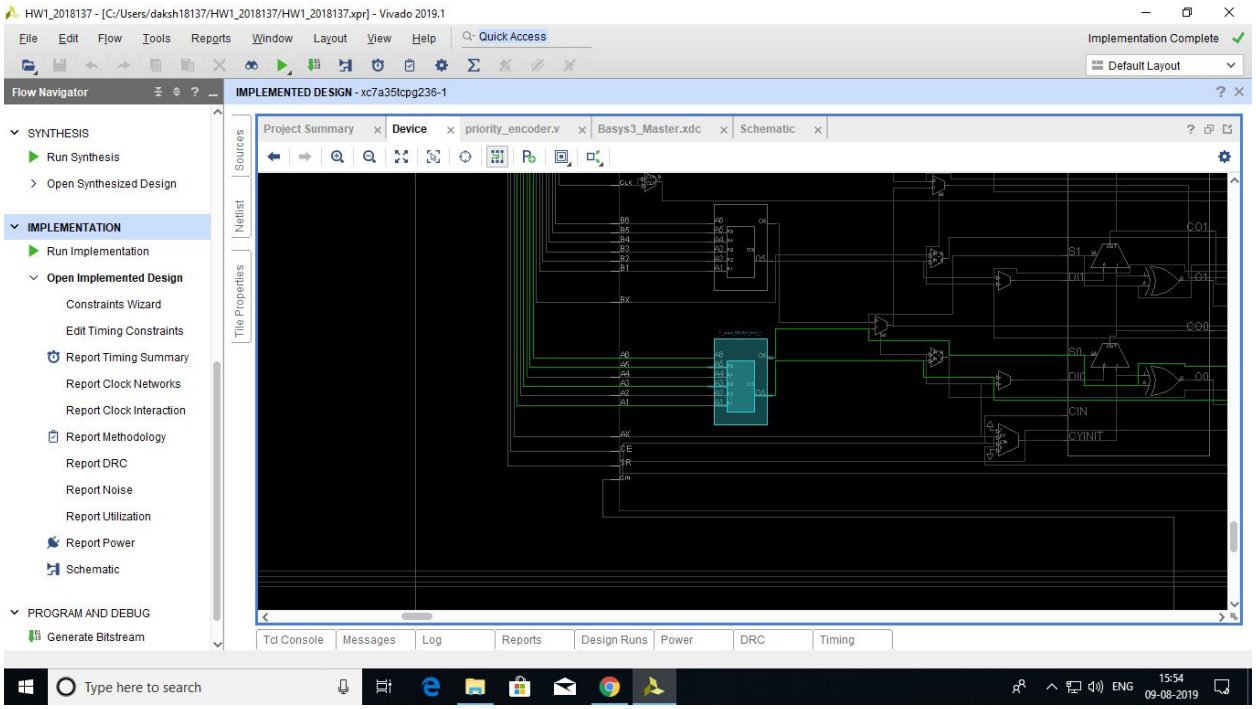


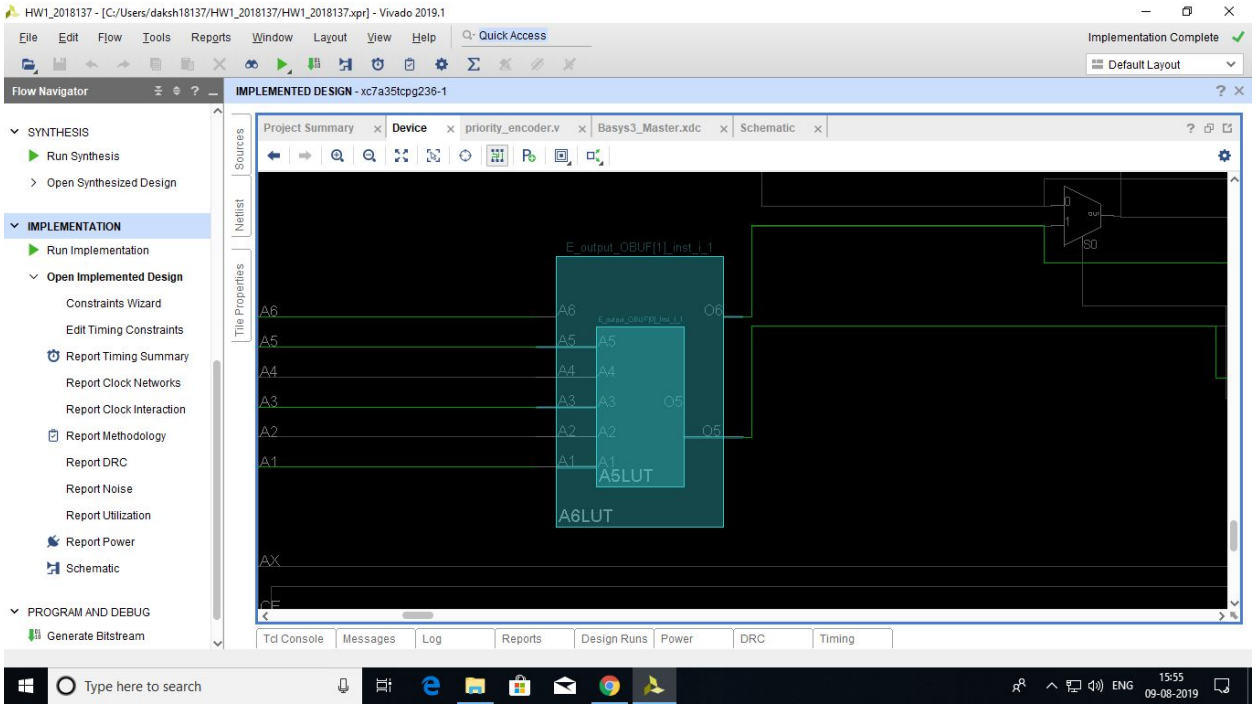
Device Layout before routing



Device Layout after routing




HW1_2018137 - [C:/Users/daksh18137/HW1_2018137/HW1_2018137.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a35tcpg236-1
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Project Summary
Device
priority_encoder.v
Basys3_Master.xdc
Schematic
Sources
Netlist
Tile Properties
CO1
O1
CO0
O0
CIN
CYINIT
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Type here to search
ENG
15:54
09-08-2019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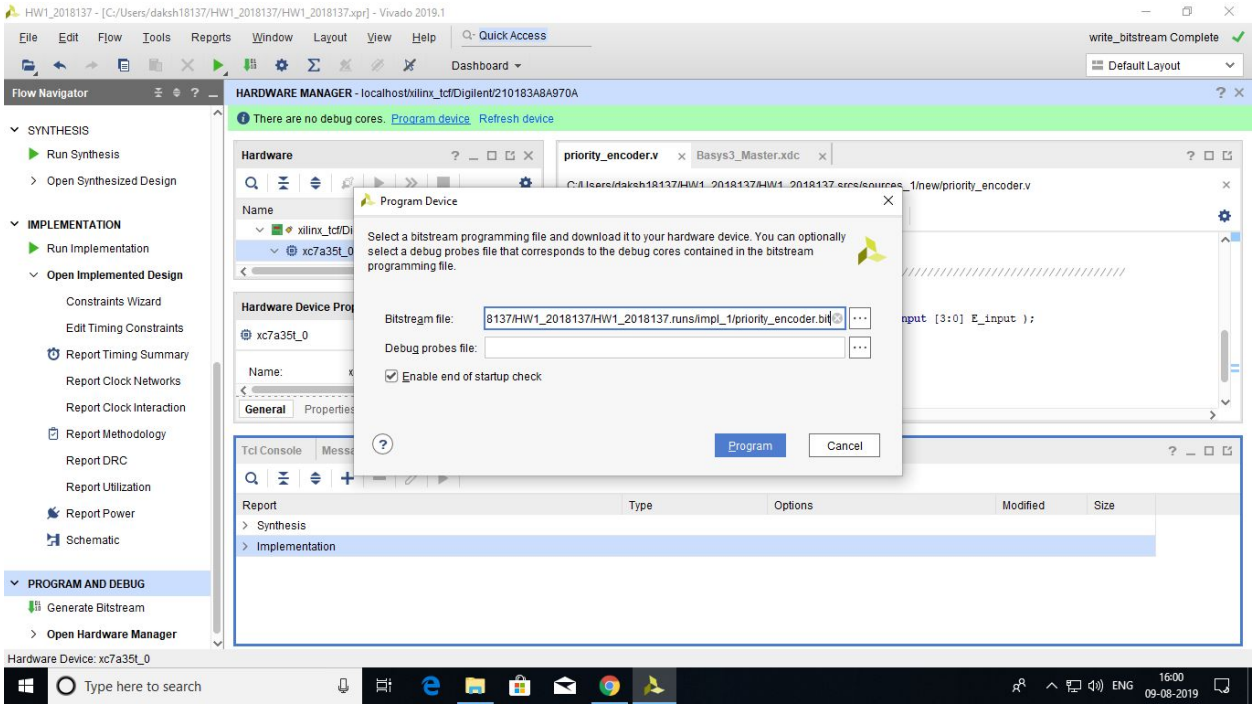
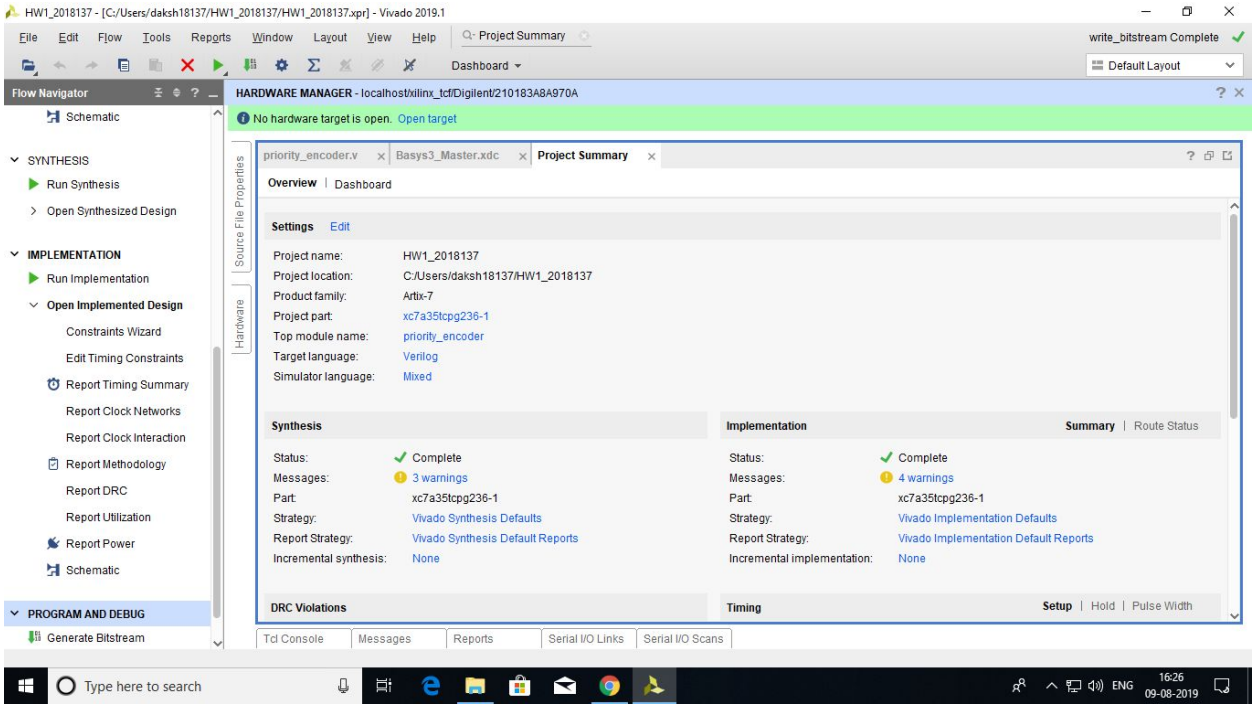
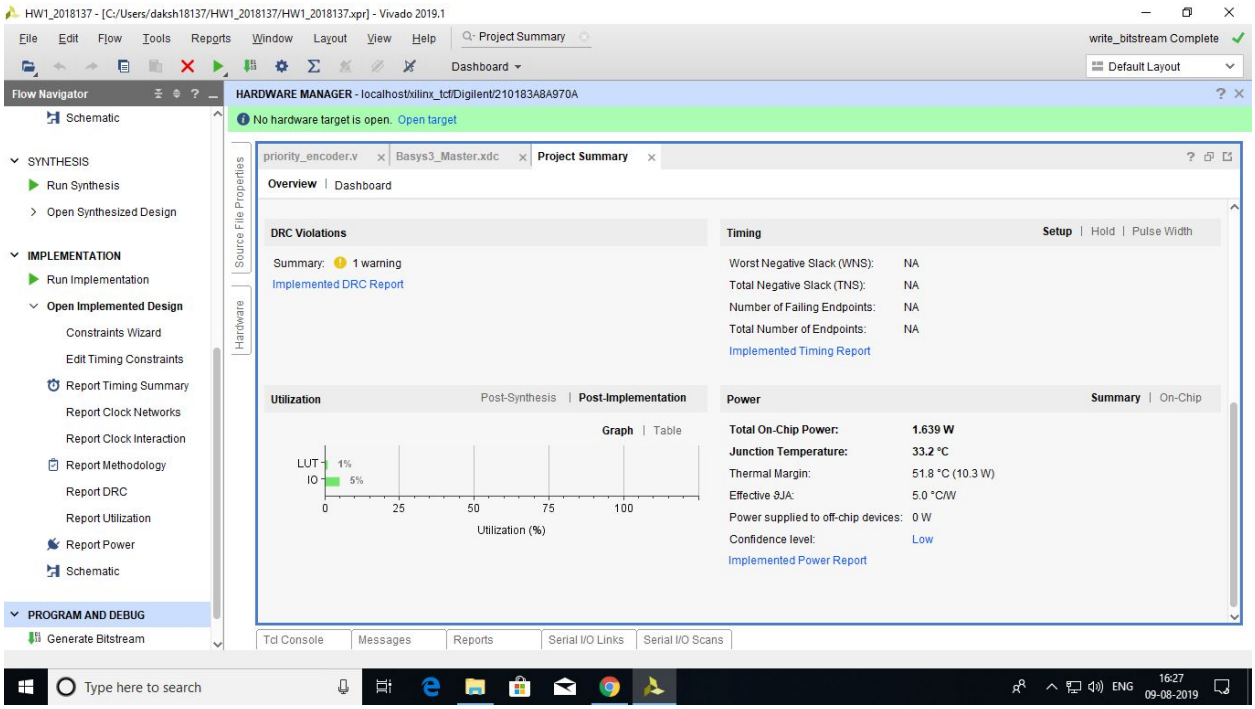
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Project Summary
Device
priority_encoder.v
Basys3_Master.xdc
Schematic
Sources
Netlist
Tile Properties
E_output_OBUF[1]_inst_i_1
A6
A5
A4
A3
A2
A1
O6
O5
A5LUT
A6LUT
AX
CE
SO
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Type here to search
ENG
15:55
09-08-2019

Bitstream generated



Project Summary




HW1_2018137 - [C:/Users/daksh18137/HW1_2018137/HW1_2018137.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Project Summary
write_bitstream Complete
Dashboard
Default Layout
Flow Navigator
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210183A8A970A
No hardware target is open. Open target
Source File Properties
Hardware
priority_encoder.v
Basys3_Master.xdc
Project Summary
Overview | Dashboard
DRC Violations
Summary: 1 warning
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
LUT 1%
IO 5%
0 25 50 75 100
Utilization (%)
Power
Summary | On-Chip
Total On-Chip Power: 1.639 W
Junction Temperature: 33.2 °C
Thermal Margin: 51.8 °C (10.3 W)
Effective θJA: 5.0 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report
Tcl Console
Messages
Reports
Serial I/O Links
Serial I/O Scans
Type here to search
ENG
16:27
09-08-2019