

HW1 ELD

PRIORITY ENCODER 4:2

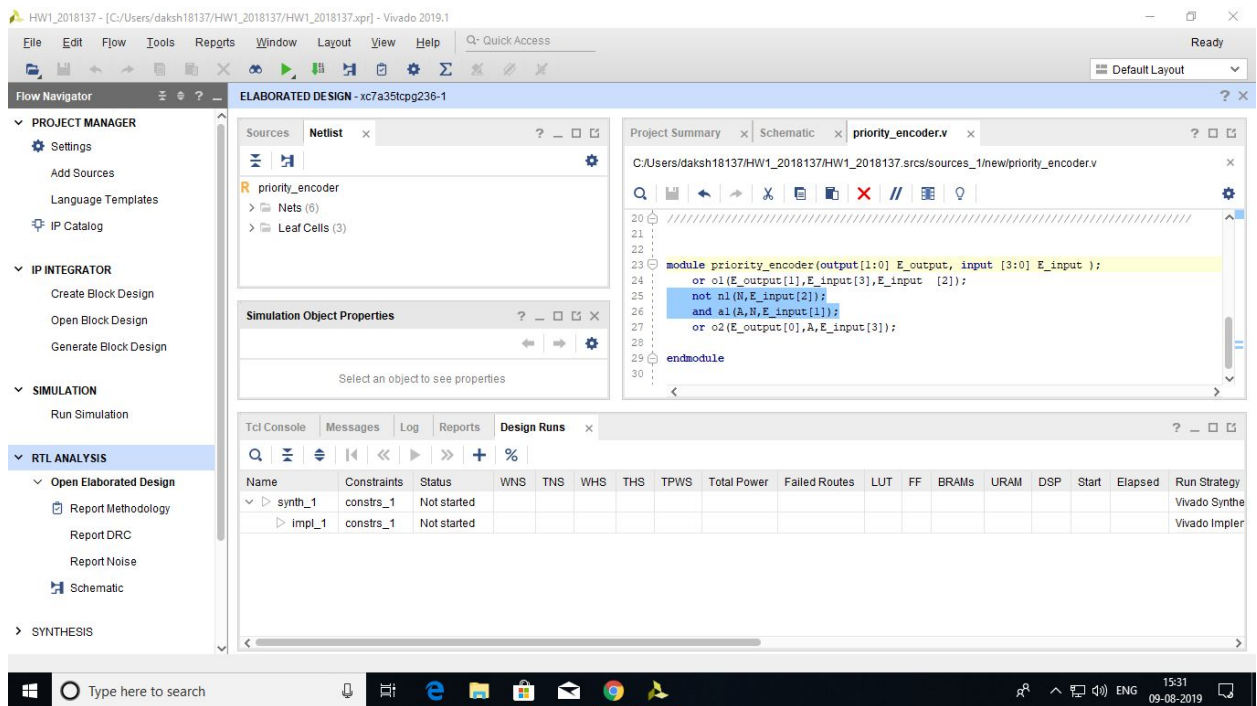
Daksh Thapar 2018137 (grp 2)

Verilog code

```

module priority_encoder(output[1:0] E_output, input [3:0] E_input );
    or o1(E_output[1],E_input[3],E_input [2]);
    not n1(N,E_input[2]);
    and a1(A,N,E_input[1]);
    or o2(E_output[0],A,E_input[3]);
endmodule

```



Elaborated Design after RTL analysis

HW1_2018137 - [C:/Users/daksh18137/HW1_2018137/HW1_2018137.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

Ready

Default Layout

ELABORATED DESIGN - xc7a35tqpg236-1

Project Summary x Schematic x priority_encoder.v x

3 Cells 6 I/O Ports 6 Nets

Sources Notlist x

priority_encoder

Nets (6)

Leaf Cells (3)

Simulation Object Properties

Select an object to see properties

Tcl Console Messages Log Reports Design Runs x

Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAMS URAM DSP Start Elapsed Run Strategy

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMS	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthe
impl_1	constrs_1	Not started															Vivado Implem

E_input[3:0]

RTL_AND

RTL_OR

RTL_OR

E_output[1:0]

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Output waveform for all possible inputs

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write_bitstream Complete

Default Layout

SIMULATION - Behavioral Simulation - Functional - sim_1 - priority_encoder

priority_encoder.v x Basys3_Master.xdc x Untitled 2 x

Name Value

Name	Value
E_output[1:0]	3
E_input[3:0]	1
N	0
A	0

0 us 50 us 100 us 151.000000 us

0 1 2 3 4 5 6 7 8 9 a b c d e f

Sim Time: 151 us

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Constraint- file uploaded

HW1_2018137 - [C:/Users/daksh18137/HW1_2018137/HW1_2018137.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Q Project Summary write_bitstream Complete

Dashboard

Flow Navigator

- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Utilization
 - Report Power
 - Schematic
- PROGRAM AND DEBUG
 - Generate Bitstream

HARDWARE MANAGER - localhost\linx_tcf\Digilent210183484970A

No hardware target is open. Open target

priority_encoder.v x Basys3_Master.xdc x Project Summary x

C:/Users/daksh18137/Downloads/Basys3_Master.xdc

```
4 ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6 # Clock signal
7 #set_property PACKAGE_PIN W6 [get_ports clk]
8 # set_property IOSTANDARD LVCMOS33 [get_ports clk]
9 # create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
10
11 ## Switches
12 set_property PACKAGE_PIN V17 [get_ports {E_input[0]}]
13 set_property IOSTANDARD LVCMOS33 [get_ports {E_input[0]}]
14 set_property PACKAGE_PIN V16 [get_ports {E_input[1]}]
15 set_property IOSTANDARD LVCMOS33 [get_ports {E_input[1]}]
16 set_property PACKAGE_PIN W16 [get_ports {E_input[2]}]
17 set_property IOSTANDARD LVCMOS33 [get_ports {E_input[2]}]
18 set_property PACKAGE_PIN W17 [get_ports {E_input[3]}]
19 set_property IOSTANDARD LVCMOS33 [get_ports {E_input[3]}]
20 #set_property PACKAGE_PIN W15 [get_ports {sv[4]}]
21 # set_property IOSTANDARD LVCMOS33 [get_ports {sv[4]}]
22 #set_property PACKAGE_PIN V15 [get_ports {sv[5]}]
23 # set_property IOSTANDARD LVCMOS33 [get_ports {sv[5]}]
24 #set_property PACKAGE_PIN W14 [get_ports {sv[6]}]
25 # set_property IOSTANDARD LVCMOS33 [get_ports {sv[6]}]
26 #set_property PACKAGE_PIN W13 [get_ports {sv[7]}]
27 # set_property IOSTANDARD LVCMOS33 [get_ports {sv[7]}]
```

Tcl Console Messages Reports Serial I/O Links Serial I/O Scans

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Design after Synthesis

HW1_2018137 - [C:/Users/daksh18137/HW1_2018137/HW1_2018137.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Q Quick Access Implementation Complete

Default Layout

Flow Navigator

- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic
- PROGRAM AND DEBUG
 - Generate Bitstream

IMPLEMENTED DESIGN - xc7a35tqg236-1

Project Summary x Device x priority_encoder.v x Basys3_Master.xdc x Schematic x

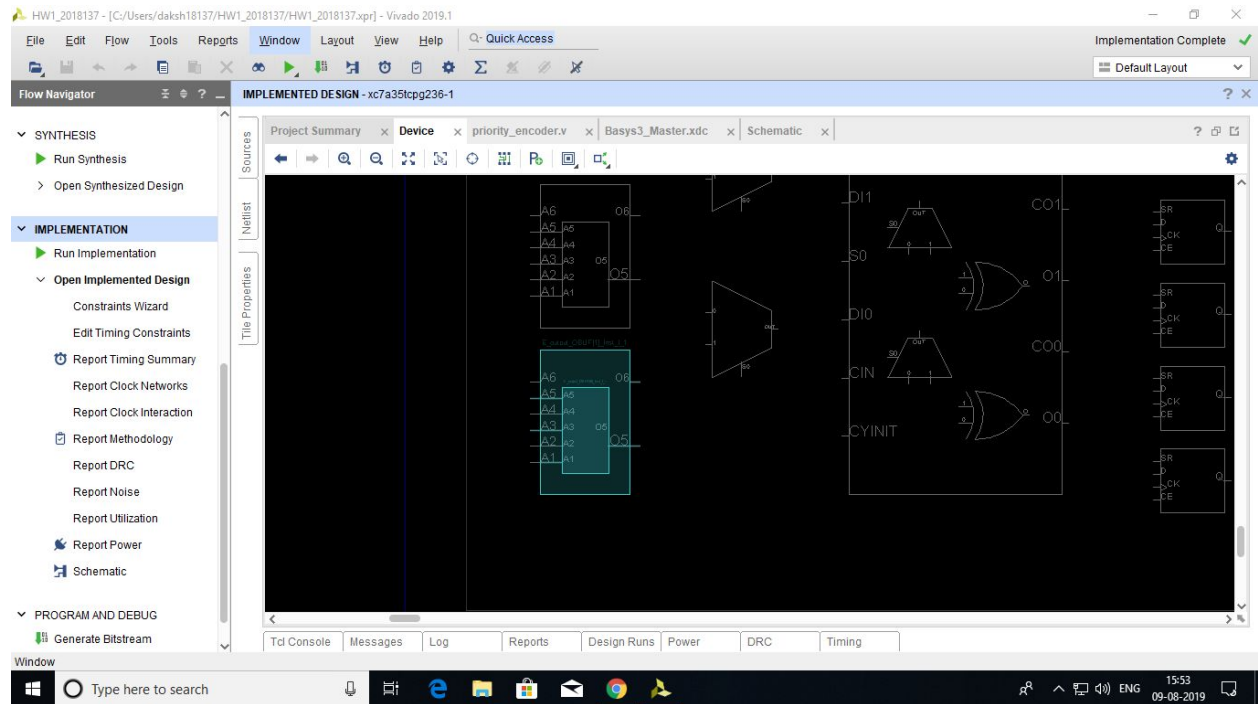
7 Cells 6 I/O Ports 10 Nets

Tcl Console Messages Log Reports Design Runs Power DRC Timing

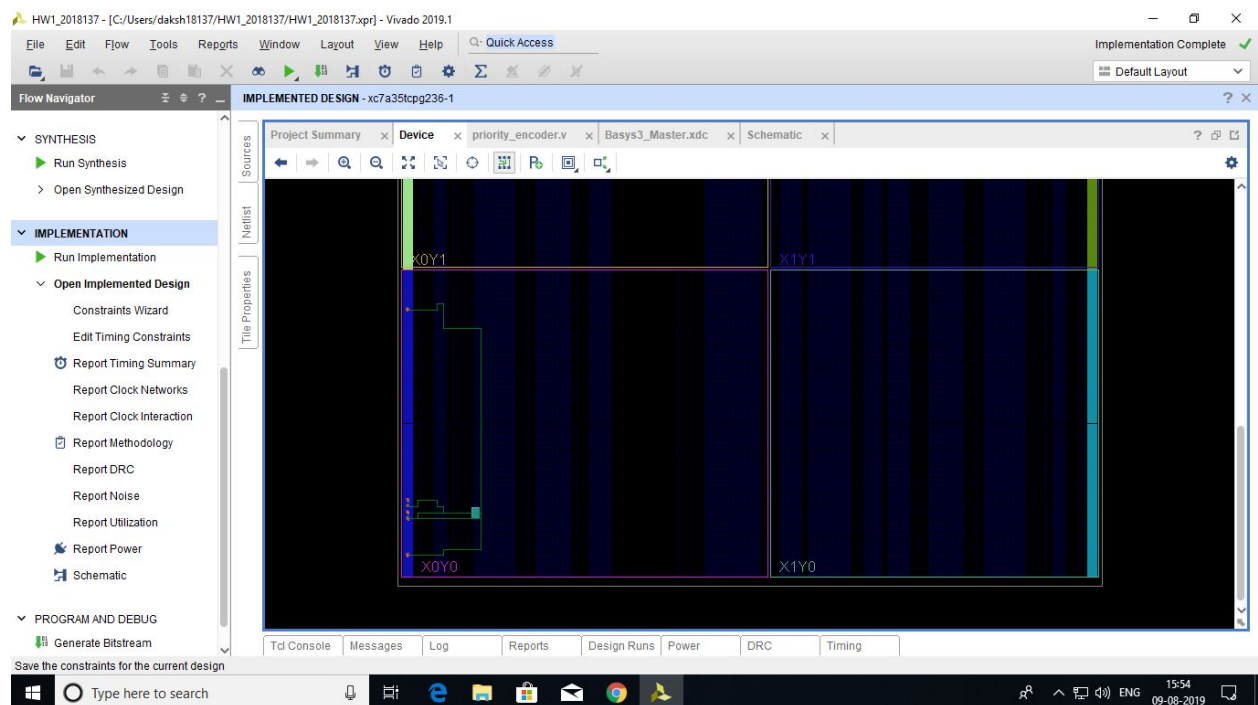
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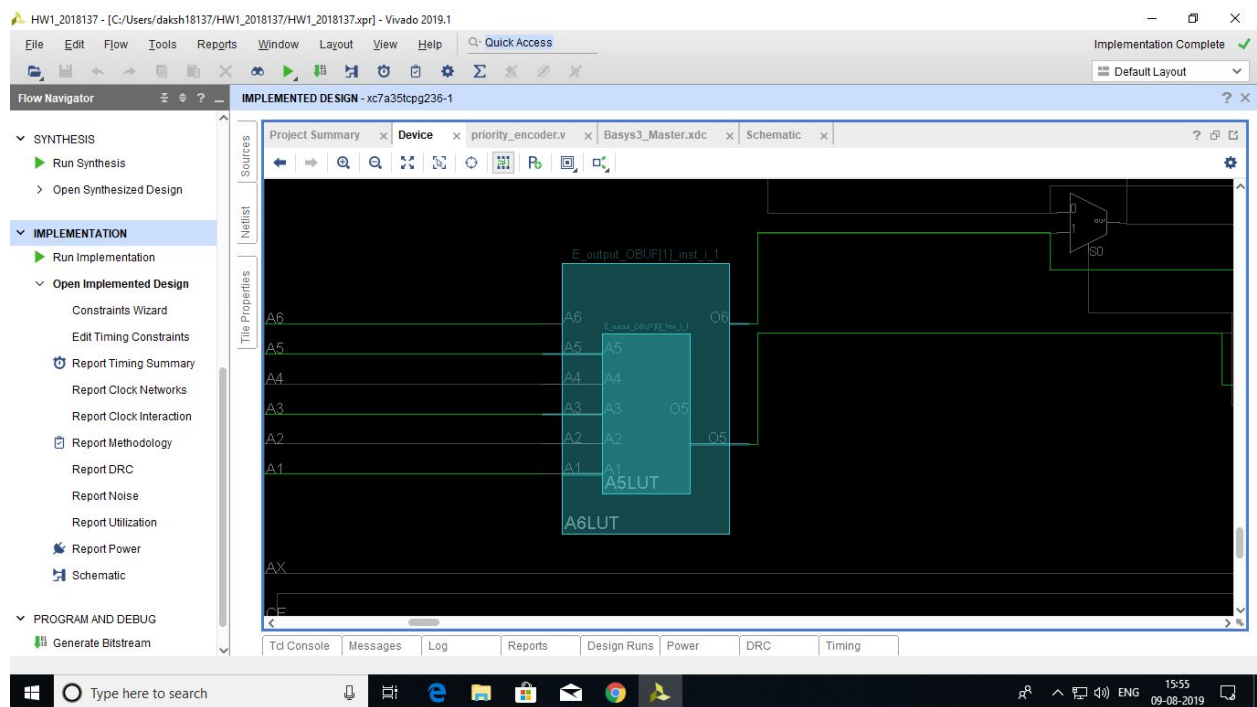
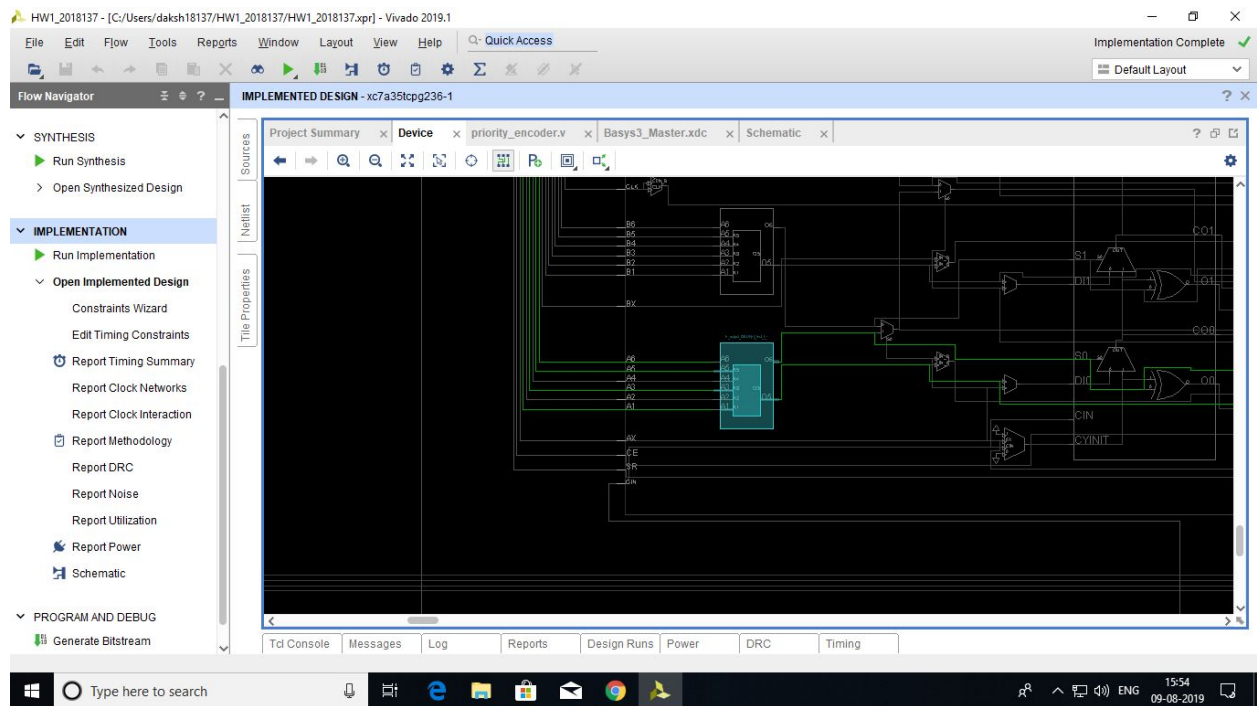
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Device Layout before routing

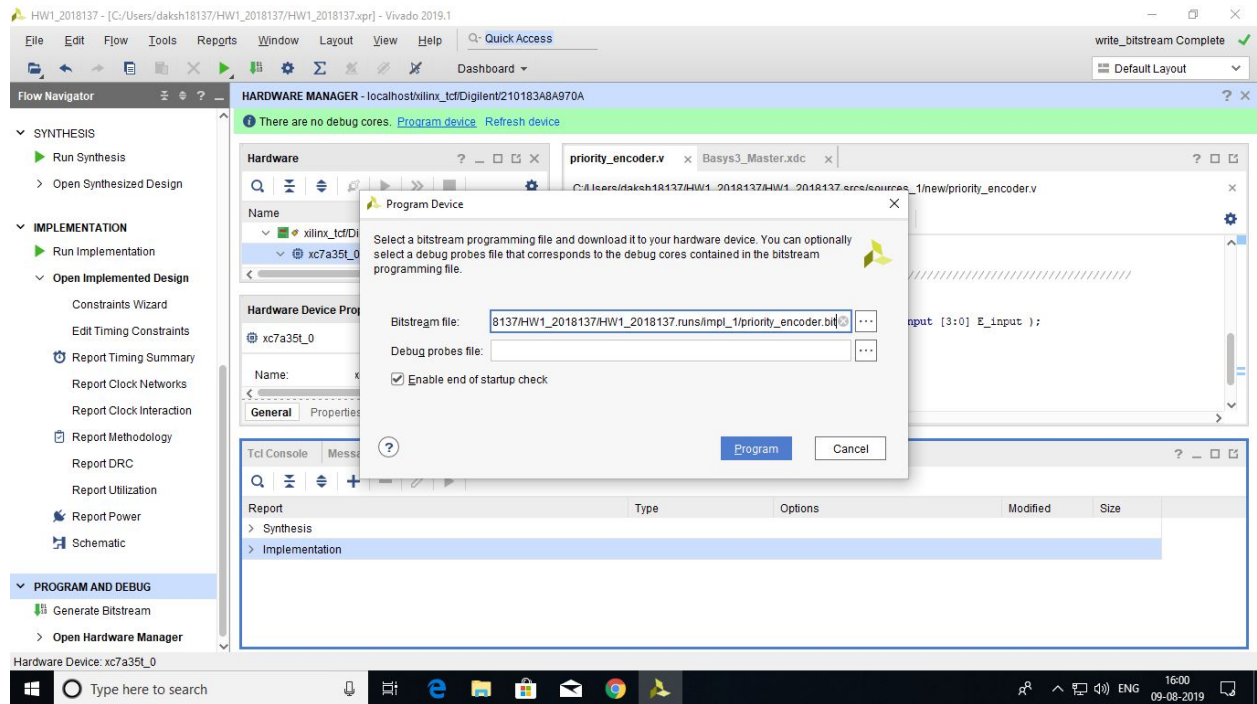


Device Layout after routing

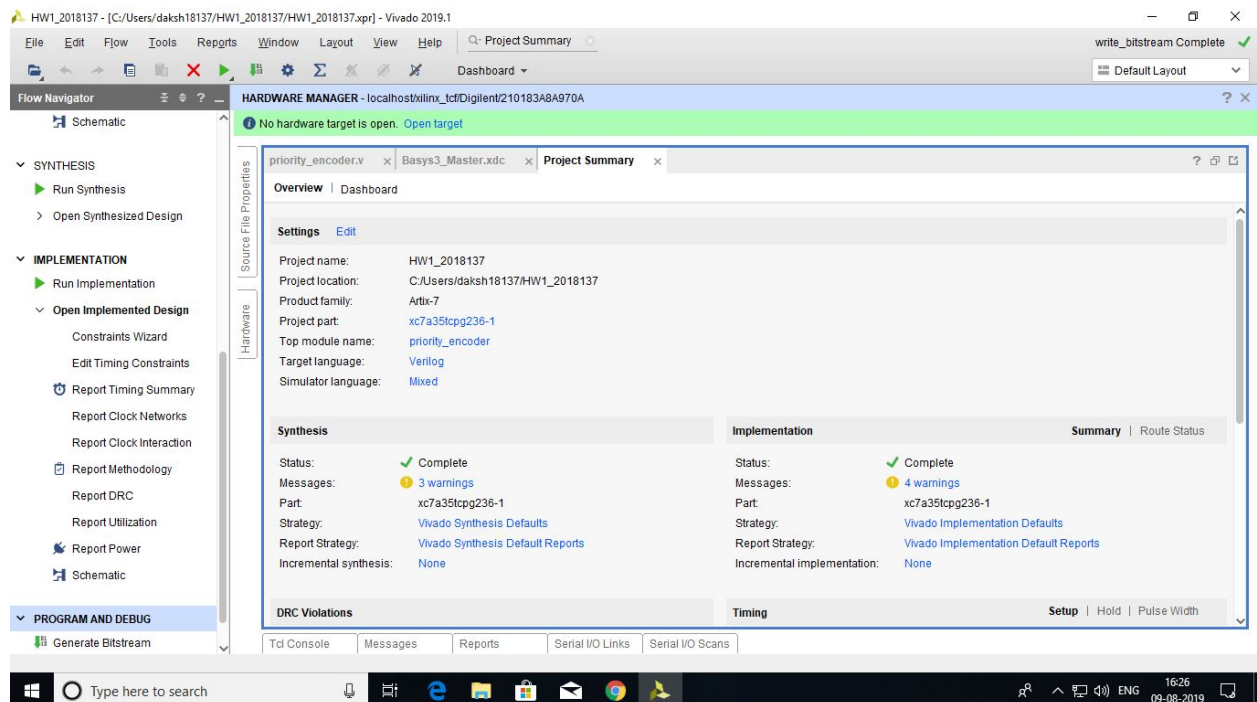




Bitstream generated



Project Summary



HW1_2018137 - [C:/Users/daksh18137/HW1_2018137.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Project Summary write_bitstream Complete

Flow Navigator Schematic

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
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 - Schematic

PROGRAM AND DEBUG

- Generate Bitstream

HARDWARE MANAGER - localhost:xlrx_tcf/DigilentZ10183A8A970A

No hardware target is open. Open target

priority_encoder.v Basys3_Master.xdc Project Summary

Overview | Dashboard

DRC Violations

Summary: 1 warning

[Implemented DRC Report](#)

Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS): NA

Total Negative Slack (TNS): NA

Number of Failing Endpoints: NA

Total Number of Endpoints: NA

[Implemented Timing Report](#)

Utilization

Post-Synthesis | Post-Implementation

Graph | Table

LUT: 1%

IO: 5%

Utilization (%)

Power

Summary | On-Chip

Total On-Chip Power: 1.639 W

Junction Temperature: 33.2 °C

Thermal Margin: 51.8 °C (10.3 W)

Effective θJA: 5.0 °C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

[Implemented Power Report](#)

Tcl Console Messages Reports Serial I/O Links Serial I/O Scans

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