**Lab 3**

**4 bit adder/subtractor**

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**Verilog Code**

module addition(input a, input b, input c, output sum, output carry);

assign sum = a^b^c;

assign carry = (a&b)|(c&(a^b));

endmodule

module papa(input [3:0] a, input [3:0] b, input S, output [3:0] out, output V);

wire C1,C2,C3,C4;

assign x0=b[0]^S;

assign x1=b[1]^S;

assign x2=b[2]^S;

assign x3=b[3]^S;

addition

A0(.a(x0),.b(a[0]),.c(S),.sum(out[0]),.carry(C1)),

A1(.a(x1),.b(a[1]),.c(C1),.sum(out[1]),.carry(C2)),

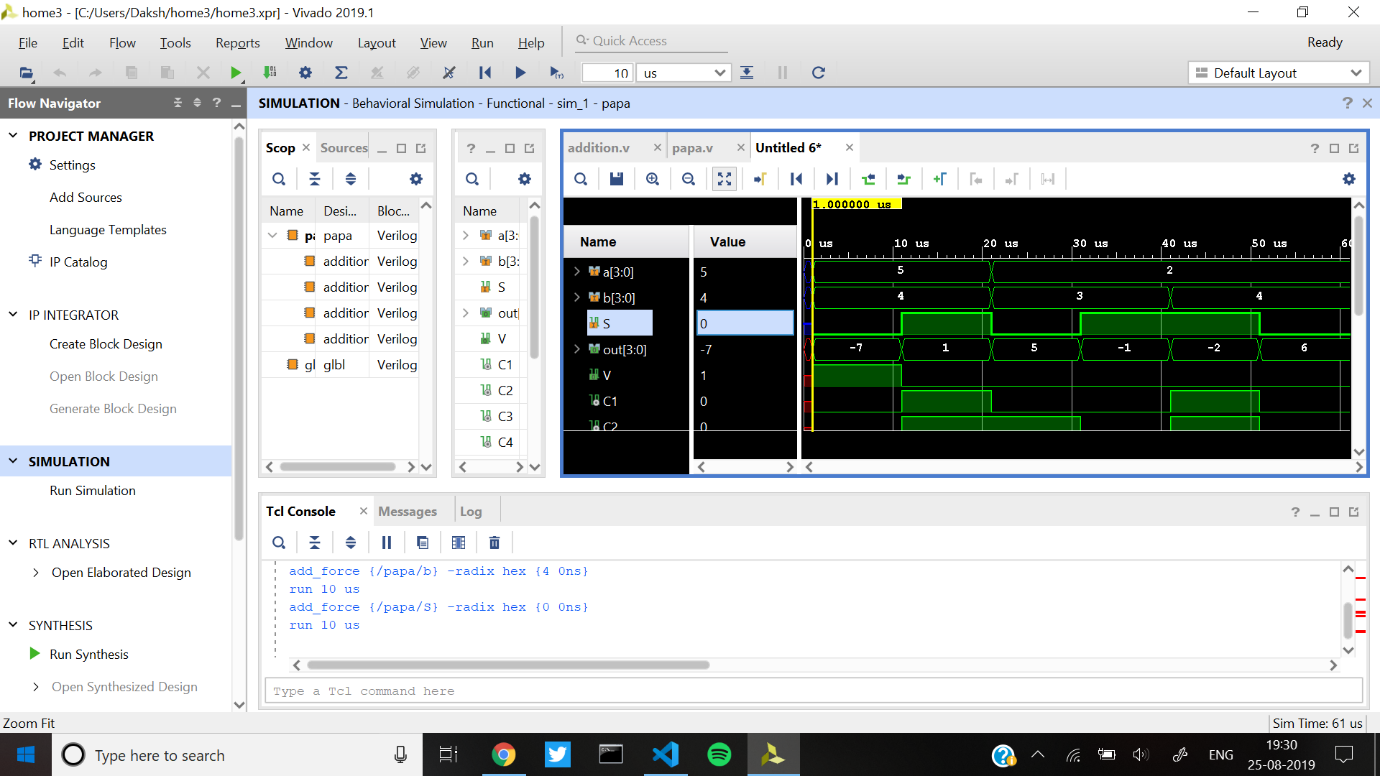
A2(.a(x2),.b(a[2]),.c(C2),.sum(out[2]),.carry(C3)),

A3(.a(x3),.b(a[3]),.c(C3),.sum(out[3]),.carry(C4));

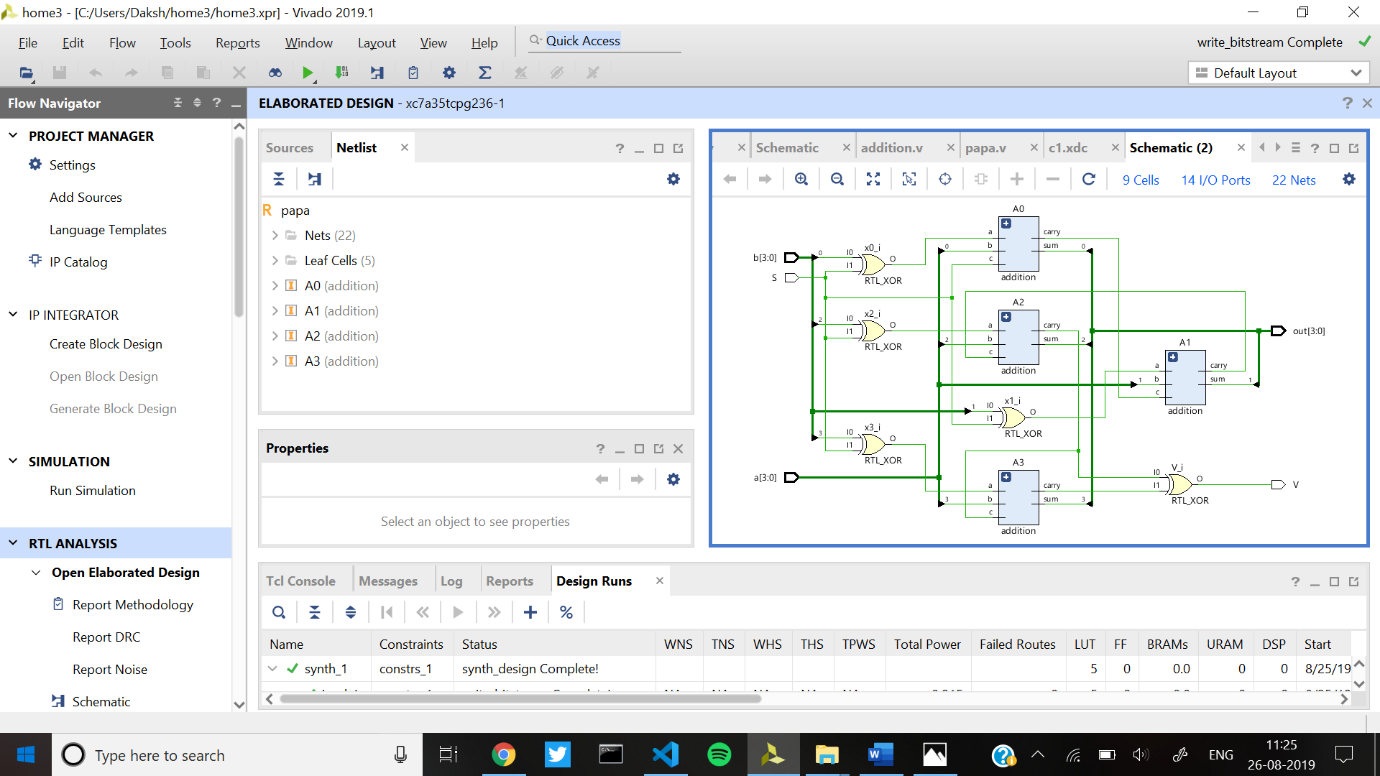
assign V = C3^C4;

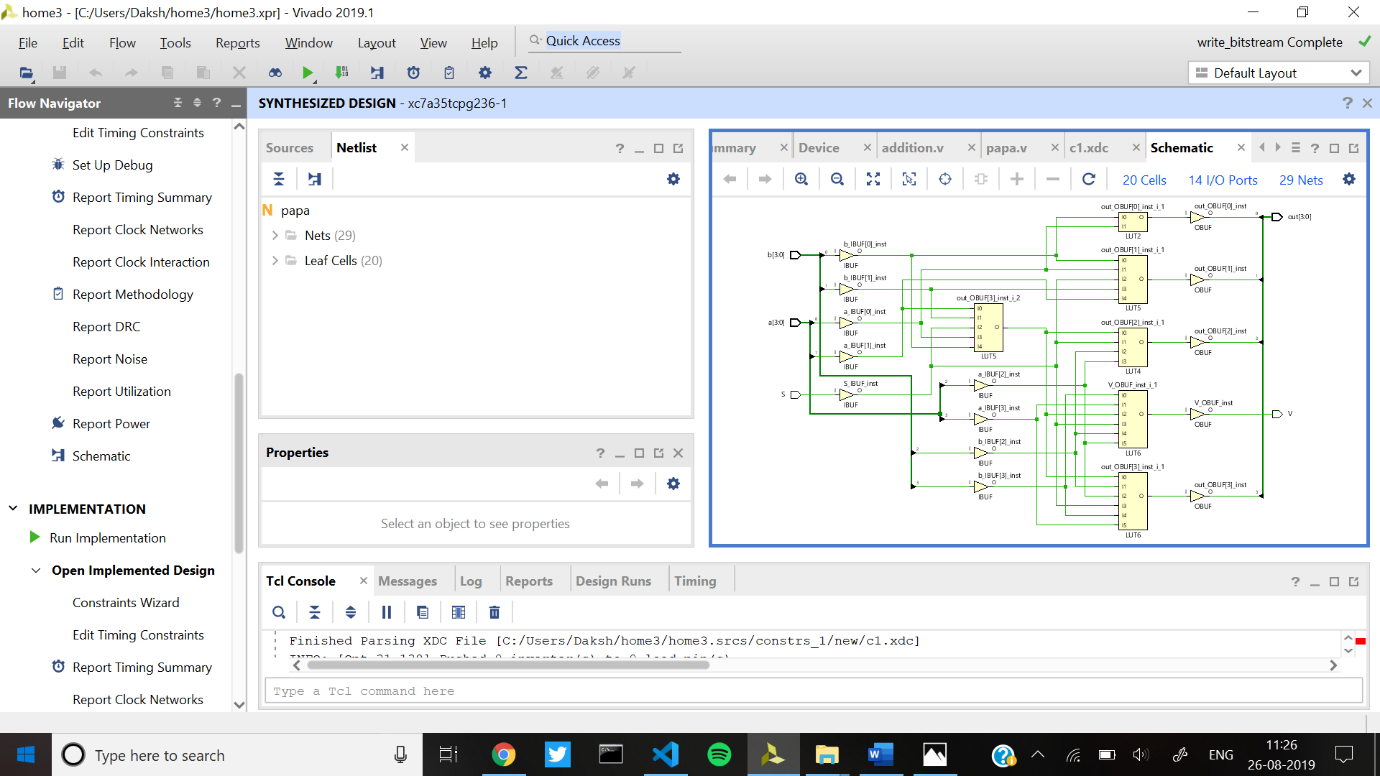
endmodule

output waveform



Schematic after RTL



Implemented Design

Designs after implementation