**LAB 7**

**-Daksh Thapar 2018137**

**-Tanmaya Gupta 2018200**

`timescale 1ns / 1ps

module top(

input clk,

input enable,

input srst,

output reg f,

output empty,

output [3:0] anode,

output [7:0] cathode

);

reg [3:0] addr = 4'd0;

wire [17:0] douta;

wire [17:0] doutb;

wire full;

wire clk\_5M;

wire clk\_deb,clk1K;

clk\_wiz\_0 clk\_gen\_5M(.clk\_out1(clk\_5M),.clk\_in1(clk));

clk\_div #(12) u2(.clk\_in(clk\_5M),.clk\_out(clk1K));

clk\_div #(19) u(.clk\_in(clk), .clk\_out(clk\_deb));

blk\_mem\_gen\_0 alphabets (.clka(clk),.addra(addr),.douta(douta));

blk\_mem\_gen\_1 numbers(.clka(clk),.addra(addr),.douta(doutb));

wire en;

debouncer d(.clk\_in(clk\_deb), .rst(enable), .rst\_out(en));

reg wr\_en = 1'b1;

wire [15:0] dout;

wire [3:0] data\_count;

always @(posedge clk\_deb)

begin

if(data\_count<5)

f = 0;

else if(data\_count== 4'd5 || srst==1'b1)

f = 1;

end

always @(posedge clk\_deb)

begin

if(wr\_en)

begin

if(addr <= 4'd4 )

begin

addr = addr + 1;

end

if( addr >4'd4)

wr\_en = 0;

end

if(srst)

begin

addr = 0;

wr\_en = 1;

end

end

wire [3:0] ones;

wire [3:0] tens;

wire [3:0] hundreds;

wire [3:0] thousands;

bin2bcd btb(.number(douta+doutb), .ones(ones), .tens(tens), .hundreds(hundreds), .thousands(thousands));

wire [15:0] sum;

assign sum = {ones,tens,hundreds,thousands};

fifo\_generator\_0 fifo (

.clk(clk\_deb),

.srst(srst),

.din(sum),

.wr\_en(wr\_en),

.rd\_en(en),

.dout(dout),

.full(full),

.empty(empty),

.data\_count(data\_count)

);

ssd s(.clk(clk1K), .ones(dout[15:12]), .tens(dout[11:8]), .hundreds(dout[7:4]), .thousands(dout[3:0]), .anode(anode), .cathode(cathode));

endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 26.09.2019 15:30:14

// Design Name:

// Module Name: clk\_div

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module clk\_div

#(

parameter divide\_by = 19

)

(

input clk\_in,

output clk\_out

);

reg [divide\_by-1:0] count = 0;

always @(posedge clk\_in)

begin

count = count+1;

end

assign clk\_out = count[divide\_by-1];

endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 26.09.2019 16:01:33

// Design Name:

// Module Name: debouncer

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module debouncer(

input clk\_in,input rst,output rst\_out

);

reg d1,d2,d3;

always@(posedge clk\_in)

begin

d1<=rst;

d2<=d1;

d3<=d2;

end

assign rst\_out=d1&d2&~d3;

endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 26.09.2019 15:41:57

// Design Name:

// Module Name: bin\_to\_bcd

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module bin2bcd(

input [7:0] number,

output reg [3:0] ones,

output reg [3:0] tens,

output reg [3:0] hundreds,

output reg [3:0] thousands

);

reg [19:0] shift = 0;

integer i;

always @(number)

begin

shift[19:8] = 0;

shift[7:0] = number;

for(i=0;i<8;i = i+1)

begin

if(shift[11:8]>=5)

shift[11:8] = shift[11:8] + 3;

if(shift[15:12]>=5)

shift[15:12] = shift[15:12] + 3;

if(shift[19:16]>=5)

shift[19:16] = shift[19:16] + 3;

shift = shift << 1;

end

thousands <= 4'b0000;

hundreds <= shift[19:16];

tens <= shift[15:12];

ones <= shift[11:8];

end

endmodule

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 26.09.2019 15:31:10

// Design Name:

// Module Name: sevenSeg

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module ssd(

input clk,

input [3:0] ones,

input [3:0] tens,

input [3:0] hundreds,

input [3:0] thousands,

output [3:0] anode,

output [7:0] cathode

);

reg [6:0] cathode\_temp = 7'b1111111;

reg [3:0] anode\_temp = 4'b1110;

reg [1:0] count = 0;

always @(posedge clk)

begin

count = count + 1;

end

always @(\*)

begin

case(count)

2'b00:

begin

case(ones)

4'd0: cathode\_temp = 7'b0000001;

4'd1: cathode\_temp = 7'b1001111;

4'd2: cathode\_temp = 7'b0010010;

4'd3: cathode\_temp = 7'b0000110;

4'd4: cathode\_temp = 7'b1001100;

4'd5: cathode\_temp = 7'b0100100;

4'd6: cathode\_temp = 7'b0100000;

4'd7: cathode\_temp = 7'b0001111;

4'd8: cathode\_temp = 7'b0000000;

4'd9: cathode\_temp = 7'b0000100;

4'hA: cathode\_temp <= 7'b0001000;

4'hB: cathode\_temp <= 7'b1100000;

4'hC: cathode\_temp <= 7'b0110001;

4'hD: cathode\_temp <= 7'b1000010;

4'hE: cathode\_temp <= 7'b0110000;

4'hF: cathode\_temp <= 7'b0111000;

default : cathode\_temp = 7'b1111111;

endcase

anode\_temp = 4'b1110;

end

2'b01:

begin

case(tens)

4'd0: cathode\_temp = 7'b0000001;

4'd1: cathode\_temp = 7'b1001111;

4'd2: cathode\_temp = 7'b0010010;

4'd3: cathode\_temp = 7'b0000110;

4'd4: cathode\_temp = 7'b1001100;

4'd5: cathode\_temp = 7'b0100100;

4'd6: cathode\_temp = 7'b0100000;

4'd7: cathode\_temp = 7'b0001111;

4'd8: cathode\_temp = 7'b0000000;

4'd9: cathode\_temp = 7'b0000100;

4'hA: cathode\_temp <= 7'b0001000;

4'hB: cathode\_temp <= 7'b1100000;

4'hC: cathode\_temp <= 7'b0110001;

4'hD: cathode\_temp <= 7'b1000010;

4'hE: cathode\_temp <= 7'b0110000;

4'hF: cathode\_temp <= 7'b0111000;

default : cathode\_temp = 7'b1111111;

endcase

anode\_temp = 4'b1101;

end

2'b10:

begin

case(hundreds)

4'd0: cathode\_temp = 7'b0000001;

4'd1: cathode\_temp = 7'b1001111;

4'd2: cathode\_temp = 7'b0010010;

4'd3: cathode\_temp = 7'b0000110;

4'd4: cathode\_temp = 7'b1001100;

4'd5: cathode\_temp = 7'b0100100;

4'd6: cathode\_temp = 7'b0100000;

4'd7: cathode\_temp = 7'b0001111;

4'd8: cathode\_temp = 7'b0000000;

4'd9: cathode\_temp = 7'b0000100;

4'hA: cathode\_temp <= 7'b0001000;

4'hB: cathode\_temp <= 7'b1100000;

4'hC: cathode\_temp <= 7'b0110001;

4'hD: cathode\_temp <= 7'b1000010;

4'hE: cathode\_temp <= 7'b0110000;

4'hF: cathode\_temp <= 7'b0111000;

default : cathode\_temp = 7'b1111111;

endcase

anode\_temp = 4'b1011;

end

2'b11:

begin

case(thousands)

4'd0: cathode\_temp = 7'b0000001;

4'd1: cathode\_temp = 7'b1001111;

4'd2: cathode\_temp = 7'b0010010;

4'd3: cathode\_temp = 7'b0000110;

4'd4: cathode\_temp = 7'b1001100;

4'd5: cathode\_temp = 7'b0100100;

4'd6: cathode\_temp = 7'b0100000;

4'd7: cathode\_temp = 7'b0001111;

4'd8: cathode\_temp = 7'b0000000;

4'd9: cathode\_temp = 7'b0000100;

4'hA: cathode\_temp <= 7'b0001000;

4'hB: cathode\_temp <= 7'b1100000;

4'hC: cathode\_temp <= 7'b0110001;

4'hD: cathode\_temp <= 7'b1000010;

4'hE: cathode\_temp <= 7'b0110000;

4'hF: cathode\_temp <= 7'b0111000;

default : cathode\_temp = 7'b1111111;

endcase

anode\_temp = 4'b0111;

end

endcase

end

assign cathode = {cathode\_temp,1'b1};

assign anode = anode\_temp;

endmodule

set\_property PACKAGE\_PIN W5 [get\_ports clk]

set\_property IOSTANDARD LVCMOS33 [get\_ports clk]

set\_property PACKAGE\_PIN V17 [get\_ports {srst}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {srst}]

set\_property PACKAGE\_PIN U16 [get\_ports {f}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {f}]

set\_property PACKAGE\_PIN U19 [get\_ports {empty}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {empty}]

set\_property PACKAGE\_PIN W7 [get\_ports {cathode[7]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {cathode[7]}]

set\_property PACKAGE\_PIN W6 [get\_ports {cathode[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {cathode[6]}]

set\_property PACKAGE\_PIN U8 [get\_ports {cathode[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {cathode[5]}]

set\_property PACKAGE\_PIN V8 [get\_ports {cathode[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {cathode[4]}]

set\_property PACKAGE\_PIN U5 [get\_ports {cathode[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {cathode[3]}]

set\_property PACKAGE\_PIN V5 [get\_ports {cathode[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {cathode[2]}]

set\_property PACKAGE\_PIN U7 [get\_ports {cathode[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {cathode[1]}]

set\_property PACKAGE\_PIN V7 [ get\_ports {cathode[0] }] set\_property IOSTANDARD LVCMOS33 [get\_ports {cathode[0] }]

set\_property PACKAGE\_PIN U2 [get\_ports {anode[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {anode[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {anode[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {anode[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {anode[2]}]

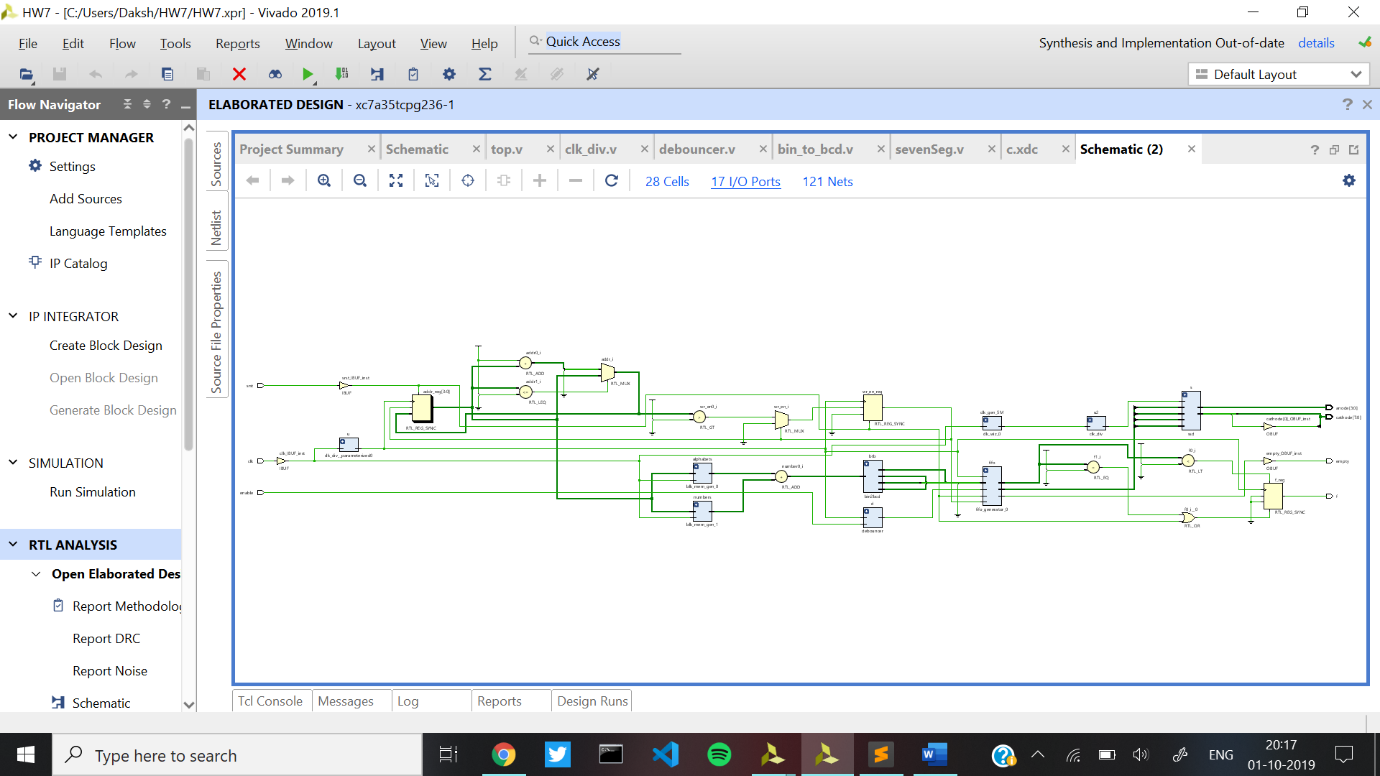
set\_property IOSTANDARD LVCMOS33 [get\_ports {anode[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {anode[3]}]

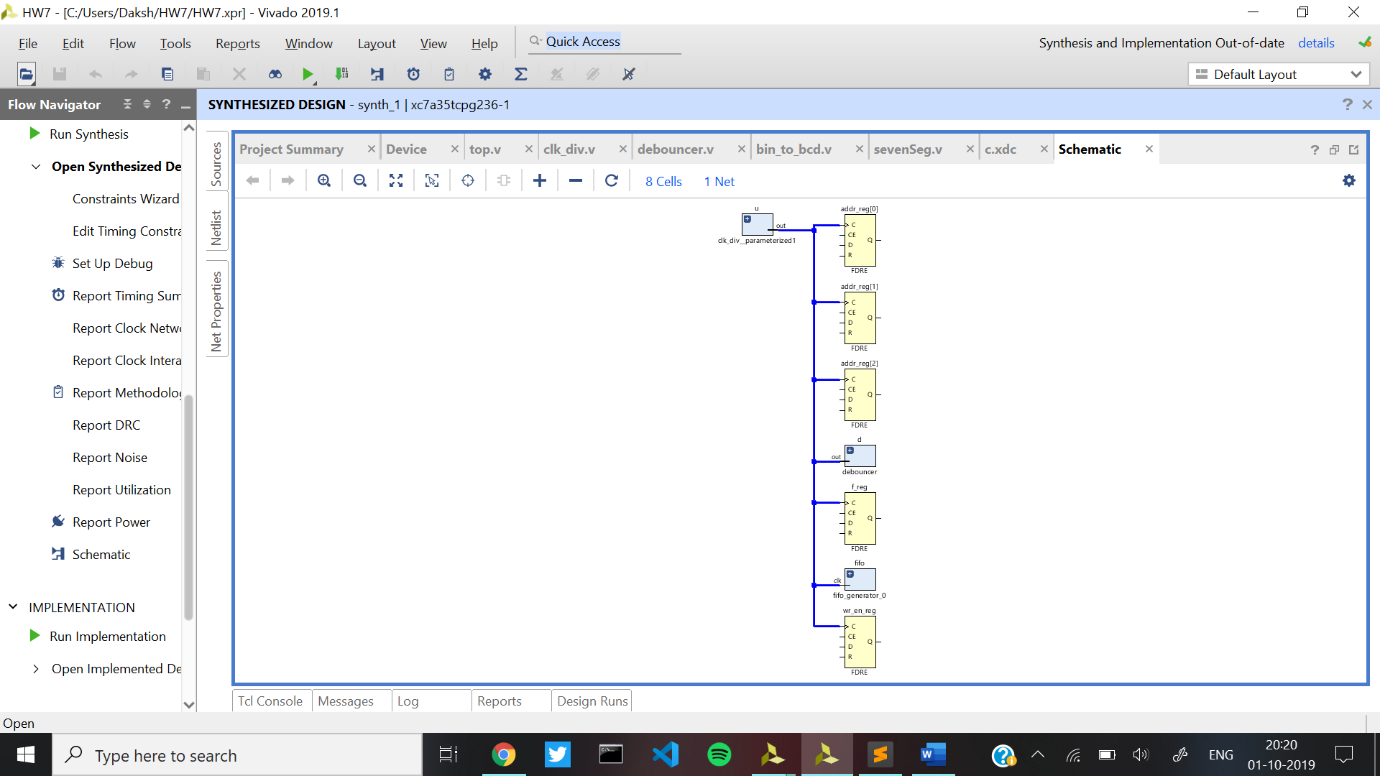
set\_property IOSTANDARD LVCMOS33 [get\_ports {anode[3]}]

set\_property PACKAGE\_PIN W19 [get\_ports enable] set\_property IOSTANDARD LVCMOS33 [get\_ports enable]

**Elaborated Design-**



**Synthesised Design**



**Implemented Design-**

