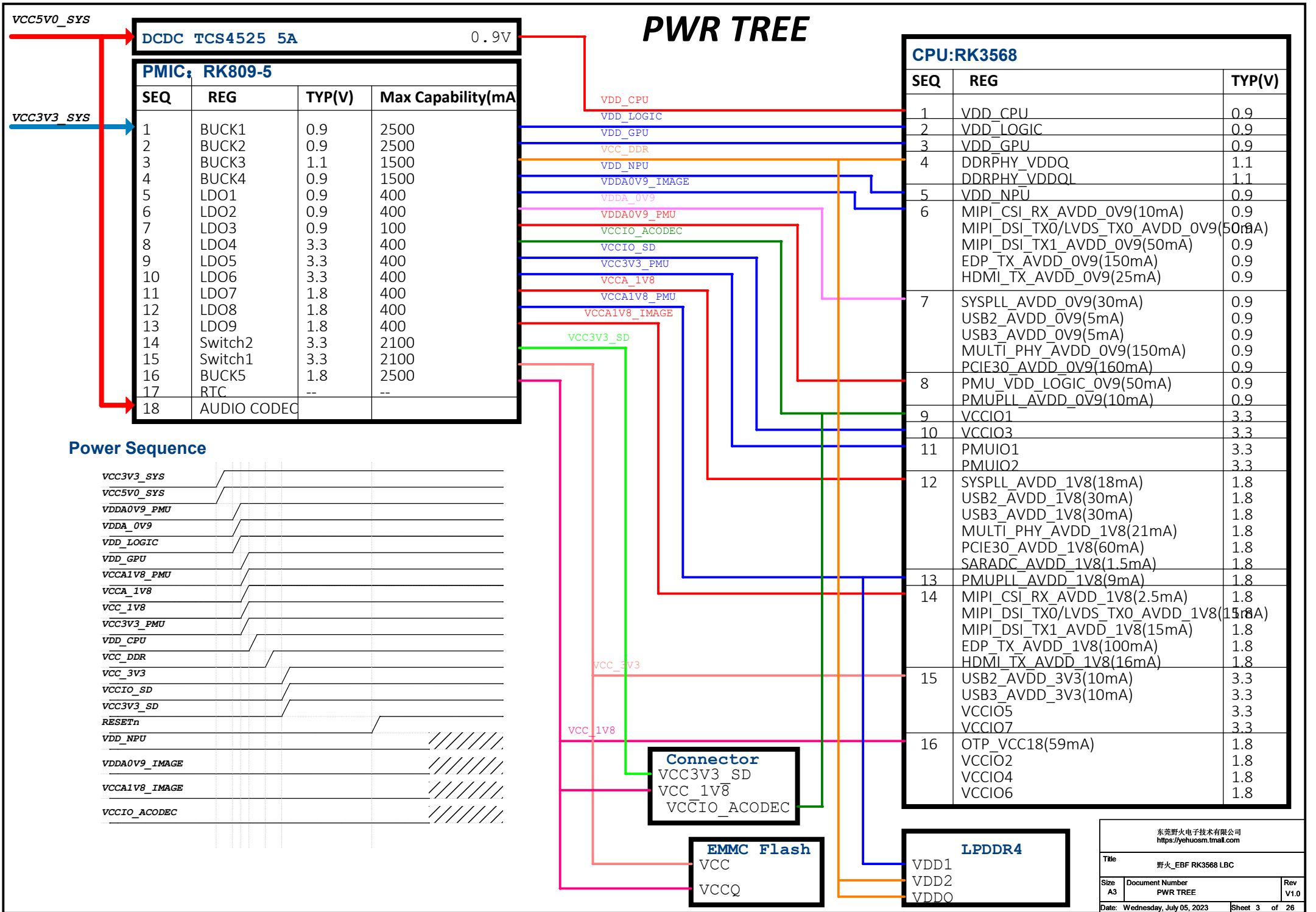


野火 EBF RK3568 LBC

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历史版本

版本号	日期	设计	描述
V1.0	2022-01-25	llm	初始版本, 开发阶段
V1.1	2022-05-18	llm	修复初始版本的一些问题，增加SATA接口， typec添加OTG自动识别host/device功能
V1.2	2022-07-27	llm	1.MIPI CSI 添加2 Lanes 2.更新MINI PCIE、M.2 PCIE封装，添加独立的定位孔 3.把Z4、Z3、Z2、Z1位号改前缀为D的位号 4.把sim卡座位号U18改为J18 5.把mini pcie位号CON1改为J17
V1.2	2022-11-29	llm	添加LPDDR4x注释，电路不做任何更改
V1.3	2022-12-08	llm	1.网口外壳增加阻容到地隔离 2.IR接收更换为PWM3_IR, IR接收器电源更改为VCC3V3_PMU, 以支持休眠唤醒 3.修复以太网PHY复位引脚漏电问题，并兼容RTL8211F
V1.3	2023-05-29	llm	1.添加一个mipi dsi接口，一个mipi csi接口 2.把M2 pcie信号耦合电容改为0201封装



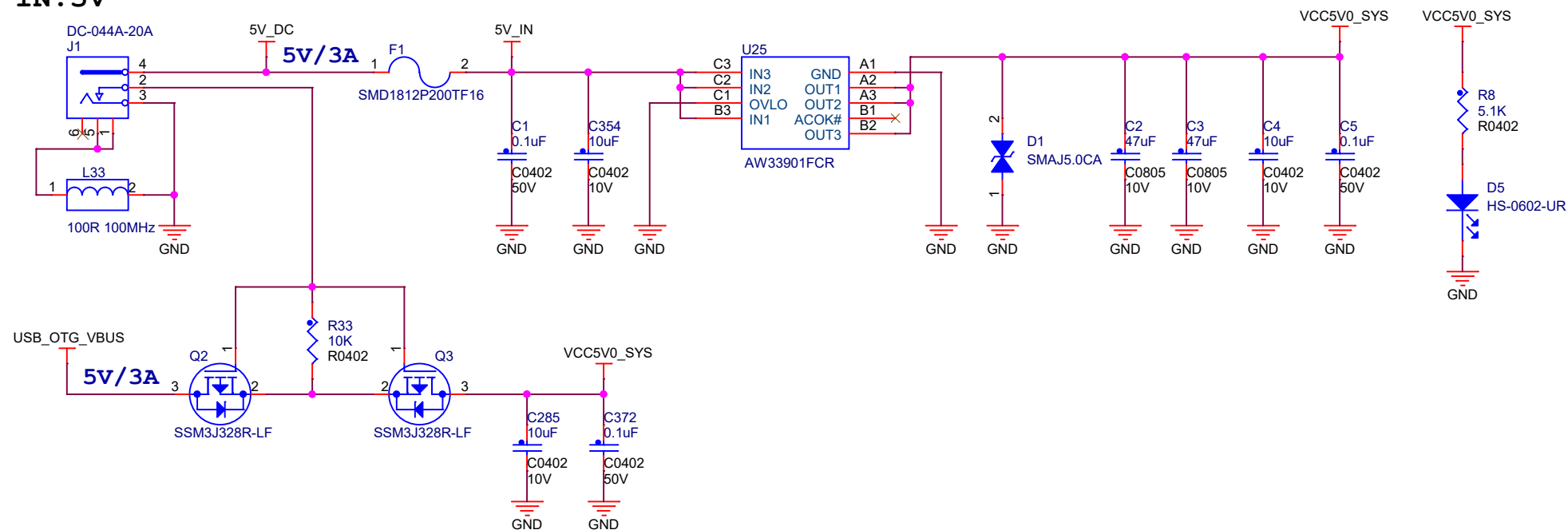
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Title 野火\_EBF RK3568 LBC

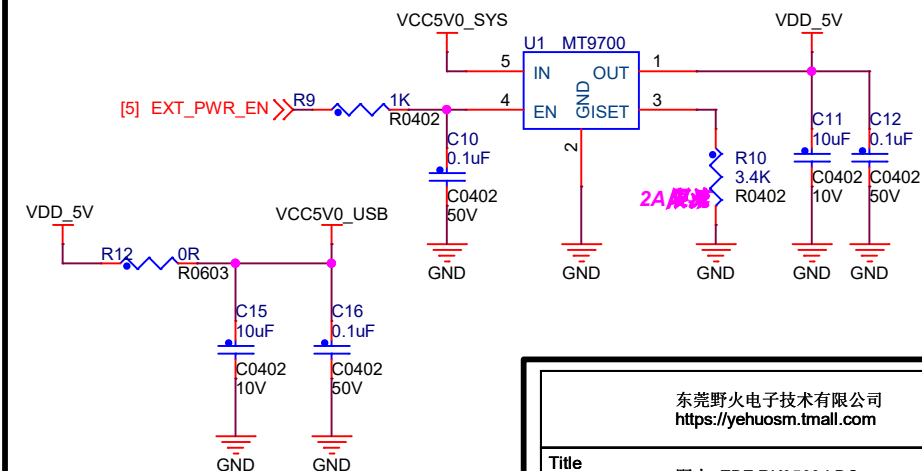
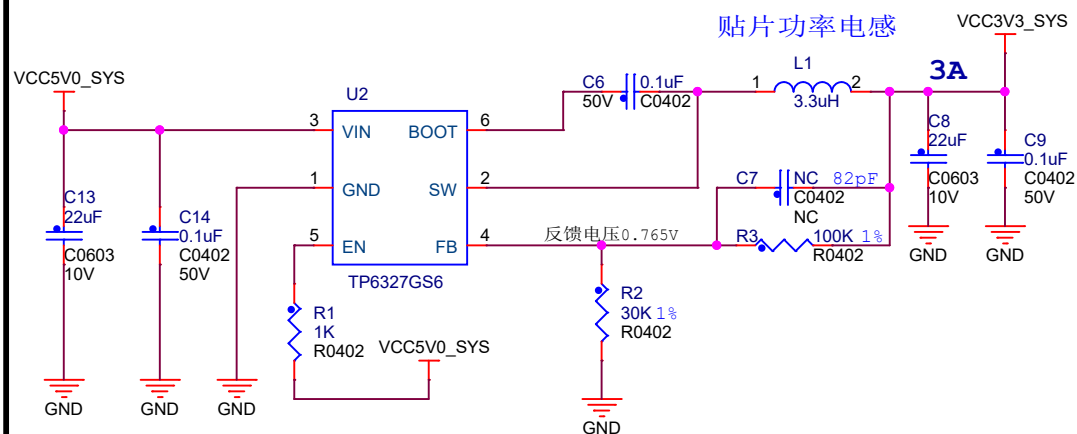
Size A3	Document Number PWR TREE	Rev V1.0
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DC IN: 5V



## 5V转3.3V



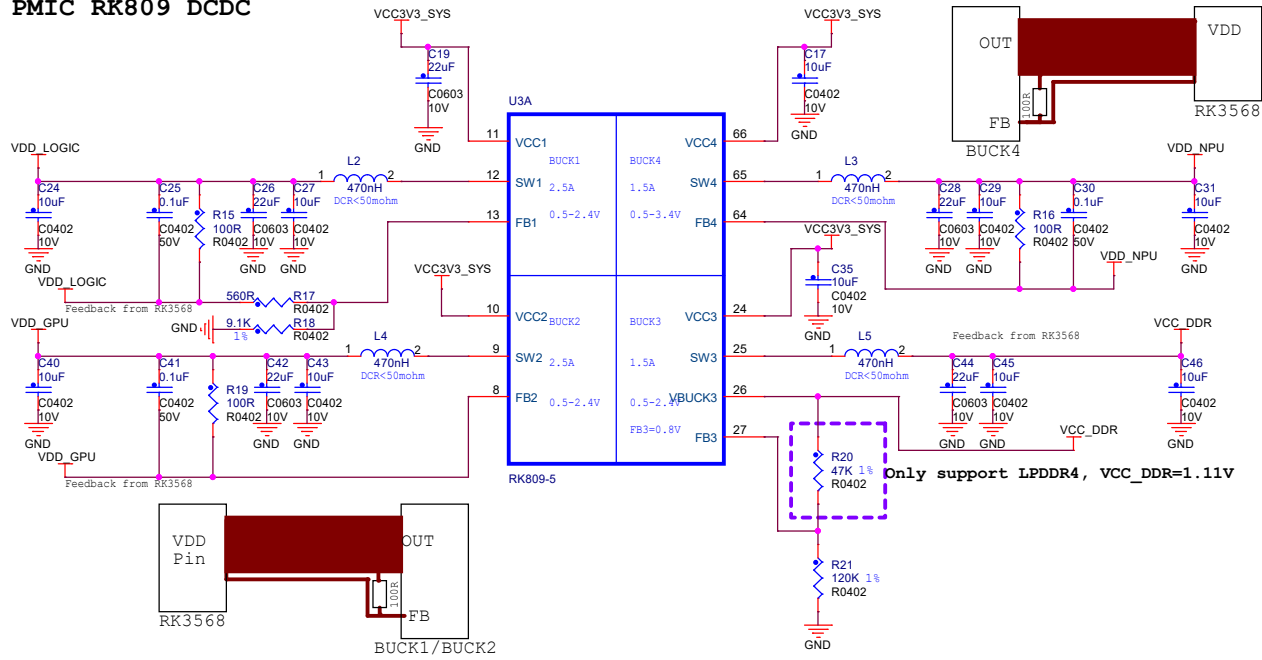
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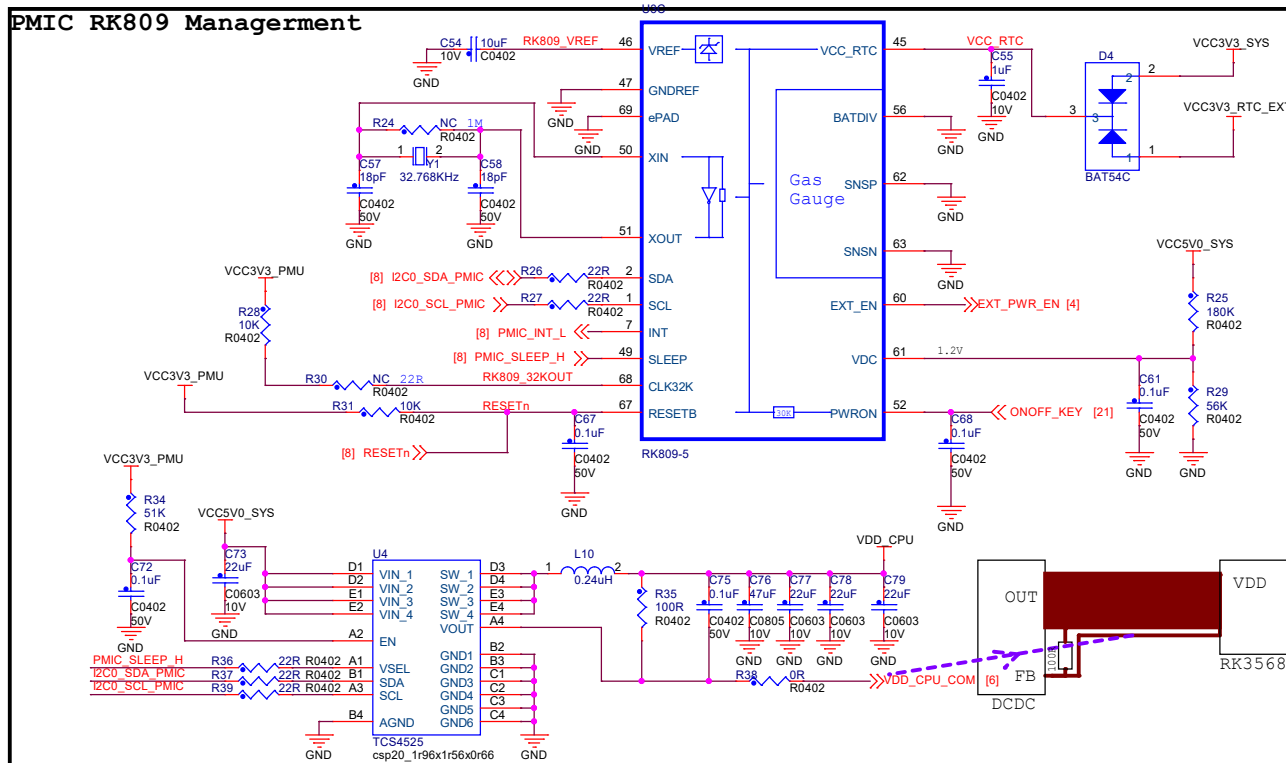
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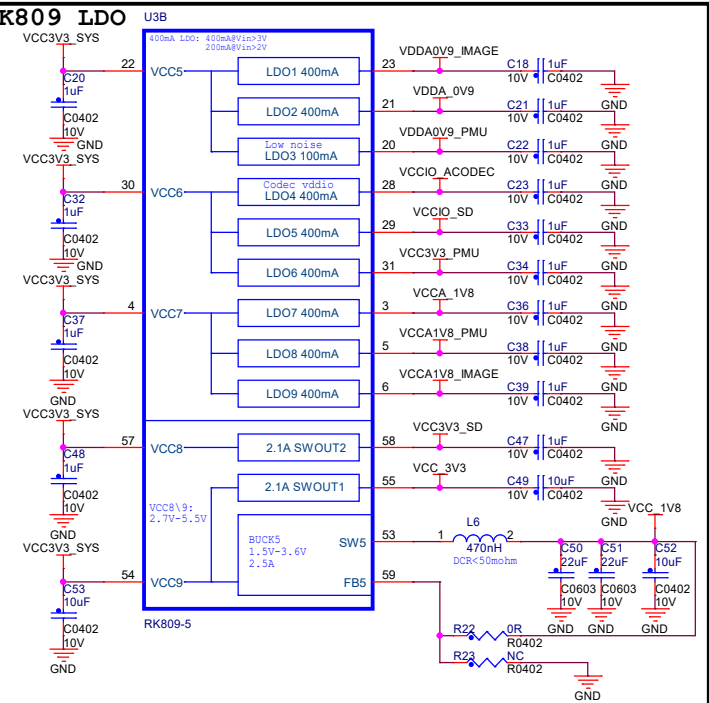
## PMIC RK809 DCDC



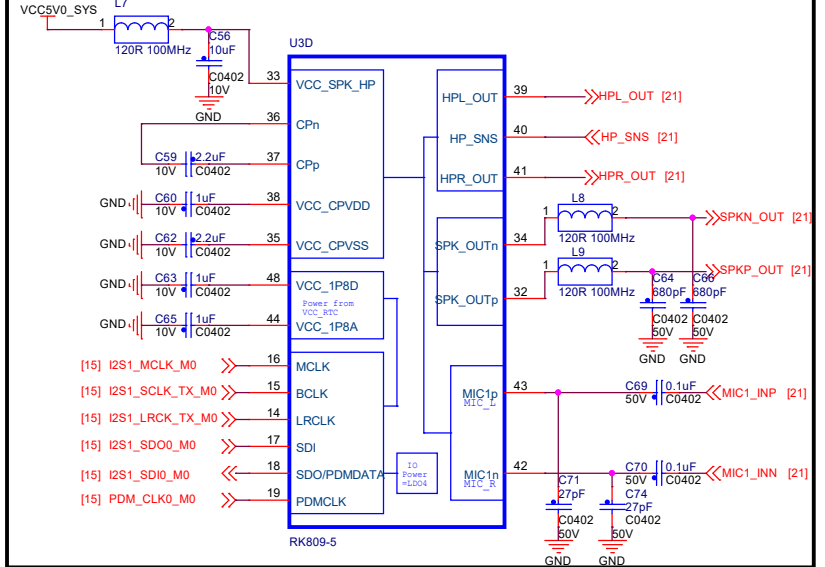
# PMIC RK809 Managerment



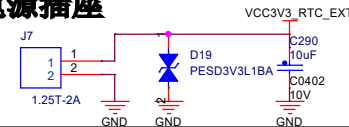
## PMIC RK809 LDO



## PMIC RK809 CODEC



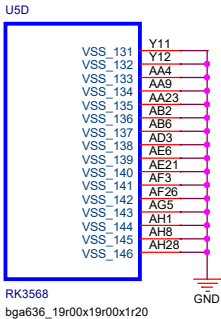
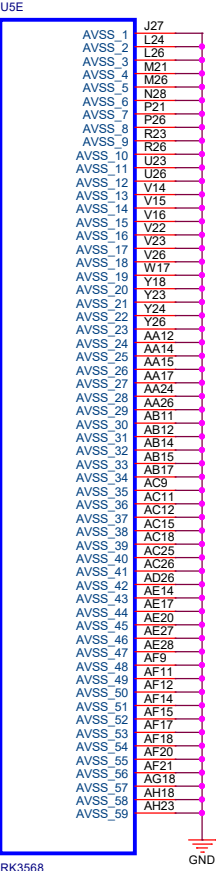
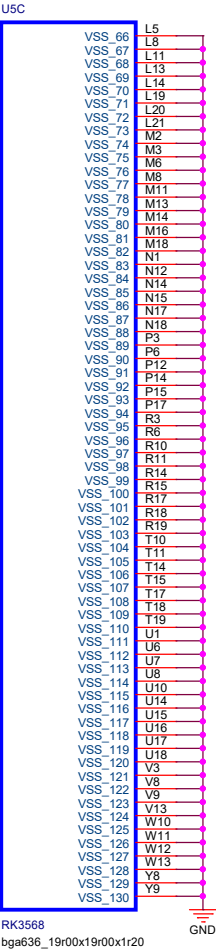
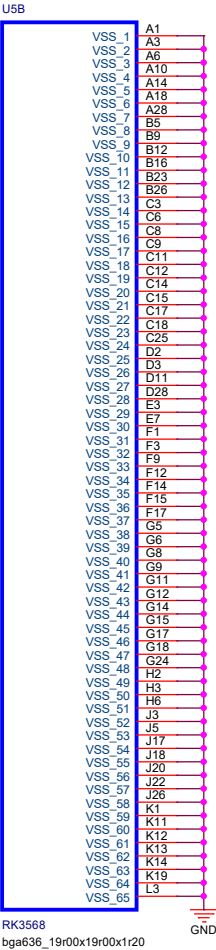
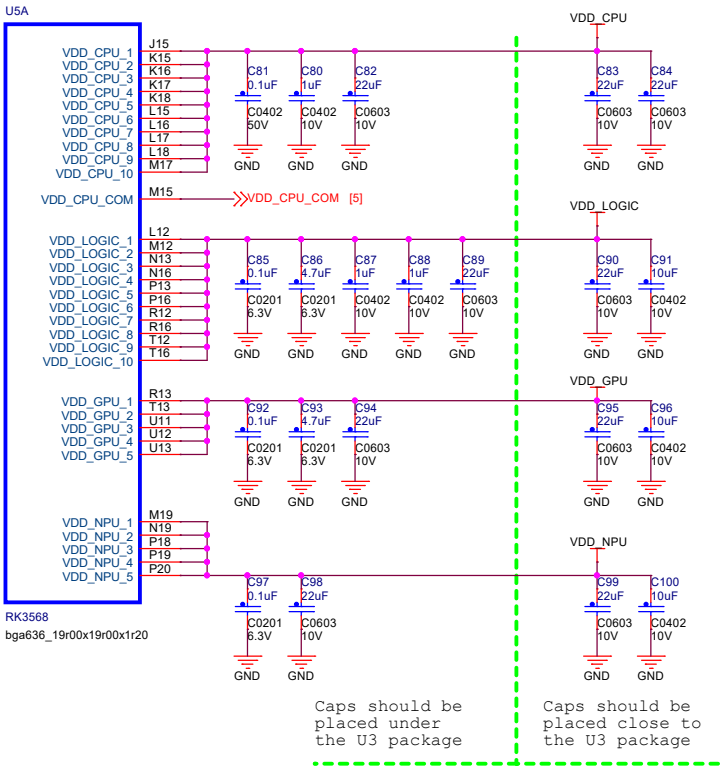
## RTC电源插座



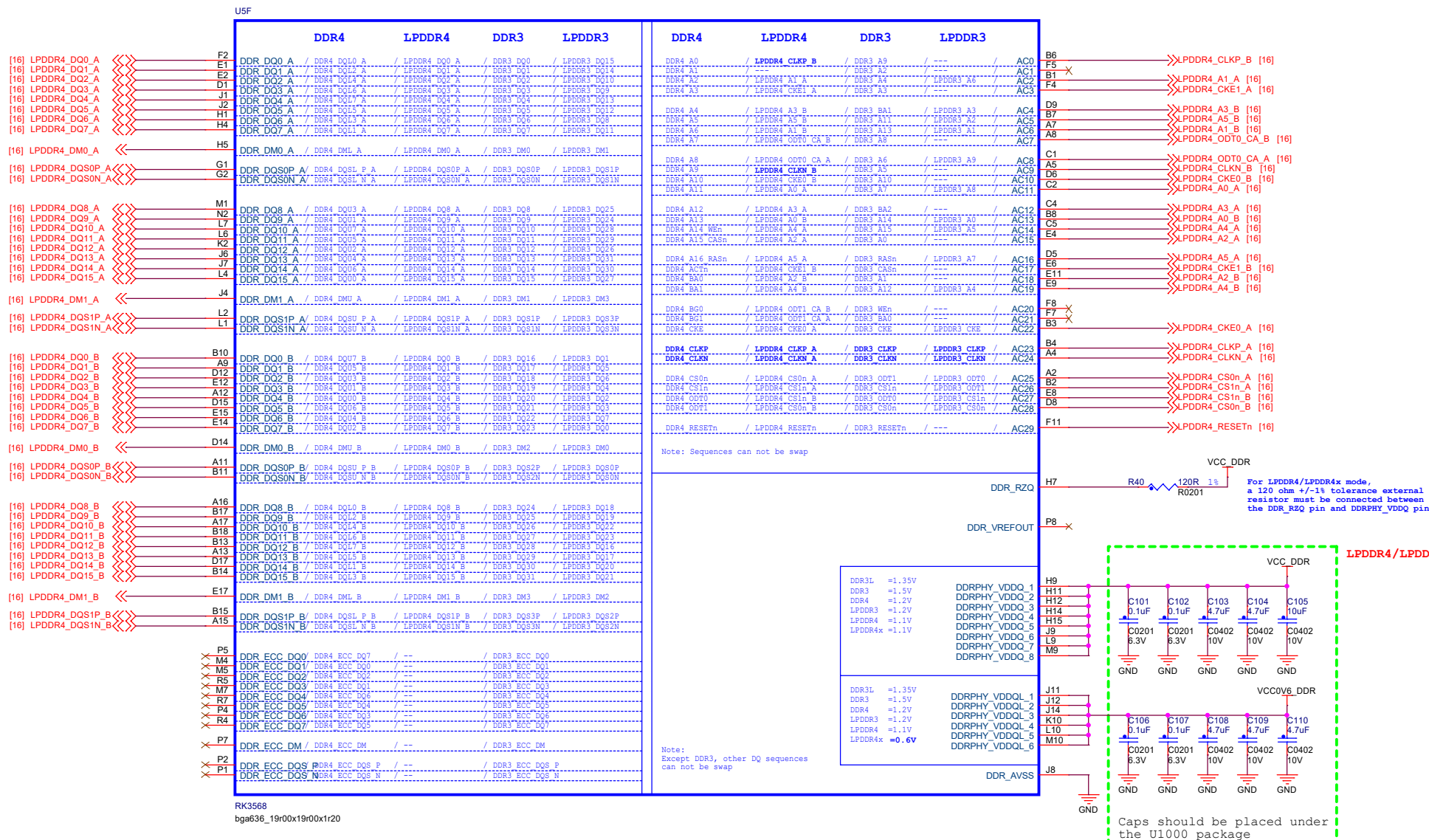
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野火_EBF RK3568 LBC		
Size A3	Document Number SYS PMIC	Rev V1.0
Date: Wednesday, July 05, 2023	Sheet 5	of 26

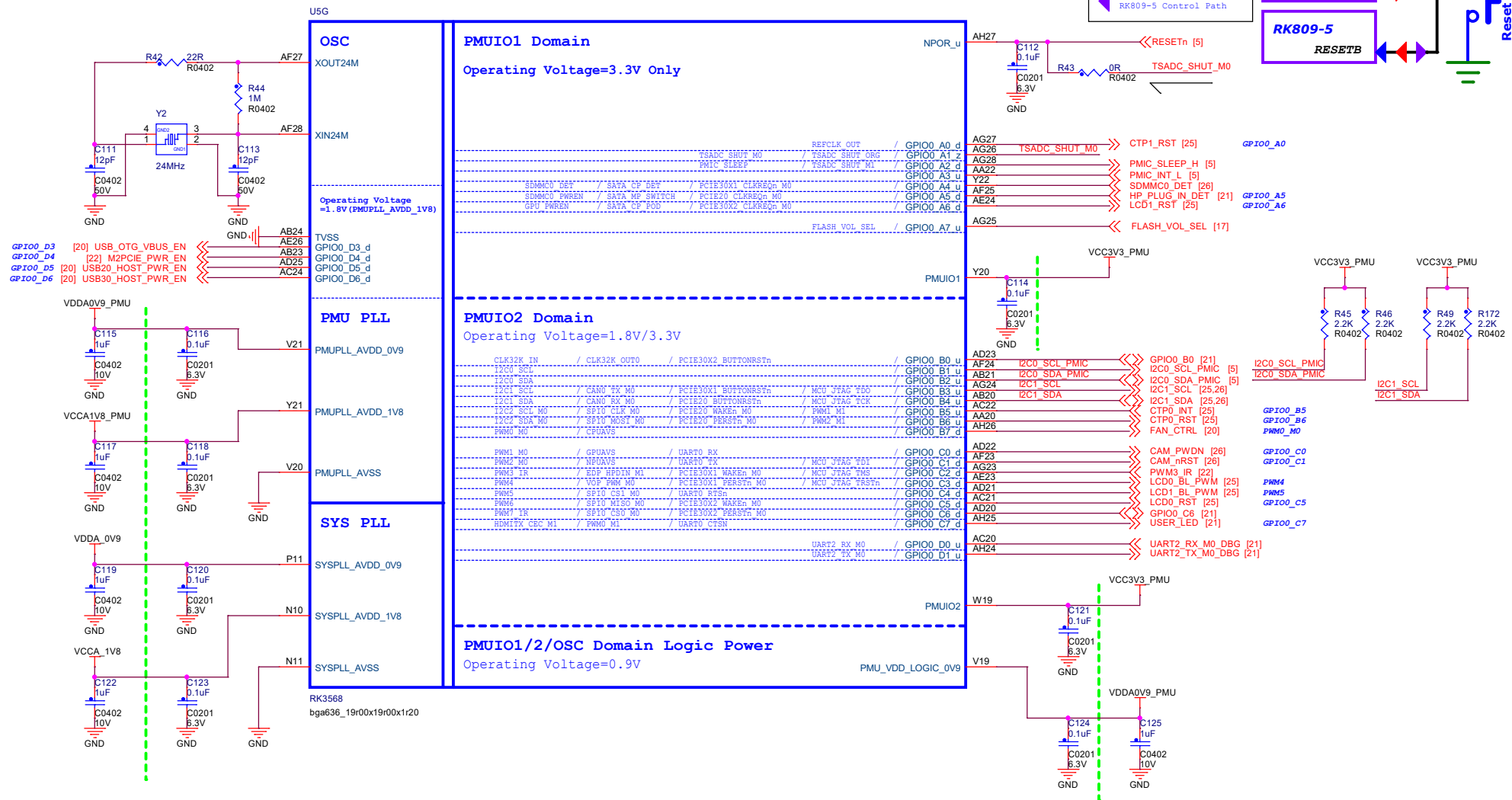
RK3568 PWR



# RK3568 DDR PHY



# RK3568 OSC/PLL/PMUIO

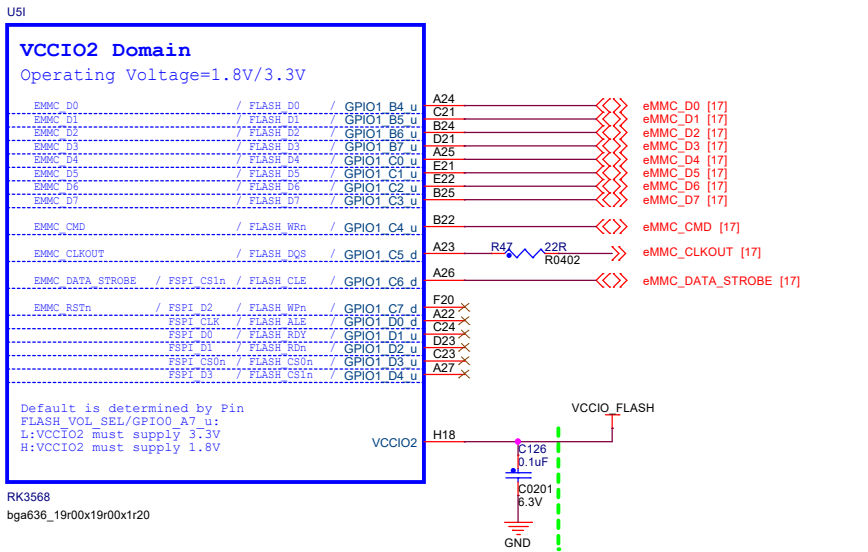


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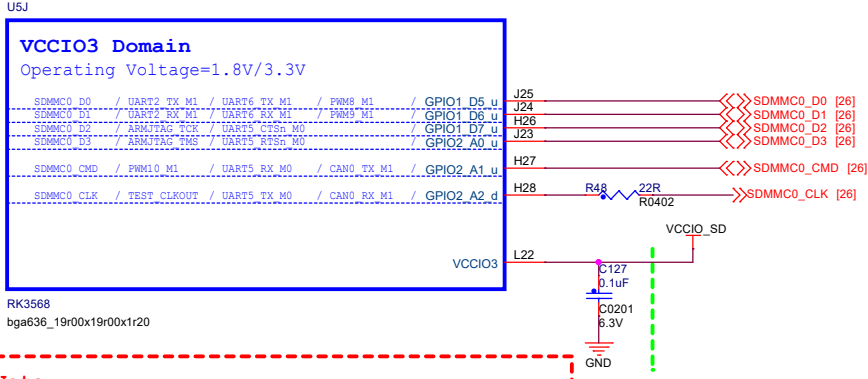
Caps of between dashed green lines and U3 should be placed under the U3 package. Other caps should be placed close to the U3 package



# RK3568 VCCIO2 Domain

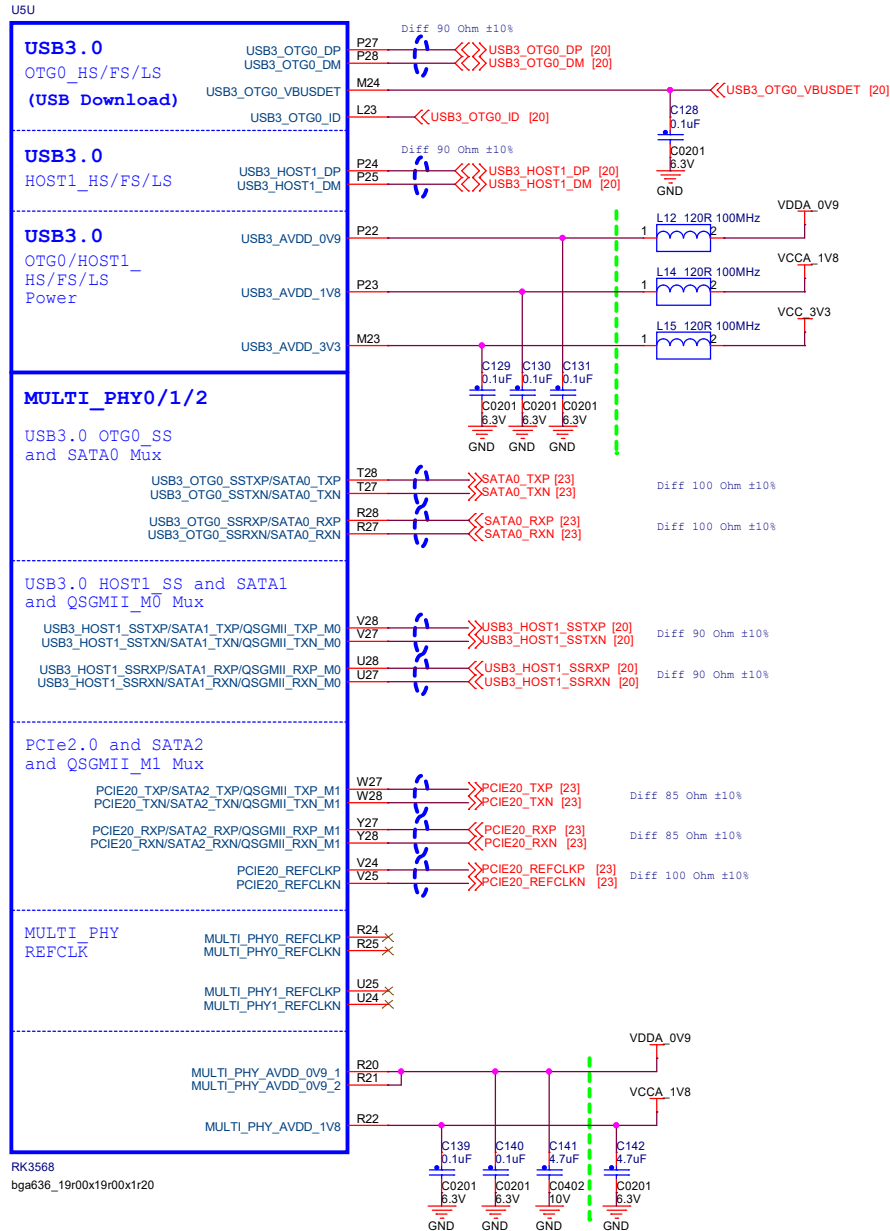


# RK3568 VCCIO3 Domain



**Note:**  
Caps of between dashed green lines and U3 should be placed under the U3 package.  
Other caps should be placed close to the U3 package

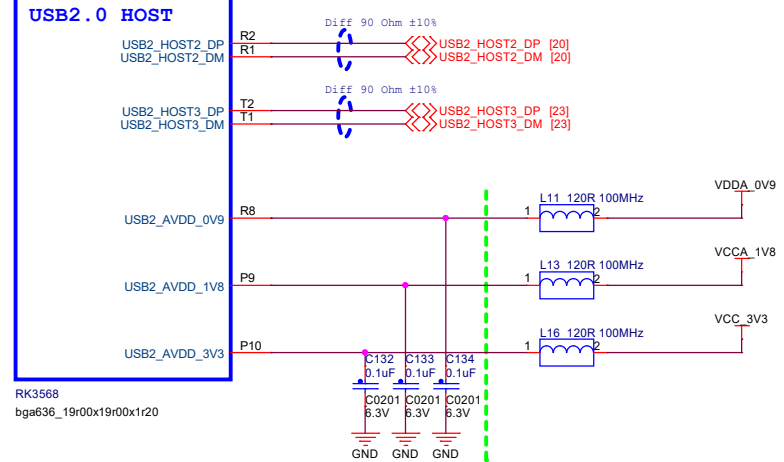
# RK3568 USB3.0/SATA/QSGMII/PCIE2.0 x1



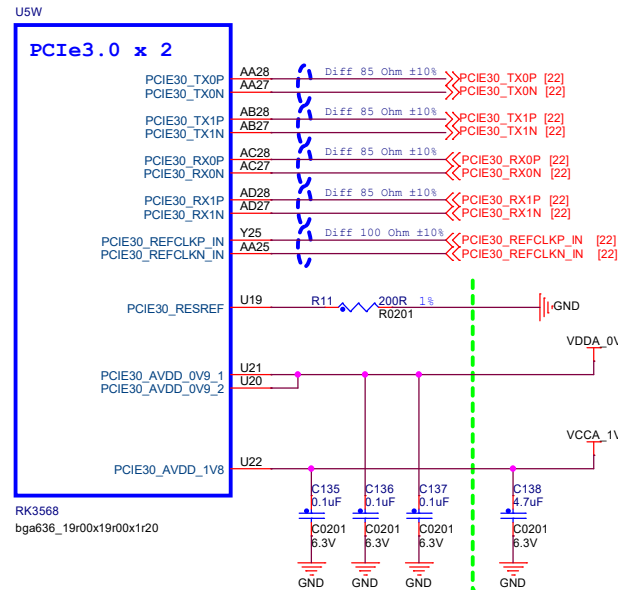
## Note:

Caps of between dashed green lines and U3 should be placed under the U3 package.  
Other caps should be placed close to the U3 package

# RK3568 USB2.0 HOST



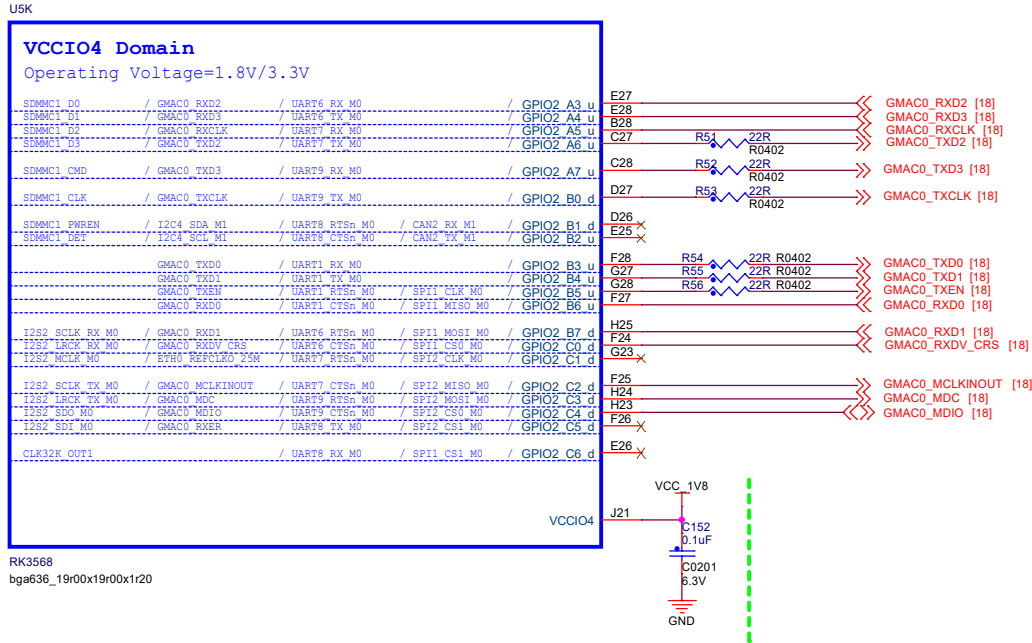
# RK3568 PCIE3.0 x2



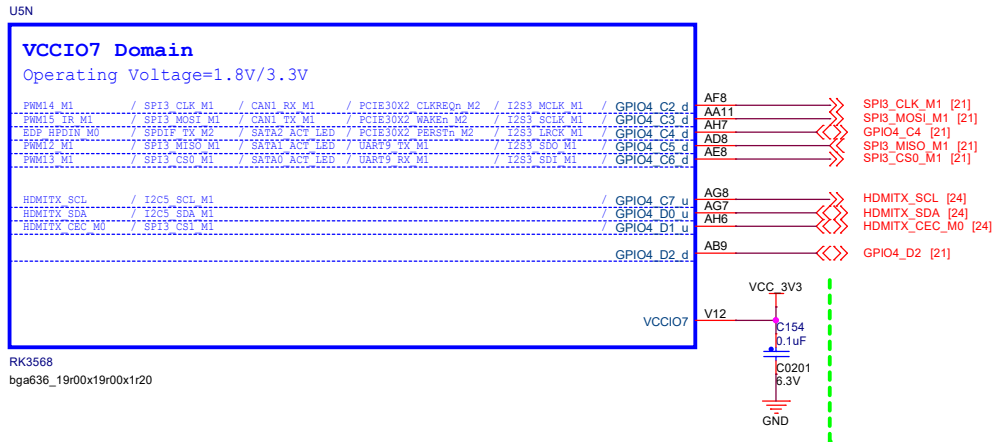
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Title			野火_EBF RK3568 LBC
Size	Document Number	Rev	
A3	USB/PCIE/STAT PHY	V1.0	
Date:	Wednesday, July 05, 2023	Sheet	10 of 26

## RK3568 VCCIO4 Domain



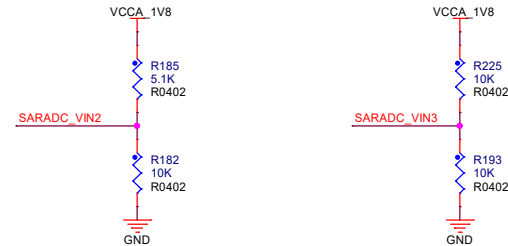
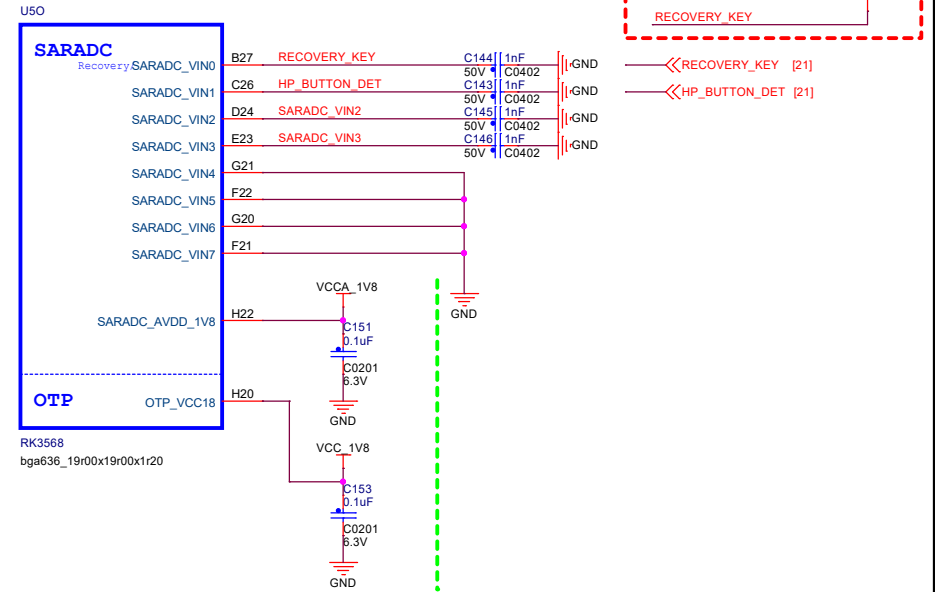
## RK3568 VCCIO7 Domain



### Note:

Caps of between dashed green lines and U3 should be placed under the U3 package.  
Other caps should be placed close to the U3 package

## RK3568 SARADC/OTP



Board ID:0x0403 电压: VIN2:1.192V VIN3:0.9V ADC:VIN2:678 VIN3:512

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Title 野火_EBF RK3568 LBC		
Size A3	Document Number SARADC/GPIO	Rev V1.0
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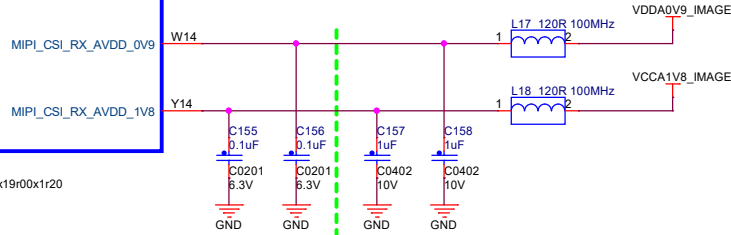
# RK3568 MIPI\_CSI\_RX

U5P

## MIPI CSI RX

MIPI_CSI_RX_D0P	AG12	Diff 100 Ohm ±10%	MIPI_CSI_RX_D0P [26]
MIPI_CSI_RX_D0N	AH12		MIPI_CSI_RX_D0N [26]
MIPI_CSI_RX_D1P	AG11	Diff 100 Ohm ±10%	MIPI_CSI_RX_D1P [26]
MIPI_CSI_RX_D1N	AH11		MIPI_CSI_RX_D1N [26]
MIPI_CSI_RX_D2P	AE11	Diff 100 Ohm ±10%	MIPI_CSI_RX_D2P [26]
MIPI_CSI_RX_D2N	AD11		MIPI_CSI_RX_D2N [26]
MIPI_CSI_RX_D3P	AD9	Diff 100 Ohm ±10%	MIPI_CSI_RX_D3P [26]
MIPI_CSI_RX_D3N	AE9		MIPI_CSI_RX_D3N [26]
MIPI_CSI_RX_CLK0P	AG10	Diff 100 Ohm ±10%	MIPI_CSI_RX_CLK0P [26]
MIPI_CSI_RX_CLK0N	AH10		MIPI_CSI_RX_CLK0N [26]
MIPI_CSI_RX_CLK1P	AG9	Diff 100 Ohm ±10%	MIPI_CSI_RX_CLK1P [26]
MIPI_CSI_RX_CLK1N	AH9		MIPI_CSI_RX_CLK1N [26]

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1



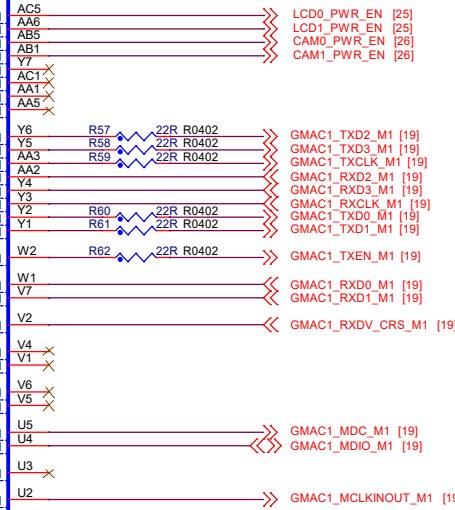
# RK3568 VCCIO6 Domain

U5M

## VCCIO6 Domain

Operating Voltage=1.8V/3.3V

CIF_D0	/ EBC SDD00	/ SDMMC2_D0_M0	/ I2S1_MCLK_M1	/ VOP_BT656_D0_M1	/ GPIO3_C6_d
CIF_D1	/ EBC SDD01	/ SDMMC2_D1_M0	/ I2S1_SCLK_TX_M1	/ VOP_BT656_D1_M1	/ GPIO3_C7_d
CIF_D2	/ EBC SDD02	/ SDMMC2_D2_M0	/ I2S1_LCLK_TX_M1	/ VOP_BT656_D2_M1	/ GPIO3_D0_d
CIF_D3	/ EBC SDD03	/ SDMMC2_D3_M0	/ I2S1_SDO0_M1	/ VOP_BT656_D3_M1	/ GPIO3_D1_d
CIF_D4	/ EBC SDD04	/ SDMMC2_D4_M0	/ I2S1_SDO1_M1	/ VOP_BT656_D4_M1	/ GPIO3_D2_d
CIF_D5	/ EBC SDD05	/ SDMMC2_D5_M0	/ I2S1_SDO2_M1	/ VOP_BT656_D5_M1	/ GPIO3_D3_d
CIF_D6	/ EBC SDD06	/ SDMMC2_DET_M0	/ I2S1_SDO2_M1	/ VOP_BT656_D6_M1	/ GPIO3_D4_d
CIF_D7	/ EBC SDD07	/ SDMMC2_PAREN_M0	/ I2S1_SDO3_M1	/ VOP_BT656_D7_M1	/ GPIO3_D5_d
CIF_D8	/ EBC SDD08	/ GMAC1_TXD2_M1	/ UART1_TX_M1	/ PDM_CLK0_M1	/ GPIO3_D6_d
CIF_D9	/ EBC SDD09	/ GMAC1_TXD3_M1	/ UART1_RX_M1	/ PDM_SDO1_M1	/ GPIO3_D7_d
CIF_D10	/ EBC SDD010	/ GMAC1_RXCLK_M1	/ UART1_TX_M1	/ PDM_CLK1_M1	/ GPIO4_A0_d
CIF_D11	/ EBC SDD011	/ GMAC1_RXD2_M1	/ UART1_TX_M2	/ PDM_SDO1_M1	/ GPIO4_A1_d
CIF_D12	/ EBC SDD012	/ GMAC1_RXD3_M1	/ UART1_TX_M2	/ PDM_SDO2_M1	/ GPIO4_A2_d
CIF_D13	/ EBC SDD013	/ GMAC1_RXD0_M1	/ UART1_RX_M2	/ PDM_SDO1_M1	/ GPIO4_A3_d
CIF_D14	/ EBC SDD014	/ GMAC1_TXD0_M1	/ UART1_RX_M2	/ I2S2_LCLK_RX_M1	/ GPIO4_A4_d
CIF_D15	/ EBC SDD015	/ GMAC1_TXD1_M1	/ UART1_RX_M2	/ I2S2_LCLK_RX_M1	/ GPIO4_A5_d
ISP_FLASHTRIGOUT	/ EBC SDCE0	/ GMAC1_TXEN_M1	/ SPI3_CS0_M0	/ I2S1_SCLK_RX_M1	/ GPIO4_A6_d
CAM_CLKOUT0	/ EBC SDCE1	/ GMAC1_RXD0_M1	/ SPI3_CS1_M0	/ I2S1_LCLK_RX_M1	/ GPIO4_A7_d
CAM_CLKOUT1	/ EBC SDCE2	/ GMAC1_RXD1_M1	/ SPI3_MISO_M0	/ I2S1_SDO1_M1	/ GPIO4_B0_d
ISP_PRELIGHT_TRIG	/ EBC SDCE3	/ GMAC1_RXDV_CRS_M1	/ I2S1_SDO2_M1	/ I2S1_SDO2_M1	/ GPIO4_B1_d
I2C4_SDA_M0	/ EBC VCOM	/ GMAC1_RXER_M1	/ SPI3_MOSI_M0	/ I2S2_SDI_M1	/ GPIO4_B2_d
I2C4_SCL_M0	/ EBC GD08	/ ETH1_REFCLK0_25M_M1	/ SPI3_CLK_M0	/ I2S2_SDO_M1	/ GPIO4_B3_d
I2C2_SDA_M1	/ EBC GDSP	/ CAN2_RX_M0	/ I2S2_SDO1_M1	/ I2S2_SDO1_M1	/ GPIO4_B4_d
I2C2_SCL_M1	/ EBC SD58A	/ CAN2_TX_M0	/ I2S1_SDO2_M1	/ I2S1_SDO2_M1	/ GPIO4_B5_d
CIF_HREF	/ EBC SDLE	/ GMAC1_MDC_M1	/ UART1_RTS_M1	/ I2S2_MCLK_M1	/ GPIO4_B6_d
CIF_VSYNC	/ EBC SD0E	/ GMAC1_MDIO_M1	/ I2S2_SCLK_TX_M1	/ I2S2_SCLK_TX_M1	/ GPIO4_B7_d
CIF_CLKOUT	/ EBC GDCLK	/ GMAC1_MDC_M1	/ PWM1_IR_M1	/ I2S2_SCLK_TX_M1	/ GPIO4_C0_d
CIF_CLKIN	/ EBC SDCLK	/ GMAC1_MCLKINOUT_M1	/ UART1_CTS_M1	/ I2S2_SCLK_RX_M1	/ GPIO4_C1_d



RK3568  
bga636\_19r00x19r00x1r20

## Note:

Caps of between dashed green lines and U3 should be placed under the U3 package. Other caps should be placed close to the U3 package

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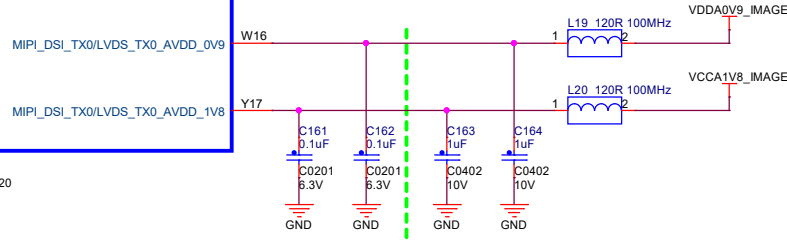
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Size A3	Document Number VI Interface	Rev V1.0
Date: Wednesday, July 05, 2023 Sheet 12 of 26		

# RK3568 MIPI\_DSI\_TX0/LVDS\_TX0

U5R

## MIPI DSI TX0/LVDS TX0

MIPI\_DSI\_TX0\_D0P/LVDS\_TX0\_D0P AH17 Diff 100 Ohm ±10% MIPI\_DSI\_TX0\_D0P [25]  
 MIPI\_DSI\_TX0\_D0N/LVDS\_TX0\_D0N AG17 MIPI\_DSI\_TX0\_D0N [25]  
 MIPI\_DSI\_TX0\_D1P/LVDS\_TX0\_D1P AH16 Diff 100 Ohm ±10% MIPI\_DSI\_TX0\_D1P [25]  
 MIPI\_DSI\_TX0\_D1N/LVDS\_TX0\_D1N AG16 MIPI\_DSI\_TX0\_D1N [25]  
 MIPI\_DSI\_TX0\_D2P/LVDS\_TX0\_D2P AH14 Diff 100 Ohm ±10% MIPI\_DSI\_TX0\_D2P [25]  
 MIPI\_DSI\_TX0\_D2N/LVDS\_TX0\_D2N AG14 MIPI\_DSI\_TX0\_D2N [25]  
 MIPI\_DSI\_TX0\_D3P/LVDS\_TX0\_D3P AH13 Diff 100 Ohm ±10% MIPI\_DSI\_TX0\_D3P [25]  
 MIPI\_DSI\_TX0\_D3N/LVDS\_TX0\_D3N AG13 MIPI\_DSI\_TX0\_D3N [25]  
 MIPI\_DSI\_TX0\_CLKP/LVDS\_TX0\_CLKP AH15 Diff 100 Ohm ±10% MIPI\_DSI\_TX0\_CLKP [25]  
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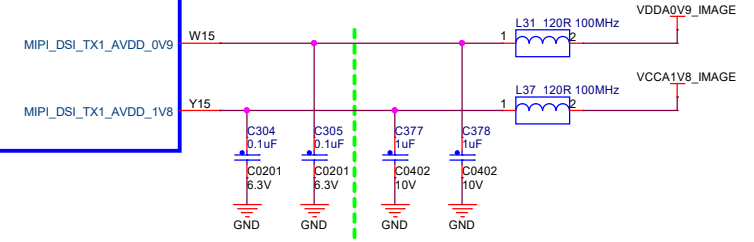
RK3568  
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# RK3568 MIPI\_DSI\_TX1

U5S

## MIPI DSI TX1

MIPI\_DSI\_TX1\_D0P Diff 100 Ohm ±10% MIPI\_DSI\_TX1\_D0P [25]  
 MIPI\_DSI\_TX1\_D0N AE18 MIPI\_DSI\_TX1\_D0N [25]  
 MIPI\_DSI\_TX1\_D1P Diff 100 Ohm ±10% MIPI\_DSI\_TX1\_D1P [25]  
 MIPI\_DSI\_TX1\_D1N AC17 MIPI\_DSI\_TX1\_D1N [25]  
 MIPI\_DSI\_TX1\_D2P Diff 100 Ohm ±10% MIPI\_DSI\_TX1\_D2P [25]  
 MIPI\_DSI\_TX1\_D2N AC14 MIPI\_DSI\_TX1\_D2N [25]  
 MIPI\_DSI\_TX1\_D3P Diff 100 Ohm ±10% MIPI\_DSI\_TX1\_D3P [25]  
 MIPI\_DSI\_TX1\_D3N AE12 MIPI\_DSI\_TX1\_D3N [25]  
 MIPI\_DSI\_TX1\_CLKP Diff 100 Ohm ±10% MIPI\_DSI\_TX1\_CLKP [25]  
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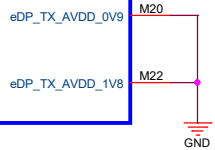
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# RK3568 eDP TX

U5T

## eDP\_TX

eDP\_TX\_D0P J28 X  
 eDP\_TX\_D0N K27 X  
 eDP\_TX\_D1P K28 X  
 eDP\_TX\_D1N L27 X  
 eDP\_TX\_D2P L28 X  
 eDP\_TX\_D2N M27 X  
 eDP\_TX\_D3P M28 X  
 eDP\_TX\_D3N N27 X  
 eDP\_TX\_AUXP L25 X  
 eDP\_TX\_AUXN M25 X



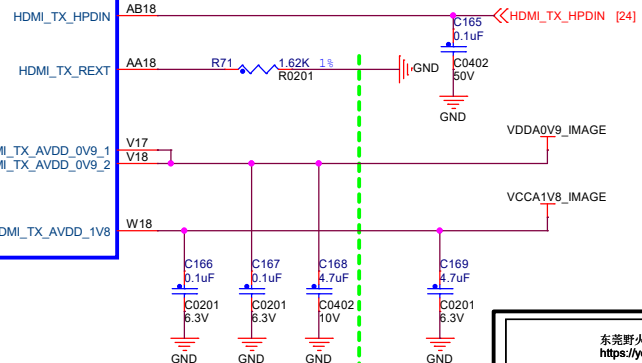
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# RK3568 HDMI2.0 TX

U5Q

## HDMI2.0 TX

HDMI\_TX\_D2P Diff 100 Ohm ±10% R63 2.2R R0201 HDMI\_TX2P\_PORT [24]  
 HDMI\_TX\_D2N AH22 R64 2.2R R0201 HDMI\_TX2N\_PORT [24]  
 HDMI\_TX\_D1P AG21 R65 2.2R R0201 HDMI\_TX1P\_PORT [24]  
 HDMI\_TX\_D1N AH21 R66 2.2R R0201 HDMI\_TX1N\_PORT [24]  
 HDMI\_TX\_D0P AG20 R67 2.2R R0201 HDMI\_TX0P\_PORT [24]  
 HDMI\_TX\_D0N AH20 R68 2.2R R0201 HDMI\_TX0N\_PORT [24]  
 HDMI\_TX\_CLKP AH19 2.2R R0201 HDMI\_TXCLKP\_PORT [24]  
 HDMI\_TX\_CLKN AG19 R70 2.2R R0201 HDMI\_TXCLKN\_PORT [24]



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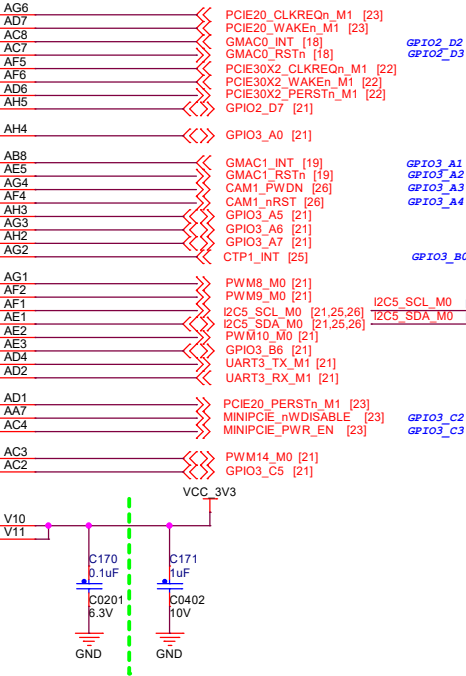
Title		
野火_EBF RK3568 LBC		
Size	Document Number	Rev
A3	VO Interface_1	V1.0
Date: Wednesday, July 05, 2023		
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RK3568 VCCIO5 Domain

USL

VCCIO5 Domain									
Operating Voltage=1.8V/3.3V									
LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREQn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d				
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d				
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREQn M1	/ I2S1 LCLK TX M2	/ GPIO2 D2 d				
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDIO M2	/ GPIO2 D3 d				
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREQn M1	/ I2S1 SDIO M2	/ GPIO2 D4 d				
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SDIO M2	/ GPIO2 D5 d				
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ I2S1 SDIO M2	/ GPIO2 D6 d				
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART9 TX M1	/ I2S1 SDIO M2	/ GPIO2 D7 d				
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART9 RX M1	/ I2S1 SDIO M2	/ GPIO3 A0 d				
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d				
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d				
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d				
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LCLK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d				
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 CS0 M1	/ SDMMC2 CS0 M1	/ GPIO3 A5 d				
LCDC D13	/ VOP BT1120 D1X	/ GMAC1 RXCLK M0	/ I2S3 SD1 M0	/ SDMMC2 CLK M1	/ GPIO3 A6 d				
LCDC D14	/ VOP BT1120 D5	/ GMAC1 RXCLK M0	/ SDMMC2 DEN M1	/ SDMMC2 DEN M1	/ GPIO3 A7 d				
LCDC D15	/ VOP BT1120 D6	/ ETH1 REPCIO 25M M0	/ SDMMC2 PWREN M1	/ SDMMC2 PWREN M1	/ GPIO3 B0 d				
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d				
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d				
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXD0 CHS M0	/ I2C5 SCL M0	/ PWM SDIO M2	/ GPIO3 B3 d				
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXD1 M0	/ I2C5 SDA M0	/ PWM SDIO M2	/ GPIO3 B4 d				
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C5 SCL M1	/ PWM10 M0	/ GPIO3 B5 d				
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d				
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SD12 M2	/ GPIO3 B7 d				
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SD13 M2	/ GPIO3 C0 d				
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDIO M2	/ GPIO3 C1 d				
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDIO M2	/ GPIO3 C2 d				
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d				
PWM14 M0	/ VOP PWM M1	/ GMAC1 NDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d				
PWM15 TX M0	/ SP015 TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LCLK RX M2	/ GPIO3 C5 d				
					VCCIO5_1				
					VCCIO5_2				

RK3568  
bga636\_19r00x19r00x120



Note:

Caps of between dashed green lines and U3 should be placed under the U3 package.  
Other caps should be placed close to the U3 package

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## RK3568 VCCIO1 Domain

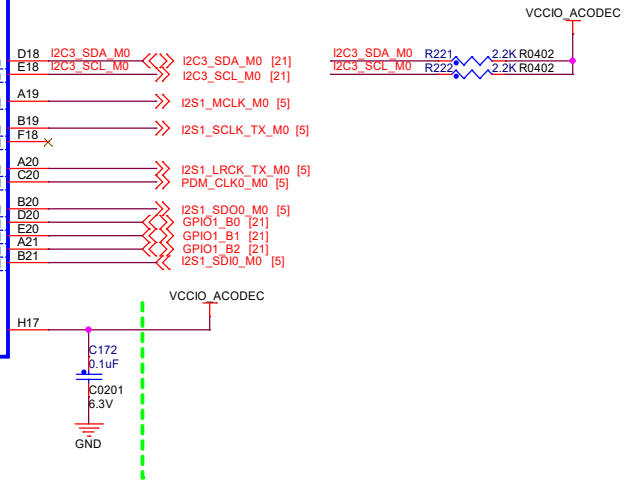
U5H

## VCCI01 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA M0	/ UART3_RX M0	/ CAN1_RX M0	/ AUDIOPWM_LOUT P	/ ACODEC_ADC_DATA	/ GPIO1_A0 u
I2C3_SCL M0	/ UART3_TX M0	/ CAN1_TX M0	/ AUDIOPWM_LOUT N	/ ACODEC_ADC_CLK	/ GPIO1_A1 u
I2S1_MCLK M0	/ UART3_RTSn M0	/ SCR_CLK	/ PCIE30X1_PERSTn M2		/ GPIO1_A2 u
I2S1_SCLK_TX M0	/ UART3_CTSn M0	/ SCR_IO	/ PCIE30X1_WAREn M2	/ ACODEC_DAC_CLK	/ GPIO1_A3 u
I2S1_SCLK_RX M0	/ UART4_RX M0	/ FSW_CLKn M0	/ SPI0F_TX M0		/ GPIO1_A4 u
I2S1_LRCK_TX M0	/ UART4_RTSn M0	/ SCR_RST	/ PCIE30X1_CLERQn M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5 u
I2S1_LRCK_RX M0	/ UART4_TX M0	/ FSW_CLKO M0	/ AUDIOPWM_ROUT P		/ GPIO1_A6 u
I2S1_SDOO M0	/ UART4_CTSn M0	/ SCR_DET	/ AUDIOPWM_ROUT N	/ ACODEC_DAC_DATA	/ GPIO1_A7 u
I2S1_SDO1 M0	/ I2S1_SDO1 M0	/ FSW_SDO1 M0	/ PCIE200_CLKREQn M2	/ ACODEC_DAC_RESET	/ GPIO1_B1 u
I2S1_SDO2 M0	/ I2S1_SDO2 M0	/ FSW_SDO2 M0	/ PCIE200_WAREn M2	/ ACODEC_DAC_SYNC	/ GPIO1_B2 u
I2S1_SDO3 M0	/ I2S1_SDO1 M0	/ FSW_SDO1 M0	/ PCIE200_PERSTn M2		/ GPIO1_B3 u
	/ I2S1_SDO0 M0	/ FSW_SDO0 M0			/ GPIO1_B4 u

VCCIO1



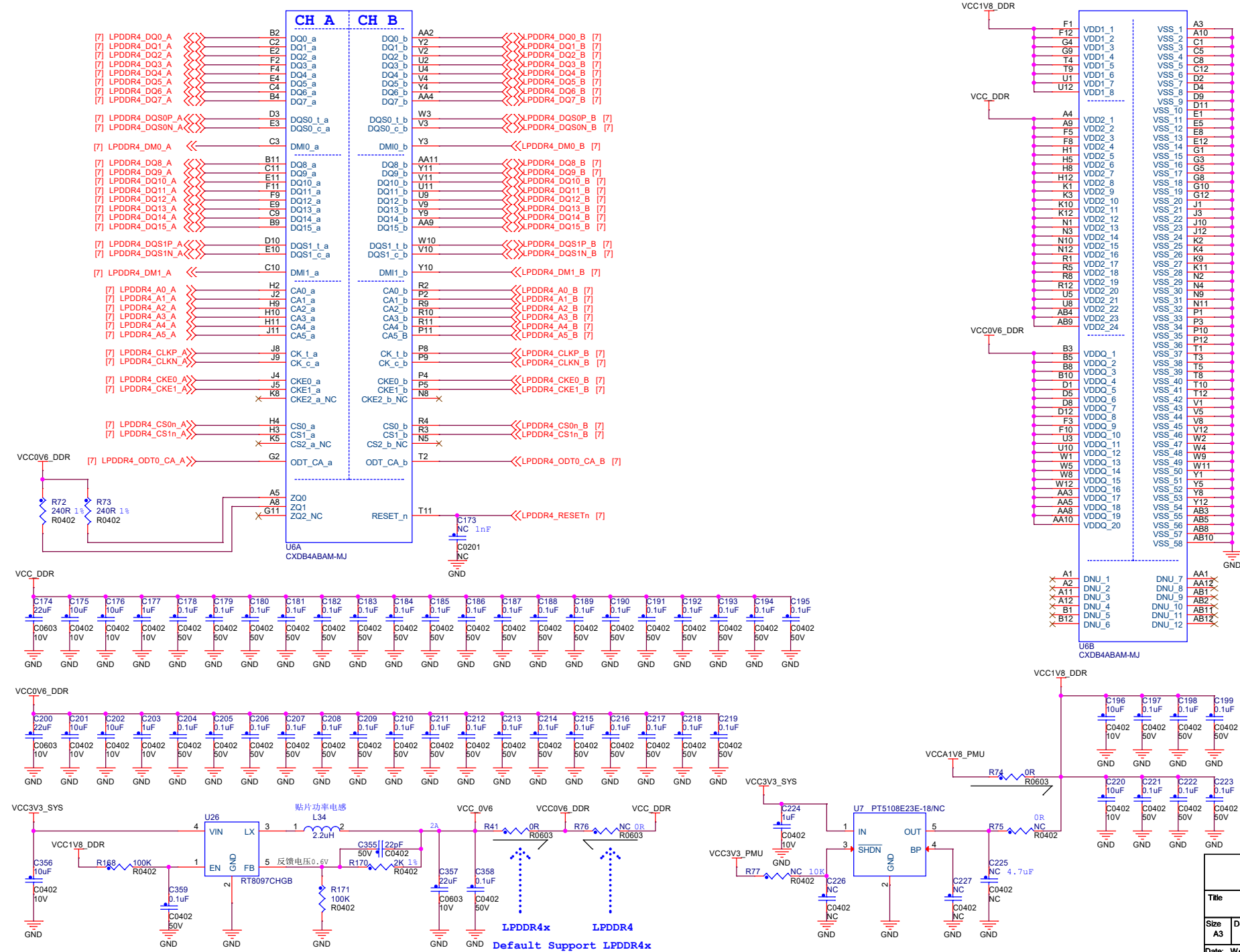
**Note:**

Caps of between dashed green lines and U3  
should be placed under the U3 package.  
Other caps should be placed close to the U3 package

Title	野火_EBF RK3568 核心板
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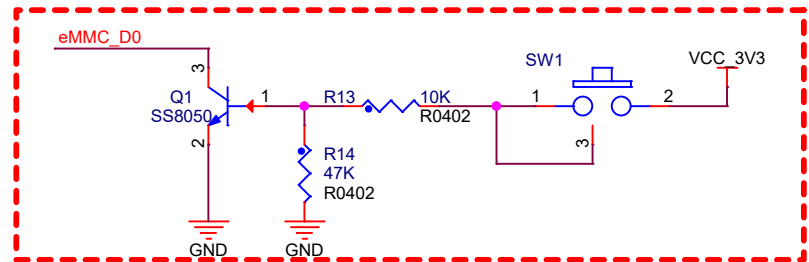
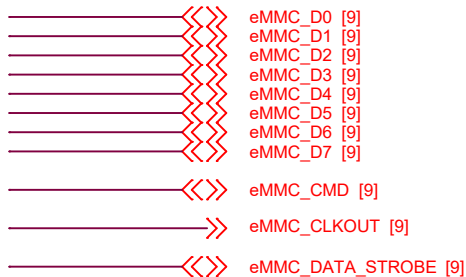
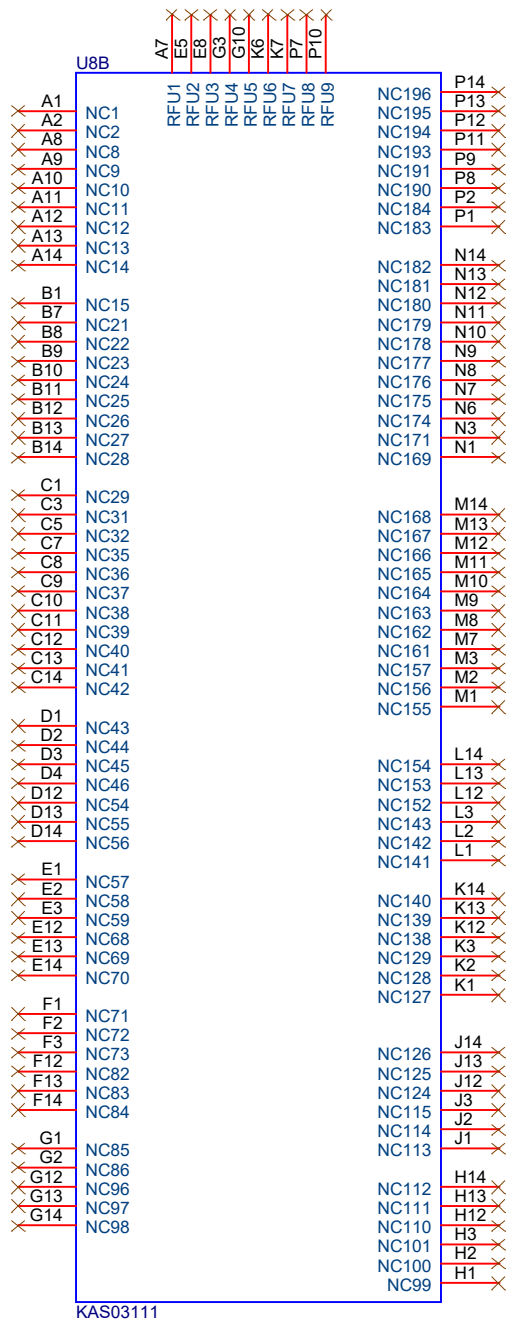
Size A3	Document Number Audio Interface	Rev V1.0
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**LPDDR4 / 4x**



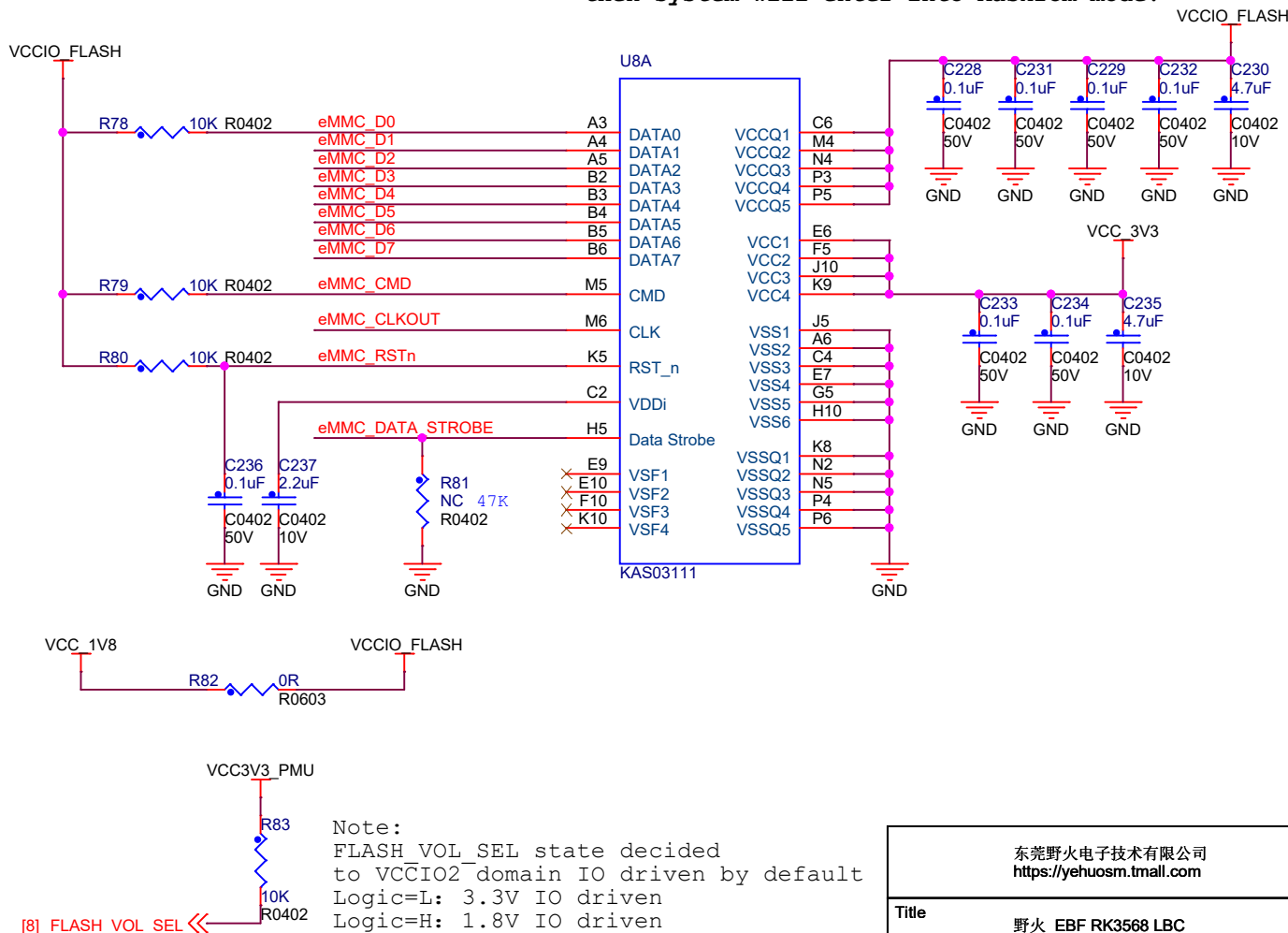


# eMMC Flash



Note:

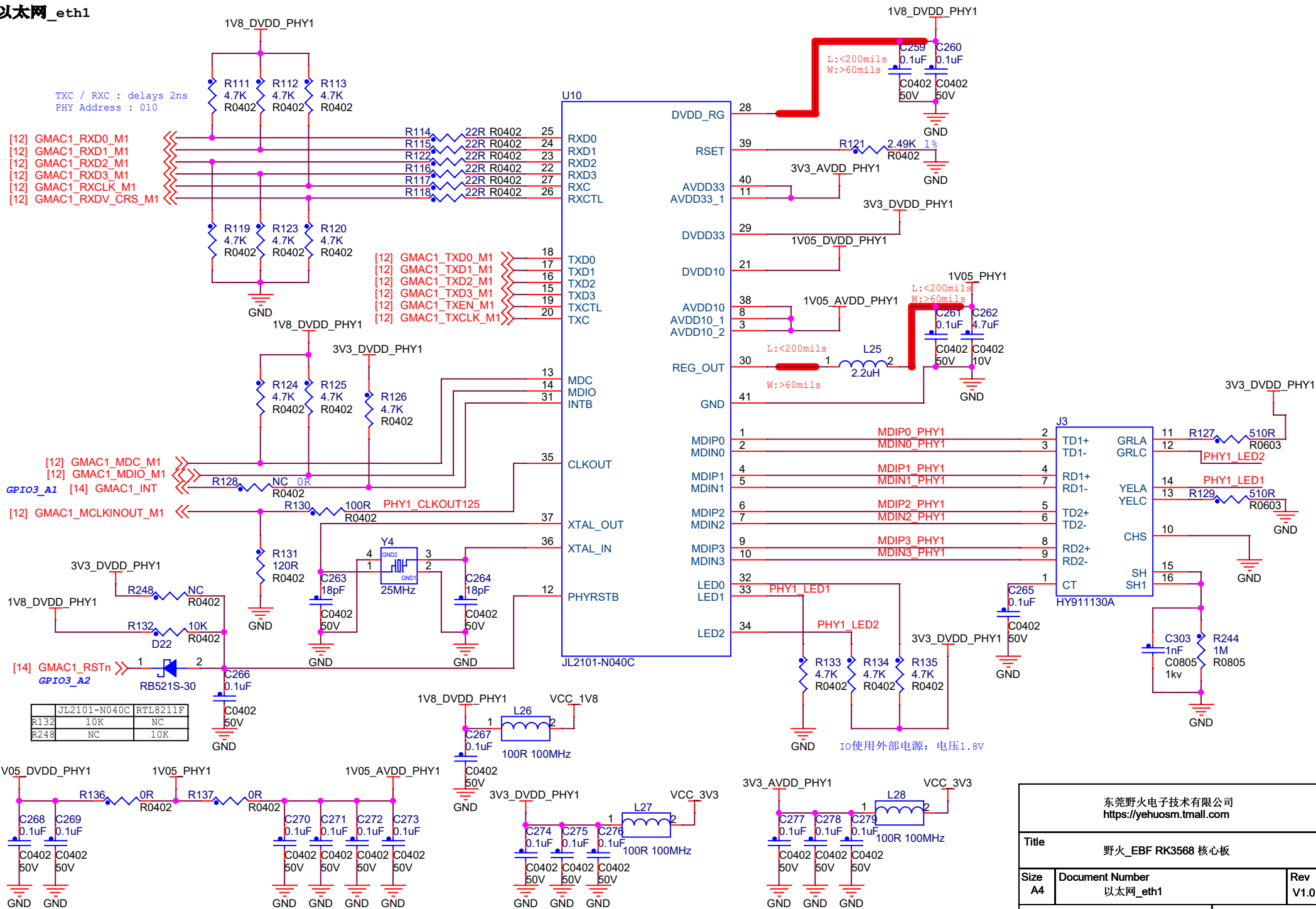
For eMMC or Nand Flash:  
If eMMC\_D0/FLASH\_D0=0V at after power on and reset,  
then system will enter into Maskrom mode.



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## 以太网\_eth1



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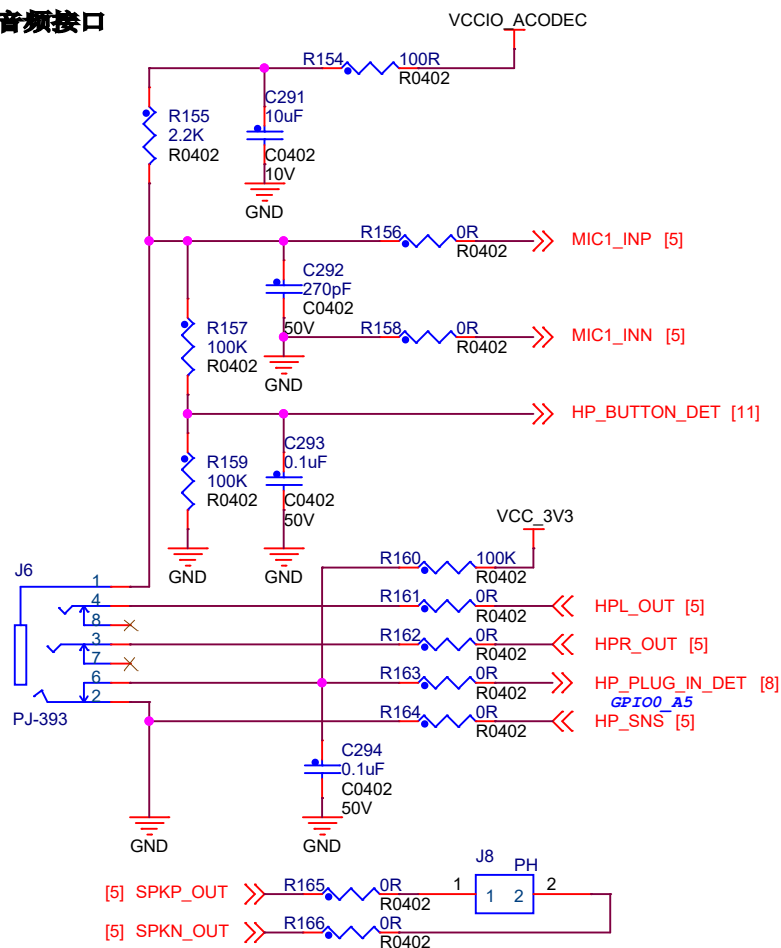
Title	野火_EBF RK3568 核心板
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Size A4	Document Number 以太网_eth1	Rev V1.0
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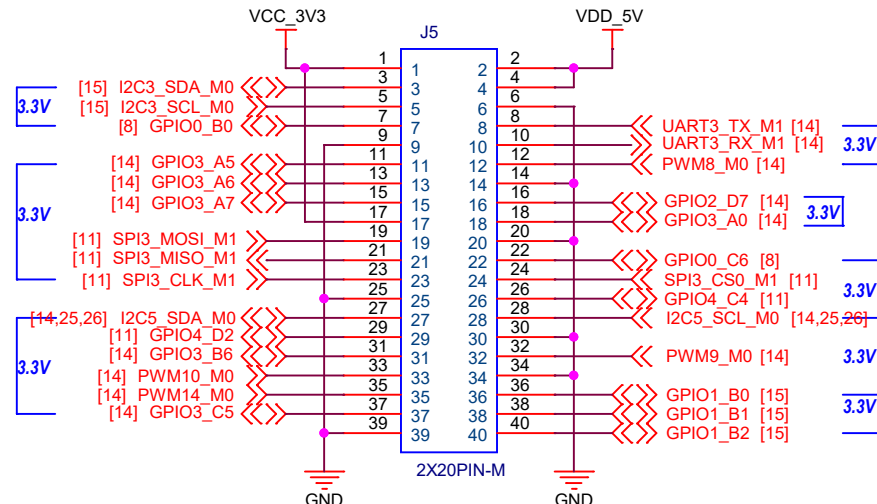
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## 音频接口

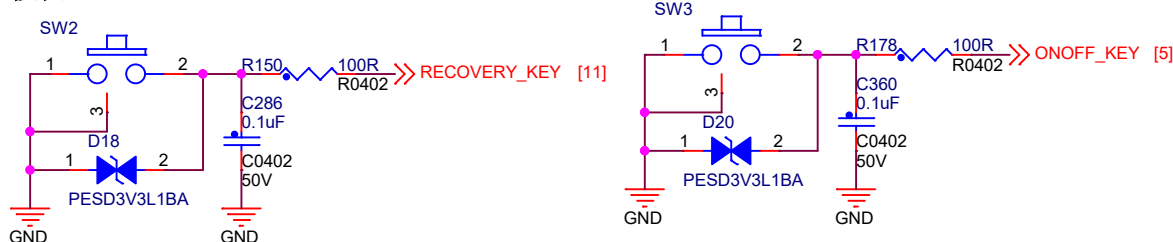


## IO 引出

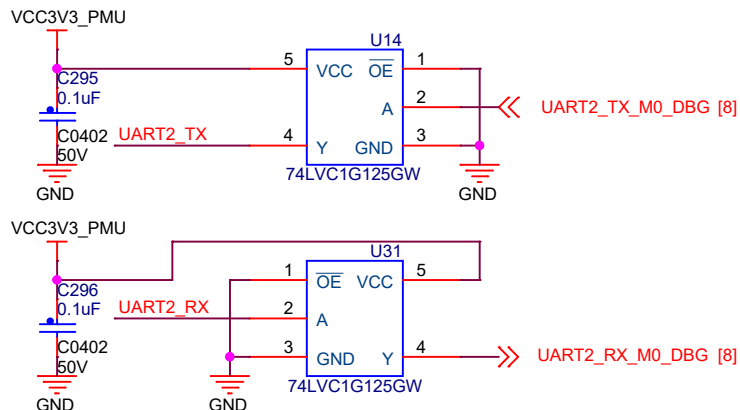
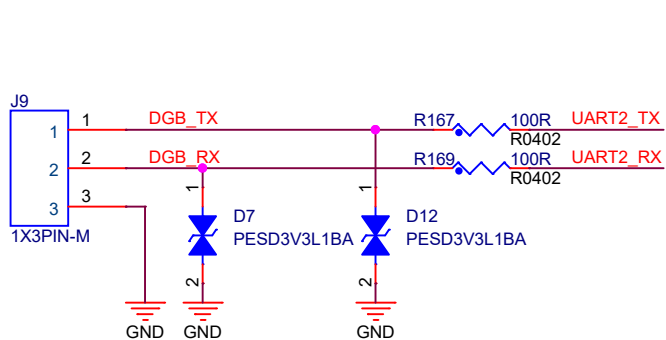


注：所有引出的GPIO只兼容3.3V

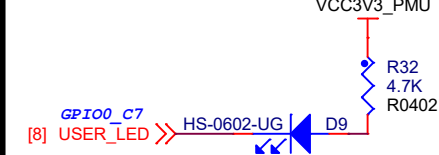
## 按键



## Debug接口



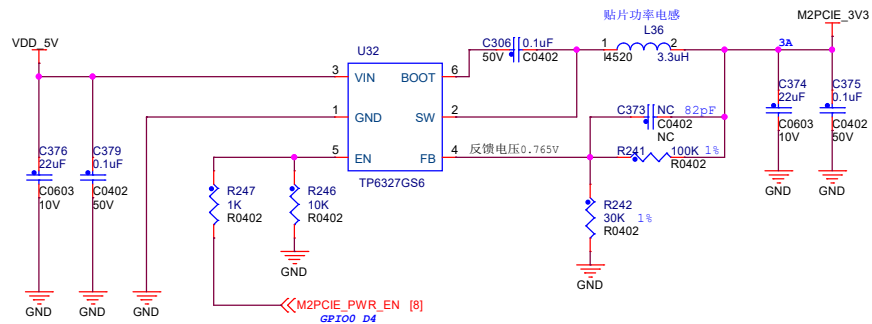
## LED



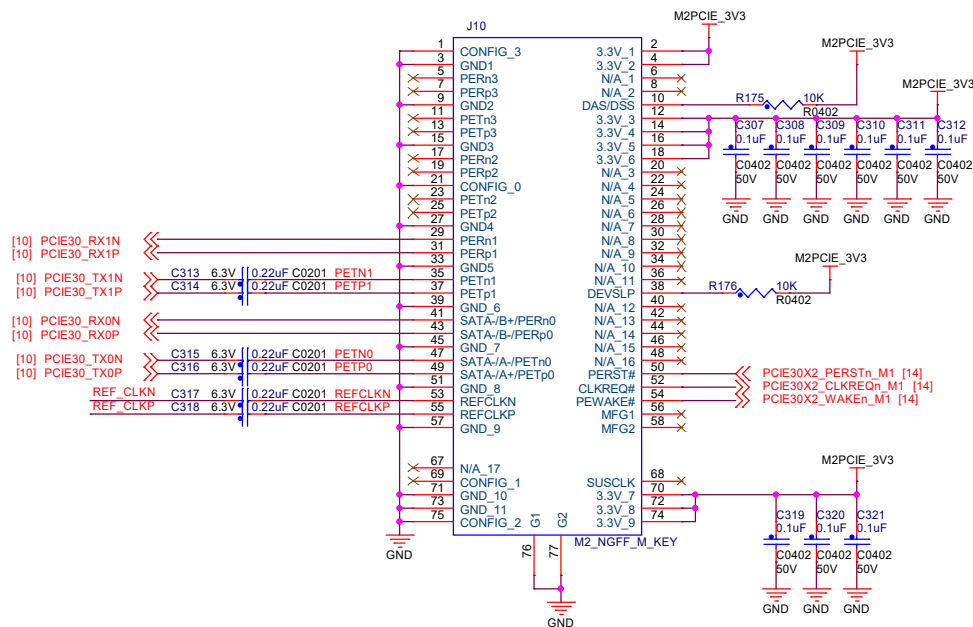
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Size A4	Document Number 音频/DEBUG/IO引出/按键/LED	Rev V1.0
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M.2 PCIE POWER 3.3V



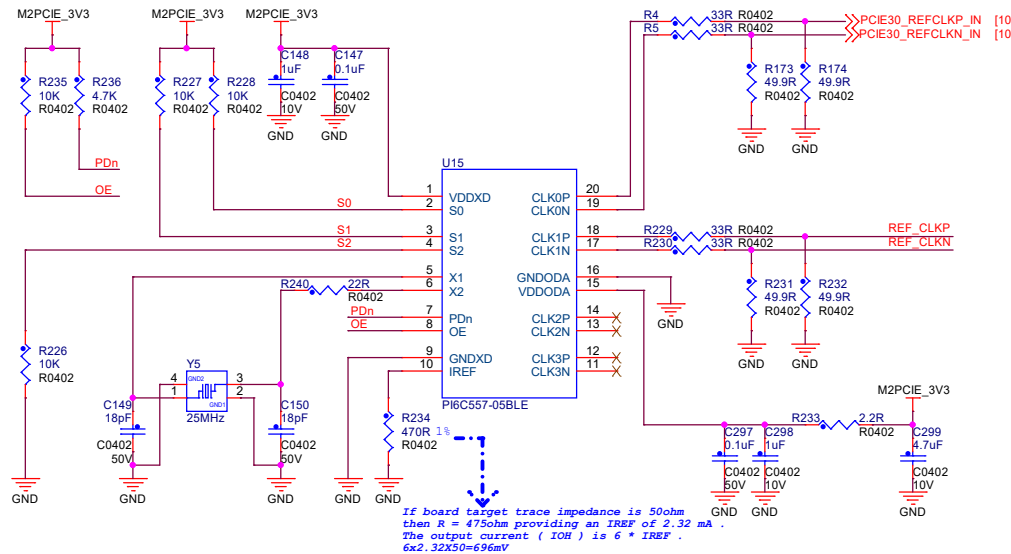
M.2 PCIE3.0 x 2Lanes



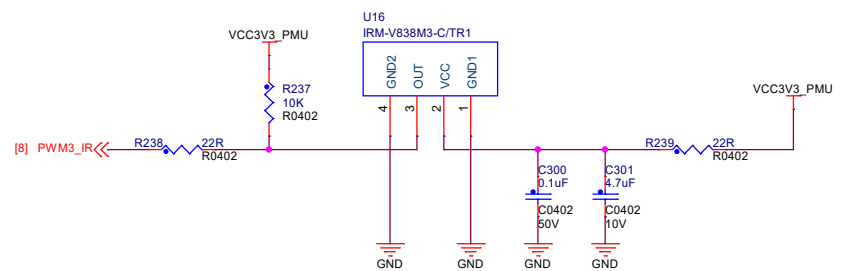
## 贴片螺母



```
M.2 PCIE REF_CLKP 100MHz
```



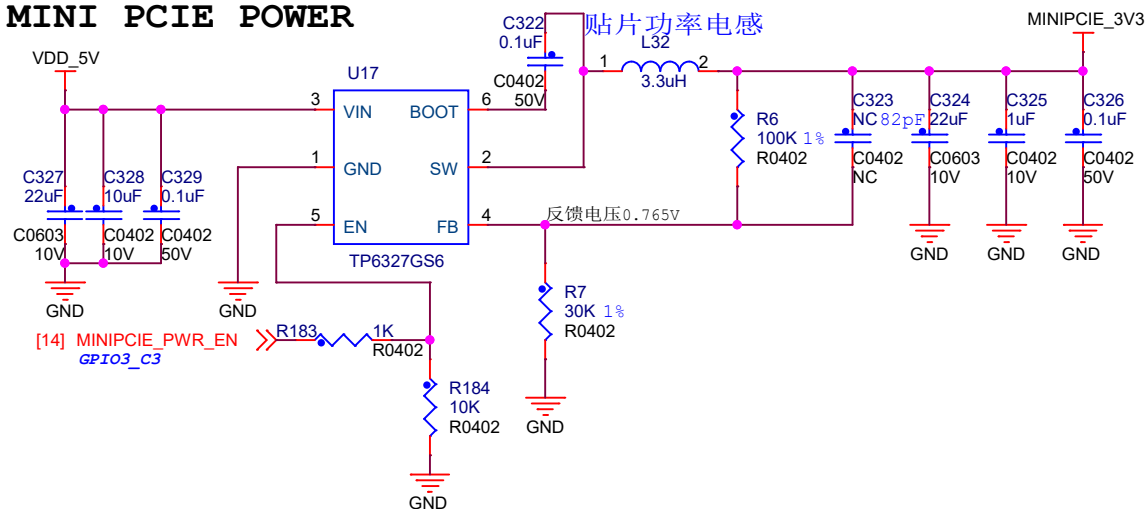
## IR 吸收峰



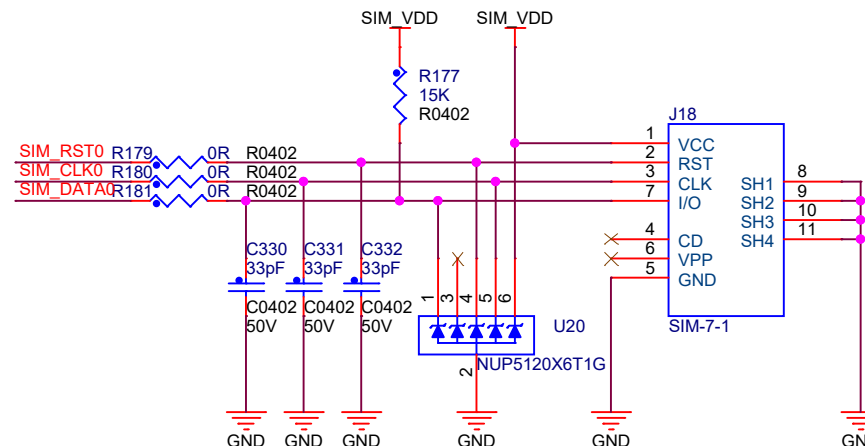
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Title			野火_EBF RK3568 LBC		
Size A3	Document Number M.2 PCIE3.0接口/IR接收器				Rev V1
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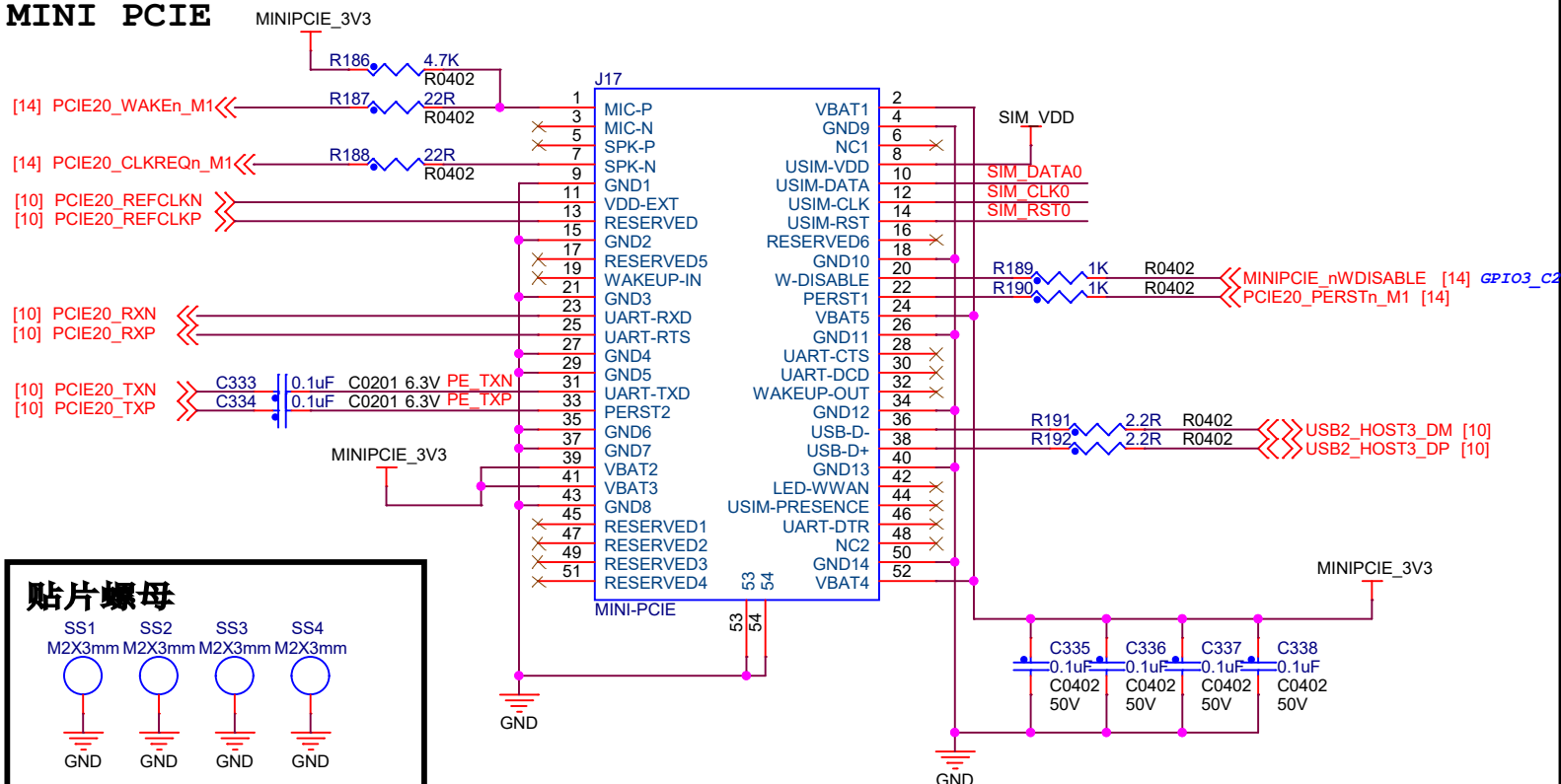
## MINI PCIE POWER



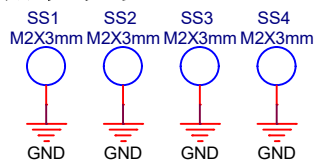
## SIM CARD



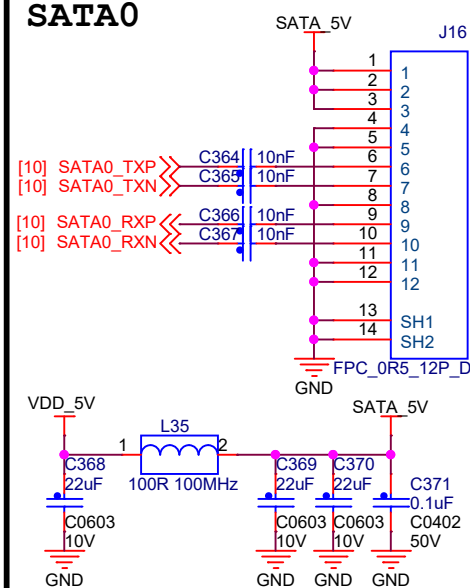
## MINI PCIE



### 贴片螺母



## SATA0

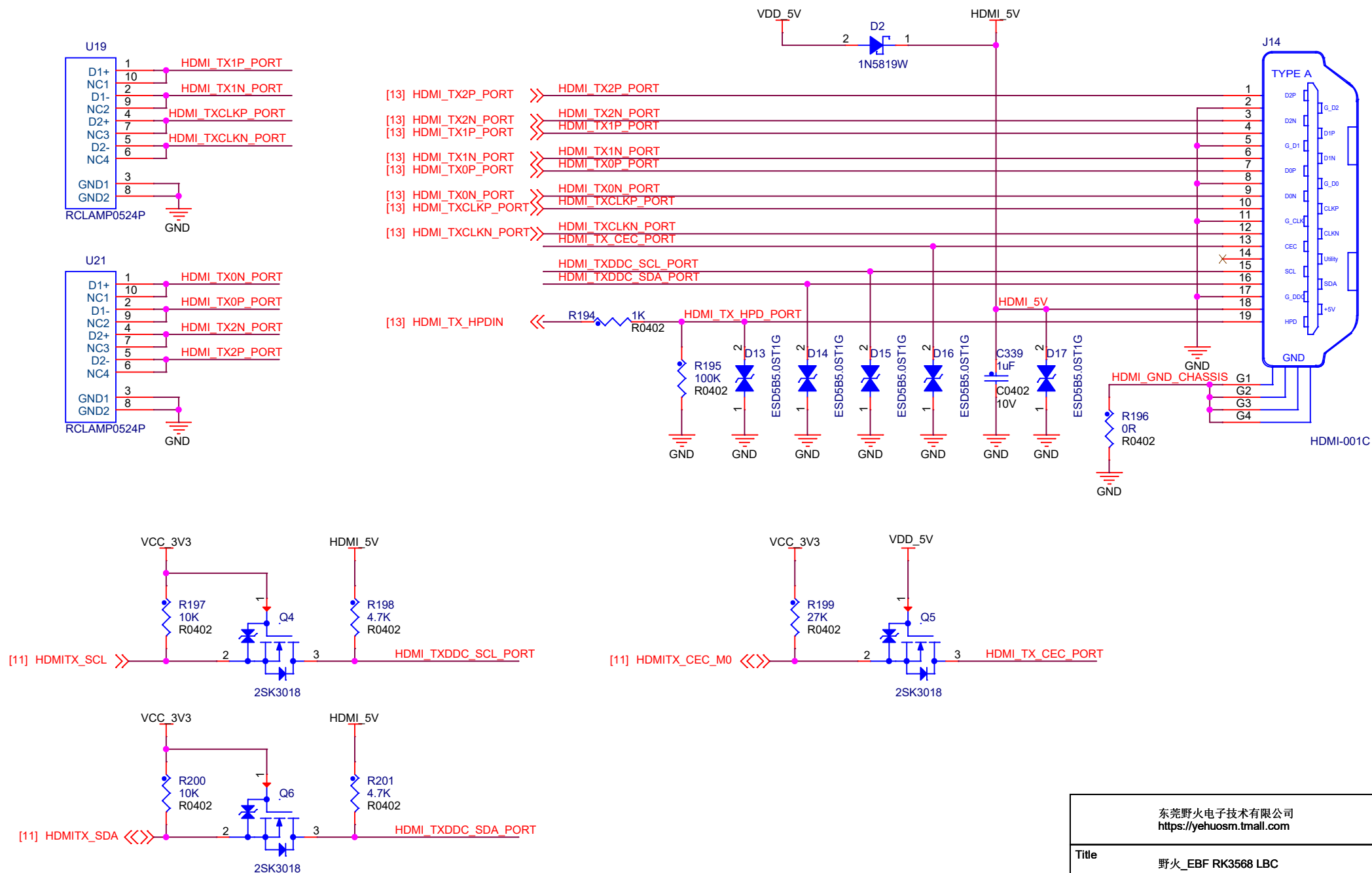


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## HDMI2.0接口



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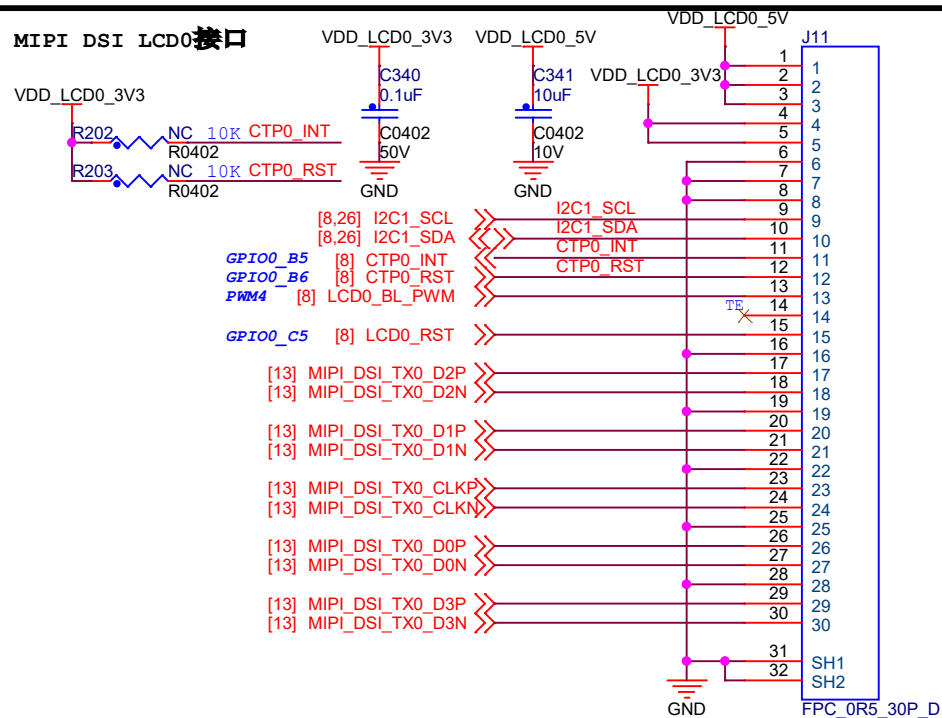
Title	野火_EBF RK3568 LBC
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Size A4	Document Number M.2 PCIE3.0接口	Rev V1.0
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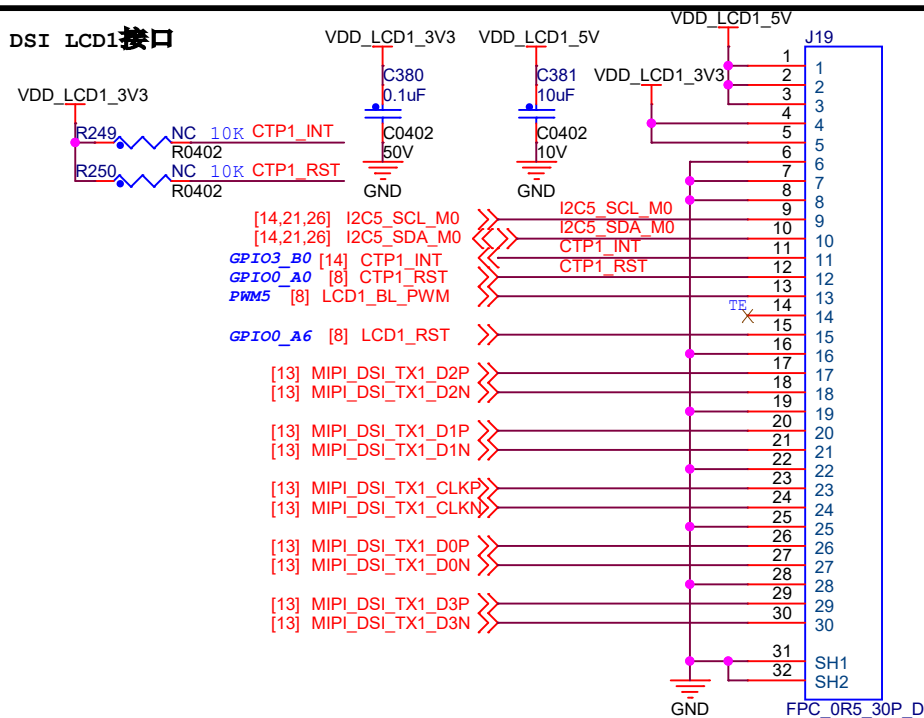
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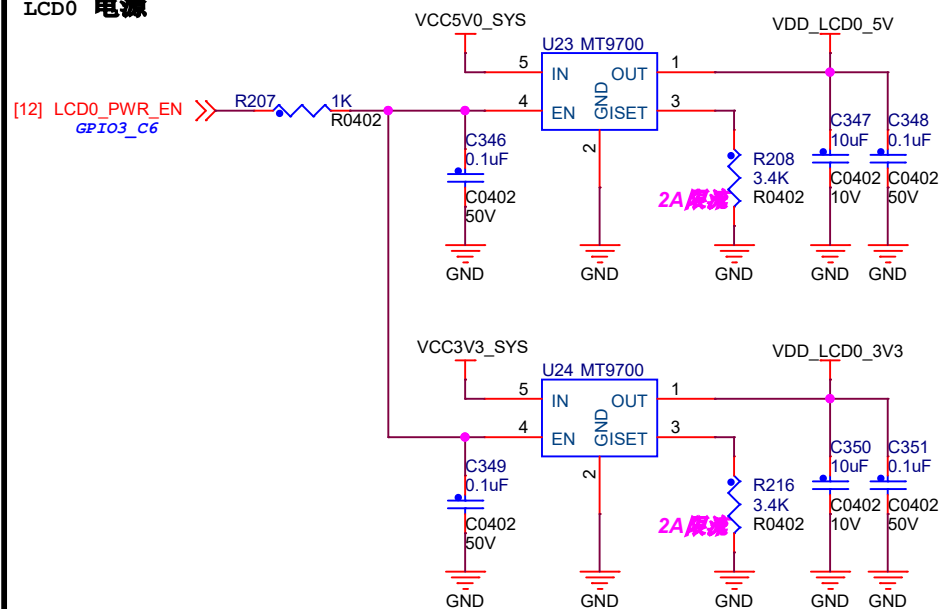
## MIPI DSI LCD0接口



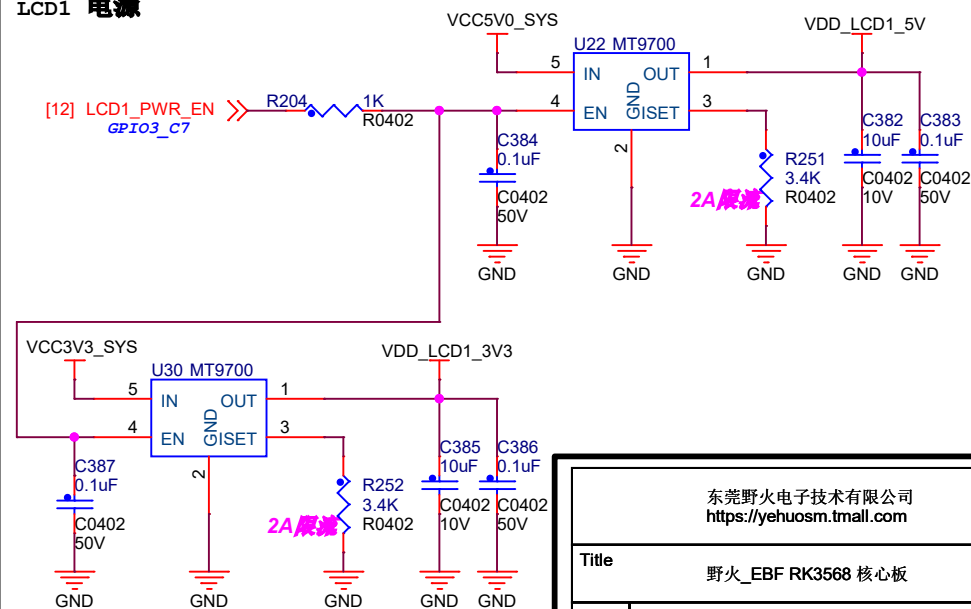
## MIPI DSI LCD1接口



## LCD0 电源



## LCD1 电源



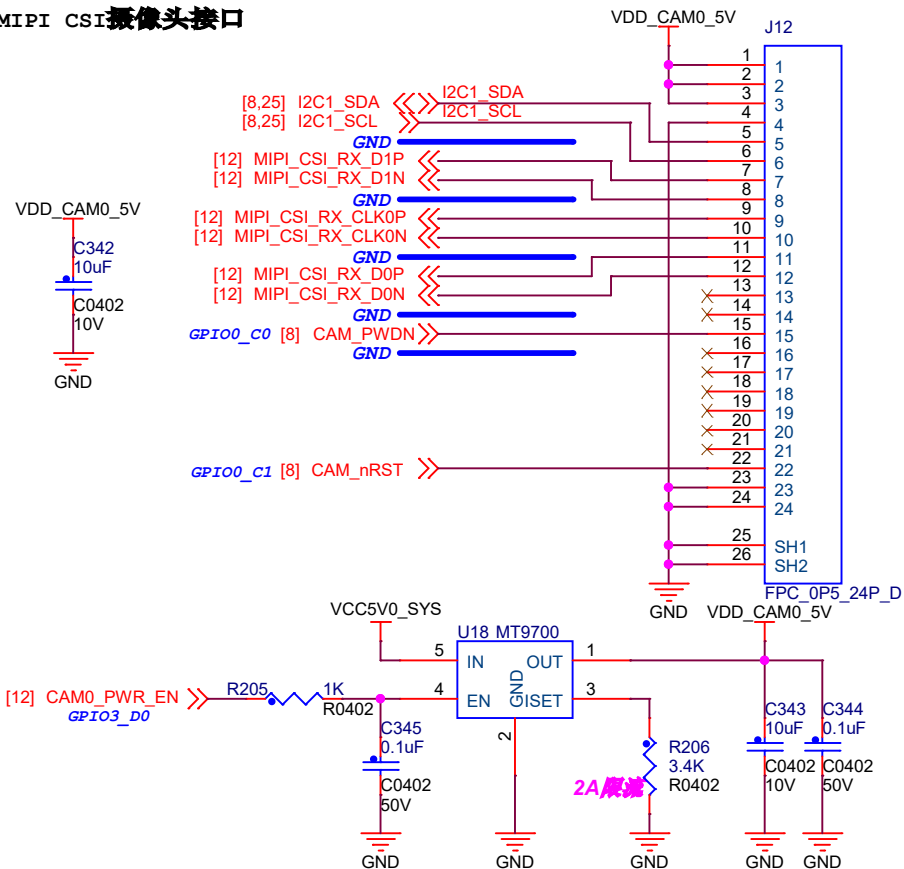
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Title 野火\_EBF RK3568 核心板

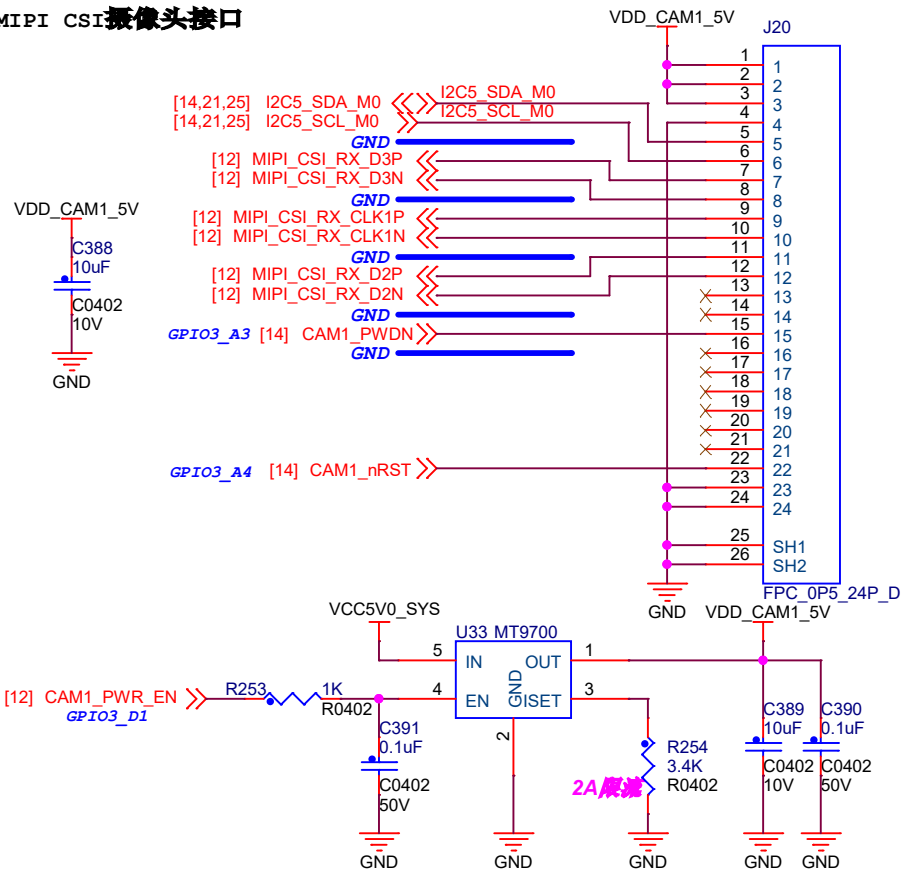
Size A4 Document Number M.2 PCIe3.0接口 Rev V1.0

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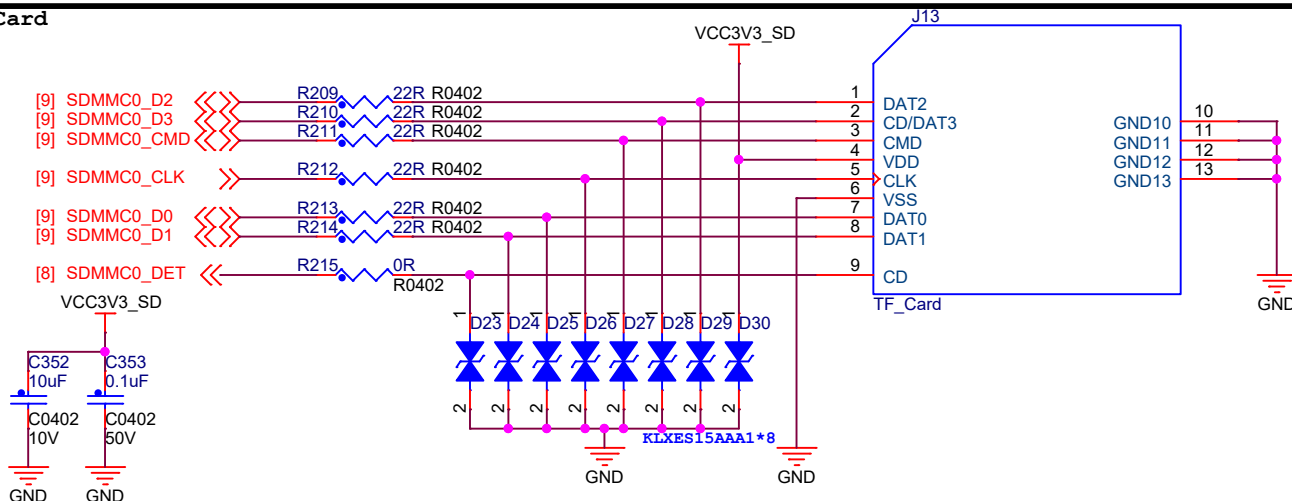
# MIPI CSI摄像头接口



# MIPI CSI摄像头接口



# SD Card



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