Questa Instance Coverage

Instance: /tb_fifo

Instance Path	/tb_fifo (summary.html?f=1&s=3&type=inst)
Design Unit	work.tb_fifo (summary.html?b=1&s=1&type=du)
Language	Verilog
Source File	tb_fifo.sv

Coverage Summary By Instance (86.21%)

Instance	Branches	Conditions	Expressions	Statements	
Search...	Search...	Search...	Search...	Search...	Sea
Total	87.09%	81.81%	100%	98.29%	
tb_fifo (summary.html?f=1...	77.77%	33.33%	-	97.84%	
dut (summary.html?f=1&s...	100%	100%	100%	100%	

Local Instance Coverage Details (65.61%)

Coverage Type	Bins	Hits	Misses	Coverage
Search...	Search...	Search...	Search...	Search...
Branches	18	14	4	77.77%
Conditions	3	1	2	33.33%
Statements	93	91	2	97.84%
Toggles	228	122	106	53.5%

Recursive Hierarchical Coverage Details (86.21%)

Coverage Type	Bins	Hits	Misses	Coverage
Search...	Search...	Search...	Search...	Search...
Branches	31	27	4	87.09%
Conditions	11	9	2	81.81%
Expressions	3	3	0	100%
Statements	117	115	2	98.29%
Toggles	498	318	180	63.85%