CSE 341
Fall 2015
Project #2

Due: Monday, November 30, 2015 at 11:59 PM

Extra Credit: 5 points extra credit will be received for submissions submitted before Monday, November 23, 2015 at 11:59 PM

Project Description

Your task is to implement a 16-bit ripple carry adder and a 16-bit carry lookahead adder. The carry lookahead adder should have 2-levels of carry lookahead. A functional (zero delay) simulation should be used to verify the circuits works properly and a nonzero gate delay model simulation should be used to evaluate performance. Structural (not behavioral) Verilog must be used.

Simulation & Writeup

A written report should be submitted which includes circuit diagrams of the both adders (down to the gate level), functional (zero delay) simulation results proving that the adders work properly, and unit gate delay simulation results which will allow you to analyze performance and gain a better understanding the effect of delay on processor design. The following checklist will help ensure that you have included all the required components with your writeup.

- Circuit diagrams of the both adders down to the gate level.
- Critical path & delay of both adders under the unit gate delay model.
- Gate cost of the both adders.
- Functional (zero delay) simulation results for the both adders proving the Verilog implementation of your circuits work properly. Multiple data sets should be used to prove this. There should be ten data sets spanning all 16-bits of the operands.
- Analysis (including specific examples) of the temporal dependence of the delay on the previous set of inputs applied to the ***ripple carry adder*** under the nonzero gate delay model. At least 5 specific examples simulations should be used to show this. The specific examples ***must*** be highlighted in your writeup.
- Analysis of the average delay across 5,000 randomly selected input patterns for both adders using the unit gate delay model. Specifically state how this average compares to the critical path delay. You should ***not*** include a list of the detailed simulation results for this portion, but rather a summary indicating the average delay across all 5,000 samples for each adder. In addition, include a small writeup on how you accomplished this. Setting up 5,000 simulation sets manually and manually studying the results is not the efficient way to do this.

Submission

Your *commented* Verilog code must be submitted online using the command ***submit_cse341 rca_unit_5000.v, cla_zero.v, cla_unit_5000.v, ALU_README***. ***rca_unit_5000.v*** and ***cla_unit_5000.v*** are the simulations used to obtain the average delay over 5,000 input patterns for the ripple carry adder and carry lookahead adder respecively. ***cla_zero.v*** is the functional simulation of the carry lookahead adder. ***ALU_README*** is a README file providing details about your submission that the grader may find helpful. The files you submit must contain the

complete simulation which was used to obtain the data for your writeup. The simulation should be well commented so that the results can be easily understood. The simulations will be run using *iverilog* when graded.