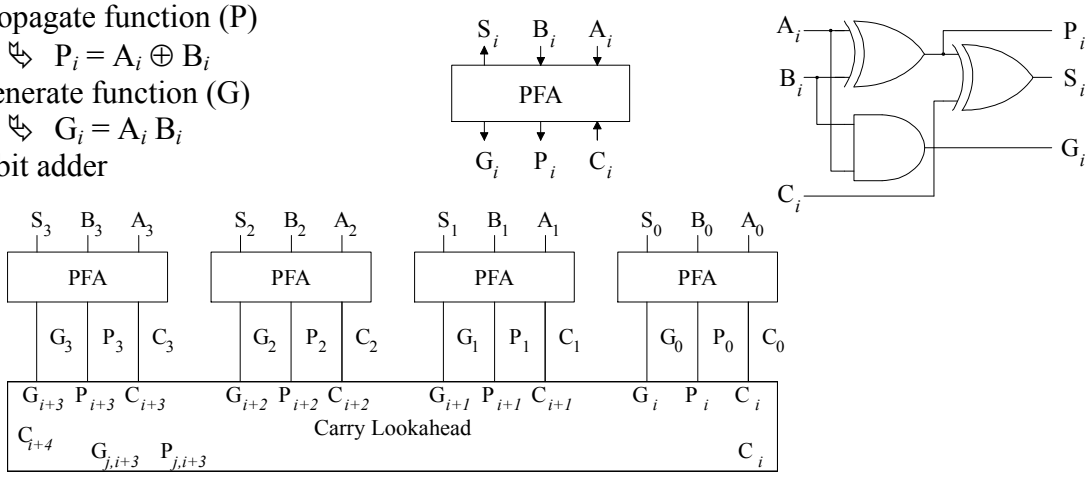
CSE 341

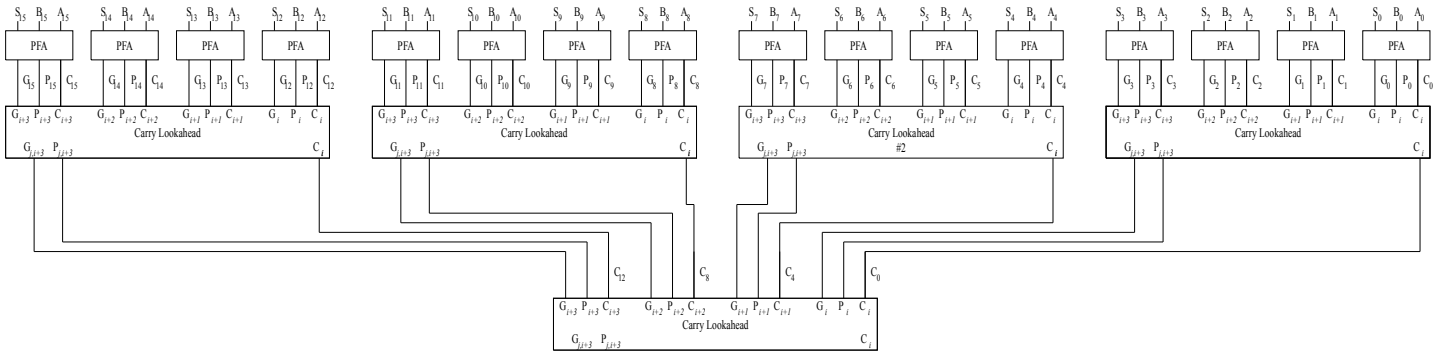
The Adder

- Carry Lookahead Adder
  - Significantly reduces delay over the ripple carry adder
  - Adder design separated into two parts
    - Partial full adder (PFA)
      - ✓ Does not contain carry propagation path
    - Carry lookahead unit
      - ✓ Contains carry propagation path
  - Propagate function (P)
    - $P_i = A_i \oplus B_i$
  - Generate function (G)
    - $G_i = A_i B_i$
  - 4-bit adder



    - Carries
      - ✓ $C_1 = P_0 C_0 + G_0$
      - ✓ $C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$
      - ✓ $C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$
      - ✓ $C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$
    - Group propagate & generates are for a group of four bits
      - ✓ Used to introduce another carry lookahead unit, as shown in the 16-bit carry lookahead adder
      - ✓ Group propagate
        - $P_{0\text{-}3} = P_0 P_1 P_2 P_3$
      - ✓ Group generate
        - $G_{0\text{-}3} = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$

☞ 16-bit adder



References

- M. Morris Mano and Charles R. Kime, *Logic and Computer Design Fundamentals*, Prentice Hall, Inc., 2000
- Victor P. Nelson, H. Troy Nagle, Bill D. Carroll, and J. David Irwin, *Digital Logic Circuit Analysis & Design*, Prentice-Hall, Inc., 1995
- Donald D. Givone, *Digital Principles and Design*, McGraw-Hill, 2003
- Wayne Wolf, *FPGA-Based System Design*, Pearson Education, Inc. (Prentice Hall), 2004