**Student Name/Last Name: David Akre**

**ECE506 HW1 (100pts)**

**Objective:**

Implement the structural design of the sorting algorithm and verify its functionality through both behavioral and post-synthesis simulations.

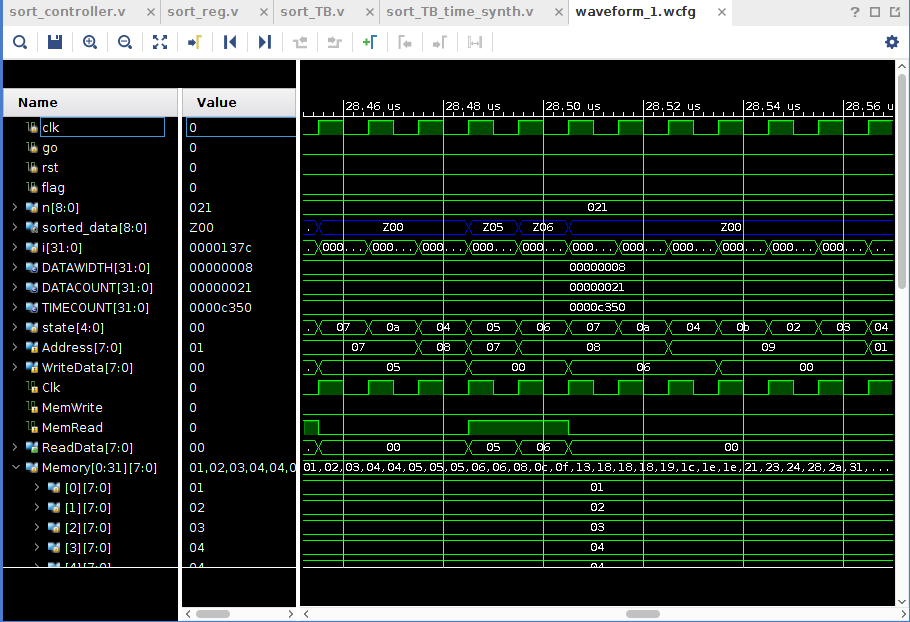
**Method:**

Implement the controller, datapath modules and integrate under the sort top module (sort\_top.v).

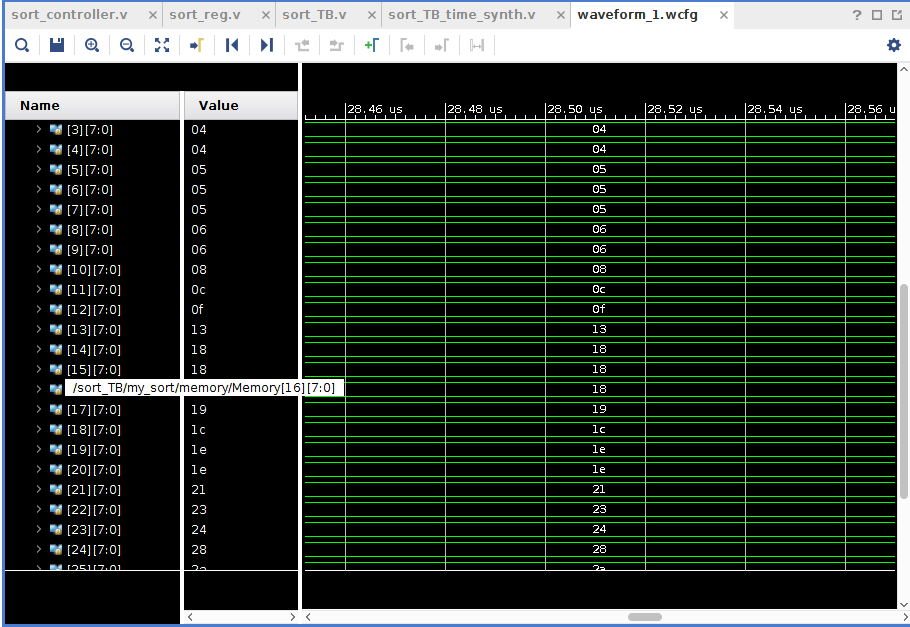
**Logistics:**

* Testbench along with the data memory modules are included.
* Assume that number of elements is 32 for this assignment but make sure that N value is an input from the testbench. I should be able to run your design with any size N by simply replacing your data memory with another.
* First conduct functional verification based on behavioral simulation only. Include your waveform displaying the sorted data here:

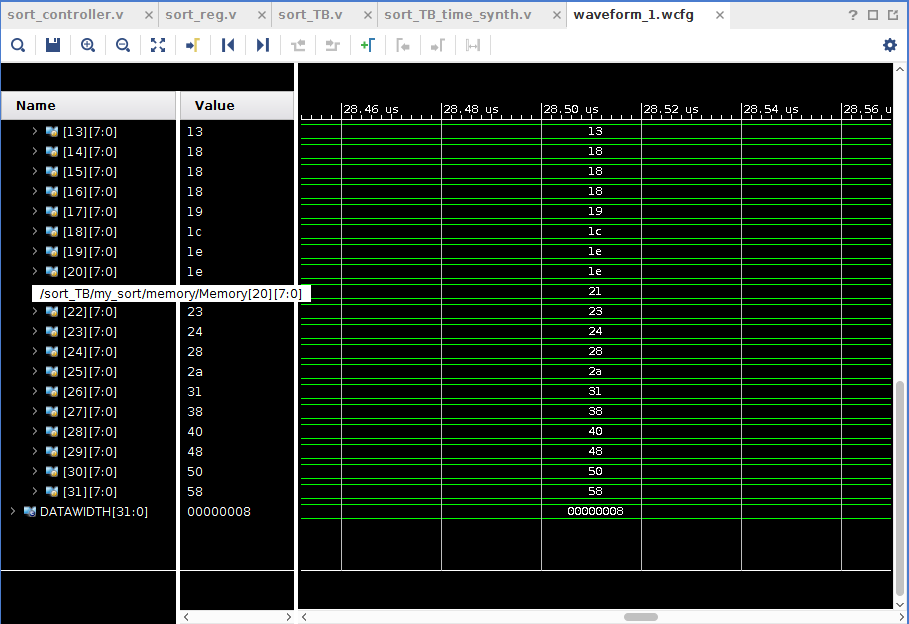
**WAVEFORM-1-1**

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**WAVEFORM-1-2**

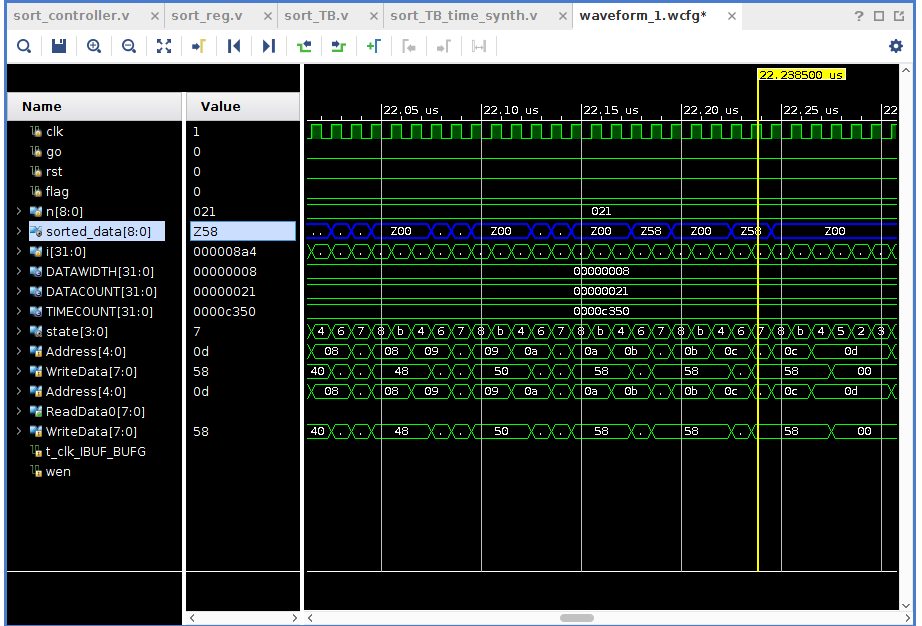
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**WAVEFORM-1-3**

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* Then conduct post-routing simulation and include your waveform displaying the sorted data here:

**WAVEFORM-2-1**

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**Submission:**

* Submit your verilog source files (.v only) including testbenche on D2L to the designated dropbox.
* Submit this file (ece506\_hw1.docx) in the same dropbox folder

**Grading**

* Individual submission
* Late submission (**20pts penalty** per day)
* Do not zip/tar and Do not submit as a folder. Submit all files individually. Submitting files in a folder or in compressed form (zip/tar). (**50pts penalty**)
* Design works in behavioral simulation but fails to synthesize (**maximum 50%**)
* Design works in behavioral simulation, synthesizes with warnings but post-routing simulation fails (**maximum 75%**)