Notes

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1 Processor

- No Pipelining
- No floating point
- Registers only, no memory
- Puts result of operation in the first operand
- 4 bit opcode for 13 insturctions
- 7 usable registers 1 PC register
- 128 words of instruction memory or 128 instructions
- Address registers are 3 bits: 000 for the PC or 001 for r1 so on and so forth
- Words are 16 bits
- All numbers are two's compliment

2 Instruction Set

- add
- addi
- shift left arithmetic
- shift left logical
- shift right
- or
- ori
- and
- andi
- negate
- jump zero
- unconditional jump
- load immediate
- move

3 R-Type Instructions

- 4 bit opcode
- 3 bits for operand 1
- 3 bits for operand 2

Instruction	description	opcode	parameters
add	Add two registers	0000	2 reg
and	And two registers	0001	2 reg
or	Or two registers	0010	2 reg
mov	Moves first register to second register	0011	2 reg

4 I-Type Instructions

- 4 bit opcode
- 3 bits for reg 1
- 9 bits for immedate value

Instruction	description	opcode	parameters
sll	shift left logical	0100	1 reg 1 immediate
sla	shift left arithmetic	0101	1 reg 1 immediate
sr	shift right arithmetic	0110	1 reg 1 immediate
neg	Negate 1 register	0111	1 reg
andi	Does the and operation on a register and an immedate	1000	1 reg 1 immediate
addi	Add an immediate value to a register	1001	1 reg 1 immediate
ori	Does the or operation on a register and an immedate	1010	1 reg 1 immediate
loadi	Loads an immedate value into a register	1011	1 reg 1 immedate

5 J-Type

- 4 bit opcode
- 3 bits for jump address
- 9 bits for immedate value

Instruction	description	opcode	parameters
j	Jump unconditionally	1100	immediate
jz	Jump to an offset if a register is zero	1101	1 reg 1 imm