SHRIDEVI INSTITUTE OF ENGINEERING & TECHNOLOGY

Computer Organization And Architecture (21CS34)

Presentation

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*Data-lines P7 through Po can be used for either input or output purposes.

*The DATAOUT register is connected to data-lines via 3-state drivers that are controlled by a DDR.

*The processor can write any 8-bit pattern into DDR. (DDR→ Data Direction Register).

* If DDR=1,
Then, data-line acts as an output-line;
Otherwise, data-line acts as an input-line.

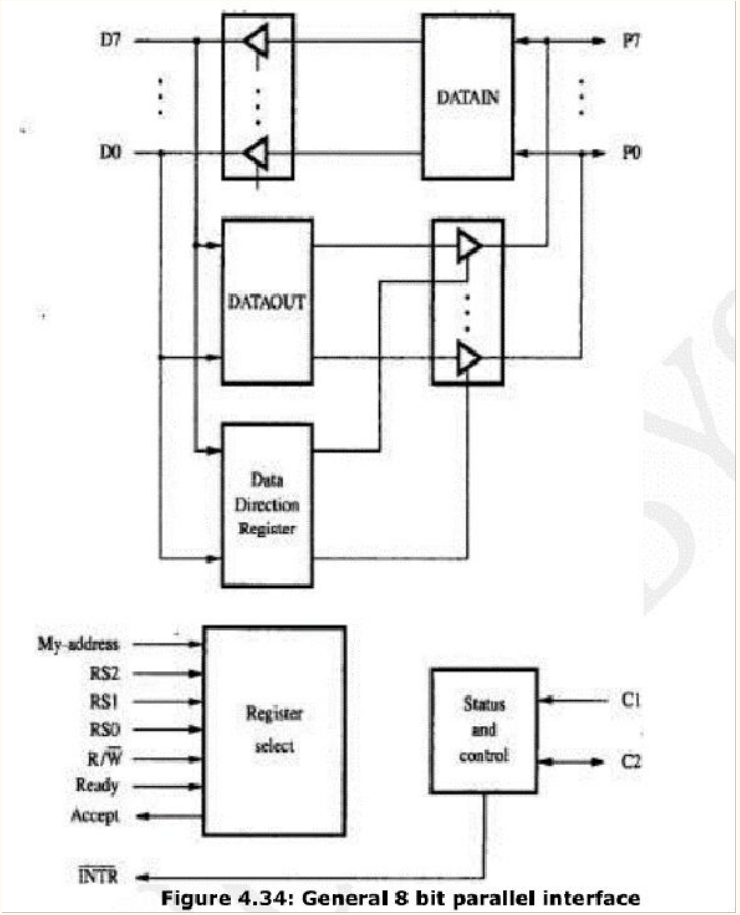


Figure 4.34: General 8 bit parallel interface

*Two lines, C1 and C2 are used to control the interaction between interface-circuit and I/O device.

*Two lines, C1 and C2 are also programmable.

*The Ready and Accept lines are the handshake control lines on the processor-bus side.

*Hence, the Ready and Accept lines can be connected to Master-ready and Slave-ready.

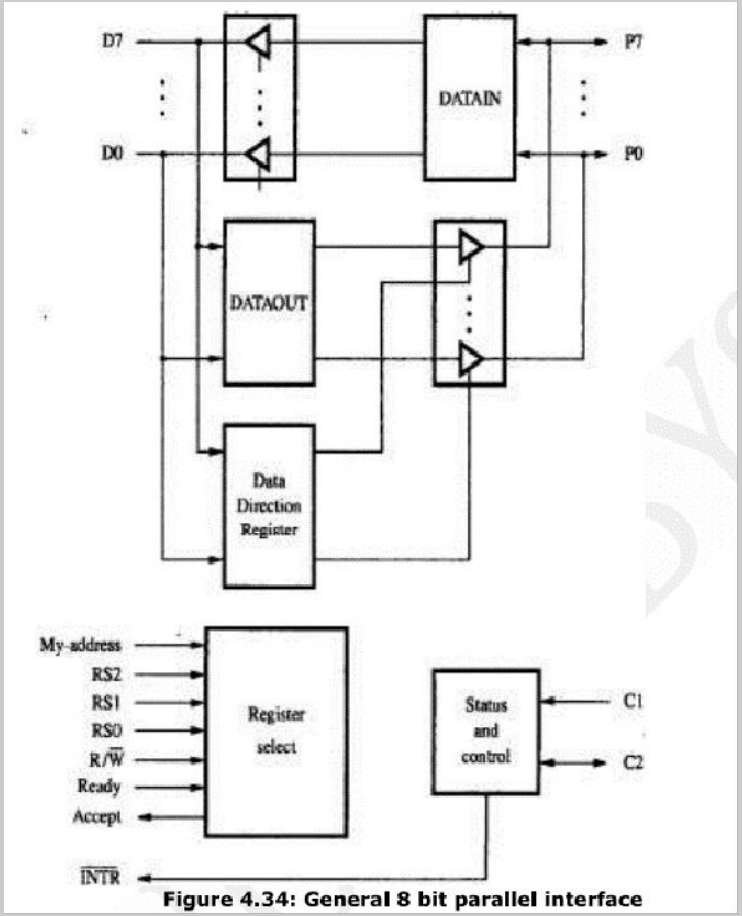


Figure 4.34: General 8 bit parallel interface

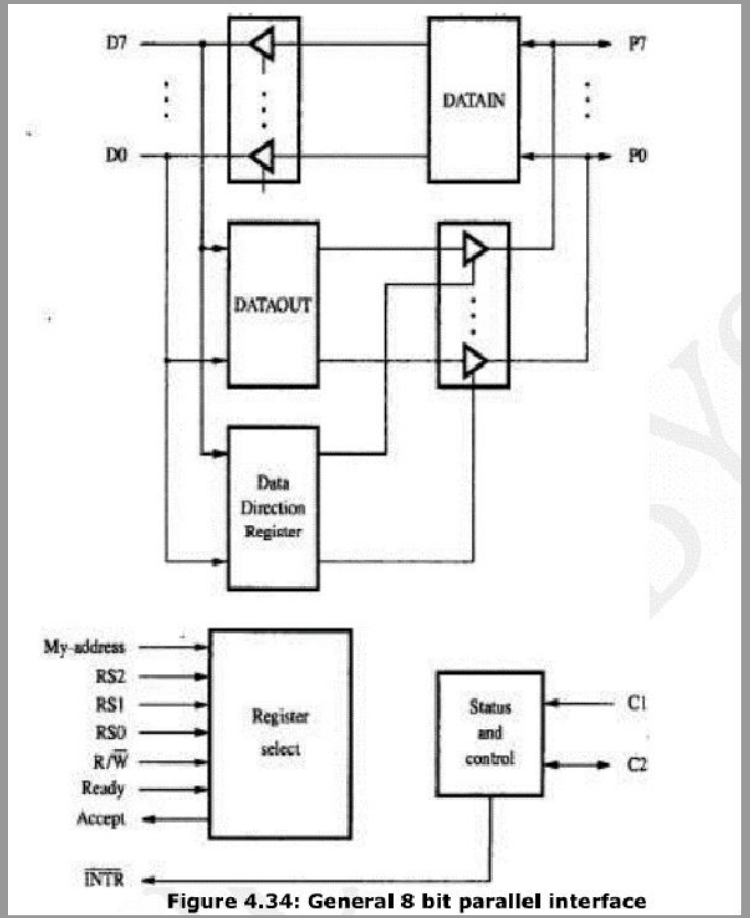
* The input signal My-address should be connected to the output of an address-decoder. The address-decoder recognizes the address assigned to the interface.

* There are 3 register select lines: RS0-RS2.

Three register select lines allows up to eight registers in the interface.

* An interrupt-request INTR is also provided.

INTR should be connected to the interrupt-request line on the computer-bus.



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THANK YOU