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A multiple antenna wireless testbed for the validation of DoA estimation algorithms

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ABSTRACT

In this paper, a wireless testbed with a multiple antenna receiver is described. It comprises a rotating four-element antenna array connected to a quad radio frequency (RF) front-end, and a channel acquisition board equipped with a field programmable gate array (FPGA). The algorithms can be implemented directly on the FPGA, but they can also be tested via simulation, e.g., with Matlab, since the acquired data can be transferred from the board memory to a personal computer (PC). Moreover, the algorithm implementation on the FPGA can be done by exploiting the System Generator for DSP Xilinx tool that allows the algorithm synthesis from a Simulink block diagram. These features make the testbed useful for rapid prototyping. In particular, the presence of the rotating antenna array enables the analysis of direction of arrival (DoA) estimation techniques. We report the main results from the experimental measures conducted to characterize the hardware non idealities. We then describe a DoA estimation algorithm that has been used to compare real and simulated results. It is shown that the results are in good agreement with the simulations, also when the effect of non isotropic antenna gains and/or phase noise originated from non co-phased RF front-ends becomes considerable.

1. Introduction

Multiple antenna systems are of high interest because of their capability of offering higher throughput and reliability [1]. Furthermore, the presence of an antenna array at the receiver can be used to exploit the directional properties of the channel in order to provide spatial diversity, beamforming capabilities, and/or to implement direction of arrival (DoA) estimation based positioning systems [2]. All these applications have been investigated theoretically and via simulations in the past, showing their benefits under ideal conditions. However, hardware platforms do not always exhibit such behavior. In fact, there are many implementation non idealities that can affect the system performance. To this end, hardware platforms and testbeds are essential in validating algorithms.

Wireless testbeds and prototyping play an important role in both academia and industry. They give greater insight into wireless system design, and they provide hands-on experiences to researchers [3]. Furthermore, it is important to have reliable information about future designs and developments, especially in a very competitive market like the telecommunication one [4].

As explained in [5], hardware implementations can be divided into three groups: demonstrators, that serve to show an existing technology to customers; testbeds, that are generally used for research; prototypes that are the initial realization of a research idea. In this paper we concentrate in testbeds. According to the definition in [5], a testbed allows real-time experimentation, even if signal processing is performed in part off-line.

Various testbeds have been built for testing new wireless technologies, in particular for multiple-input multiple-output (MIMO) data communication schemes [6]. They are complete solutions, e.g., available from Lyrtech (now Nutaq), Signalion or other vendors, or they are assembled with commercial off-the-shelf components. Several classifications have been suggested, according to different selection criteria. One of these can be the final purpose, i.e., if the testbed is developed to study a specific standard [7] or for a more general purpose [8]. Another classification criteria can be based on the technology used, e.g., a software-defined testbed [9], a digital signal processor (DSP) based testbed [10], an FPGA-based testbed [11], etc. Alternatively, flexibility, development time, throughput or cost, and the educational purposes are other possible classification criteria.

1.1. Previous work

We now describe some testbed examples that can be found in the literature. In [7], a 4×4 FPGA-based wireless testbed for long

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term evolution (LTE) cellular applications was assembled by using two off-the-shelf main boards. They are equipped with an Altera Stratix II FPGA. These main boards are capable of controlling up to 4 RF front-ends each. The RF front-ends are based on the integrated circuit (IC) MAX2829 from Maxim that is herein set up to work in the frequency range from 2.4 to 2.5 GHz and allows for the use of up to 40 MHz of bandwidth. Furthermore, this testbed can store up to 15.7 ms using 12 bit I&Q data, so it is adequate for testing short burst transmission.

An example of a testbed designed for a more general purpose can instead be found in [8]. It was developed to examine MIMO algorithms and channel models, in a maximum of 20 MHz bandwidth around the 2.45 GHz carrier frequency. A particular feature of this testbed is the possibility to variate the antenna distances, allowing the study of channel capacity as a function of the spatial correlation [12]. To the best of our knowledge, direction of arrival experiments, which is our target scenario, have not been conducted with this testbed.

A low cost 4×4 software-defined system testbed was presented in [13]. Herein, the MAX2829 evaluation kit from Maxim is incorporated in the testbed design. The digital back-end consists of the ICS-660B digital-to-analog converter (DAC) and the ICS-645B analog-to-digital converter (ADC). They are installed in the PCI slots of a control PC and exploit this bus to transfer data into the Matlab environment for off-line signal processing. Since the RF front-end is the same as in [7], this testbed has the same bandwidth and frequency constraints. Differently from the other platforms, in [13] the testbed was used to conduct DoA experiments. In this respect, a two element uniform linear array (ULA) of patch antennas was used, and few indoor measurements were conducted. In this case, the calibration of the phase offsets between the receivers was addressed by using an RF switch board that injects a common RF signal to both the receivers. This is one of the simplest calibration techniques, as explained in [14]. Nonetheless, the lack of a rotating antenna array yields these kind of experiments cumbersome and non systematic.

Other examples of MIMO wireless testbed can be found in [15–18]. The testbed in [15] was used for MIMO channel measurements. Wireless LAN applications were considered in [16]. The solution described in [17] comprises a 16×16 MIMO testbed for multiuser MIMO downlink transmission. The testbed was used to implement an adaptive modulation scheme employing a bit interleaver in the space and frequency domain. A system comprising one base station and two mobile stations was implemented in [18] using software defined radio platforms.

1.2. Contributions

Motivated by the above considerations, we have assembled our own testbed that we refer to as *WiPLi Lab Wireless Testbed*, and that we describe in this work. It resembles the above mentioned examples, and in particular [8,13] where a Matlab interface improves flexibility and allows a multitude of experiments with different constraints. Our testbed is equipped with 4 antennas and it can be exploited to implement novel MIMO algorithms or beamforming techniques but, in our context and differently from the work cited above, it has been used to compare simulation and experimental DoA estimation results for wireless localization purposes. Since the performance of the DoA estimator is affected by the hardware impairments, we have firstly used the testbed to identify, characterize and model them. A measurement campaign was carried out to characterize some hardware parameters (gain and bandwidth), and the main hardware non idealities, i.e., phase noise originating from non co-phased RF front-ends, and also the radiation patterns of the antennas. Then, a simple DoA estimation algorithm based on a correlation between successive antennas has been implemented. Such an implementation has allowed the comparison between the performance obtained from simulations and that from the experimental analysis.

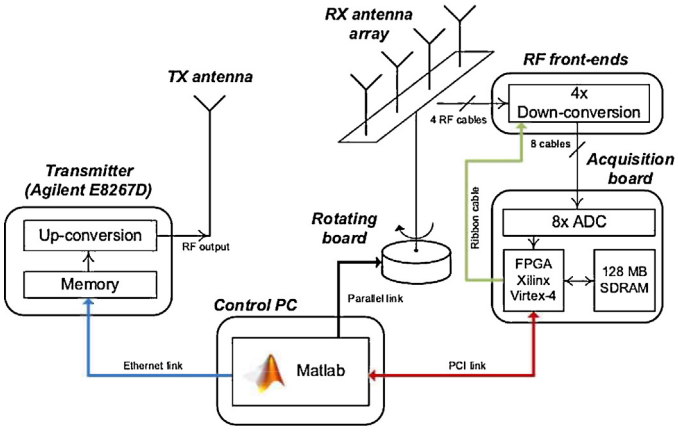


Fig. 1. WiPLi Lab wireless testbed.

In more detail, the paper is organized as follows. In Section 2, the testbed description is provided, with particular emphasis to the experimental characterization of some receiver parameters such as gains, bandwidth, and phase noise. Several considerations about the maximum achievable signal-to-noise ratio (SNR) are described in Section 3. In Section 4, the DoA estimation algorithm is firstly described, and the experimental results are successively reported. Finally, the conclusions follow.

2. Testbed description

A block diagram of the WiPLi Lab wireless testbed is depicted in Fig. 1. As it can be observed, it comprises several main blocks, listed as follows.

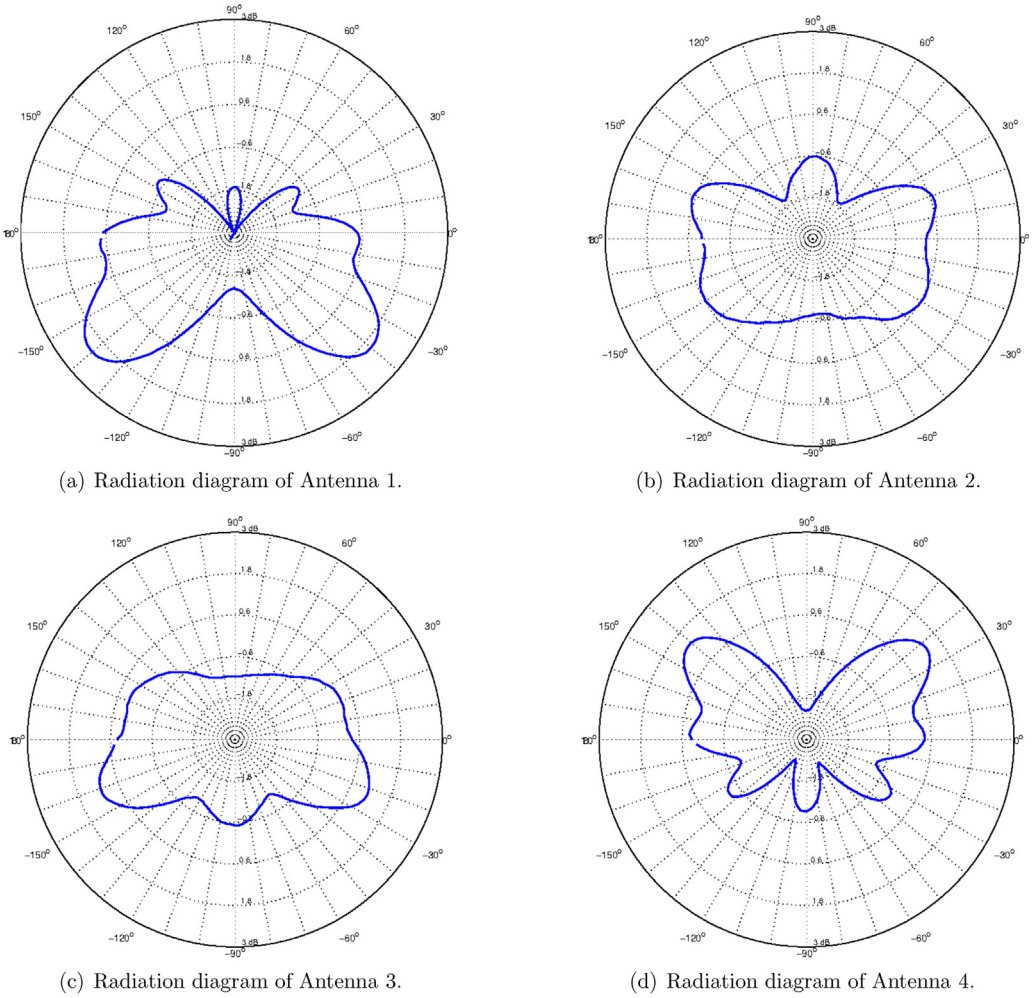
- A vector signal generator, Agilent *E*8267*D*, used as the transmitter;
- a rotating board with a four-element antenna array;
- four direct-conversion RF front-ends;
- an eight channel acquisition board equipped with a Xilinx Virtex 4 FPGA and a 128 MB of memory;
- a control PC for the devices management and the post-processing.

All these devices will be separately analyzed in order to highlight the main features.

2.1. Transmitter

The Agilent E8267D is a vector signal generator [19] that can work in the frequency range from 250 kHz to 20 GHz. It is able to generate a wide range of modulated signals, both analog (AM, FM, PM) and digital (ASK, FSK, PSK, QAM). Furthermore, it can be used to create multi-tone signals and also to generate arbitrary waveforms. All these signals are generated with an internal baseband (BB) generator that has a maximum bandwidth of 40 MHz. The BB signals can be up-converted and amplified up to about 16 dBm of power.

In the WiPLi Lab testbed, this device is used as the transmitter. It is connected via an Ethernet link to the control PC, from which its set up can be properly controlled using an application programming interface (API) running in the Matlab environment. Moreover, a specific waveform can be uploaded, if needed. The memory of the instrument accepts waveforms that occupy up to a maximum of 8 mega samples (MS) that correspond to a trace of about 200 ms.



(a) Radiation diagram of Antenna 1.

(b) Radiation diagram of Antenna 2.

(c) Radiation diagram of Antenna 3.

(d) Radiation diagram of Antenna 4.

Fig. 2. Radiation patterns of the array elements. (a) Radiation diagram of Antenna 1. (b) Radiation diagram of Antenna 2. (c) Radiation diagram of Antenna 3. (d) Radiation diagram of Antenna 4.

Finally, an external clock input and an external trigger input are available.

The RF output of the signal generator is connected to a dual band microstrip antenna tuned to both the 2.4 GHz and the 5.8 GHz bands.

2.2. Rotating antenna array and RF front-ends

The receiver is equipped with a four-element antenna array, mounted on a rotating board. This can be controlled via the parallel port of the control PC, and it has a 2.5 degree of angular resolution.

The antenna array is a linearly equispaced array with inter-element distance $d = 6.2$ cm, i.e., $d = \lambda/2$ when the carrier frequency is $f_c = 2.412$ GHz. This array configuration has been chosen since our target application is the DoA estimation. The elements of the array are four $\lambda/4$ dipole antennas with a common ground plane, printed on a glass epoxy (FR-4) substrate. The radiation pattern is reported in Fig. 2. In principle, other antenna configurations can be deployed.

The antennas of the array are connected to the inputs of the RF multiple antenna front-end, shown in Fig. 3. It is a Comlab quad dual-band RF transceiver, that we use in the reception mode. It has four direct-conversion receiver based on the IC MAX2829 [20]. The receivers can be used both in the 2.4 and 5.8 GHz bands. However, for what the DoA estimation experiments concern, they are used only in the 2.4 GHz band since the antenna array is $\lambda/2$-spaced at this frequency.

All the front-end parameters are controlled through API functions. In particular, the main analog parameters are the gain and the bandwidth. In Fig. 4 we show the gain measurement as a function of the gain setting and the low noise amplifier (LNA) gain mode. It can be observed that there are three LNA gain modes: low, medium, and high gain that give 3, 17 and 33 dB of gain, respectively. Furthermore, the gain setting parameter controls the voltage gain amplifier (VGA) amplification, with a step of 2 dB. It should be noted that the gain curves in Fig. 4 of the different channels practically overlap for both the I&Q paths. With respect to the I&Q gain imbalance, we have found a maximum value of 0.5 dB.

In Fig. 5 we report the first channel frequency response for the I path, as function of the bandwidth setting. We have observed good correspondence with the main bandwidth setting, that can be BW = {7.5, 9.5, 14, 18} MHz, and the measured results. In the

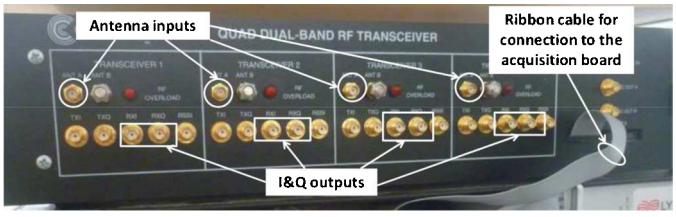


Fig. 3. RF front-ends of the WiPLi Lab testbed.

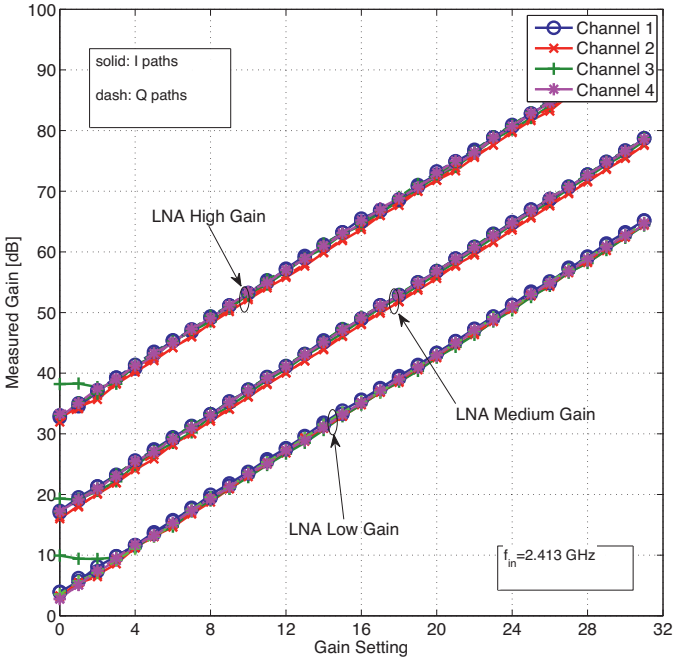


Fig. 4. RF gain measurement as a function of the gain setting and the LNA gain mode, measured with a single tone signal at 2.413 GHz.

figure, we also report the frequency response of the front-end when the bandwidth is set at the 90% and at the 110% (dash and dash-dot curves, respectively). Even in these cases we have found good agreement between the theoretical and the experimental results. Finally, we have observed a similar behaviour for the Q path of the first channel, as well as for the I&Q paths of the other front-ends.

For what the DoA estimation concerns, it should be noted that the four ICs of the receivers internally generate their own RF local oscillator (LO) signal. For this reason, this testbed does not have co-phased RF LOs, and it needs to be calibrated. A calibration method

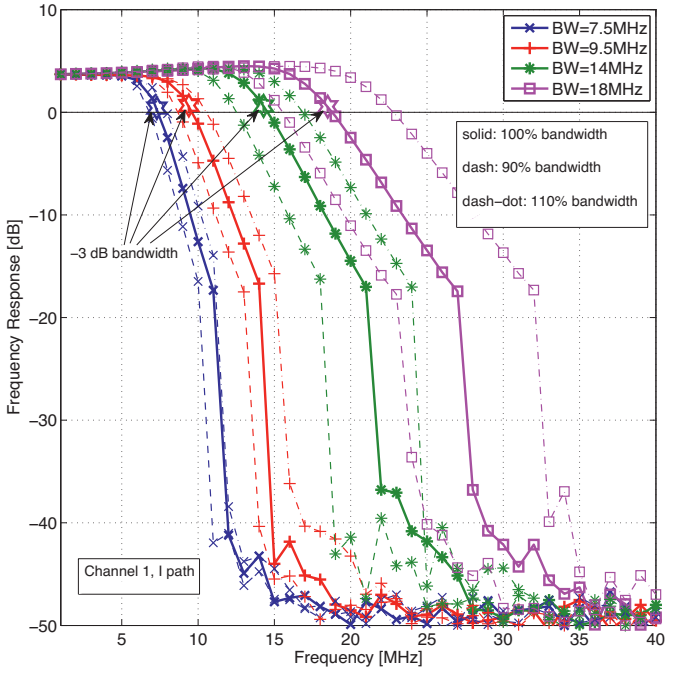


Fig. 5. First channel frequency response measurement for the I path as function of the bandwidth setting, with low gain mode.

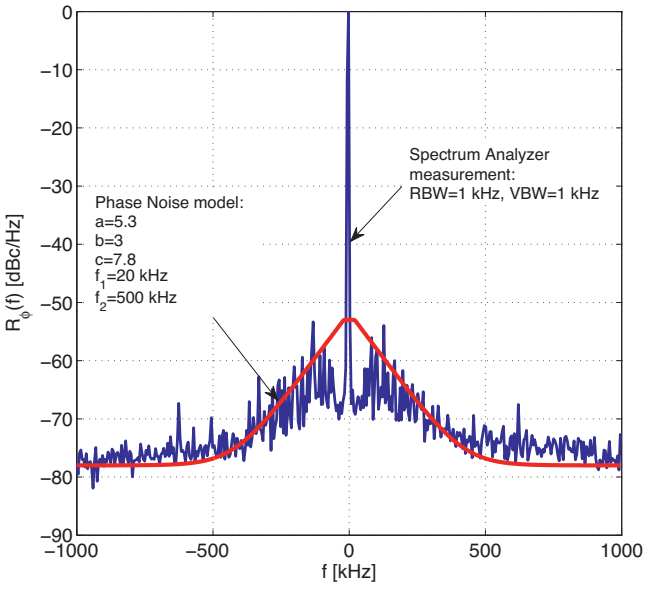


Fig. 6. Phase noise spectrum measurement and its derived model.

is described in [13]. Furthermore, we have observed that the LO signals have different carrier frequency offsets, even if we have shown in [21] that the observed quantities don't affect the performance. Also, different phase noise processes among the channels further impair the LOs. Temporally but not spatially correlated phase noise samples have been measured, and we have observed that they follow a Gaussian distribution, with zero mean and standard deviation 1.57°. As described in [21], the parametric approach in [22] has been used to describe the phase noise power spectrum (in particular, we have fitted the model with the following parameters: $a = 5.3$, $b = 3$, $c = 7.8$, $f_1 = 20$ kHz, $f_2 = 500$ kHz). In Fig. 6 we report the measured phase noise power spectrum with the derived model for the I path of the channel 1.

Finally, it is well known that direct-conversion receivers, that are very attractive due to their simplicity and the reduced costs, have the drawback of the DC offset. This problem appears also in our testbed. However, preliminary to each experimental test, the DC offset is estimated in order to remove it later digitally. This is possible since the DC offset remains constant over a long period of time.

2.3. Acquisition board

The acquisition board is a Lyrtech VHS-ADC [23], shown in Fig. 7. It is an eight channel acquisition board that allows the acquisition of all the I&Q outputs of the four direct-conversion receivers, with sampling frequency from 32 to 104 MHz. The analog to digital converters (ADCs) have 14 bit of resolution, 2.2 V_{pp} of dynamic range, and they can be controlled by using an external clock and/or an external trigger.

2.3.1. Maximum write speed constraint

The acquisition board is equipped with a Xilinx Virtex-4 XC4VLX160 FPGA, and two SDRAM banks each with 64 MB of memory. Data is stored with 16 bit precision, so the capacity of the memory allows for recording up to 64 MS. The limited write speed of the memory introduces a constraint in the acquisition rate. In fact, in order to correctly record the data samples, the maximum write rate of the memory, R_{mem} that corresponds to 225 MS/s, must be larger than the total data rate, $R_{data} = F_s \times N_{ch}$, where F_s is the sampling frequency, and N_{ch} is the number of channels. This brings to a maximum sampling frequency of 26 MHz when the whole

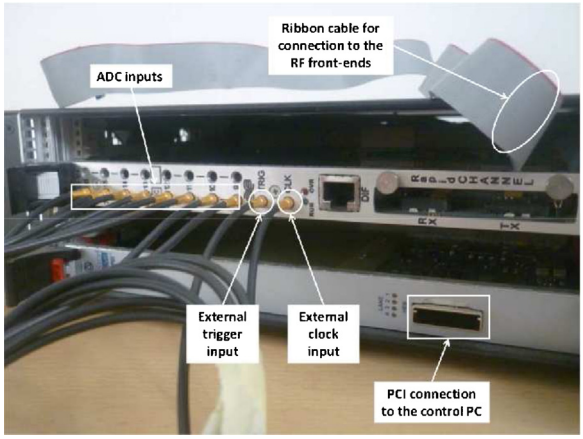


Fig. 7. Lyrtech VHS-ADC acquisition board.

antenna array is used. Obviously, this limits the front-end bandwidth.

It should be noted that the API function that allows for acquiring the data samples, provided by Lyrtech, uses a fixed clock at 104 MHz. Hence, if we want to modify the data rate we have to downsample the data by a factor that is a multiple of two, i.e., 52 MHz, 26 MHz, etc. Alternatively, if a different sampling frequency is required, an external clock can be used.

After having stored the data samples, a PCI bus is used to transfer them to the control PC. This transfers the data for post-processing into the Matlab environment.

2.3.2. Rapid prototyping with System Generator for DSP

Since data must be written into the acquisition board memory before being available for the off-line post-processing, a minimum verilog hardware description language (VHDL) project has to be preliminary developed in order to instantiate at least the ADC and the memory interfaces. This bitstream can be developed directly in VHDL code. Alternatively, it can also be synthesized by using a Xilinx tool, the *System Generator for DSP*, that allows for developing a project in the Simulink environment. In this way, it is possible to develop a specific application at a system block level by using the block libraries provided by Xilinx. In fact, portions of VHDL code are synthesized when a specific block, e.g., the ADC interface, or a complex multiplier, etc., is included into the project.

It should be noted that, if we develop the complete receiver algorithm into the FPGA, the execution will be real-time. However, even if the System Generator for DSP is an useful tool for rapid prototyping, the development of an application takes time. As explained before, we can use the acquisition board only to record the ADC samples and to transfer them into the Matlab environment. To do so, a System Generator for DSP project has to be developed, and it is shown in Fig. 8.

As it can be observed, this design includes an eight channel ADC block, 8 downsample blocks, and a memory block. The sampled data is acquired at the maximum sampling rate, i.e., 104 MHz, and it is downsampled by a factor of four. Finally, data is recorded into the memory. It should be noted that the effective total data rate is R_{data} = 208 MS/s, so the memory write constraint is respected.

On the left side of Fig. 8, other blocks are depicted. They are used to set the FPGA parameters (FPGA model, clock frequency, etc.). In particular, the *RFFE Control* block instantiates the interfaces that allow us to change the RF front-end parameters.

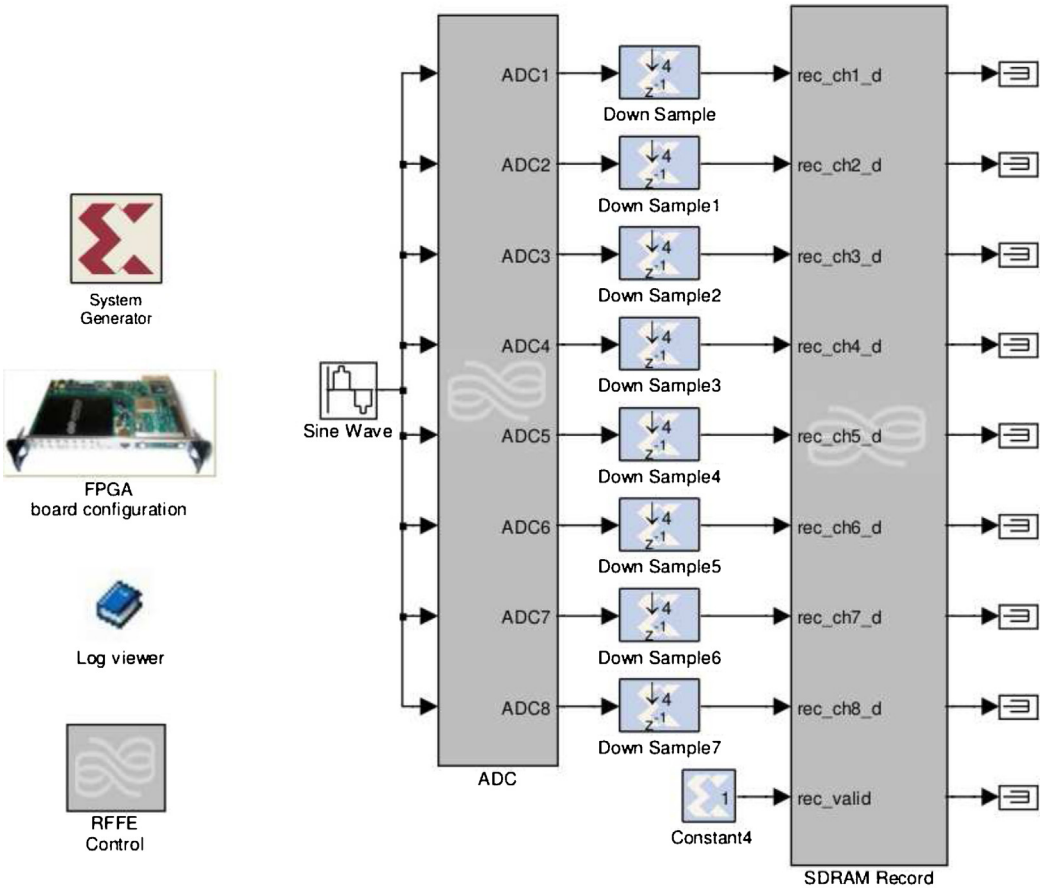


Fig. 8. System Generator for DSP/Simulink design for the off-line processing.

2.4. Control PC

The control PC manages all the system devices (transmitter, receiver, antenna rotating board) through the Matlab environment. For instance, data to be transmitted can be transferred from the PC to the transmitter, the angle of the rotation board can be set, as well as, the received samples can be downloaded into the PC.

3. Maximum achievable SNR

In this section we analyze the performance of the WiPLi Lab wireless testbed in terms of achievable SNR. The achievable SNR is an important performance figure that allows the comparison of results obtained by the hardware platform with those obtained via simulations.

If we assume a system model as

$$y(nT) = x(nT) + w(nT), \quad n \in \{0, \ldots, N-1\}, \tag{1}$$

where $y(nT)$ are the complex received samples, $x(nT)$ are the signal of interest samples, $w(nT)$ are the noise samples, and N is the total number of acquired samples, the SNR can be defined as

$$\text{SNR} = \frac{M_x}{M_w}, \tag{2}$$

where $M_x = E\{|x(nT)|^2\}$ is the statistical signal power, while $M_w = E\{|w(nT)|^2\}$ is the statistical noise power, and $E\{.\}$ denotes expectation. It is worth nothing that $x(nT)$ and $w(nT)$ are the quantized voltages of the signal of interest and of the noise, respectively. Since the ADC dynamic is limited to 2.2 V_{pp}, also the signal power (and the noise power) is limited. In this respect, we can define the peak-to-average power ratio (PAPR) [24] as

$$\text{PAPR} = \frac{\max |x(nT)|^2}{M_x}. \tag{3}$$

This parameter relates the signal power M_x to the signal dynamics. In fact, it is easy to prove that $\max |x(nT)|^2 = x_{pp}^2/2$, where x_{pp} is the maximum peak-to-peak signal amplitude, obtaining

$$\text{SNR} = \frac{x_{pp}^2}{2 \cdot \text{PAPR} \cdot M_w}. \tag{4}$$

In this way, once we know the signal waveform (that gives the PAPR), we can obtain the maximum signal power, and consequently the maximum achievable SNR when the signal amplitude completely spans the ADC dynamics, i.e., $x_{pp} = 2.2\ V_{pp}$.

We have measured the total noise power M_w (comprising the contribution due to both the analog front-end and the baseband board) of our testbed to evaluate the maximum achievable SNR as a function of the gain parameters and the signal waveform. In Fig. 9 we show the maximum achievable SNR for a complex sinusoidal signal (PAPR= 3 dB), a single carrier 64 QAM signal (PAPR= 3.7 dB), and an orthogonal frequency division multiplexing (OFDM) signal (PAPR ≈12 dB) [24], when the first channel of the testbed is used (similar results can be obtained with the other channels). As it can be observed, the maximum achievable SNR decreases with the increase of the gain setting due to the increase of the noise power. Thus, if the received power were too low, it would be necessary to amplify the received signal, i.e., to increase the gain in order to reach the ADC dynamic range, with the consequence of a reduction of the maximum achievable SNR. However, opportunely setting the transmitted power, we can obtain SNR values up to approximately 60 dB.

4. DoA estimation

In this section we present several DoA estimation results obtained by using the WiPLi Lab testbed in an anechoic chamber.

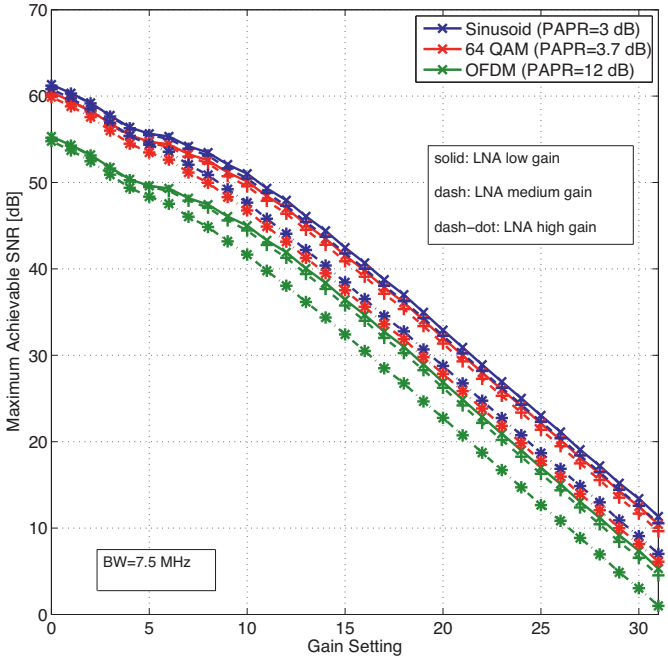


Fig. 9. Maximum achievable SNR at the channel 1 as a function of both the gain setting and the signal waveform, with BW= 7.5 MHz.

This has been done to isolate the system from the environment and concentrate on the hardware performance. The considered testbed parameters are: BW= 7.5 MHz, high gain mode with gain setting 17 (which corresponds to a gain of 67 dB), transmitted power from −37.5 to −2.5 dBm that yield SNRs from −7 to 28 dB, and a TX-RX distance of about 1.5 m.

The tested DoA estimation algorithm is the one presented in [21], whose main steps are reported below.

4.1. DoA estimation algorithm

The received sample at time nT for the i-th antenna array element can be written as

$$\begin{aligned} y^{(i)}(nT) &= \alpha e^{j2\pi f_0 nT + j\varphi} e^{-j\pi(i-1)\sin(\phi_0) + j\Phi^{(i)}} \\ &\quad + w^{(i)}(nT), \quad i \in \{1, \ldots, M\}, \end{aligned} \tag{5}$$

where α is the real signal amplitude, f_0 is the frequency of the transmitted single tone signal (in our implementation the RF signal is down-converted at baseband frequency $f_0 = 200$ kHz). Furthermore, φ is a random phase contribution due to the propagation, ϕ_0 is the phase associated to the DoA, $\Phi^{(i)}$, $i \in \{1, \ldots, M\}$ are the phase offsets introduced by the RF LO and the path cable lengths, $w^{(i)}(nT)$ are the complex noise samples, and $M = 4$ is the number of antenna elements. As described in Section 2.2, the system has to be calibrated in order to compensate the phase offsets $\Phi^{(i)}$, $i \in \{1, \ldots, M\}$. In particular, in the considered DoA algorithm, the phase offset differences $\hat{\Phi}^{(i)} = \Phi^{(i)} - \Phi^{(i+1)}$ are estimated over N samples as

$$\hat{\Phi}^{(i)} = \angle \left\{ \frac{1}{N} \sum_{n=0}^{N-1} x^{(i)}(nT) x^{(i+1)^*}(nT) \right\}, \quad i \in \{1, \ldots, M-1\}, \tag{6}$$

where $\angle$ is the argument function and $.^*$ is the complex conjugate operator, when the DoA ϕ_0 is set to 0°.

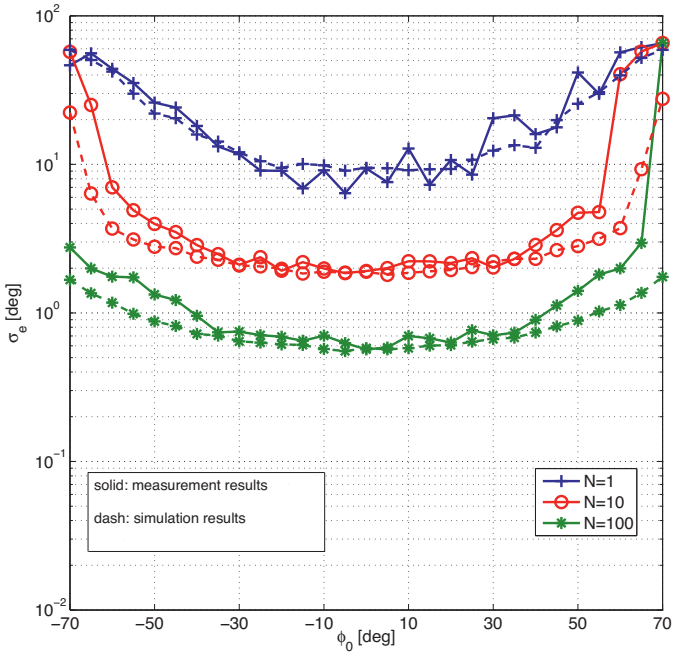


Fig. 10. Standard deviation of the error as a function of the AoA ϕ_0, with SNR= 3 dB.

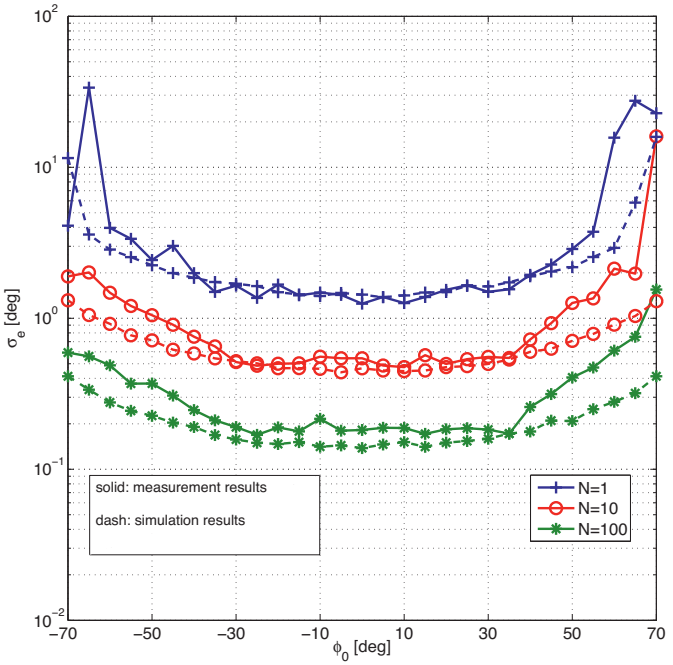


Fig. 11. Standard deviation of the error as a function of the AoA ϕ_0, with SNR= 13 dB.

After the phase offset estimation, a generic DoA ϕ_0 can be estimated as

$$\hat{\phi}_0 = \arcsin\left\{\frac{\angle z}{\pi}\right\}, \qquad z = \frac{1}{N(M-1)}\sum_{n=0}^{N-1}\sum_{i=1}^{M-1} x^{(i)}(nT)x^{(i+1)^*}(nT)e^{-j\hat{\Phi}^{(i)}}. \tag{7}$$

The performance of this estimator can be evaluated in terms of root mean square error (RMSE), that is defined as

$$\mathrm{RMSE} = \sqrt{E\left\{\left(\phi_0 - \hat{\phi}_0\right)^2\right\}}, \tag{8}$$

and that can be approximated as

$$\mathrm{RMSE} \approx \sqrt{\frac{1}{N_{it}}\sum_{k=1}^{N_{it}}\left(\phi_0 - \hat{\phi}_{0,k}\right)^2}, \tag{9}$$

where $\hat{\phi}_{0,k}$ is the estimate obtained at the k-th experiment trial, and N_{it} is the total number of trials (in our case, $N_{it} = 100$).

4.2. Experimental results

We have conducted two experiments in order to show the performance first as a function of the angle of arrival ϕ_0, and then as a function of the SNR. However, w.r.t. the first experiment, the accuracy in the rotation of the rotating board is 2.5°, which may introduce an instrumental bias in the estimation error. Hence, in order to study this kind of performance, we report the standard deviation of the error that can be approximated as

$$\sigma_e \approx \sqrt{\frac{1}{N_{it}}\sum_{k=1}^{N_{it}}(e_k - \mu_e)^2}, \tag{10}$$

where $e_k = \phi_0 - \hat{\phi}_{0,k}$, while $\mu_e = 1/N_{it}\sum_{k=1}^{N_{it}} e_k$ represents the mean value of the error.

In Figs. 10 and 11 we show the performance results of the considered estimator in terms of standard deviation of the error as a function of the angle of arrival ϕ_0 and the number of samples N, with SNR= 3 dB and SNR=13 dB, respectively.

We can observe that the measurement results are in good agreement with the simulation results, at least in the angle range $\{-45°, 45°\}$. The deviation of the experimental results from the simulated one when the DoA is out of this angle range can be simply justified by the fact that the antenna array elements have not the same gain as a function of the DoA, as it can be observed in Fig. 2 where the radiation pattern of the four antennas is reported. When the DoA exceeds ±45°, the array gain decreases, so the effective SNR decreases in turn and, consequently, the performance degrades.

In the second experiment, we consider the performance of the algorithm in terms of RMSE as a function of the SNR. We have considered only two test DoAs, $\phi_0 = \{0, 30°\}$, that have been obtained by orientating the receiver antenna array manually. The performance result is shown in Fig. 12 for $\phi_0 = 0°$, and in Fig. 13 for $\phi_0 = 30°$. The simulation results are obtained in an ideal case, i.e., without hardware impairments, and in the case of correlated phase noise, as described in Section 2.2.

Even in this case, good agreement between simulation and experimental results can be seen. In particular, we can observe the presence of an error floor due to the presence of some phase noise that is not compensated by the algorithm. Nevertheless, this error floor ensures 0.1 degree of RMSE.

As explained above, the characterization and performance analysis reported has been done by installing the testbed in an anechoic chamber in order to isolate the system from the environment and concentrate on the hardware performance. Indeed, the propagation medium has also an effect on performance since it introduces attenuation and multipath propagation. Some results on the DoA estimation performance of the testbed in a real context can be found in [25], while an algorithm for the mitigation of multipath propagation has been recently described in [26]. Another issue is the presence of co-channel interference. Two scenarios can be envisioned: (a) if we wish to realize an ad hoc radio localization system a dedicated band can be used; (b) the direction finding system is an overlay system that operates in the same band as other systems.

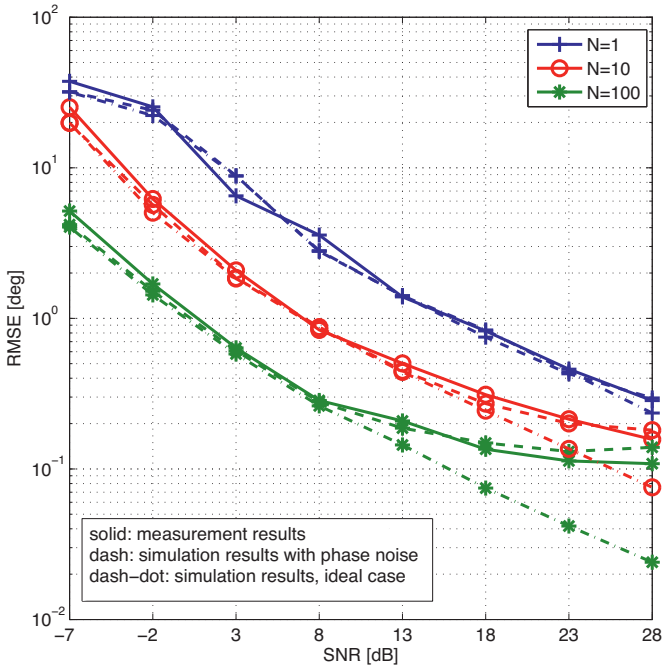


Fig. 12. RMSE as a function of the SNR, with $\phi_0 = 0^\circ$.

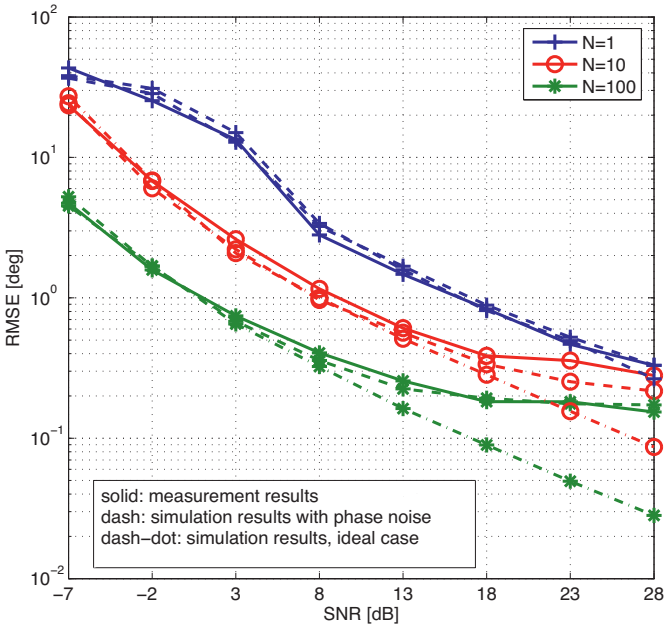


Fig. 13. RMSE as a function of the SNR, with $\phi_0 = 30^\circ$.

In the scenario (b), some form of coexistence mechanism through media access techniques, e.g., CSMA, can be implemented, as well as interference mitigation through signal processing algorithms can be studied.

5. Conclusion

In this paper we have described the main components of the WiPLi Lab wireless testbed. In particular, it comprises a single transmitter, a rotating four-element antenna array connected to a quad radio frequency (RF) front-end, an eight channel acquisition board (to process four pairs of I&Q signals). It is also equipped with an FPGA, and a control PC that manages all the devices. We have described each component of the testbed. In particular, we have completely characterized the four RF front-ends in terms of gain and bandwidth. Furthermore, we have highlighted that the limited write rate of the memory poses a constraint in the maximum sampling rate, and the RF signal bandwidth. Moreover, we have illustrated the basic System Generator for DSP design that can be used to record data into the memory, and to process it offline. Considerations about the maximum achievable SNR have been done. We have presented a simple DoA estimation algorithm that has been used to compare the results obtained via simulation and those obtained in a real hardware implementation. Good agreement has been found. In particular, the effects of both non isotropic antenna gains and phase noise originating from non co-phased RF front-ends have been reported.

Overall, the developed testbed has proven to be a valid tool to perform practical experimentation of multiple antenna algorithms for DoA estimation and validate simulation results. Although we have focused on DoA estimation for localization purposes, it is interesting to use the testbed for other applications, e.g., MIMO data communications and channel acquisition and characterization. In this respect, the testbed already provides a platform for single input multiple output (SIMO) implementations. For full MIMO experimentation another multiple antenna node needs to be integrated.

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