

This is the title of the thesis

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A thesis presented for the degree of
Doctor of Philosophy

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University College London, UK
January 2015

*I, AUTHORMNAME confirm that the work presented in this thesis is my own.
Where information has been derived from other sources, I confirm that this
has been indicated in the thesis.*

Abstract

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Acknowledgements

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Abbreviations

API	Application Programming Interface
JSON	JavaScript Object Notation

Chapter 1

Introduction

1.1 Motivation

Car manufactures want to reduce cost in terms of money and time required to develop, test and validate a new piece of software due to a change of supplier. For that reason, centralized end-to-end architectures are the solution they are aiming to, because for car companies such as BWW and Audi the car of future will be similar to a “data center on wheels” [1].

Centralized end-to-end architectures would be the first step stone toward to decoupling software and hardware [2]. This type of architectures not only will take advantage of internet connectivity, cloud computing and powerful heterogeneous processing units, but also will allow scalable, hierarchical and highly integrated system.

In other words, car manufactures prefer now a days low-latency, hierarchical and cost effectiveness of centralized end-to-end architectures, because today requirements of computational power, bandwidth, integration, safety and real-time [3].

However, car manufactures don’t forget that at the end, in centralized end-to-end architectures, different types of software would run on top of an heterogeneous hardware supplied by companies such as NVIDIA, Mobileye or Qualcomm. Thus, it’s important to analyze and understand how software

will behave under those conditions, in order to ensure a predictable and efficient system.

1.2 Industrial challenge WATERS 2019

Predictability is a key property for safety-critical and hard real-time systems [4]. Analyzing time related characteristics is an important step to design predictable embedded systems. However, in multi-core or heterogeneous systems based on centralized end-to-end architectures is harder to satisfy timing constraints due to scheduling, caches, pipelines, out-of-order executions, and different kinds of speculation [5]. Thus, development of timing-analysis methods for these types of architectures has become, nowadays, one of the main focus of research in both industry and academic environment.

Robert Bosch GmbH or Bosch, the German multinational engineering and electronics company, and one of the top leaders in development technology for the automotive industry announces every year *the WATERS Challenge*. The purpose of the WATERS industrial challenge is to share ideas, experiences and solutions to concrete timing verification problems issued from real industrial case studies [6].

This year, 2019, the challenge focuses on timing-analysis for heterogeneous software-hardware systems based on centralized end-to-end architectures. The platform chosen for this purpose is the NVIDIA® Jetson™ TX2 platform which has an heterogeneous architecture equipped with a Quad ARM A57 processor, a Dual Denver processor, 8GB of LPDDR4 memory and 256 CUDA cores of NVIDIA’s Pascal Architecture. For the challenge it is available an Amalthea model for this platform to design a solution, and test it later on real hardware.

1.3 NVIDIA Jetson TX2: Architecture Overview

NVIDIA Jetson TX2 is an embedded system-on-module (SOM). It is ideal for deploying advanced AI to remote field locations with poor or expensive internet connectivity, Robotics, Gaming Devices, Virtual Reality (VR), Augmented Reality (AR) and Portable Medical Devices. In addition, it offers near-real-time responsiveness and minimal latency—key for intelligent machines that need mission-critical autonomy [7].

The main components of the Jetson TX2 are dual-core ARMv8 based NVIDIA Denver2, quad-core ARMv8 Cortex-A57, 8GB 128-bit LPDDR4 and integrated 256-core Pascal NVIDIA GPU. The quad-core Cortex-A57 and dual-core NVIDIA Denver2 can be seen as a cluster of heterogeneous multiprocessors (HMP) [8]. Both HMP and GPU shares a 8GB SRAM memory as shown in Figure 1.1. Hereafter, whenever we use the term **host**, we will refer to HMP, similarly we will use **device** to refer to GPU.

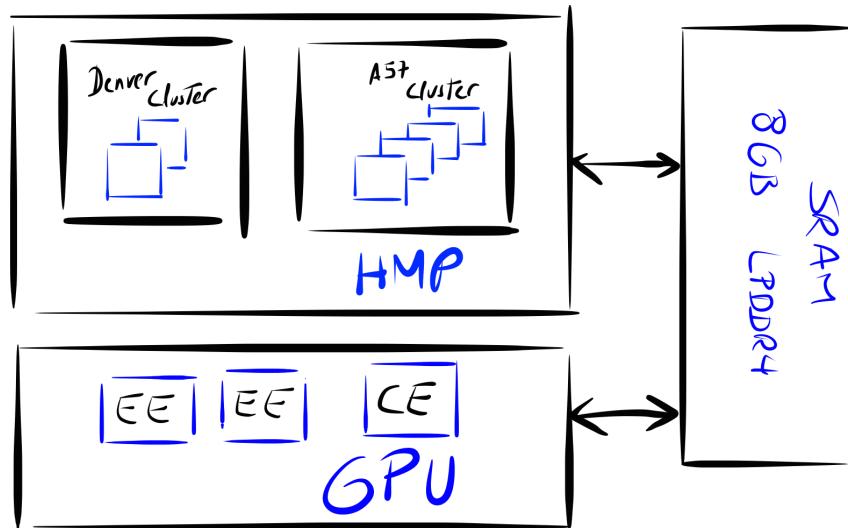


Figure 1.1: Jetson TX2 Architecture Overview

Any NVIDIA GPU has two types of engines, **Copy Engines (CE)** and **Execution Engines (EE)**. The Jetson TX2 has only one CE and two EE also known as **Streaming multiprocessors**. CE is in charge of data transfers from host to device and viceversa. There is, moreover, the possibility that

EE and CE can run concurrently.

The GPU uses **streams** to run applications. The number of streams depends on the GPU resources. An application can run in one or multiple streams, the GPU scheduler, by default, manages how the application will be allocated on streams in order to maximize throughput. In Chapter 2, we will discuss in more detail how the TX2 GPU scheduler behaves in case of multiple applications.

1.4 Jetson TX2 Amalthea Model

AMALTHEA is a platform for engineering multi- and many-core embedded systems. This platform enables the creation and management of complex tool chains including simulation and validation [9]. In the context of WATERS Challenge 2019, Bosch offers an AMALTHEA model of the Jetson TX2. In this model, a CPU runnable will read data from memory, execute some computation (Ticks) and write back data into memory as shown in Figure 1.2.

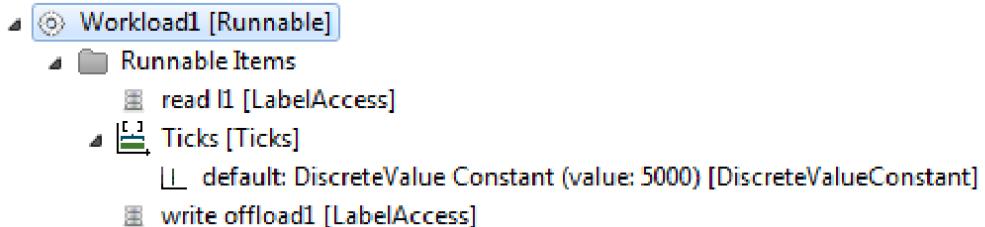


Figure 1.2: Runnable example for a CPU [6]

In the case of GPU modeling, the runnable will follow the same pattern as in the CPU case: read, execution, write back. However, the reading operation is actually to copy memory from host to device, thus it is modeled as *memory reading from host* and then as *memory writing to device*. On the other hand, the writing back operation requires to copy memory from device to host, therefore it is modeled as *memory reading from device* and then as *memory writing to host* as shown in Figure 1.3.

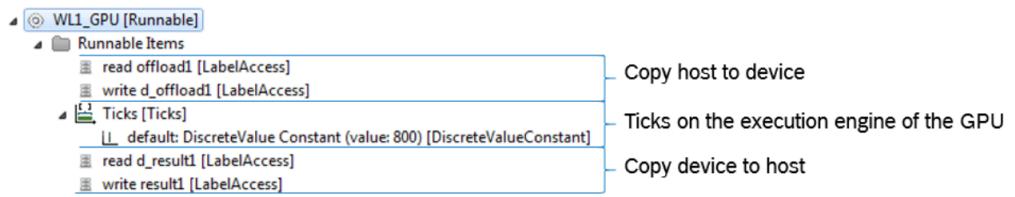


Figure 1.3: Runnable example for a GPU [6]

Chapter 2

CUDA and Jetson TX2

In this chapter...blablabla

2.1 NVIDIA GPU Software Model

Now a days computer applications run on heterogeneous hardware and GPUs are important in order to achieve high performance computing. Since 2006 running software on NVIDIA GPUs are known as a *CUDA application* [10]. A CUDA application will run concurrently multiple instances of special functions called **kernel**s. Each instance runs on a **thread**. Moreover, these threads are arranged in **block**s, and blocks compose **grid**s as shown in Figure 2.1.

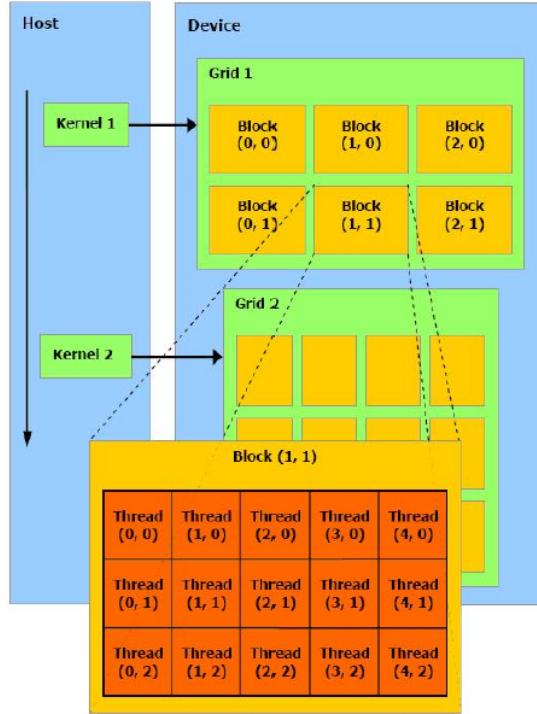


Figure 2.1: Organisation of grids, blocks, threads, and kernels [11].

It's logical to think that there is also a hierarchical memory structure. Threads, blocks and grids have access to different memory spaces as illustrated in Figure 2.2. The types of memory are summarized in Table 2.1.

Table 2.1: Types of memories in a GPU

Memory	Main Characteristics	Scope	Lifetime
Global	R/W, Slow and big	Grid	Application
Texture	ROM, Fast, Optimized for 2D/3D access	Grid	Application
Constant	ROM, Fast, Constants and kernel parameters	Grid	Application
Shared	R/W, Fast, it's on-chip	Block	Block
Local	R/W, Slow as global, when registers are full	Thread	Thread
Registers	R/W, Fast	Thread	Thread

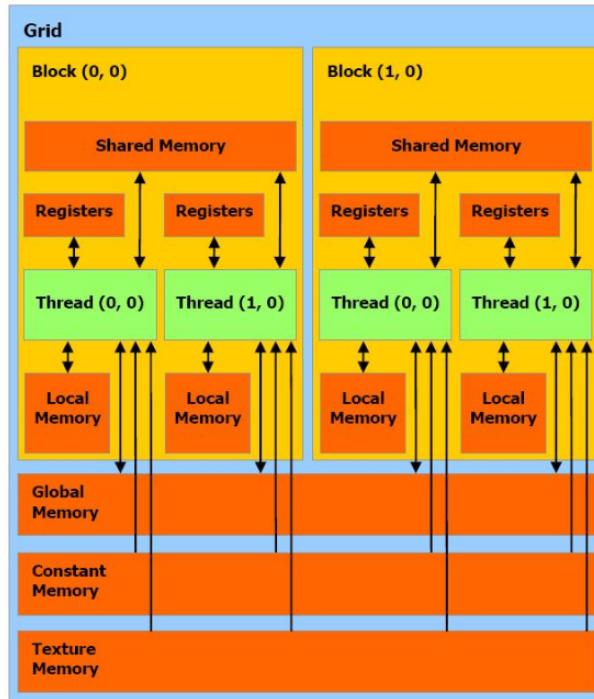


Figure 2.2: Memory hierarchy [11].

In summary, CUDA application solve problems that were modeled based on *divide and conquer* principle. Moreover, CUDA software model not only allow users to achieve high computational performance, but also CUDA application are highly scalable.

2.2 NVIDIA GPU Hardware Model

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2.3 NVIDIA processors inside Jetson TX2

2.3.1 NVIDIA DENVER2

The other ARM cluster is composed of two NVIDIA Denver2 cores and 2MB of L2 Cache. Each NVIDIA Denver2 is a custom made 64-bit processing based on ARMv8, which is optimized for single-thread performance [12].

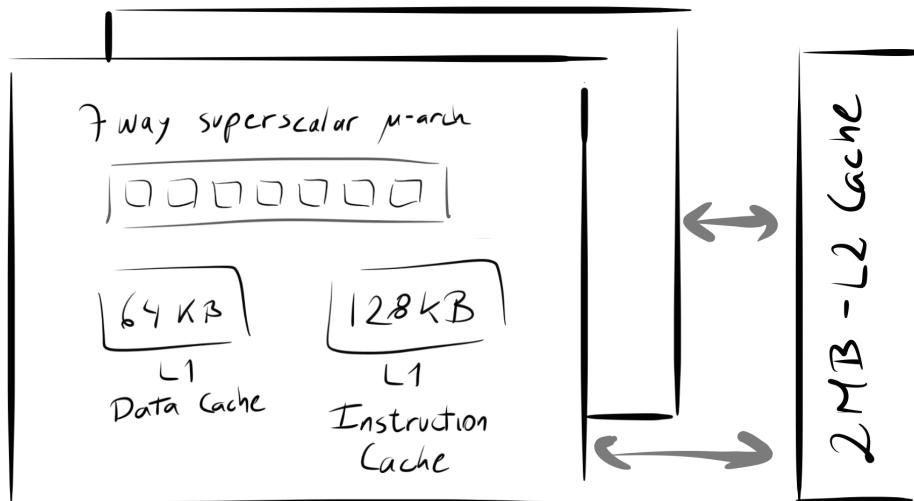


Figure 2.3: Diagram of the Denver Cluster in TX2

This custom processor has two main characteristics. First, it has a 7-way superscalar microarchitecture. It means that a Denver2 core can process 7 operations per clock cycle. Secondly, it uses *Dynamic Code Optimization*. Frequently used software routines are converted into a dense and highly tunned equivalent microcode executable only by Denver2 cores. A Denver2 core analyze the ARM code just before execution and look for places where instructions can be handle together to maximize throughput taking in advan-

tage the 7-way superscalar microarchitecture. In Figure 2.3 can be observed that each Denver2 core has 64KB of L1 Data Cache, and 128KB of Instruction Cache. The optimized code is stored in the former one, also known as *Optimization Cache* [12].

2.4 Introduction

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$$f(x) = ax^3 + bx^2 + cx + d \quad (2.1)$$

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2.6 Conclusion

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Chapter 3

First research study, with code

3.1 Introduction

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3.2 Method

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3.2.1 SUBSECTION 1 WITH EXAMPLE CODE BLOCK

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quam sit amet nunc maximus, id bibendum ex blandit.

For syntax highlighting in code blocks, add three ““” characters before and after a code block:

```
mood = 'happy'  
if mood == 'happy':  
    print("I am a happy robot")
```

Alternatively, you can also use LaTeX to create a code block as shown in the Java example below:

Listing 3.1: Main.java

```
1 /**
2 * Hello, world – example in Java.
3 */
4 public class Main{
5     // says hello to the world
6     public static void main(String[] args) {
7         System.out.println("Hello, world!");
8     }
9 }
```

If you use `javaCodeStyle` as defined in the `preamble.tex`, it is best to keep the maximum line length in the source code at 80 characters.

3.2.2 SUBSECTION 2

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Chapter 4

Research containing a figure

4.1 Introduction

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4.2 Method

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4.3 Results

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4.4 Discussion

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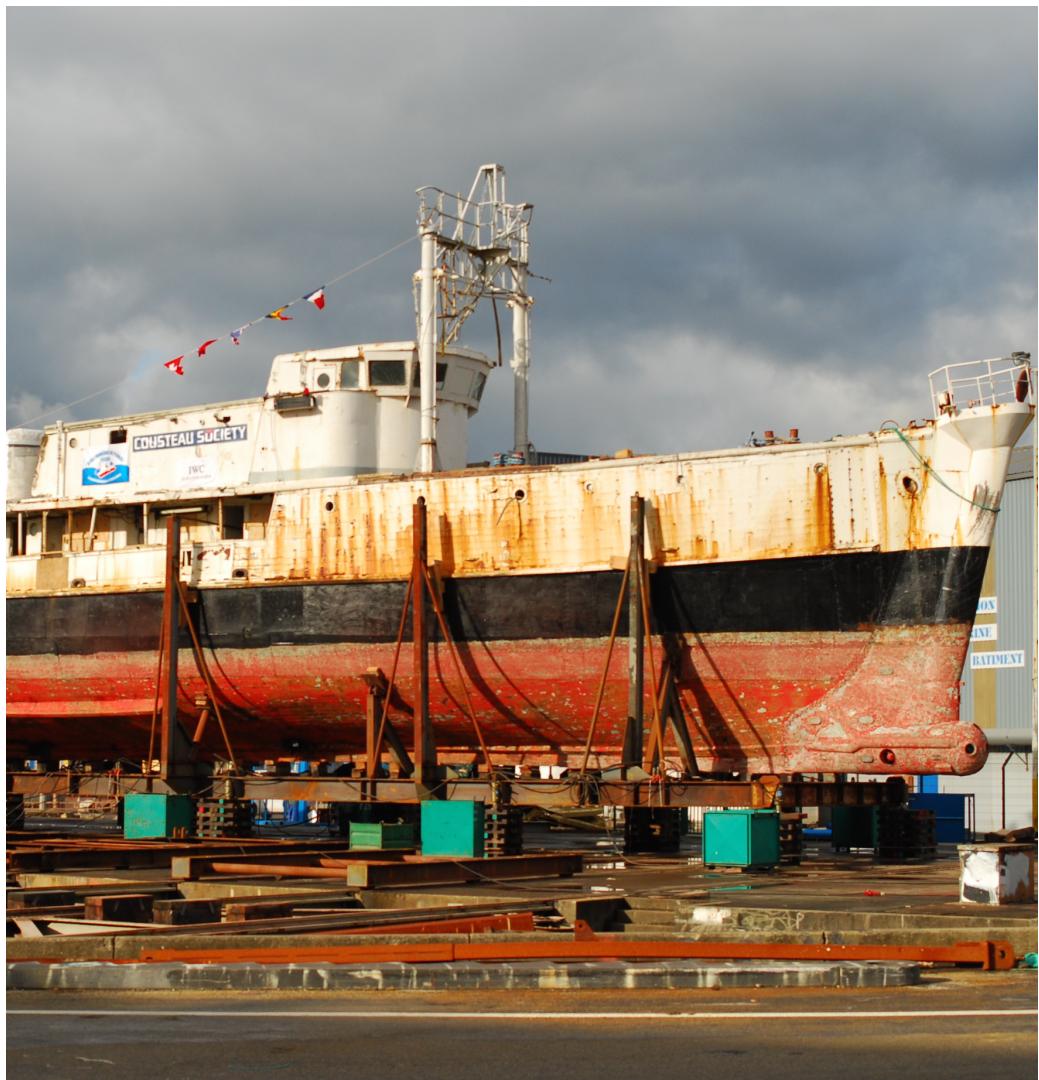


Figure 4.1: RV Calypso is a former British Royal Navy minesweeper converted into a research vessel for the oceanographic researcher Jacques-Yves Cousteau. It was equipped with a mobile laboratory for underwater field research.

4.5 Conclusion

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Chapter 5

Research containing a table

5.1 Introduction

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5.2 Method

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5.3 Results

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Column 1	Column 2	Column 3
Row 1	0.1	0.2
Row 2	0.3	0.3
Row 3	0.4	0.4
Row 4	0.5	0.6

5.4 Discussion

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5.5 Conclusion

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Chapter 6

Final research study

6.1 Introduction

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6.2 Method

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6.3 Results

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6.4 Discussion

This is the discussion. Curabitur gravida nisl id gravida congue. Duis est nisi, sagittis eget accumsan ullamcorper, semper quis turpis. Mauris ultricies diam metus, sollicitudin ultricies turpis lobortis vitae. Ut egestas vehicula enim, porta molestie neque consectetur placerat. Integer iaculis sapien dolor, non porta nibh condimentum ut.

6.5 Conclusion

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Chapter 7

Conclusion

7.1 Thesis summary

In summary, pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Nunc eleifend, ex a luctus porttitor, felis ex suscipit tellus, ut sollicitudin sapien purus in libero. Nulla blandit eget urna vel tempus. Praesent fringilla dui sapien, sit amet egestas leo sollicitudin at.

7.2 Future work

There are several potential directions for extending this thesis. Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam gravida ipsum at tempor tincidunt. Aliquam ligula nisl, blandit et dui eu, eleifend tempus nibh. Nullam eleifend sapien eget ante hendrerit commodo. Pellentesque pharetra erat sit amet dapibus scelerisque.

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Appendix 1: Some extra stuff

Add appendix 1 here. Vivamus hendrerit rhoncus interdum. Sed ullamcorper et augue at porta. Suspendisse facilisis imperdiet urna, eu pellentesque purus suscipit in. Integer dignissim mattis ex aliquam blandit. Curabitur lobortis quam varius turpis ultrices egestas.

Appendix 2: Some more extra stuff

Add appendix 2 here. Aliquam rhoncus mauris ac neque imperdiet, in mattis eros aliquam. Etiam sed massa et risus posuere rutrum vel et mauris. Integer id mauris sed arcu venenatis finibus. Etiam nec hendrerit purus, sed cursus nunc. Pellentesque ac luctus magna. Aenean non posuere enim, nec hendrerit lacus. Etiam lacinia facilisis tempor. Aenean dictum nunc id felis rhoncus aliquam.

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