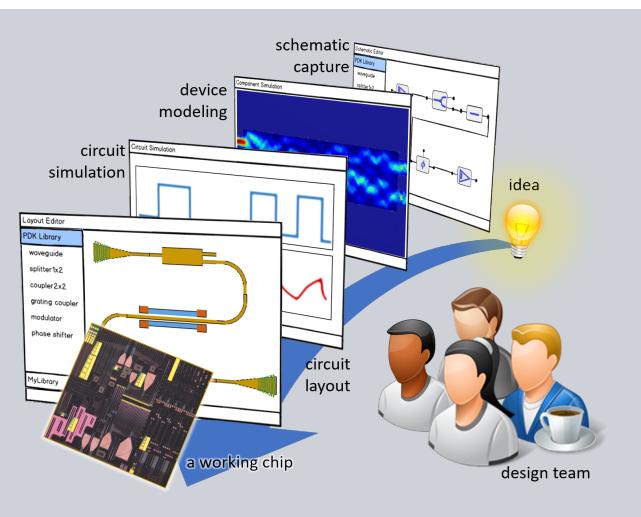


**Abstract** Silicon Photonics technology is rapidly maturing as a platform for larger-scale photonic circuits. As a result, the associated design methodologies are also evolving from component-oriented design to a more circuit-oriented design flow, that makes abstraction from the very detailed geometry and enables design on a larger scale. In this paper, we review the state of this emerging photonic circuit design flow and its synergies with electronic design automation (EDA). We cover the design flow from schematic capture, circuit simulation, layout and verification. We discuss the similarities and the differences between photonic and electronic design, and the challenges and opportunities that present themselves in the new photonic design landscape, such as variability analysis, photonic-electronic co-simulation and compact model definition.



## Silicon Photonics Circuit Design: Methods, Tools and Challenges

Wim Bogaerts<sup>1,2,\*</sup> and Lukas Chrostowski<sup>3</sup>

### 1. Introduction

Silicon photonics is the technology to integrate a large number of optical functions on a chip using the fabrication technology of the CMOS industry, thereby enabling low cost, large volume, manufacturing [1–3]. The field has rapidly evolved from a ‘scientific hot topic’ to an industrially viable platform, largely driven by telecom and datacom applications, and enabled by the growing number of manufacturing and prototyping facilities (‘fabs’) [4].

Today there coexist a wide diversity of technology platforms to build photonic integrated circuits (PIC) [5], using different material systems such as III-V semiconductors, Lithium Niobate, high-index glasses and nitrides, polymers, and of course silicon. What makes silicon photonics a unique technology is exactly its compatibility with the manufacturing processes and tools used in the CMOS industry: this offers a route towards high volume manufacturing at potentially low cost per device. The second unique feature of silicon photonics is its high refractive index contrast, which allows for sub-micrometer waveguide dimensions, tight bends and close spacing, and in turn, this allows for dense packing of optical functions on the surface of a chip [6]. This combination makes silicon photonics the only viable technology platform for high complexity, large-scale photonic integrated circuits. However, the high refractive index contrast comes with a weakness: it imposes very strin-

gent requirements on the dimensions of the silicon photonic circuits, as nanometer-scale variations in waveguide core width or thickness can have non-negligible effects on the performance of the photonic circuits [7]. This implies that variability introduced by the fabrication process can have a significant impact on the overall performance of a circuit. Large complex circuits will automatically suffer more from variability than simple circuits. In the end, it is the overall yield of a circuit that determines whether it is commercially viable. As CMOS manufacturing technologies continue to advance, higher precision lithography is required to fabricate ever smaller devices. While transistors continue shrinking in size, photonic devices are fundamentally limited and remain approximately constant as a function of the technology node (e.g., a ring modulator has a fixed size determined by the design target free spectral range); the benefit of improved manufacturing is that it reduces the manufacturing variability and improves yield [8].

Still, silicon photonics processes are now considered to be sufficiently good for a number of applications, as is demonstrated by products released on the market. The various fabs provide processes for silicon waveguides with acceptable propagation losses around 1–2 dB/cm [9], thermal tuners with phase shifter efficiencies ranging from  $100 \mu\text{W}/\pi$  to  $100 \text{ mW } \pi$  [10], carrier-based electro-optic modulators working in both travelling wave and resonant modes [11, 12], and Germanium photodetectors with effi-

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ciencies of  $\approx 1A/W$  [13–15], with both modulators and detectors operating at high-speeds of many tens of gigahertz. Spectral filters can be implemented using combinations of waveguides and coupling structures [16–19]. Only the integration of the laser source, optical amplifier, and optical isolator is somewhat lagging, but solutions are becoming available based either on external sources [20] or heterogeneous integration [21–24]. While the majority of silicon photonics technologies operate around wavelengths in the traditional telecommunication bands between 1.2 - 1.6  $\mu m$ , the wavelength range can be extended to the visible domain using silicon nitride [25]. SOI wafers (silicon on insulator, with silicon as the waveguide core and silicon dioxide as the cladding) can be used up to 3.6  $\mu m$  (limited by silicon dioxide absorption), and even longer wavelengths in the mid-infrared can be accessed using germanium waveguides on a silicon substrate [26, 27]. These technologies don't lose their compatibility with CMOS manufacturing technologies and dense integration, and therefore fall under the same definition of *silicon photonics* used at the start of this article.

Even when silicon photonics enables high complexity and large circuits, today's circuit demonstrations are generally quite small and/or simple. For datacom applications, optical transceivers usually consist of a single light path between 3-10 optical elements. Larger optical circuits usually consist of simple repetitive scaling, such as switch matrices [28, 29] or phased arrays for beam steering [30]. While these circuits demonstrate the integration potential of silicon photonics, they are not very complex, and their functionality is limited. Other applications may leverage the potential of added complexity in photonic circuits. Silicon photonics is seen as an enabling technology for biosensing and diagnostics [31–33], spectroscopy [25], structural monitoring [34, 35], quantum information / quantum computing [36–38], microwave photonics [39–42], and can be applied for various sensor functions (accelerometers, gyroscopes, magnetic fields), etc. Such applications will require custom chip designs with very different requirements than transceivers for datacenter and telecom applications.

Fabrication processes for silicon photonics have become good enough to make large, complex circuits, with waveguide losses smaller than 1dB/cm, low-loss crossings, splitters, couplers, as well as good modulators and excellent photodetectors, all integrated into technology platforms that are subject to *statistical process control* (SPC) [43–45]. Even though there is still ample headroom for technological improvements, the complexity of the optical circuits is now largely limited by the capability to design them, while taking into account the limitations of the fabrication process such as variability and parasitics. A reliable *design flow*, transforming a circuit concept into a working chip, should accurately predict the yield of a complex circuit. Today, many photonic circuit designers employ manual techniques to compose their photonic circuits, with a focus on the physical geometry. This is reminiscent of the first electronic circuit design in the 1960s and early 1970s.

Photonic integrated circuits share many characteristics of electronic integrated circuits. They are defined by planar

processes on semiconductor wafers. The functionality can be described and modelled as a circuit, with signals propagating between the functional building blocks. As with electronics, the functionality of a photonic circuit does not come from a single element, but from the connectivity between many functional building blocks and subcircuits. The design of the chips eventually translates into a set of geometric 'mask layers' with the patterns for each planar processing step. The first photonic integrated circuits were defined as a single device, and usually simulated using direct (but approximate) electromagnetic simulation techniques such as *beam propagation methods* (BPM) [46, 47].

But with the large number of process steps in silicon photonics, as well as the increasing size of the circuits, the PIC design process is evolving along the lines of *electronic design automation* (EDA), with circuit hierarchy and reusable parametric building blocks as used in analog electronics [48, 49]. In electronics, this has led to a situation where circuit designers can create a first-time-right design for extremely complex integrated circuits with billions of components. The scaling of circuit design has been enabled by a number of factors

- **A standardized workflow:** most electronic IC design teams follow a similar workflow, separating the logical design from the actual physical implementation.
- **Accurate models:** Circuit simulation can accurately predict the behavior of a large circuit because the building blocks have been thoroughly characterized and the models are very accurate. Models also contain statistical information on their components' performance, such as *slow and fast corners*.
- **Design kits and reusable IP blocks:** Foundries provide design kits with building blocks that can be directly used by the designer. At a higher level, reusable subcircuits, so-called *intellectual property (IP) blocks* found in libraries, allow designers to focus on higher-level functionality.
- **Automation:** Modern EDA tools help the designer to automate increasingly complex tasks, including the synthesis of circuits from high-level specifications.
- **Comprehensive verification** allows designers to check the final design against the original specifications.

Given the same technology foundation, it is no surprise that the silicon photonics ecosystem is evolving along the same lines as electronics, where a small number of foundries ('fabs') manufacture the chips for a much larger community of designers [4]. In such a 'fabless' model, designers cannot steer fabrication process improvements, so they should have sufficient information about the process and qualified building blocks to reliably design circuits. For this, fabs supply *process design kits* (PDK) with details about the fabrication process and with building blocks that contain both the geometric layout, and in some cases *behavioral models*.

It is with these behavioral models (also called *compact models*) that we identify some of the key limitations for photonic circuit design. While today there exist several powerful circuit simulation tools for photonics, they all have their own *compact model implementation*. There is no common definition of the models for even the simplest components (e.g.,

waveguide, directional coupler), and the implementation of models in each tool is very different. This raises a significant barrier for fabs to invest in a compact model library for their PDK. A standard model implementation language (like Verilog-A for analog electronics [50]), or even an agreement on standard model definitions for the most common building blocks (like the BSIM transistor models [51]) would present a strong incentive to invest in compact model libraries for circuit-driven photonic design. Without reliable models, the added value of a photonic circuit design flow as in electronics is limited.

Still, the parallels between electronic and photonic design automation are driving a convergence in design flows, as design tools for photonic circuits are now being coupled to established electronic design tools [49, 52–55]. This convergence is driven by necessity, and among all the different PIC technologies, this necessity is most acute in silicon photonics, because silicon photonics is both the most sensitive and most scalable of PIC technologies. First, silicon photonic circuits need electronic interfaces such as for the processing of high-speed signals and for electronic control loops that govern and stabilize the behavior of the photonic circuit. Second, electronics is also looking in the direction of silicon photonics to solve the interconnect bottlenecks [2, 56]. Photonic-electronic co-integration and co-design will make it possible to create integrated photonic-electronic-software systems with control and monitoring. These can compensate the process variability and enable larger, more complex circuits, and create opportunities to implement functionality that cannot be achieved with photonics or electronics separately.

Photonics is in many ways very different from electronics, and these differences are also reflected in the design flows. Photonic layouts are usually not based on rectangular patterns, and this can create difficulties for design verification, and control of pattern density. Photonic signals are also different from electrical signals, and cannot be expressed as voltages and currents. Rather, the signal propagation bears a stronger resemblance to radio-frequency (RF) signals. True electronic-photonics co-design will therefore require a new mixed-signal model for co-simulation.

In this paper, we present a review of the landscape of silicon photonics design methodologies, from the perspective of the *circuit* designer (as opposed to the device/component designer). First, we give a brief introduction about what constitutes a circuit design flow in section 2. In section 3 we start with an analysis of today’s historically grown design processes, which are an evolution of component/device design. The requirements for component design, with a focus on geometrical optimization, are very different from those of circuit design, where circuit functionality is governed by the connectivity of functional building blocks. Section 4 then discusses the emerging trend towards an EDA-like design flow, with a focus on a schematic-based circuit design. Design tools are evolving at a rapid pace in this domain, but the necessary shift in mindset in the actual design community is experiencing some inertia, especially where designers have built custom tools for their specific needs, and where foundries do not yet supply PDKs compatible with

schematic-driven design. In section 5 we discuss a number of significant challenges that will need to be addressed in the near future to give photonics circuit designers similar *first-time-right* capabilities as electronics designers have today. Finally, section 6 presents a number of opportunities for the research community and the important actors in *photonic design automation* (PDA) to provide a dramatic boost to the photonic design community.

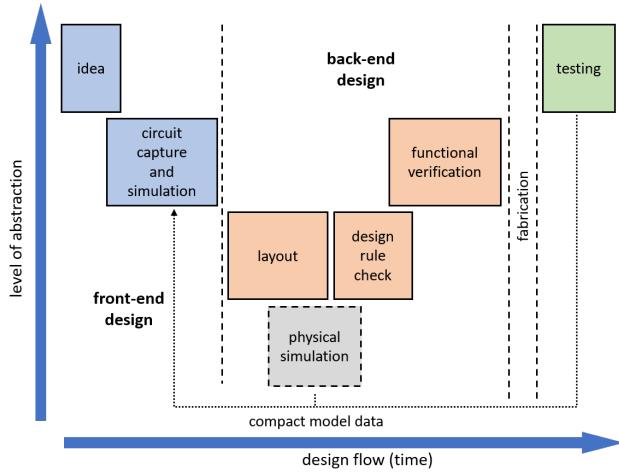
## 2. Design Flows

The purpose of a *design flow* is to translate a functional idea into a *working chip* (*i.e.*, the *design*), using a reproducible method (*the flow*). The final objective, *i.e.*, a *working chip*, is important. While the design of simple photonic components can be done intuitively, a reproducible flow, backed up by efficient software tools, is important to guarantee that more complex chips and circuits are fabricated with sufficient yield.

When implementing functionality on a photonic chip, the first step is to articulate the needed functionality. This system-level consideration is usually expressed as a relation between inputs and outputs: what behaviour or output signal is expected for a given input signal? From this abstract level, this functionality should be translated into a gradually more refined description (a circuit) until it can be implemented as a photonic integrated circuit (PIC). In a PIC, light is manipulated on the surface of a chip. At the basic level, this manipulation is done by the geometric distribution of material (or by locally changing material properties). At this detailed level, the exact behavior of the electromagnetic waves in the structure can be engineered. However, when the dimensions of the circuit become larger, this level of detail can no longer be captured efficiently, and a more abstract design approach is needed.

The different levels of abstraction in a circuit design flow are illustrated in Fig. 1. We can roughly break down the design flow into the following steps:

- **Design Capture:** the functional idea is converted into a logical circuit of functional building blocks or hierarchical subcircuits. There can be an exploration of different circuit architectures or topologies, with different choices of building blocks.
- **Circuit simulation:** The logical circuit is simulated and its parameters are optimized so it will perform as intended. This can also include a yield analysis by introducing variability in the circuit parameters.
- **Circuit Layout:** The logical circuit is converted into a mask layout representation that can be used for fabrication. This results eventually in a large number of polygons on different mask layers.
- **Global Chip Design:** The logical circuits put together, and connected to a power supply distribution network, electrical I/Os, and generation of dummy tiling patterns to maintain uniform pattern density.
- **Verification:** The layout is checked against errors, making sure it is compatible with the fabrication process and



**Figure 1** Different levels of abstraction in a circuit design flow. The horizontal axis indicates the sequence of design steps, while the vertical axis indicates the level of abstraction. In a circuit design flow, the physical modelling of components is preferably avoided, and circuit simulations are based on compact models.

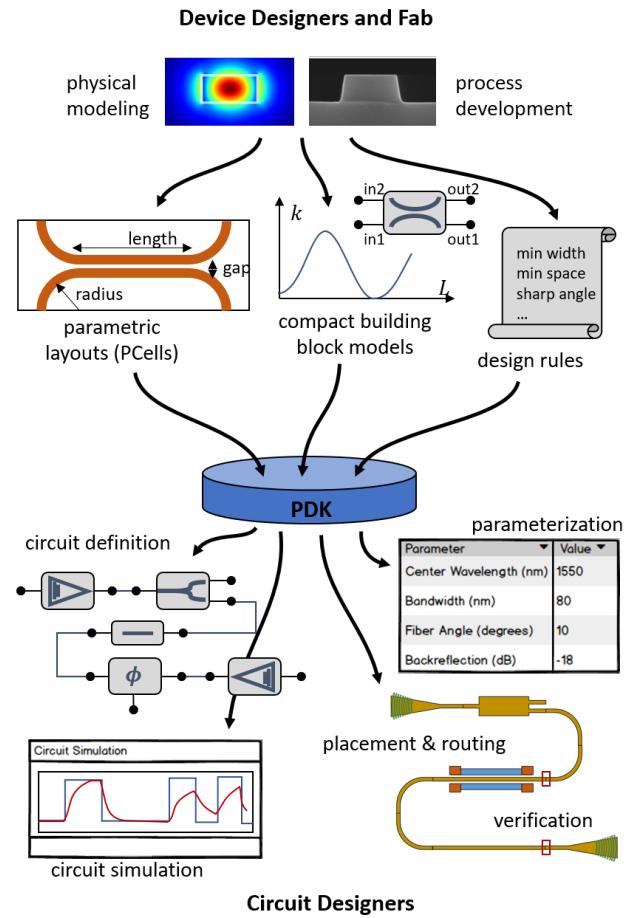
post-layout simulations are performed to ensure that the layout will perform the intended function.

- **Tape-out and fabrication:** The layout file undergoes a number of post-processing steps to convert it into the actual write patterns, and the chip is fabricated.
- **Testing and Packaging:** The fabricated chip is packaged and tested, and the results are compared with the original design. If needed, the design information will be updated to improve the next generation of designs.

Clearly identifying and separating these steps and levels of abstraction in the design is essential to the scaling of circuits. This is a lesson that has been learned in electronics [57]. Electronic circuits are not designed at the geometry of the individual transistors. Rather, known transistor devices, or known subcircuits consisting of many transistors, diodes and other electrical elements, are reused to compose larger circuits. The circuit designers trust that the building blocks have been properly designed and qualified by the fabs and device designers, and that the relevant geometries and models are supplied in a *process design kit* (PDK) and external libraries.

A *process design kit* (PDK), in general, is an information package that contains sufficient information for a designer to create a chip design that can be fabricated in a fab [49, 58]. As illustrated in Fig. 2, it is the primary interface between the fab and the designer. A PDK thus acts as a bridge between the level of abstraction required by the circuit designer and the electromagnetic device designer. It shields the circuit designer from the details of the fabrication process, and reduces the needs to optimize the geometry of every individual device.

It is important that a design flow is supported by software tools that automate repetitive tasks, manage the design data at the different levels of abstraction, and enable collaboration between designers. Design automation tools make it possible for the designer to go back and forth in the de-



**Figure 2** A *process design kit* (PDK) separates the fab and component designers from the circuit designers. It contains the descriptions of the building blocks (layout as well as circuit models) and the design rules of the fabrication process. Based on this information, a circuit designer should not need to perform physical modelling of the (parametric) building blocks.

sign flow, iterate the circuit and device parameters and run different simulations without creating (accidental) inconsistencies in the design. For instance, the design software should ensure that the circuit being simulated consists of the same components as the circuit laid out for fabrication.

Note that the design flow extends well beyond the generation of a layout for fabrication. The design flow should be aware of the post-fabrication packaging requirements, and should incorporate test structures and procedures to verify the fabricated chip against the original design intent.

In the following section, we will discuss the current practices in silicon photonic circuit design. Section 4 will then discuss the recent developments in design techniques and tools that are based on the electronic design automation (EDA) flows and are gradually being adopted for photonic circuits.

### 3. Silicon Photonics Design Today

Most photonic circuit designers today are still firmly rooted in the physical component design process that has been used for photonic chips for the past 2-3 decades. The focus is on defining a geometry that performs the required optical function, by defining mask patterns that are used to fabricate the chip. This method is still very successful because often a lot of optical functionality can be implemented in a single device or building block (e.g., a diffraction grating can perform a demultiplexing of many wavelength channels), and because an optimized geometry often gives the best performance for a given function in terms of footprint, power consumption, and optical losses. Often, device design constitutes the largest design effort in the overall chip design process.

As the need for photonic chips with more complex functionality grows, it becomes harder to construct a monolithic geometry that implements the entire function, and the dimensions of the geometry become unwieldy large for electromagnetic simulations. Circuit design is changing this, but as the performance of circuits is largely determined by the performance of the individual devices, it is important to be aware of the methods used for device design, and we briefly discuss this in the next section.

#### 3.1. Device Design (Physical Design)

In a photonic device, the light is controlled by the distribution of the optical materials. In the case of silicon photonics, this translates into the geometry of the silicon, germanium, dopants, metals, and dielectrics. To accurately design an optical device, the geometries of the materials need to be optimized, and their effects need to be simulated. This is done by calculating the propagation of light waves through the geometry, using electromagnetic modeling techniques such as *finite difference time domain* (FDTD) [59], *eigen-mode expansion* (EME) [60], *finite element* (FE) [61] or *beam-propagation method* (BPM) [46]. These are still the preferential methods when new geometries are explored. Photonic devices can have a wide variety of geometries, including simple waveguide components [62], highly regular photonic crystals [63], and even optimized but irregular looking geometries [64–71]. When thermal, electronic, and even nanomechanical effects are taken into account, these devices need to be simulated in multiple physical domains. Such simulations are extremely resource intensive (in terms of simulation time and processing power), and optimizations require iterative processes with many simulations, even when using efficient techniques like adjoint sensitivity analysis [72, 73] for example in topology optimization [74, 75], or when using non-gradient approaches like Kriging [76].

Optimizing the actual detailed geometry gives the designer an enormous degree of freedom to improve a device's footprint, power consumption and optical performance (e.g. insertion loss, filter linewidth, cross-talk). Especially in silicon photonics, with its high index contrast, the manipulation at the nanometer level can significantly impact a device's

performance (e.g., shift the resonance wavelength of a filter or resonator). However, this also makes devices especially sensitive to stochastic variations in the fabrication process due to wafer thickness variations, lithography effects, pattern density affecting the etching plasma density, etc. [77, 78]. Better fabrication processes using immersion lithography [8] or thickness-corrected wafers [7] produce higher-fidelity geometries, but device designers will always have to take into account the ‘last nanometer’ sensitivity [8]. That is why tolerance analysis, mostly to linewidth and thickness variations, is becoming an increasingly important aspect of device design [79, 80].

Photonic devices eventually need to be fabricated and embedded in a larger circuit. Most physical simulation tools therefore already have functionality that imports the fabrication layout files in GDSII format and converts them into a physical representation of the component. Such *virtual fabrication*, particularly when lithography effects are included, is an essential aid for exploring the design space of photonic components, as it enables the designer to start from (parametric) layouts that later need to be used as circuit building blocks. Also, some photonic circuit design tools integrate with electromagnetic simulators to automatically run simulations of building blocks [49, 81].

#### 3.2. Circuit Design and Simulations

Device design techniques are computationally very intensive and do not scale well for larger geometries. In a circuit, the individual devices are abstracted into behavioral responses between input and output ports. These circuit blocks are then connected together to obtain even more complex behavior.

Historically, photonic circuits have been fairly simple, consisting of a few tens of devices. This makes it possible to capture the entire complexity of the circuit in a paper sketch or Powerpoint slide. Even larger circuits, such as multi-channel transceivers, are just parallel repetitions of a more simple circuit.

There are several dedicated photonic circuit design tools that allow the schematic creation of a photonic circuit [82–88]. Their adoption is growing, but in practice they are still only used by a small fraction of the photonic chip designers. While these tools offer circuit simulation capability, designers still often rely on custom home-grown simulation algorithms coded in Matlab or C++, solving transfer matrix equations or time-step simulation.

We can discern two classes of optical circuit simulation: *Frequency domain* and *time domain*. Frequency domain simulations calculate the linear response between different optical ports of the circuits, as a function of wavelength. This information is encoded in a scattering matrix. Such circuit simulations are especially useful to calculate the response of wavelength filters or other interference-based devices, and can give a good impression of the insertion losses of a larger circuits. Linear frequency domain simulations can be very efficient.

Time domain circuit simulations solve the response of a circuits to a time-variant stimulus in one or more input ports.

This is done by passing signals between the circuit blocks, and calculating the response of the individual blocks at each time step. The optical signals are usually complex numbers, a so-called *analytic signal*, encoding the amplitude and the *optical phase* versus time [89]. Depending on the application, a physical waveguide connection can simultaneously carry many optical signals in different eigenmodes at different wavelengths.

The quality of optical circuit simulation today is not limited by the capabilities of the circuit simulation tools. Rather, a reliable circuit simulation requires models for the individual circuit blocks that represent the real device with sufficient accuracy, and can be evaluated in a minimum of time. For frequency domain simulations, this means an accurate wavelength response (often in phase and amplitude) between all input-output ports. For time domain, this requires a set of governing equations (e.g., a state-space model) that captures the physics in the device. Generating such compact models from physical simulations can be extremely time-consuming, and reliable parameter extraction from measurement is far from trivial. As will be discussed in section 5, the creation of good compact models is one of the main obstacles for the scaling of photonic circuit design.

Time domain models for passive linear components can be derived from the frequency response by deriving a corresponding linear filter model, either with a *finite impulse response* (FIR) or *infinite impulse response* (IIR). This can be done for all linear building blocks individually, or by treating entire linear subcircuits as a single filter element [90–92]. This latter approach can significantly reduce the time-domain simulation time and improve its accuracy [93], but limits the introspection of signals inside the circuit.

To assess the yield of a circuit after fabrication, a sensitivity analysis is needed. This is far from an established practice, mainly because the preferred technique is a Monte-Carlo analysis, which requires a large number of circuit simulations. Worst-case/best-case simulations (also called a corner analysis) takes fewer simulations, but are less representative for a photonic circuit, for two reasons: 1) In electronics, the meaning of *better* and *worse* is usually quite clear (*better* corresponding to lower resistance, faster switching times, etc.). For photonic building blocks the concepts of *better* or *worse* are less straightforward to determine. While some functional metrics for building blocks can be measured like this (e.g. *insertion loss*, *modulation efficiency* for modulators, or *responsivity* for photodetectors), other critical parameters for building blocks, such as the *effective index* of a waveguide or the *resonance wavelength* of a ring resonator do not have an intrinsic *good* or *bad* value. Rather, the impact of changes in such variables is often due to deviations of the design value (in either direction) or mismatch of the values between two or more components. 2) A corner analysis simulation assumes that all components in a circuit are thicker/thinner, but this assumption ignores the manufacturing mismatch between components that plays a dominant role the yield of photonics integrated circuits. For example, a lattice MZI filter spectrum depends strongly on waveguides being precisely phase matched, and a corner analysis

neglects the differential phase errors. In contrast to a corner analysis, the impact of effective index variations can be very well captured using Monte-Carlo simulations [94]. This is discussed in more detail in Section 5.1.

### 3.3. Circuit Layout

Today, photonic circuit design is still often considered equivalent to circuit layout. Originally, photonic circuits were manually laid out as a single non-hierarchical layout consisting of many polygons. However, over the past 10 years hierarchical layout has become commonplace. The layout is built out of reusable hierarchical cells where some parts of the geometry can be parameterized (so-called PCells).

To define optical connections in the layout, the designer should draw waveguides. This is less straightforward than it seems, as waveguides should respect a minimum bend radius and spacing. Some photonic design tools offer tools that facilitate waveguide creation, either by automatically calculating the shape between two ports, or by generating the shape from a simple path drawn by the user [53, 95, 96]. Placement and routing is still a very manual process, where, if needed, dedicated waveguide crossings need to be added.

PCells are usually defined in a scripting language. This can be a proprietary language such as SKILL [97], Ample [98] in Mentor Graphics Pyxis, SPT in Phoenix Software [99], or an established standard language such as Python, which is used in IPKISS [100, 101], KLayout [96, 102], and Synopsys PyCell Studio [103], Tcl, used by Synopsys and Mentor Graphics or Matlab [104, 105]. Even with standard languages, code will be specific to the *application programming interface* (API) of the particular tool (e.g., Python code to add a polygon will differ between tools as there is no standardization).

Based on the design parameters, PCell code generates a set of geometric primitives on different mask layers. The resulting hierarchical layouts are saved as a GDSII or OASIS file compatible with most mask design tools.

### 3.4. Verification

Once a circuit layout has been created, it should be checked against potential errors. Today, the main automated verification process consists of a *design rule check* (DRC), where the layout is checked against design rules provided by the fab. This includes specifications on minimal line/space widths, sharp angles, or overlap of layers that might cause bad or unpredictable results during processing. This (DRC) is usually performed with verification tools designed for electronics, such as Mentor Graphics Calibre [106], Synopsys IC Validator [107] or Cadence Physical Verification System [108], or open source tools such as KLayout [102]. Such checks often reveal hard-to-detect errors, such as small misalignments between waveguides. Most fabs providing fabrication services to externals [4] provide verification decks to designers and require that designs are '*DRC clean*' before they are submitted for fabrication.

However, because photonic geometries differ significantly from rectangular electronic geometries, automated DRC is not always trivial, and often results in false positives. Recent developments with new DRC rules aimed at curvilinear structures and all-angle polygons have steadily been improving this process [109].

A second level of verification should validate the circuit design at the **functional level**, to verify connectivity. For this, the layout should be compared to the original design intent of the abstract circuit. This type of verification is known in electronics design as *layout versus schematic (LVS)*. Because the photonics circuit layout process has historically been disjoint from the circuit simulation process, it is largely the responsibility of the designer to make sure that the correct components (and their parameters) are used, that they are properly connected, and that waveguide length differences are properly matched. This is one of the most error-prone aspects of today's design processes, and it is mostly guaranteed by good discipline in data management and peer review of designs. A partial solution is the verification of waveguide connections in a layout, even without the presence of a schematic, by checking if the waveguide end points are properly aligned and connected to components (connectivity verification). From this connectivity information, a connectivity map or *netlist* can be extracted, which can be used for post-layout circuit simulation; these simulation results can be compared with original circuit simulations and verified against the design intent [53, 96].

### 3.5. Tape-out and Mask Preparation

When the mask layout is sent to the fab for fabrication, the geometric patterns are usually adjusted so they can be written onto a photomask, or in the case of e-beam lithography, directly onto the silicon chip. In this step, the geometric primitives are *fractured* into smaller polygons, and depending on the writing strategy all geometries also need to be rasterized/staircased to a fine grid [97]. This process can have some influence on the quality of the patterns, especially in photonic layouts with many curvilinear shapes. This discretisation and stair casing can lead to variations in waveguide width (changing the optical propagation constants) or increased roughness and hence propagation loss. This is particularly evident in electron beam lithography. In fabrication processes using optical lithography (or deep UV lithography) the imaging process acts as a spatial low-pass filter smoothing out the short-range stair casing, reducing the roughness-induced losses and back scattering.

### 3.6. Process Design Kits (PDK)

In the past decade, the concept of a PDK for silicon photonics has become commonplace. However, the actual implementation of a silicon photonics PDK can differ strongly from fab to fab. The first PDKs for silicon photonics consisted of little more than a design manual describing the mask layers to be used and how these would translate into an

on-chip geometry. In essence, they allowed for device design on an existing fabrication process. This was complemented with a simple design rule verification deck that checked the mask layout for minimum linewidths and spaces.

Today, photonic PDKs have expanded to enable circuit designers in their current layout-oriented design flow. fabs supply a library of elementary building blocks, such as waveguides, grating couplers, splitters, modulators and photodetectors that designers can reuse and combine into circuits. At minimum, these PDK components contain the geometry of the components, with an indication of their input and output ports. Sometimes, these geometries are obfuscated (so-called *black-box* components) in situations where the fab considers the internal layout of the component as proprietary intellectual property. While most building blocks are static, some PDKs already support *parametric cells* (PCells), where the designer can adjust parameters. Today, these are mostly geometric parameters, such as the length of a phase shifter or the shape of a waveguide.

While static PDK cells are easily portable between design tools (e.g., in the form of an annotated GDSII file), parametric cells are usually bound to the specific implementation of a single design framework. Therefore, to support multiple tools, a fab needs to invest in the creation and maintenance of multiple PCell libraries.

Until very recently, most public PDKs did not include device models that the circuit designer could use to simulate the performance of larger circuits. Usually, the model data for a number of basic performance parameters (e.g., insertion loss for a coupler, responsivity and dark current for a photodetector) are provided in a specification sheet or documentation, leaving it up to the designer to implement a model in their preferred simulation tool. This situation is changing, and more PDKs now come with basic models for the essential building blocks, capturing at least the ideal behavior of the component.

Apart from PDKs provided by foundries, many design groups maintain their own component libraries with internally developed device designs. While in this case the connection between the device and circuit designer is much closer (or even the same person), the need for reliable models is still the same to guarantee a working circuit. Every device designer needs to understand and model the devices' sensitivity to fabrication. This can be done as a simple corner analysis [1], or by developing models that are continuous versus all fabrication parameters [79], so a circuit designer can perform a Monte-Carlo simulation for yield analysis.

### 3.7. Summary: PIC Design Today

The PIC design process today is a somewhat disconnected process where the main focus is on the physical layout. While concepts from electronic circuit design, such as hierarchical layout and PDKs, are already adopted, the disconnect between functional front-end design and physical back-end design makes it very difficult to scale up the complexity of circuits and verify their functionality.

## 4. The Emerging Circuit Design Flow

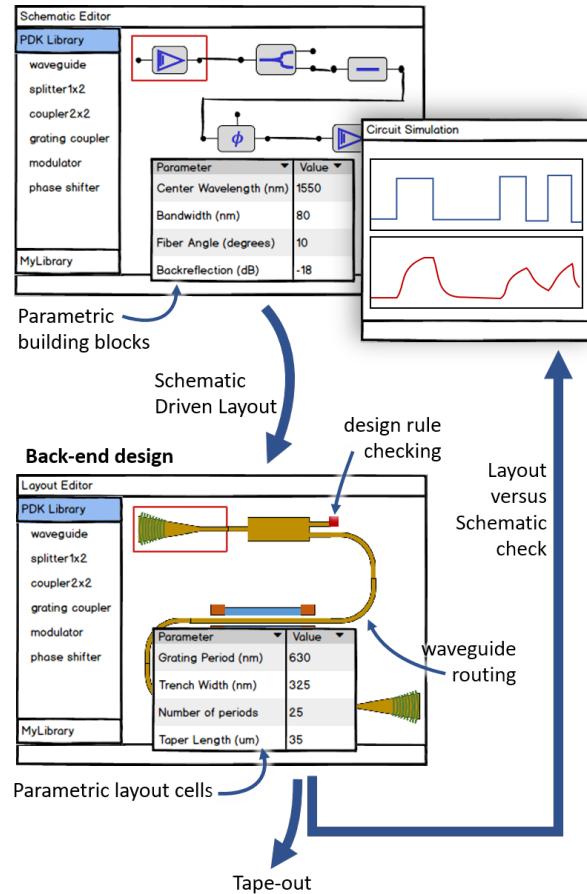
Photonic ICs have been going through a similar evolution as electronic ICs. Integration of many functions onto a semiconductor substrate, and a steady increase in the number of components integrated in a single circuit, characterize both types of ICs. In electronics, the small set of basic building blocks allowed for an early start of circuit-oriented design approaches, even before the introduction of electronic ICs. As circuit complexity increased, and the development cost for a new chip went up, the design techniques and software tools improved to guarantee designers a first-time-right result. Just as silicon photonics has leveraged the manufacturing technology of CMOS electronics, *photonic design automation* (PDA) is steadily taking up design methodologies from *electronic design automation* (EDA), and integrating with existing EDA tools, especially those for analog full-custom IC design.

The EDA design flow for analog ICs follows very rigorously the circuit design methodology outlined in section 2, also shown in Fig. 3. Based on a logical schematic, a circuit is synthesized until it meets the required functional specifications. The detailed geometry is abstracted into building blocks with a compact numerical model, and the full electromagnetic waves are replaced with signals. This is called the *front-end* design. The schematic consists of connected functional blocks, which can in turn be circuits of their own, resulting in a hierarchical description that keeps the overall complexity manageable.

The resulting circuit schematic is then handed over to the *back-end* designers that transform it into a mask layout, which is functionally compared against the original schematic and resimulated. After fabrication, the design and simulations can be compared to actual measurements and test results, which can be fed into the design of subsequent circuits.

The design flow supports the designer (or the team of designers) step by step through a process that can accurately predict the functioning of the fabricated circuit. In the hands of an experienced designer, the design flow predicts the performance even under conditions of variability in the fabrication process. The software tools manage the data handover between the steps in the design process, reducing the chances of errors. This results in chips with a high yield, i.e., a high fraction of working chips after fabrication. Techniques like *schematic driven layout* (SDL) and *layout-versus-schematic verification* (LVS) that are now being introduced in photonic circuit design are directly coming from established EDA flows.

There is also growing trend to implement photonic design directly into an established EDA tool [97, 110–113], giving the photonics designers all the tools of an electronics designer. However, as we discuss in detail in section 5, the differences between photonics and electronics make it difficult to capture some aspects of a photonics design accurately in a pure EDA tool, and workarounds/customizations are needed to approximate photonics in an electronics design environment.



**Figure 3** Photonic design flow based on existing EDA flows. The flow is separated into a front-end (using a schematic editor) and a back-end (using a layout editor). The library-based approach helps to keep the schematic and layout aligned, and allows for functional verification of the layout before tape-out.

We will now discuss how the recent developments in the photonic design landscape are driving the convergence of photonic and electronic design automation.

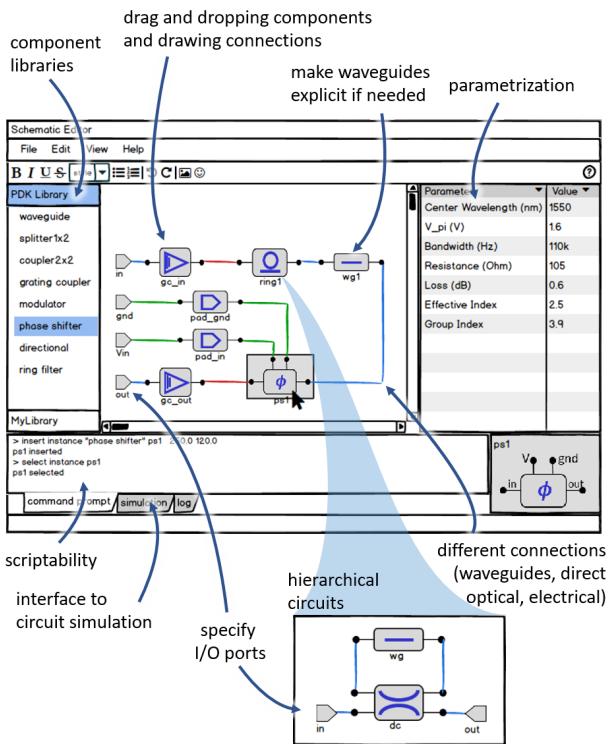
### 4.1. Schematic Capture

The first design steps of a circuit is always to capture the functional intent, and translate that into a circuit description, typically referred to as *design capture* or *schematic capture*. This is the least trivial step of the design process, as it often requires significant creative thinking. This task can be facilitated by breaking up the system or circuit into subcircuits, and composing these hierarchically. Both in electronic and photonic design tools, a *schematic editor* is used, where blocks are represented by abstract symbols and an indication of their input/output ports.

As already discussed in section 3, there are already several dedicated photonic schematic editors [82–88]. It is also possible to use the schematic editors of established EDA tools. Most schematic editors have an interface similar to the one sketched in Fig. 4. Schematic information is stored

in a database or file (*e.g.*, the EDIF file format), and contains both the logical connectivity data and a graphical representation. This latter data is purely for the convenience of the designer, as it communicates no functional information. The logical connectivity information is called the *netlist*. It can be expressed in different formats, such as EDIF, SPICE or tool-proprietary file formats, or in a database. This contains a list of the building blocks with their parameters, as well as the *nets* and the ports to which they are connected.

The blocks are connected by signal lines. In this formalism, signals are transmitted instantaneously. This means that optical waveguides, which introduce phase or time delay, dispersion or loss, should eventually be represented as individual building blocks.



**Figure 4** Anatomy of a typical schematic editor used to define circuits: Symbols are placed and connected, both electrically and optically (either with explicit definition of waveguides or implicit). Components can be parameterized and hierarchically broken down in subcircuits.

A good schematic capturing tool supports the designer in detecting inconsistencies in the circuits, such as disconnected ports, nonsensical parameters in building blocks, and improper connections. For instance, in a mixed photonic-electronic circuit, the schematic capture tool should differentiate between the photonic and the electronic signal lines, and make it impossible to connect an electrical net to an optical port.

While most photonic circuits can be conceived as a purely logical schematic, many photonic designers are more comfortable capturing the circuit schematic as something that is closer to the physical layout. As we will discuss in

section 4.3 and 4.5, this makes more sense for photonics with its more stringent routing and packaging restrictions. Several tools therefore offer the opportunity to use a layout editor for capturing schematics, drag-and-dropping components and connecting them with logical and physical waveguide connections, that can then be simulated as a circuit as if it were defined in a schematic editor [53, 96].

## 4.2. Circuit Simulation

Once a design is represented as a circuit, its behavior can be simulated. This requires, of course, that all elementary building blocks (*i.e.*, blocks that do not consist of a subcircuit themselves) have a compact model that describes the response between the input and output ports. When designing circuits, it would rapidly become impractical to simulate the actual electromagnetic fields in the building blocks, as is done in the device design stage. During circuit design, the physical electromagnetic simulations need to be replaced by much more efficient compact models that capture the device’s *behavior*, without simulating the detailed physics.

For analog electronics, which most resembles today’s photonic circuits, the circuit simulation is usually based on a variation of SPICE, using a technique called *modified nodal analysis* (MNA) that relies on Kirchhoff’s conservation laws for voltage and current [114]. This is called the *effort-flow formalism*. The building block models are usually implemented as a *SPICE* subcircuit or a *Verilog-A* coded model.

Unlike other physical domains such as mechanics and fluidics, photonic circuits cannot be described with the effort-flow formalism. Optical signals are waves travelling along waveguides, and due to reflections, propagate in both directions. Waves oscillate with a given wavelength and frequency, and at any given time can be defined by an amplitude and phase. When considering multiple light paths, the interaction needs to be added as a phasor to include optical interference effects (coherent), rather than as a scalar quantity (voltage or current) as in electronics.

Today, the common signal representation on a photonic signal line is an *analytic signal* [89], *i.e.*, a complex number describing the amplitude and phase modulation of a single-tone carrier wave propagating on a single waveguide mode/polarization. While a photonic circuit described by the scattered wave formalism can be mapped onto an equivalent circuit described by MNA [115, 116], this is not a natural way of representing a compact model for a photonic building block.

The mismatch between photonic signals and electronic signals make it difficult to model both together rigorously in their native formalism within the same simulation environment. There are currently four approaches to this, illustrated in Fig. 5:

- **Simulate photonics and electronics together in a photonic circuit simulator.** This is already possible in different simulators [82, 83, 86–88], but this would force electronic designers to abandon their trusted SPICE simulation environment. Also, the photonic circuit simulators

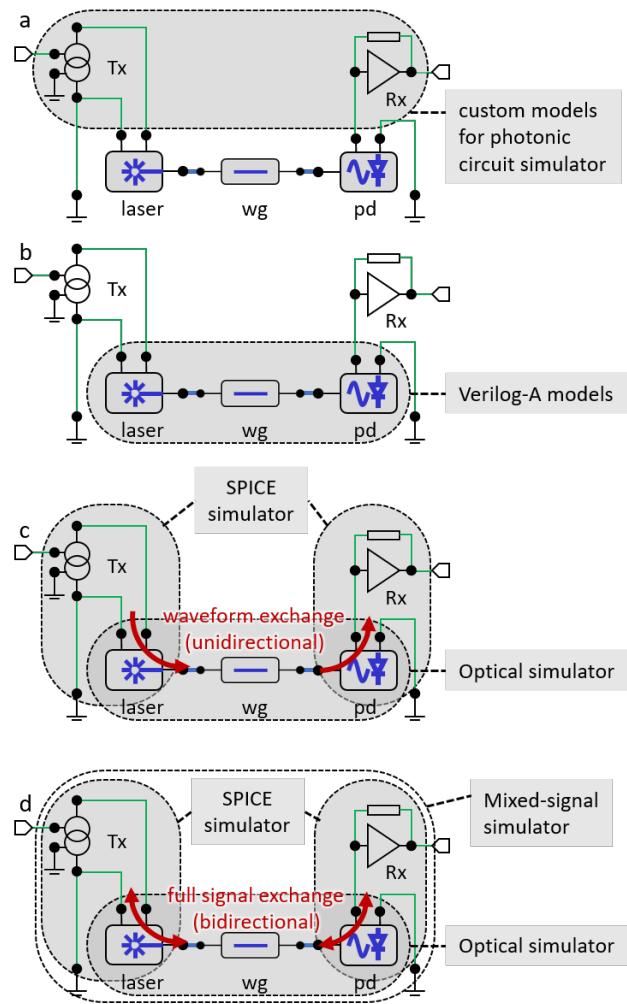
are not as efficient for the simulation of large electronic circuits and do not necessarily support the models for the electronic building blocks and CMOS foundry-provided PDKs.

- **Simulate photonics and electronics together in an electronic circuit simulator.** Designers have already successfully implemented photonic circuit models in Verilog-A, mapping photonic quantities onto internal electronic quantities [110, 117]. This approach already provides a working environment where mixed electronic-photonic circuits can be designed and simulated for a subset of applications, but as we will discuss in section 5 and 6, there are limits to the photonic phenomena that can be captured with this technique.
- **Partitioning and simulation using separate electronic and photonic circuit simulators.** In this approach, the circuit is split into electrical and optical partitions, and a flow of information is defined (*e.g.*, from transmitter to receiver). The parts are simulated in the right order over the complete time domain, and the output signals of one partition are fed as inputs to the next (waveform exchange). This technique leverages the strengths of the particular simulators, but it is not possible to simulate circuits that operate in both directions or that have feedback loops between the optical and electronic partitions.
- **Co-simulation using separate electronic and photonic circuit simulators.** In this approach, the simulators are operating in lockstep (slaving one simulator to another) and the signals are exchanged and converted between simulators. Such a technique is already established in electronic for mixed analog/digital circuits (*analog-mixed signal* or AMS), and is being developed for photonics [118].

The circuit simulations are usually run in an iterative process with schematic capture, until the circuit has the desired performance. It is important in this stage to introduce estimates of the variability to obtain estimates of the yield of the circuit after fabrication. In electronics this is done through *corner analysis*, where the circuit is simulated in a best case (fast transistors) and worst case (slow transistors) scenario. As described in Section 3.2, in photonics, this concept of fast and slow is not applicable, and therefore more generalized *Monte-Carlo* simulations need to be used [94, 119].

### 4.3. Circuit Layout

The translation from a circuit schematic to a circuit layout marks the handover between front-end design and back-end design. Circuit layout requires a similar but still different tool set than the schematic capture. A mock-up of a typical layout editor is shown in Fig. 6. The layout is represented hierarchically, mostly corresponding to the hierarchy in the circuit schematic. A significant improvement in design productivity comes from *schematic driven layout* (SDL). This technique comes from analog electronic design, where the hierarchy and connectivity in the schematic is used to prepopulate the photonic circuit layout with building blocks

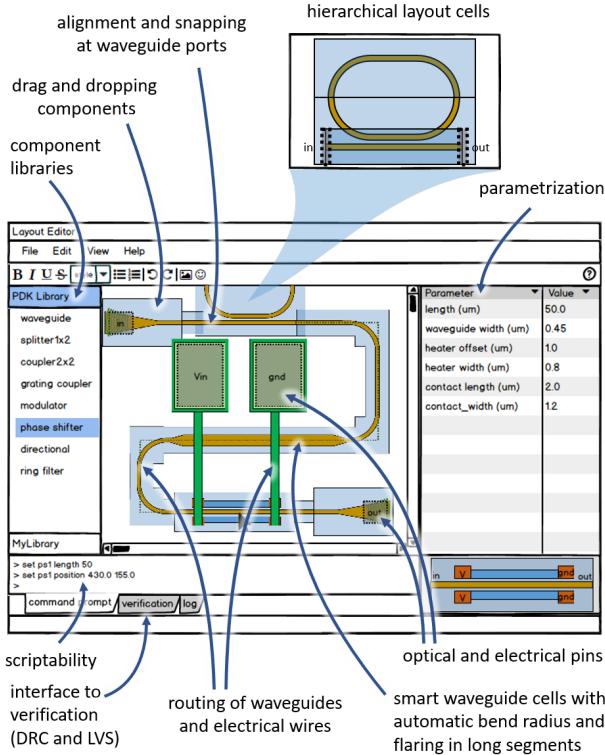


**Figure 5** Techniques for electronic-photonic co-simulation. (a) Running electrical models in an optical simulator. (b) Running photonic models in an electrical simulator. (c) Sequentially running electrical and optical simulations and exchanging waveforms. (d) Mixed-signal co-simulation where photonic and electronic simulations are running in lockstep, continuously exchanging signals.

and indicative connection lines (flylines). This makes it much easier for the layout designer to connect components together.

SDL is also finding its ways in photonics, but defining the optical waveguide connections is less straightforward than drawing electrical wires that are usually oriented along Manhattan directions (*i.e.* along X or Y-axis) with changes in direction implemented as sharp 90° corners. In contrast, waveguides should respect a minimum bend radius and spacing. For this, photonic design tools offer tools that facilitate waveguide creation, either by automatically calculating the shape between two ports, or by generating the shape from a simple path drawn by the user [53, 95].

Fully-automatic routing of optical waveguides connecting photonic components is not trivial. While this has become commonplace in electronics, photonic routing is complicated by the fact that there is generally only a single



**Figure 6** Anatomy of a typical layout editor used to place circuits: Schematic-driven layout tools can pre-place the components from the schematic, and automatic or assisted routing tools can route the waveguides and electrical wiring. The circuit illustrated corresponds to the circuit shown in Fig. 4.

optical waveguide layer, in contrast with the many metal layers available in electronics. Furthermore, modern CMOS processes required certain metal layers to only be used for X direction interconnects and others only for Y direction interconnects. This greatly simplifies automated routing of electrical interconnects. In single layer photonics there are often no solutions without the need for waveguide crossings. Therefore, a photonic router should be able to assess possible topological conflicts, and if necessary introduce optimized waveguide crossings.

As already mentioned, connection waveguides between optical building blocks cannot be considered as perfect. Therefore, they are usually represented as a building block in the schematic, and as a PCell in the layout. The layout generation in the waveguide PCell should take into account the bend algorithms with a minimal radius, and can incorporate additional optimizations such as broadening in straight sections [120, 121]. To keep the schematic and layout information coupled, the data cannot be just stored in a simple GDSII or OASIS layout file. Therefore, the parametric cells, including their different views, are stored in a database such as *OpenAccess*, which can be read by the different tools in the design flow, and a back-annotation is needed so the schematic circuit can be updated with the actual waveguide parameters.

#### 4.4. Layout-Aware Circuit Design

It is not always possible to fully decouple the front-end (schematic) and back-end (layout) design of a photonic circuit. Given that for most silicon photonics technologies there is only a single interconnecting layer, layout constraints often dictate the possible circuit topologies. While it is obvious that physical layout parameters can strongly dictate circuit performance, the layout parameters also have an influence on how circuits are connected, and what functionalities can be implemented. Therefore, design solutions are emerging where a strong coupling between layout and schematic views allow the design to rapidly construct interconnected photonic circuits while iteratively incorporating information from the circuit layout [122]. An alternative is defining the logical connections directly in a layout view, thereby reducing the exchange between two different tools [53].

#### 4.5. Design for Packaging

The layout of the circuit not only translates the logical representation of the circuit into a physical one, but it also defines the actual optical and electrical input and output interfaces. These introduce a number of constraints coming from the packaging and characterization requirements, such as the orientation and spacing of fiber couplers (either edge couplers or vertical grating couplers), and the pads for electronic wire bonding or flip chipping (often with the need for high-speed signals). The combination of optical and electrical interfaces reduces the degrees of freedom for the overall circuit layout.

To support this, design tool vendors are collaborating with packaging service providers to provide packaging templates or design frames with standard positioning for the optical couplers and electrical pads, alignment fiducials and even active optical alignment structures for fiber arrays.

#### 4.6. Verification

Design rule checking for photonics is systematically improving, taking into account the curvilinear nature of photonic waveguides. New DRC algorithms look deeper into the design intent [123]. For instance, the linewidth of a discretized waveguide polygon is compared to the desired linewidth over the entire length of the waveguide, and excessive width variations are reported [124].

A second level of verification looks at the functional behavior of the layout, by comparing the laid out hierarchy with the hierarchy in the schematic. This *layout versus schematic* (LVS) step requires that an equivalent circuit is extracted from the layout, including the parameters of the individual subcircuits and building blocks [124]. The connectivity between all the blocks should be verified. A good optical connectivity is different than a good electrical connectivity. While for the latter only a shortcut between metal layers is needed, optical ports must be properly aligned (position and angle) and of the same waveguide type to avoid

reflection or scattering. Also, LVS should check against unintentional waveguide crossings and close proximity of waveguides or components that could lead to parasitic coupling or reflection.

After verifying that the physical layout matches the schematic, a *post-layout simulation* is required to: 1) include effects not captured in the original schematic, such as the precise waveguide lengths, and 2) as a verification step to double-check that the circuit is correctly drawn. LVS tools can already extract a logical circuit from a layout, either from the GDSII file with annotations [96, 98], or a layout created using an OpenAccess database [53]. If the identified building blocks have associated circuit models, the entire circuit can be simulated and compared to the original schematic design.

#### 4.7. Process Design Kits (PDK) and Libraries

What makes PDKs successful for full-custom analog electronics design is the inclusion of reliable compact models for all the qualified building blocks in the process. This way, designers are sure that whatever circuit they design with those blocks can be simulated, and that this simulation is representative for the eventually fabricated chip.

Photonic PDKs are steadily moving towards this point, with some design kits already including basic compact models for one or more simulation tools. However, even though the need for such compact models is generally recognized, this inclusion is a slow process. As we will discuss in 5, this can be partially attributed to the prohibitive amount of work needed to develop models for the different tools.

#### 4.8. Summary: The emerging circuit design flow

There is a strong momentum to migrate the photonic circuit design flow to one resembling the electronic design flow, and to integrate photonic tools with established EDA tools. An overview of these integration efforts is shown in Table 4.8. It will then become easier to define hierarchical circuit schematics and simulate them, even in mixed photonic-electronic circuits. Techniques such as schematic-driven layout and assisted routing significantly reduce the chances of errors in the conversion process from schematic to layout, and verification techniques enable circuit extraction so the final design can be verified against the original intent.

### 5. Challenges for an integrated photonic design flow

As circuit-oriented (and EDA-based) design flows are gradually being adopted, a number of challenges are becoming more clear. These are now, or will soon be, limiting the scaling of the complexity of silicon photonic circuits, both in the front-end and in the back-end of the design flow. The current flows are also limited in applicability: as the PIC market

Photonic Design Tools					
Phoenix Software † [99]	[118]	*	*		
Lumerical † [82, 125]	[118]	[54]	*		
Luceda Photonics [86]			[55]		
VPIphotronics † [83]		[126]	*		
Photon Design † [85]					
Synopsys (RSoft) † [88]					
Optiwave † [127]					*

Electronic Design Tools					
Cadence Virtuoso/Spectre					
Mentor Graphics Pyxis/Eldo					
Mentor Graphics Tanner L-Edit/S-Edit					
Synopsys IC design tools					

† Member of the *PDAFlow* foundation [128].

\* Known collaboration, unpublished in a conference/journal

**Table 1** Overview of current interfaces and collaborations between mainstream EDA tools/vendors and Photonic Circuit design tool vendors.

today is largely driven by communications, the emerging design and simulations tools are primarily supporting these applications. But there are numerous other applications in sensing, signal processing, spectrometry, and quantum information processing that cannot be captured with the design paradigms of transceivers or switch fabrics.

Both for the scaling of complex circuits and new applications, we identify some of the key challenges in the realm of design automation:

- **Capturing the effects of variability** to enable accurate yield prediction: silicon photonics is so sensitive to small perturbations that this will become an integral aspect of large circuit design. But there are as yet no efficient techniques to adequately simulate large circuits while taking into account variability. This should translate into *design for manufacturability* (DfM) strategies for photonics.
- **Circuit and signal representation** for photonic circuits to accurately capture wavelength dependence, nonlinear effects, etc. This is necessary for applications that are not satisfied with simple single-wavelength linear circuit, especially where significant optical power densities are used.
- **Building reliable compact models** that can also be qualified against fabricated structures, including the characterization methodologies for experimental parameter extraction. These models should include manufacturing variability.
- **Photonic-Electronic co-design**, similar to analog-mixed signal approaches in electronics. This includes co-simulation but is also influenced by different photonic-electronic integration strategies.
- **Photonic Routing**: There are currently no good solutions for automated routing of large photonic circuits.

For larger circuits, manual routing will become an intractable problem.

In the following paragraphs we go into detail on some of these challenges.

### 5.1. Yield Prediction

The objective of a circuit designer is to create a working chip, taking into account the effects of the actual fabrication process. An accurate prediction of the fraction of fabricated chips that are actually going to perform as intended (*i.e.*, the yield) is essential to make a cost assessment. For example, in datacommunication transceivers, a yield analysis would determine the percentage of chips that will have ring modulators yielding links with a bit error rate below a threshold value [129]. In a photonic circuit, every building block will have a response that is somewhat different from the ideal. The effect of these non-idealities accumulate as signals propagate through the circuit. A variability analysis that extends the variability at the device level to the circuit level is needed to predict the likelihood that a chip will work as intended. To come to *uncertainty quantification* for photonic circuits, the variability needs to be mapped at various levels of abstraction, as shown in Fig. 7:

- **The effects that affect the performance of the individual devices** need to be known. For instance, the effective index of a waveguide is affected by the linewidth, layer thickness, etch depth of the silicon, but also by internal stresses and the refractive index of the deposited cladding on the side and on top. And parameters such as linewidth are influenced by process parameters such as photoresist thickness and lithography dose (and variation thereof), but also by the position on the chip and the pattern density of the surrounding structures. Some origins of variability are more deterministic than others. Waveguide thickness in silicon photonics is mostly determined by the host wafer, and the variation on the wafer has a length-scale of centimeters [7, 79]. Linewidth variation is more dependent on the direction of the waveguide and the neighboring patterns and can exhibit a variation on a much shorter length scale. These parameters can be correlated between dies, wafers and lots (Fig. 8), but this requires the collection of data at every step in the fabrication process. Also, there is always an uncertainty on the collected data (*e.g.*, linewidth measured with a SEM) which complicates this analysis.
- **The statistics of the device performance** need to be known. These are either directly measured or mapped from the lower-level parameters. For instance, the effective index  $n_{\text{eff}}$  is measured directly, or derived from a linewidth/thickness map of the wafer. Ideally, both are collected and correlated. Performance of a device cannot always be captured in a single metric, and different building blocks have different metrics that respond in a different way to the lower-level fabrication parameters. In electronics, this mapping has been reduced to a best-case and worst-case situation, in the form of ‘fast’ and ‘slow’ performance corners for the individual transistors. Fast,

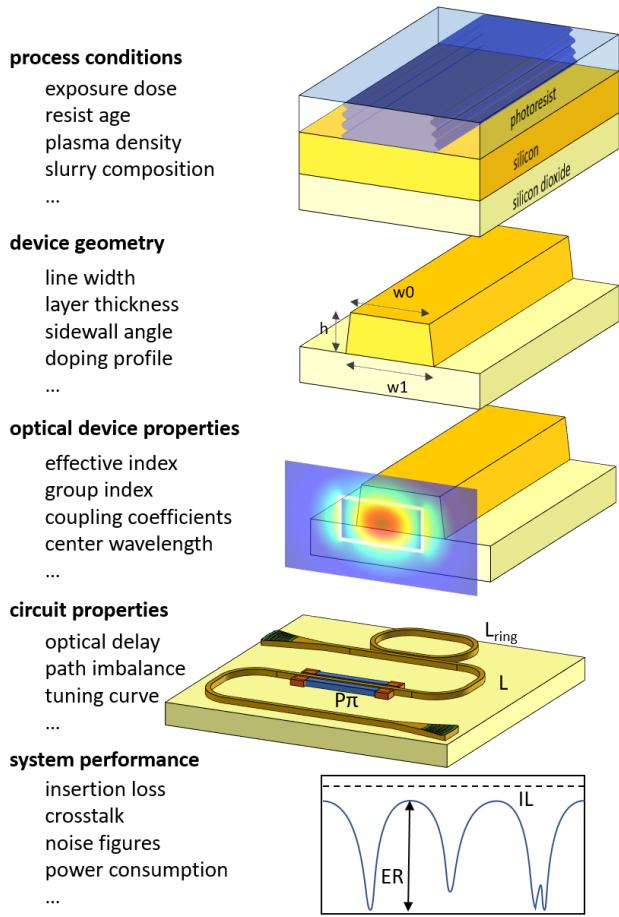
nominal and slow devices have their own device models that can be used in a circuit simulator. In photonics it is not possible to define such a one-dimensional criterion. While some device characteristics can easily be interpreted as a measure for performance (*e.g.*, waveguide propagation loss, photodetector responsivity), other metrics such as coupling coefficients or effective index do not carry an inherent performance meaning but will significantly affect the performance of a circuit.

- **The circuit performance statistics** need to be derived from the functional device statistics, to evaluate where a circuit will perform as intended. In electronics, this is evaluated through a ‘corner analysis’, where best-case (fast) and worst-case (slow) performance is tested. Today, corner analysis is gradually being replaced with full Monte-Carlo simulations where a performance distribution between slow and fast transistors is used. This should take into account the correlation between devices within a circuit: devices that are closer together will be more likely to have similar parameters than devices that are further apart [77]. This knowledge can be used to optimize circuit designs that require properly matched devices. The same techniques can be applied to photonics, but there the number of parameters can be much larger, requiring a large number of Monte-Carlo iterations.

This mapping at different levels requires models that are continuous in the variational parameter space, not just a model for the nominal design parameters, or for performance corners. For instance, a continuous model that maps the waveguide’s effective index onto the local width and thickness is needed. Such models should also come with suitable parameter extraction test devices and algorithms that allow a monitoring and mapping of the variability. When using interpolation techniques, care needs to be taken that the interpolations conserve physical properties like passivity, stability and causality [1, 130, 131].

The most simple simulation approach to map a multi-dimensional probability distribution of a parameter on a lower level (*e.g.*, width and thickness) to the distribution of a performance metric on a higher level (*e.g.*, rejection ratio of a wavelength) is the use of Monte-Carlo simulations [119]. In this technique, the higher-level circuit is simulated based on a randomly selected set of parameters at the lower level. To estimate the impact on the performance of a circuit with multiple building blocks, it is important that the correlation of the parameters in the Monte-Carlo simulation is properly captured. Many optical functions, such as wavelength filtering, depends strongly on the matching of parameters (*e.g.*, effective index or coupling coefficient) between components. As in electronics, nearby components are more likely to have matching parameters than components separated over a large distance on the chip [77, 132, 133]. Also, the environment of the components should be similar, as local pattern densities can also affect device parameters [78]. Recent developments have demonstrated location aware Monte-Carlo simulations, where parameter variations are generated as a location-dependent ‘virtual wafer map’ [79, 134].

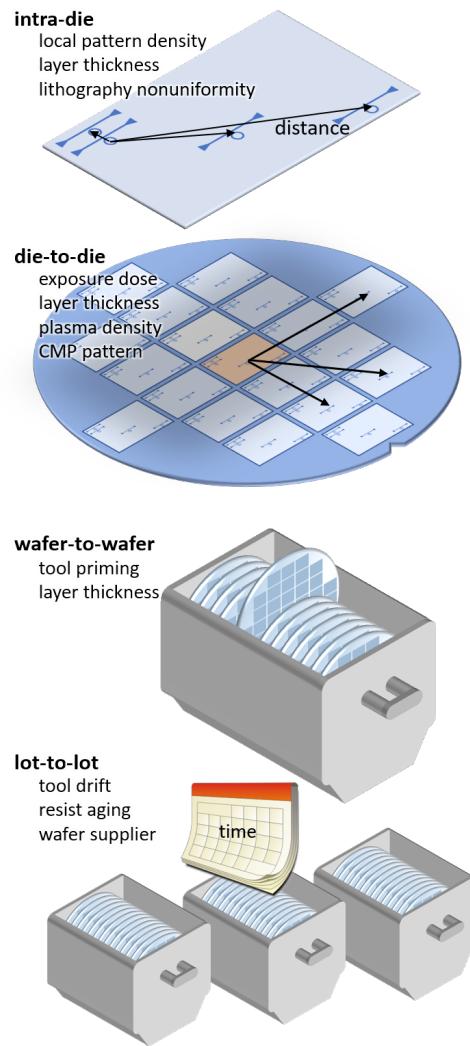
In Monte-Carlo analysis, the system is simulated many times (tens of thousands) [119]. If simulations are computa-



**Figure 7** Variability at different levels of abstraction: Fabrication parameters, geometric parameters, optical device parameters, circuit properties, performance metrics.

tionally expensive (*e.g.*, FDTD or FE for devices, or even large circuit simulations), this requires a prohibitive amount of time. Computationally efficient compact models suitable for Monte Carlo simulations need to be developed where the model is continuous within the realistic parameter space and where expensive device computations are no longer required for each Monte Carlo iteration [79]. This is the same for electronics and photonics. New statistical methods are emerging that can significantly reduce the amount of simulations. In *stochastic collocation*, a surrogate statistical model is generated from a small set of expensive simulation, capturing the distribution of the lower-level parameters, and making it possible to cheaply evaluate the system in a Monte-Carlo simulation [135].

It is also possible to expand the parameter space of the design into a set of parameters that captures not just the nominal values, but also the statistical moments of their distribution. In *polynomial chaos expansion* (PCE), the system model is replaced with a higher-order model where the distribution of the low-level parameters is directly mapped onto the distribution of the performance metrics of the system [136, 137]. This technique has already been applied to map geometric parameter variations onto device per-



**Figure 8** Variability at different scales: within a single die, between dies on the same wafer, between wafers in the same lot, and between lots spread over time.

formance statistics [138, 139]. These techniques can make yield assessment more practical, to a point where the sensitivity of circuits to stochastic variations can be efficiently assessed [140] and circuits can be optimized for yield [141].

There remains significant effort needed to improve yield estimation simulations, in particular, to combine the efficient simulation techniques mentioned above, with the necessary location-dependant or distance-aware approaches that take correlations of parameters into account.

## 5.2. Design for Manufacturability (DfM)

Even with increasingly improving manufacturing technology, silicon photonic circuits will be susceptible to variability. Advanced electronics at deep submicron technology nodes suffer from the same problem. *Design for Manufacturability* (DfM) is a common denominator for techniques

that can improve the yield of a circuit or chip in the presence of imperfections and variability. For photonics, there are as yet very few established techniques to accomplish this, but we can identify three design approaches to improve robustness and yield of photonic circuits:

- Optimizing building blocks for robust behavior
- Optimizing circuits and subcircuits for robust behavior
- Introducing active compensation for imperfections

### 5.2.1. Robust optimization of devices

When designing photonic building blocks, the performance is usually optimized by modifying the geometry, either by changing geometric parameters (*e.g.*, directional coupler gap) or by optimizing the overall geometry using techniques such as topology optimizations based on adjoint sensitivity analysis [64, 74, 75, 142] to maximize the performance (*e.g.*, the transmittance) of a device.

To assess the influence of fabrication, the optimization process should include the effects of fabrication. Most photonic simulation tools now include some functionality for virtual fabrication of a device layout [81], but this does usually not include the effects of lithography. Using lithography simulation, the spatial low-pass effects that lead to corner rounding can be included in the optimization loop [143, 144], as well as lithographically induced contour variations [98, 145].

In robust optimization, the optimization algorithms does not aim to maximize the absolute performance, but rather the performance in a window of parameters that are susceptible to variation. For instance, when a specification of variability is given (*e.g.*, linewidth or thickness), the optimization can try to optimize the design parameters to maximize the poorest performance in the window of variability [146]. Alternatively, design parameters can be optimized for minimum performance variation with fabrication, temperature, wavelength. Starting from designs that are designed to operate idiomatically, or with built-in symmetry, facilitates the process [147].

To obtain robust designs for a given component (*e.g.*, a directional coupler) it is often useful to increase the number of design parameters, providing more degrees of freedom. For instance, by varying the linewidths and gap of the directional coupler waveguides along the propagation length, the phase matching conditions can be better controlled and a more tolerant or broadband operation can be obtained [148, 149]. A variation on this scheme is the use of *sub-wavelength gratings* (SWG) which use sub-wavelength variations of the geometry to engineer the local effective optical properties of the structure. [150, 151]. The large design freedom for SWGs can be used to make more efficient, but also more robust devices [152, 153]. On the other hand, the small features of SWGs can also introduce challenges for fabrication.

Advanced optimization methods such as *Kriging* and *Stochastic Collocation*, developed for mechanical or *radio-frequency* (RF) design are now being introduced into photonic device design [76, 135, 154, 155]. These techniques

provide a rigorous framework to treat performance variability, but also help to reduce the number of expensive simulations needed for an optimization.

The optimization of photonic device geometry is currently a much-studied topic. However, the result is usually a building block with improved performance that is only a small part of a larger circuit.

### 5.2.2. Robust optimization of circuits

The optimization of circuits can happen at two levels: 1) selecting the right components, their parameters and connectivity at the schematic level, and 2) laying out the circuit on the mask. The first type of optimization is very challenging, as it requires an exploration of a discontinuous design space, and there are no automatic circuit synthesis tools that can assist the designer's creative thinking. For some types of circuits, such as wavelength filter design, synthesis techniques from electronics (digital or analog filter design) can be leveraged [18] to select the filter order or topology.

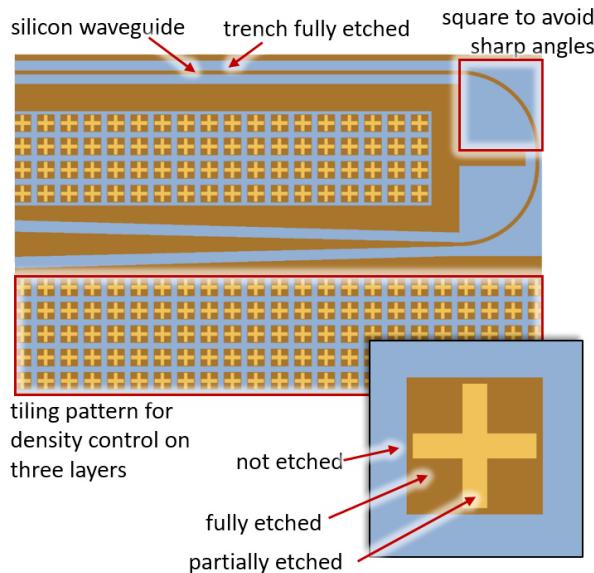
Once the circuit components and connectivity are chosen, optimization becomes a more tractable problem, and similar techniques as for device optimization can be used to optimize the circuit parameters. This also applies to robust optimization, where the circuit parameters are optimized for tolerance to a number of variations. As with device optimization, a circuit can be optimized better if the parameter space is somewhat extended. For instance, rather than using a single waveguide width for a filter delay line, using combinations of multiple widths can make filters more robust against linewidth variations, temperature and other effects [156–159]. Even though the response of all building blocks in the circuit is susceptible to fluctuations, the overall circuit is designed to cancel out these variations. This relies on the assumption that the variations between circuit components is similar and correlated.

Of course, given the nature of variability, perfect correlation cannot be assumed. But the layout of a circuit can be optimized to make this correlation as robust as possible. This device matching problem is also known in analog electronics design, and it is addressed at the layout level by

- **Positioning devices as close together as possible:** this helps to keep the layer thicknesses and local pattern densities similar.
- **Maintaining the same orientation:** As high-end optical lithography uses a step-and-scan system rather than a step-and-repeat [160], there is a small but intrinsic anisotropy in the projection system. By orienting components along the same axis, the mismatch is minimized.
- **Using so-called Manhattan geometries:** Orienting as many device facets along the X and Y direction brings two benefits: In crystalline silicon, this corresponds to crystal planes, which can give rise to a more uniform etch quality. But the main advantage is that during mask preparation, no staircasing effects will be applied. Comparisons on *arrayed waveguide gratings* show that identical devices oriented along different directions exhibit very

different crosstalk, which is a direct measure for the uncorrelated linewidth variation between waveguides [161]. Devices at Manhattan orientations (0 and 90° rotations) had the best performances, followed by devices at 45-degree angles. Performance degraded significantly for devices at arbitrary angles. Routing waveguides along Manhattan directions works well for high-contrast silicon waveguides, as bend radii of a few  $\mu\text{m}$  make sharp 90° bends possible. In lower-contrast PIC technologies, where the sensitivity to small linewidth variations is already reduced, the penalty of large bends (footprint, routing constraints) often outweighs the benefits of using Manhattan orientations.

- **Controlling pattern density:** While stacking components close together is generally beneficial for the uniformity of devices, it is also important to maintain a uniform pattern density over the chip. This provides a more uniform field of stray light during lithography, but more importantly it gives a better control over the concentration of reagents in dry etch plasmas. To maintain a uniform density, one of the final steps in the layout is the inclusion of *filler patterns* (also called *tiles*, or *tiling*). Figure 9 shows an example of a layout detail of silicon waveguides with tiling for pattern density control on a process with fully-etched silicon and partially-etched silicon.

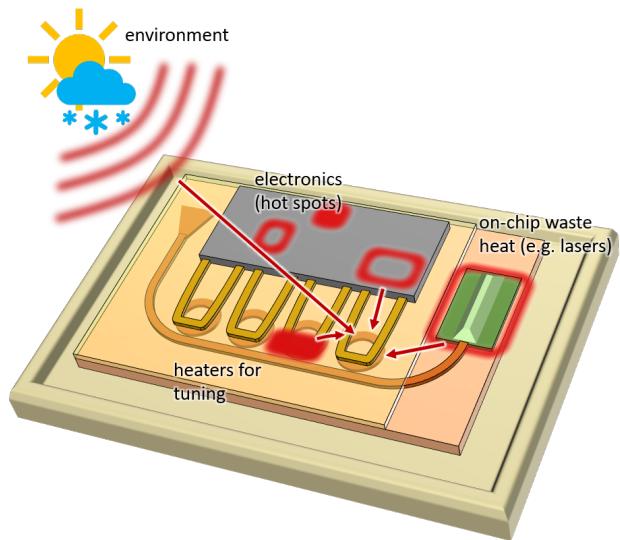


**Figure 9** Example of a layout detail of silicon waveguides with tiling for pattern density control on a process with fully-etched silicon and partially-etched silicon.

It is not straightforward to quantitatively model the impact of these effects on a circuit's performance, and therefore optimize the circuit layout for robust behavior. While it is already possible to project wafer thickness maps onto a circuit layout and predict the circuit yield [79], the effects that influence linewidth and other process parameters are not yet sufficiently known, and robust layout therefore relies to a large extent on experience and trial-and-error.

### 5.2.3. Thermal effects

Silicon photonic devices and circuits are not just sensitive to geometric variations and material composition, but also to thermal effects. Compared to low-contrast glasses [162], silicon and III-V materials have much higher thermo-optic coefficients. In wavelength filters in the wavelength band around 1550 nm, a temperature shift of 10 K gives rise to a  $\sim 1$  nm shift, which corresponds to a  $\sim 1.2$  THz shift. The effects of temperature on a silicon photonic circuit can therefore not be ignored.



**Figure 10** Thermal effects affecting the behavior of silicon photonic circuits. Influences from the environment, 'hot' components such as lasers and driver electronics, or crosstalk from thermal tuners (heaters) can propagate through various paths on a photonic chip.

Temperature variations can come in many forms, illustrated in Fig. 10

- Global (environmental) temperature changes originate from outside the chip or package. For many applications, the temperature falls in the range of 0°C-80°C, but in applications for automotive and aerospace this range can easily double. Active temperature stabilization within the package can compensate for these effects, but at the expense of significantly increased power consumption.
- Within a chip there can be temperature gradients. These can again originate from the outside, but also from spurious heat sources on the chip. The most notable components that can generate a lot of waste heat in a photonic

circuit are lasers. This is often an argument to keep lasers off chip.

- Electronics can also generate a lot of heat, and this is especially true for high-speed electronics used to drive modulators and read-out photodetectors for high-speed communication applications. Depending on how the electronics are integrated (see section 5.3), the thermal paths between the electronics and the photonics can cause significant challenges.
- Thermal effects can also be used for active tuning, by incorporating heaters. However, the generated heat needs to be dissipated. Given that silicon photonic chips reside on a silicon substrate and use metal interconnects, there can be thermal parasitic paths, giving rise to thermal crosstalk.

Being able to capture the effect of thermal variations and heat spreading at the scale of the photonic circuit will be essential in predicting circuit performance in operational settings. This requires good thermal models in the individual building blocks, but also efficient heat spreading models (*e.g.*, based on thermal circuits [163]). Electronic design automation tools already incorporate functionality for temperature-aware design that can be very beneficial for photonic designers.

#### 5.2.4. Electronic Feedback for Photonic Circuits

Silicon photonic waveguides are very sensitive to geometric variations, but also to external effects such as temperature. This means that the temperature sensitivity can also be used to actively compensate for imperfections by (locally) heating or cooling elements on the chip. There are different ways to integrate heaters with silicon chips in the form of an electrical resistor [164].

To tune the behavior of a chip, a current is driven through the heater resistor, which translates in a temperature increase of the waveguide, and then a thermally induced phase shift. This phase shift is fairly linear with temperature. A temperature increase of 10 K can roughly compensate a linewidth or thickness deviation of 1 nm.

The physical integration of a heater is not challenging, even though there is a large design space to optimize the heater power efficiency [10, 164–166]. The challenge, especially in larger circuits, is to control the heater to maintain the desired state of the chip. This requires the integration of monitoring and control mechanisms.

To monitor the local operation of a chip it is possible to incorporate photodetectors. These can be classical photodetectors [167–169], but they should be mounted that they introduce only a small power penalty. They can use a fractional tap waveguide, or they can be incorporated on a waveguide where the power needs to be minimized. As an alternative there are detection schemes where the monitor itself does not introduce an additional power loss, feeding off the intrinsic loss mechanisms of the photonic components [170, 171].

The control mechanism should couple the result of the photodetector to the heater. This can be done using elec-

tronics or software algorithms, as the timescales for thermal control are in the order  $>10 \mu\text{s}$  (the thermal RC time constants are related to the heated mass of the waveguide devices and the thermal dissipation). The algorithm is not always straightforward: photodetectors are only a measure for the optical power in the waveguide, and there is no direct measurement of phase or wavelength, even though the heaters actuate the phase. The feedback loop should therefore, if necessary, also contain the interferometric structures to translate the relevant quantities for the feedback loop to one or more optical power measurements.

Examples of active feedback to compensate for operational and fabrication variability include wavelength tracking for optical filters and modulators [172, 173], or the matching of phase delay lines [174].

Active tuning can provide a flexible solution to the problem of variability, but it introduces its own challenges. Thermal tuning consumes a lot of power, and can only be operated in one direction: local heating is much easier than local cooling. This means that the designs should be pre-compensated to accommodate the heaters, and take into account the expected average heating of all elements. Also, to avoid thermal crosstalk between tunable elements, the spacing should be sufficient. This does not only increase the overall footprint of the circuit, but it will also increase the mismatch between components. The monitors and optical feedback circuit also consume footprint of their own, especially when there is need for external electrical contacts. The electrical (or software) feedback loop should be taken on-board in the design process, which requires a co-design of the photonics and the electronics.

### 5.3. Photonic-Electronic Integration

Silicon photonics allows the integration of many optical functions on a chip. However, in a real system, the photonics needs to be integrated with electronics. This integration can serve two purposes: Either the photonics can enhance the performance of the electronics (*e.g.*, by increasing the communication bandwidth) or the electronics can enhance the photonics (*e.g.*, by electrically tuning the performance of the photonic circuit, as discussed in the previous section). In both cases, photonic and electronic circuits need to be combined into a single circuit.

There are different technological approaches for the co-integration of photonics and electronics [175] shown in Fig. 11. The photonic and electronic functions can be combined on a single chip, either by adding electronic functions on a photonic chip [111, 176] or by adding photonic functions on an electronics chip [112, 177, 178]. Such *monolithic* approach provides a very tight integration. However, it is also possible to combine separately fabricated photonics and electronics, using 3D stacking [179], flip-chipping [43], or simple side-by-side integration on an interposer or circuit board.

Irrespective of the technological implementation of the photonic-electronic integration, both the electronic and the photonic circuits need to be designed to operate together.

This requires a form of integrated co-design methodologies that supports both domains. In such a co-design, we can discern the same schematic/layout separation as in the pure electronic or photonics design flow.

### 5.3.1. Photonic-Electronic Codesign at the Schematic Level

In photonic-electronic schematic codesign, both the photonic and the electronic circuit is designed at an abstract, logical level. The capture can be done in a schematic editor [95, 118, 180]. Mature EDA tools can also be used to create photonic schematics, but the interface should also support a clear separation between optical and electrical interconnections, and make sure the designer cannot inadvertently make connections between the two domains.

The second aspect of front-end design is the co-simulation of photonic and electronic circuits. As already covered in detail in in 4.2, there are a number of approaches to combine photonic and electronic circuits in a simulation, even though the circuit formalisms are very different. Photonic-electronic cosimulation has been implemented in Verilog-A [117], where the photonic signals are represented as a voltage, current or power, and electronic-photonic links can be simulated end-to-end. This works well in situations where the photonic signals are not too complex (*e.g.*, single wavelength, linear circuits), as will be discussed in more detail in Section 5.4.

For more complex applications, where many wavelengths or photonic nonlinearities are introduced, a dedicated photonic circuit simulator is needed. For this, a co-simulation approach can be considered, where a photonic and an electronic simulator exchange state information in opto-electronic blocks (*e.g.*, photodetectors, lasers, modulators, tuners) [118]. The advantage of this approach, which is similar to the *analog-mixed-signal* (AMS) approach in electronics design, is that each domain uses the best tool, and no compromises need to be made on accuracy or richness of models and signal representation. With full cosimulation, the tight interaction between optical and electrical domains can be captured. For instance, an electrical feedback loop to tune the resonance wavelength of a ring modulator [172]. Even though this can be a relatively slow feedback loop, it requires continuous interaction between the monitor photodetector and the tuning element in the ring modulator. A more challenging co-simulation requires high-speed signals exchanged between the photonic and electronic domain, such as an electro-optic feedback loop to reduce the linewidth of a laser [181].

### 5.3.2. Photonic-Electronic Codesign at the Layout Level

The translation from a photonic-electronic logical circuit to a physical implementation depends very strongly on the fabrication technology to combine the electronic and photonic circuit elements. Different methods are illustrated in Fig. 11.

The most straightforward is probably the monolithic integration (Fig. 11e), where photonics and electronics reside side-by-side on a chip. There, photonics and electronic elements can be treated in much the same way and a traditional layout process can be used. The co-integration still imposes significant boundary conditions in local and global pattern density, where the photonics can impact the performance of the electronics and vice versa. Still, the tight integration and the fact that both are implemented on the same chip simplifies the design process. Also, electrical parasitics can be kept low due to the close distance.

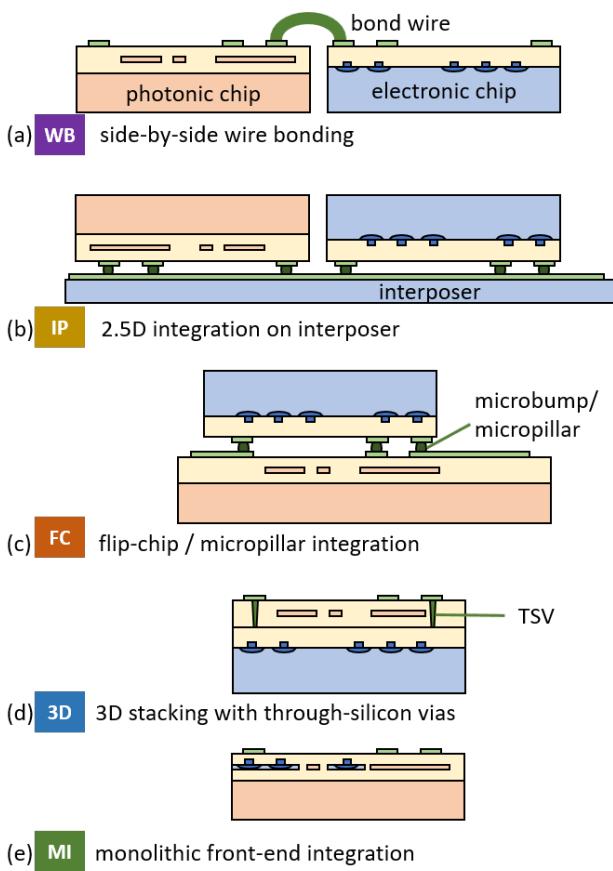
When photonics and electronics are implemented on different wafers, the integration strategies can impose significant restrictions on the design of both. First of all, the number and density of electrical connections could be a lot smaller than with monolithic integration, and the electrical parasitics increase correspondingly. Basically, all the design back-end challenges that come with multi-chip modules, 2.5D interposers (Fig. 11b) and 3D stacking (Fig. 11d) also apply for photonic-electronic integration [182]. This includes floorplanning and placements of bond-pads or *through-silicon-vias* (TSV), package co-design, thermal and mechanical management, electrical and optical input/output and power delivery networks [183]. Here, photonic-electronic integration can benefit from the developments in electronic 2.5D and 3D integration, including in the design methodologies [184, 185].

Figure 12 evaluates the integration strategies pictured in Fig. 11 against a number of criteria related to the co-design of a photonic-electronic circuit, indicating areas where significant challenges need to be addressed. We can see that from a design perspective, there is no clear winner. For instance, while monolithic co-integration clearly facilitates the process of schematic-driven layout by combining everything on the same chip, the design rules, floorplanning and thermal management become a lot more difficult. Interposer-based integration on the other hand clearly separates many design problems, but this separation makes integrated design using schematic-driven layout a lot more complex. In 3D stacking or flip-chip integration, the dense electrical interconnects (*e.g.*, copper pillars or microbumps) between the photonic and the electronic chip can give rise to electrical crosstalk (especially with high-frequency signals), but also thermal effects from the electronic chip can significantly affect the performance of the photonics.

## 5.4. Photonic signals

At the core of circuit design is the ability to simulate the signal propagation through the circuit. In an electrical circuit the representation of a signal as a voltage/current is unambiguous. In a photonic circuit however, there are different ways to describe the signals in a circuit, and depending on the richness of the signal, more optical phenomena can be described.

The use of voltage or current is not very appropriate, unless they are used to represent the coupling between the electric and magnetic component of the eigenmode(s) at the

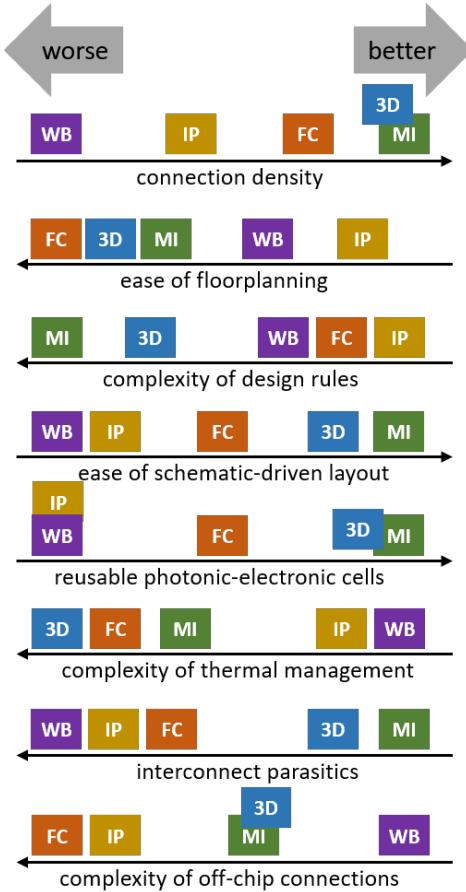


**Figure 11** Different schemes for photonic-electronic integration. The colored labels are used in Fig. 12 to compare the impact of the strategies on the design process.

electromagnetic wave propagating at in a frequency band around 200-300THz. The real-time waveform of both the electric and the magnetic field, for every mode or polarization in the waveguide, carries the complete photonic signal information. However, to process this in a (SPICE) circuit simulator, femto-second (fs) time steps would be needed, and an intractable amount of information would be needed to represent signals on the timescale of most meaningful application such as datacommunication, where time-steps of  $\approx 10\text{-}100\text{ps}$  are common.

To reduce the amount of information, photonic signals in a circuit are simplified as a time-envelope modulation of a waveguide mode around a carrier frequency (or wavelength). This modulation is complex (*analytic signal*) as it encodes both amplitude and phase, similar as in the simulation of RF circuits [89]. Because the response of an optical circuit is wavelength dependent, the response to the analytic signal will also be frequency dependent. But the use of complex signals rather than real signals implies that the circuit representation will also become complex, which makes it harder to guarantee stability, passivity and causality of time-domain simulations [130].

Waveguides can support multiple independently guided modes, each with its propagation constant, so each mode



**Figure 12** Evaluation of the different photonic-electronic integration strategies from Fig. 11 against a number of performance and design-related criteria. Right means better performance and ease of design, while left indicates poor performance or areas where significant development in design methods is needed.

requires its own propagating signal. Submicrometer silicon photonics waveguides usually support two guided modes, for the quasi-TE polarization and for the quasi-TM polarization. Because of the high refractive index contrast, these modes have very different properties (propagation constant or effective index, confinement, etc.), and these properties are also very wavelength dependent. This means that, if the circuit is used to transport multiple independent wavelength channels (WDM), these need to be treated as separate signals. So depending on the application of the circuit, the signal a photonic waveguide can be represented with tens or hundreds of numbers at each time step. This large number of signals can quickly become intractable in a standard Verilog-A simulator [186].

When carrying independent signals for individual modes, the wavelength-dependent properties of waveguide modes should be taken into account. Not only are modes dispersive (wavelength dependent propagation constants), but they can also go into cutoff for longer wavelengths, or new guided modes might appear for shorter wavelengths.

In some cases modes can also interact for certain wavelengths [187].

More simplifications are possible. In a linear photonic circuit, signals at different carrier wavelengths do not interact, and the circuit can be sequentially simulated for each individual wavelength carrier, provided that the modulation bandwidth of each wavelength channel is smaller than the separation of the carrier wavelengths. Then, for such sequential simulations, the complexity of the signal can be reduced to the amplitude and phase for two polarizations, in each propagation direction. If the wavelength itself is also part of the signal, these quantities can be represented with 9 numbers [110]. When the response of the circuit for multiple wavelengths is needed, simulations can be executed independently.

But it is not always possible to treat a photonic circuit as linear. Silicon photonic waveguides have a strong confinement of light, meaning that the optical power densities quickly grow to a level where nonlinear effects are no longer negligible [188]. Nonlinear effects can lead to coupling between signals at different wavelengths, but also signal distortion and spectral broadening [189].

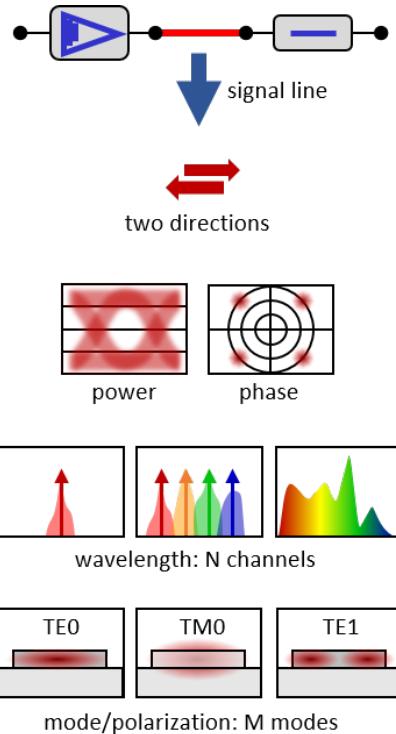
While today there are several powerful photonic circuit simulators [82–86, 88, 127], not all support more than a single carrier wavelength per simulation. There is also no common standard on signal representation, which means that model definition cannot be standardized between the tools. Without a common representation of optical signals (with multiple degrees of sophistication), barriers remain high to develop a set of common models, similar to BSIM transistor models in electronics [51]. The lack of standardization makes it difficult for foundries to invest in developing models for their PDKs.

### 5.5. Compact Models and Parameter Extraction

Going hand in hand with the representation of signals and the need for photonic-electronic cosimulation is the need to describe compact models that can capture all the relevant phenomena in a circuit building block. Given that there is no standard language equivalent to Verilog-A for electronics, it is a challenge to define models that can be widely used. This presents opportunities which we discuss in section 6.1.

However, even when a simulation tool with a model definition language is available, there is a significant challenge in defining a model's equation and populating the parameters. Even for the simplest component, the waveguide, there are different ways to represent the propagation of the guided mode, capturing dispersion, propagation loss or nonlinear effects. While the governing equations are well known, it is far from straightforward to know what the actual model parameters are for a given geometry or fabricated device.

Testing models and extracting parameters can be done through simulations and experiments. Both techniques impose different boundary conditions on a model. For instance, it is fairly easy to calculate the effective index of a waveguide mode with an eigenmode solver, but it is very difficult to directly measure the effective index of a waveguide



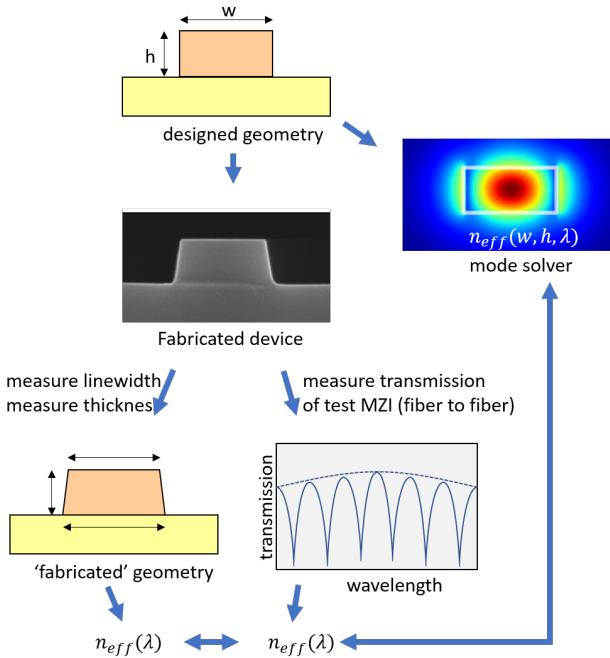
**Figure 13** Requirements of photonic signals to capture relevant phenomena in a circuit simulation approach. Top to bottom: Photonic signal lines support signals in two directions. Each signal carries amplitude or power, and a phase. A signal can be encoded on a single carrier wavelength, on multiple carriers (e.g., for WDM applications) or over an entire spectrum (for spectrometers, or for modeling nonlinear phenomena such as four-wave mixing). Most waveguides support at least two modes (two polarizations) and can support more for mode-division multiplexing.

on a chip. For this, special test structures need to be designed [190]. Therefore, it is important to include relevant test structures in the chip design. These can be used to check whether the fabrication is within the specified limits, and the parameters of the behavioral models correspond with reality. Given the high index contrast of silicon photonic devices, circuit behavior is usually wavelength dependent, and this dispersion increases the number of model parameters that need to be extracted. Extraction therefore needs multi-dimensional fitting or optimization methods [191].

Reconciliating design geometry and reality, and the model parameters extracted from simulation and measurement is quite challenging. This is illustrated in Fig. 14. To take again the example of a waveguide, the geometry that is usually used in the design process is only an approximation of the reality, where imperfections such as sidewall slope, rounding at the top or foot, or sidewall roughness modify the optical properties. The actual geometry can be extracted from SEM cross section measurements, but this can only be done with  $\approx 1\text{nm}$  precision. Also, the exact optical properties of interfaces are not always known. As a result, simulating the fabricated geometry to extract the effective index will also introduce an error. Alternatively,

a test structure can be designed to directly measure the effective index [190], but in this process there will also be errors due to measurement alignment and variability in the coupling structure.

Mapping trends and correlations between geometric parameters and model parameters, both measured and simulated, gives the most accurate results. For instance, from measurements of effective index and group index it is possible to extract the trends for linewidth and thickness of waveguides [79]. While sidewall angles and imperfections might cause the absolute extracted values of this linewidth and thickness to be slightly off compared to the actual value, the trends will be reliable, and can serve as input to variability analysis, performance monitoring and refinement of the models.



**Figure 14** Model parameters can be extracted from simulations or measurements, but each method introduces inaccuracies. The simulation geometry is usually an approximation of the reality (e.g., vertical instead of sloped sidewalls), and the actual geometry parameters measured from SEM or ellipsometry also have an uncertainty. When extracting the parameters from measurements, there is the problem of de-embedding the actual model parameter from the total response of the test circuit.

## 5.6. Photonic Routing

The curvilinear nature of waveguides also impacts the routing of optical circuits on chips. Electrical circuits are usually connected along Manhattan directions, and metal wires are allowed to make abrupt angles. Moreover, most electronic IC technologies allow for multiple metal layers interconnected with *vias*. In complex circuits, the routing problem

has become intractable for manual layout, and automatic routing tools optimize the many connections over the different metal layers.

In photonics, routing of waveguides presents a challenge. First of all, waveguides cannot make sharp bends. Even in high-contrast silicon strip waveguides a bend should have a radius of a few micrometer. In lower contrast systems, such as silicon nitride, or silicon rib waveguides, the bend radius grows to 10s or 100s of micrometers [192]. These larger bend radii make Manhattan-style routing impractical or impossible, and photonic circuits often have smoothly curved connections at arbitrary angles. Because of the large bend size and the all-angle freedom, solving the routing constraints for many waveguides becomes a much harder problem.

A second important constraint for photonic routing is the lack of multiple routing layers. While there have been some demonstrations of optical vias [193, 194], it is still impractical to make multi-layer photonic circuits. This means that all interconnecting waveguides need to be routed in the same layer. Fortunately, topological conflicts can be addressed by introducing controlled crossings between waveguides, which introduce only a small loss and crosstalk penalty [195, 196].

There have been some demonstrations of silicon photonic technologies with multiple waveguide planes, where some of the topological constraints are alleviated [197, 198]. In such an architecture routing becomes at the same time easier (fewer problems with crossings) and more difficult (more degrees of freedom and the need to manage the penalties of inter-layer transitions).

Routing can also impose additional functional constraints. In some circuits different light paths need to be closely matched. Matching propagation losses amounts roughly matching the propagation length, the number of bends and crossings. However, matching the actual phase delay of two waveguides requires length matching to deep submicrometer scale, and at the same time making sure that the waveguides remain close together to minimize variability. Therefore, phase-aware routing today is mostly done manually or using a dedicated script.

## 5.7. Summary: Design Challenges

To realize a photonic circuit design flow that is as reliable as an electronic design flow, a number of significant challenges need to be addressed. The most important ones reside in the realm of photonic compact models: the richness of photonics makes it not straightforward to define models that can capture the relevant phenomena for a broad range of applications. The fact that there is still no consensus on the nature of photonic signals or model definition increases the barrier for photonic component designers and fabs to expose their models to the circuit design community in the form of a PDK. On the back-end of the design flow, the challenges are mainly in the placement and routing, where objectives to minimize location-dependent variability interplay with the need for routing and integration with electronics.

Most of these design challenges are not unique to silicon photonics, and relate to difficulties in scaling for all photonic integration platforms. However, the high contrast of silicon photonics, with its much larger sensitivity to manufacturing variations and its potential to scale to very large circuits, makes these challenges much more acute.

## 6. Opportunities

There are many actors in the space of photonic IC design, both academic and commercial. The community has the benefit of a large number of software vendors, originating both from photonic and electronic design automation, that are willing to collaborate on solutions for specific design problems [53, 118]. But a large opportunity presents itself in true standardization. There are a number of areas where standardization could dramatically lower the barriers for designers and fabs:

- **Standardization of photonic circuit models.** In the previous section it became clear that there are still significant barriers for the widespread use of photonic compact models. Standardization on different levels (signals, model definition language, data formats, ...) could significantly boost the circuit level design
- **Standardization of photonic design primitives,** such as waveguide ports, should be natively supported in the design exchange formats and databases, just like electronic primitives are supported.
- **Curvilinear mask layouts:** While curvilinear layouts are also used in MEMS, RF and analog electronics, photonics is the first field where the fidelity of curvilinear geometries is essential to successful fabrication. Defining a back-end design flow where conversion to polygons can be eliminated offers a potentially significant increase in yield.

One of the benefits of the convergence of photonic and electronic design automation is that photonics can leverage standardization efforts in electronic design tools [199]. When design information can be exchanged between tools from different vendors, or between different versions of the same tool, this benefits the capabilities of the designer, and allows a greater reuse of design know-how. It is also essential in the creation of PDKs that fabs can share with their clients.

Another opportunity presents itself in programmable photonic circuits. Today's photonic ICs resemble very much the *application specific ICs* (ASIC) in electronics. However, the integration with electronics makes it possible to design self-configuring and self-correcting photonic ICs. The design requirements for such circuits are very different, and the implementation of actual functionality will then be programmed at a higher level.

### 6.1. Standardization of Circuit models

As extensively discussed in section 5, there is currently no standard to define circuit models so component designers

can create a model that can be used by circuit designers in different simulators. To realize this, we can identify different areas where tool vendors can collaborate:

- **Define standard circuit model interfaces:** How is a waveguide port and mode represented? What are the types of signals (see section 5.4) and how are they supported by a model? Defining such an interface does not require that all details are standardized in advance; an initial subset can be supported, and vendor-specific information can always be added as metadata.
- **Generic models and data formats:** most circuit simulators support some form of generic model. For instance, in the frequency domain wavelength-dependent S-parameters can describe any linear component, while in time-domain a set of ordinary differential equations can be used. Agreement on a terminology and a storage format of the generic model quantities (*e.g.*, the *Open-Matrices* [200] or *Touchstone* format for S-parameters) can already provide a first model standardization avenue.
- **A common application programming interface (API) for custom-defined models:** if component designers can create a compiled model routine that adheres to a set of standard function call signatures, it can be executed by circuit simulators. There are already efforts to create interchangeable parametric code libraries for photonics through the PDAFlow Foundation [128] that support exchange of layout information and scattering matrix data, but this does not extend to standard interfaces for complex, custom-written circuit models.
- **A Common model definition language:** In electronic design, custom models can be implemented in different ways, but most simulators support the interpretation of Verilog-A. There is no equivalent for photonics. While some simulators allow the custom creation of models in standard languages such as Python [91, 201], the model syntax is still specific for each simulator. What is needed is an agreement on a rich model definition language that can be parsed and interpreted by different simulators with sufficient efficiency for large-scale circuit simulation.
- **Standard Models for Photonic Building blocks:** in the electronics world, a lot of the circuit simulators rely on a limited set of agreed models for the basic building blocks: resistors, capacitors, diodes. These models have been refined over time, such as the different families of BSIM transistor models [51]. Many electronic circuit simulators incorporate optimized implementations of these standard models, requiring only the parameters to execute the simulation. For photonic ICs there is no such set of models. Most 'standard' models for optical systems relate to fiber-optic systems and lasers [202], but these models are not entirely suitable for on-chip waveguides. For many components, there exist a number of accepted models, but the discussion is mostly on the choice of parameters. For instance, how is the dispersion of a waveguide tabulated? As a baseline effective index and higher-order dispersion parameters around a central wavelength, or as a list of indices for different wavelengths? There is not even an agreement on the use of wavelength or frequency for model parameters.

Providing to component designers and fabs one or more methods to define a single compact model that can be used by different circuit simulation tools would present a dramatic saving in the effort to build PDKs.

## 6.2. Standardization of Design Data

Most electronic design automation tools support a form of database storage where the different aspects of the front-end and back-end design are kept together, so the designers can move back and forth in the flow and maintain a coherent set of data. Such databases can be proprietary, but several design vendors have already adopted the OpenAccess standard [199].

Photonics design automation is still somewhat removed from this situation. The parts of the design flow that overlap most with electronic design, such as mask layout, make use of the same standard file formats, such as GDSII and OASIS. The drawback is that these file formats do not contain any photonic-specific information such as waveguide ports, and do not support future needs such as curvilinear geometries.

Interoperability becomes even more difficult when parametric design is involved. Parametric cells require some form of automation, and this in turn requires a scripting engine to evaluate the contents of the design, based on the input parameters. The OpenAccess database format, provides a common interface to such scripted cells [199]. The database format can contain scripted and static layout information, netlist connectivity, and relations to circuit models. It is now gradually being adopted by photonic design tools [53, 58].

As already discussed, not all photonic concepts can be expressed in electronic primitives. There is a strong need for standards for the photonic design aspects that are not yet covered by the EDA standards, especially in the front-end of the design flow, such as signals, waveguide ports, modes, wavelengths. This can require extensions of existing file or database formats but also new formats for photonic-specific concepts. We already discussed the need for a signal description that can capture the richness of photonic circuits and the need for standard circuit models. Proposals have been initiated to extend the OpenAccess standard with dedicated photonic primitives [203].

This standardization problem extends to the creation of design kits. There is currently no standard format for PDK libraries, and therefore a fab needs to provide PDK flavors for the design tools of different vendors. This situation is not unique to photonics: even in electronics design standardization efforts of PDK formats have enjoyed only limited support.

## 6.3. Reproducible Curvilinear Layouts

One of the key differences between photonic circuit layouts and electronic circuit layouts is the use of arbitrary curvilinear features. Electronic circuits are usually designed on a rectangular grid (so-called *Manhattan* geometries) with

interconnects running along a north-south or east-west orientation. Electrical signals, unless at very high frequencies, suffer little from right-angle turns. Many steps in electronic layout design rely on Manhattan geometries: verification of design rules such as minimum widths, application of optical proximity corrections such as serifs, and routing of metal interconnects.

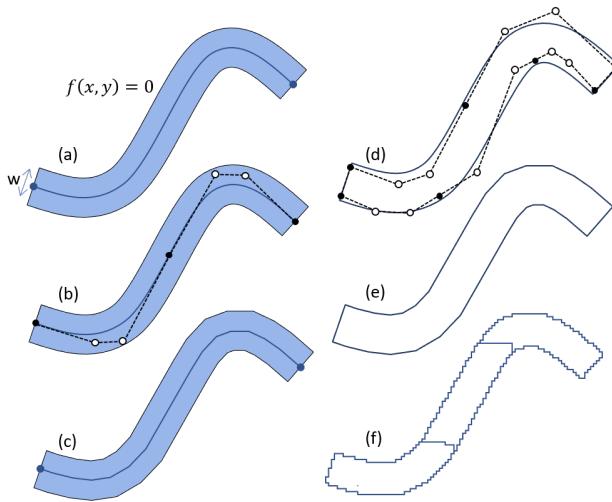
Photonic waveguides typically need smooth bends, as abrupt changes in geometry cause scattering and backreflection of light. Waveguide bends should therefore follow a smooth curve, either a circle or a more adiabatic shape [121] that can be defined by an equation [204]. There are different ways to define such arbitrary curves, as illustrated in Fig. 15. Because standard mask layout files only support polygons, the representation of these curves require a discretization step which is only an approximation of the original design intent, and therefore can impact the performance of the circuit (Fig. 15c,e,f). Because of the nanometer-scale sensitivity, the discretized polygons should not significantly deviate from the original curve. When the layout is generated to a standard GDSII or OASIS file, only the polygon data remains, and the original design intent is lost. Moreover, some silicon photonics technologies, especially those relying on unmodified CMOS technology, require layout data to follow strict Manhattan-oriented polygons. For this, an additional staircasing discretisation step is needed, shown in Fig. 15f [97].

When the mask file is known, it becomes important to compare the generated polygon layout with the original design intent. For this, a curve needs to be fitted to the polygons [123]. These two steps, discretisation and then curve fitting, can each introduce a deviation from the design intent.

During the fracturing phase, where the flattened layout data is converted into writing patterns for the photomask (or direct e-beam writer) the polygon data is again converted, depending on the writing strategy and the original data format. This can again introduce discretisation and stair-casing [205]. Customized writing strategies can reduce these effects [206, 207], but today they always start from polygon data that is already an approximation of the intended design. Advanced fracturing algorithms can also infer the curvilinear shape from the polygon and write the pattern in such a way as to minimize the discretization and stair-casing by writing the edges of the shapes in a continuous fashion [208]. Again, the discretisation step and the subsequent curve-fitting step can introduce unnecessary conversion errors. This is very important for photonic crystals, where the shape and discretization plays an important role on the performance of the device.

As there is no standard format to exchange curvilinear data, the current stop-gap approach is to embed some design intent into the meta-data into the design files, or provide accompanying files (so called *side files*) that contain the original curvilinear design intent [209]. This design intent can then be used to run verification on the polygon data (e.g., check the actual linewidth versus intended linewidth [123]), or validated fitted polynomial curves to the polygons [210].

A more fundamental solution to the representation of curvilinear features would be the creation or extension of a design data format that natively supports curves. Many graphics and CAD formats already support *non-uniform rational basis spline* (NURBS), that uses piece-wise higher-order (usually 3rd order) polynomials to represent arbitrary curves, illustrated in Fig. 15b,d. This would allow a more accurate, but also much more compact, representation of optical waveguides. Spline-based representations can require  $10\times$  fewer data points than polygons, and  $100 - 1000\times$  fewer points than staircase-approximated polygons. However, this might move the problem from the designer to the actual chip manufacturer, as the curves need to be rendered onto a mask plate before fabrication. Together with file formats, a optimization of fracturing and mask writing strategies is also needed.



**Figure 15** Representations for curvilinear shapes. Waveguide-like shapes can be either represented as paths with a given width  $w$  (left), or as boundaries where both sides of the shapes are independently defined (right) (a) Equation based path, (b) Piecewise spline-based path, (c) Polygon-based path, (d) Piecewise spline-based boundary, (e) Polygon-based boundary, (f) Staircase-based boundary.

#### 6.4. (Self-)Correcting Circuits and Programmable Photonics

Even with the ever improving technology, photonic circuits will be subject to some variability. However, when combined with electronics, monitors and tuning elements, certain imperfections in a circuit can be compensated. For instance, the resonance of ring modulators can be locked to a given wavelength by optimizing the power in the ring [172]. By considering such combinations of photonics and control electronics as reusable subcircuits, the overall performance of silicon photonics can be greatly increased. Such subcircuits should be supported in the design stage. As mentioned in section 5.3, co-integration of photonics and electronics introduces its own challenges in front-end and back-end design.

Similar approaches have been used in analog electronics, where digital feedback circuits are used to compensate the deficiencies of imperfect analog electronic elements [211].

Photonic circuit design today is mostly focused at realising circuits for a specific application, therefore, the emerging photonic design flow resembles very much the flow for analog full-custom *application-specific integrated circuits* (ASIC). Such circuits usually deliver the best possible performance in terms of power consumption and footprint, but they require a long design cycle and expensive custom fabrication. This is just as true for their photonic counterparts.

Using active tuning and feedback loops, it becomes possible to construct circuits that perform markedly better than the individual building blocks. For instance, using imperfect  $2\times 2$  couplers and electro-optic phase shifters, a  $2\times 2$  coupler with an arbitrary split ratio can be constructed [212]. This approach can be extended for larger power distribution networks, or the synthesis of optical wavelength filters. Moreover, by incorporating monitor detectors in strategic locations in the circuit, these subcircuits can be self-configuring using simple minimization or maximization algorithms [213, 214].

Turning such photonics-electronic subcircuits into a reusable IP blocks will be a great enabler for circuit design at a higher level. It will also enable a scaling of circuit size, because the self-correcting elements will reduce the problem of compound yield and variability.

The concept of self-correcting subcircuits can be extended to self-configuring or programmable photonic circuits. for example, photonic networks consisting of connected tunable  $2\times 2$  couplers and phase shifters can be configured to perform any linear operation between a set of input and output waveguides, or implement a variety of wavelength filtering functions [40, 41, 213, 215].

Such programmable photonic circuits, which actually consist of photonics, electronics and software, introduce an entirely new design paradigm for photonics. Rather than custom-designed photonic chips, generic circuits can be configured to perform a specific optical function. In this, they resemble an electronic *field-programmable gate array* [216]. The design of the optical functionality now becomes more akin to a programming step, where circuit functionality is translated into a programming strategy for the individual self-configuring subcircuits. The synthesis algorithms and strategies for such circuits could create an entirely new landscape of design IP for photonics.

#### 7. Summary

Photonic integration technology, and especially silicon photonics, has rapidly enabled the integration of hundreds to thousand optical components on a chip. However, the circuit design methodologies that can leverage the potential complexity of this large-scale integration are only just emerging. Today's design methods are still rooted into the principles of component design and do not scale well to more complex circuits. Methodologies coming from electronic design automation are gradually introduced in the photonic design

space. Schematic-driven layout and verification methods reduce the number of errors and increase the chances for first-time-right design.

Still, there are a number of considerable challenges that need to be addressed before photonic circuit design can claim the same level of maturity as today's electronic design. Rigorous variability analysis is needed to predict the yield of larger silicon photonic circuits, where nanometer-scale geometry variations have a non-negligible impact on device response. Photonic circuit models and simulators need to encapsulate the rich physics in photonic building blocks, which requires choices on model parameters and signal representation. Cosimulation and codesign of photonics and electronics requires some form of common standard to interface the optical and electrical domain.

Because photonics and electronics need each other, photonic and electronics design flows are converging. This creates a number of opportunities where photonic design tool vendors and researchers can innovate to enable a truly first-time-right design flow for photonics.

**Acknowledgements.** Some of the work of Wim Bogaerts referred to in this review paper has been supported by the Flemish Research Council (FWO-Vlaanderen) under grant G013815N.

The authors would like to thank Andre Richter, Sergei Mingaleev, Xu Wang, James Pond, Ahmadreza Farsaei, Michal Rakowski, Robert Scarmozzino, Cem Bonfil, Twan Korthorst, Chris Cone, Erwin De Baetselier and Pieter Dumon for their valuable comments.

**Key words:** Silicon Photonics, Design Automation, Variability Analysis, Compact Models



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