






Computational Lithography for Silicon Photonics Design

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Abstract—We demonstrate a method to predict the photolithography effects of a 193 nm deep ultraviolet (DUV) process, and we build a lithography model using physical measurements on a fabricated test pattern. Our model accurately predicts the proximity and smoothing effects that are characteristic of DUV lithography. We verify the accuracy of the model by visually inspecting the fabricated test patterns and comparing them to the predicted ones. Additionally, using predicted shapes, we compare experimental measurements on a benchmark device (the contra-directional coupler) against those of our predicted, computed responses. Our predictions show good agreement with the fabricated results using both verification methods. Lastly, we illustrate the design-for-manufacturability enabled by our model by demonstrating a design correction method for the contra-directional coupler that improves its compatibility with the DUV process.

Index Terms—Proximity Effects, Optical Lithography, Deep Ultraviolet 193 nm, Lithography, Bragg Gratings, Optical Proximity Correction, Design-For-Manufacturability.

I. INTRODUCTION

IN RECENT years, silicon-on-insulator (SOI) platforms have increased in popularity. Many key devices, such as, filters [1], modulators [2], and photodetectors [3] have been demonstrated on such platforms [4],[5]. SOI platforms have two common choices for patterning the silicon: electron-beam lithography (EBL) and deep-ultraviolet (DUV) lithography. EBL is performed by writing the design directly onto the resist via an electron beam. This mask-less fabrication approach can achieve smaller feature sizes with fast turn-around times, at the cost of low throughput. This makes EBL attractive for rapid-prototyping research and development purposes [6]. Conversely, DUV lithography performs the design patterning using a binary mask. The mask exposes the resist via an optical laser within

a stepper, printing a copy of the design onto each segment of a wafer. As a result, the DUV process has high throughput and is more suitable for mass production.

SOI device performance suffers from discrepancies between as-designed and as-fabricated structures. Photolithography effects, such as smoothing [7] and proximity effects [8], are large contributing factors to these discrepancies. Previous efforts have been made to correct for photolithography effects. These include optical proximity correction (OPC) [9], [10], [11], [12], [13] and using phase shifted masks [14]. However, the SOI platform does not yet have a “first-time-right” design approach akin to that of the CMOS platform [15].

As silicon photonics marches towards commercialization, it is crucial that it bring with it the robustness in fabrication that exists in mature CMOS processes [4]. Previous work demonstrated that photolithography smoothing effects of 2-port Bragg grating devices could be modelled by fitting the modelled responses to experimental responses [7],[16]. However, designers would ideally wish to understand and model the effects of photolithography prior to fabrication.

In this work, we use a computational lithography model to predict the outcomes of a dry 193 nm DUV lithography fabrication process, that uses an ArF stepper and a binary mask. The model is built using measurement data from fabricated test patterns and simulates the photolithography effects on an input shape. Our model is process specific and allows designers to predict their device’s performance for a particular fabrication process. To verify the accuracy of the model, we use the optical response of a 4-port, Bragg-grating-based filter, known as a contra-directional coupler (contra-DC) [17], as a benchmark. The configuration of the contra-DC consists of two Bragg gratings placed in close proximity to each other for coupling purposes. We use the contra-DC as a benchmark because it is particularly susceptible to photolithography effects, such as smoothing and proximity effects. The device is susceptible to smoothing because it uses sidewall-corrugated, Bragg-grating waveguides and is susceptible to proximity effects because the two waveguides are in close proximity to each other. As the contra-DC has two output ports, and an optical response sensitive to design parameters, it is an excellent candidate for the validation of our model. We are able to demonstrate excellent visual resemblance between the output of our computational lithography model and the Scanning Electron Microscopy (SEM) images of a fabricated

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test pattern set. Furthermore, we are able to accurately reproduce the experimental measurements made on our benchmark device by simulating the response of the predicted device structure generated by our model.

II. COMPUTATIONAL LITHOGRAPHY MODEL

The computational lithography model is built using the known parameters of the 193 nm DUV process, estimated parameters of the process, and feature size measurements obtained from a fabricated test pattern set. The parameters of the model are optimized such that the error between the predicted feature sizes and the measured feature sizes are minimized. As the model is built from a fabricated test pattern, it is foundry process specific. However, our methodology in building the model can be applied generally to any foundry process.

The model is built using Mentor Graphics Calibre software [18]. A standardized test pattern set is included in the software. Each test structure in the test pattern set has a feature size of interest, e.g., a gap or width, from which we take measurements. These feature size measurements are also known as critical dimension (CD) measurements.

A. Test Pattern Data Extraction

The test pattern set consists of 216 structures. The various structures used are depicted in Fig. 1. The structures can be categorized into “solid” and “inverse” structures. Solid structures have the surrounding silicon removed to obtain their shape, as shown in Figs. 1(a)–1(h). Their inverse counterparts are negative imprints of the structure, as shown in Fig. 1(k)–1(l). As the solid and inverse pairs share the same as-drawn CD, it is anticipated that they would fabricate similarly. However, in each case, the as-fabricated CD trends of the solid and inverse pairs are different. Fig. 2 shows the trends of the as-fabricated CDs for the solid and inverse structures. This indicates that different process biases are needed for different structures. Overall, the aim is to capture the photolithography effects on possible shapes that a designer might draw. SEM images are used to obtain the CD measurements of each structure on the fabricated test pattern. The measurements are performed by counting the pixels between the two locations we wish to measure. The number of pixels is then converted to SI units using a scale provided by the SEM image. The SEM images, shown in Figs. 3, 5, and 6, are taken using the Helios NanoLab 650 scanning electron microscope at a magnification of 5000x, using a voltage of 20 kV, and a beam current of 0.10 nA. The white borders of the structures in the SEM images (Fig. 3(a)) make it difficult to discern where a pixel measurement should be taken. As the white borders are very thick (Fig. 3(b)), a particular measurement depends on where we define the edge of the structure. To address this problem, our convention uses the average distance of the outer and inner edge of the white border. Here we are assuming that the white borders occur due to sidewall angles cause by fabrication processes [19] and that the sidewalls have a linear slope from the top to the bottom of the structure.

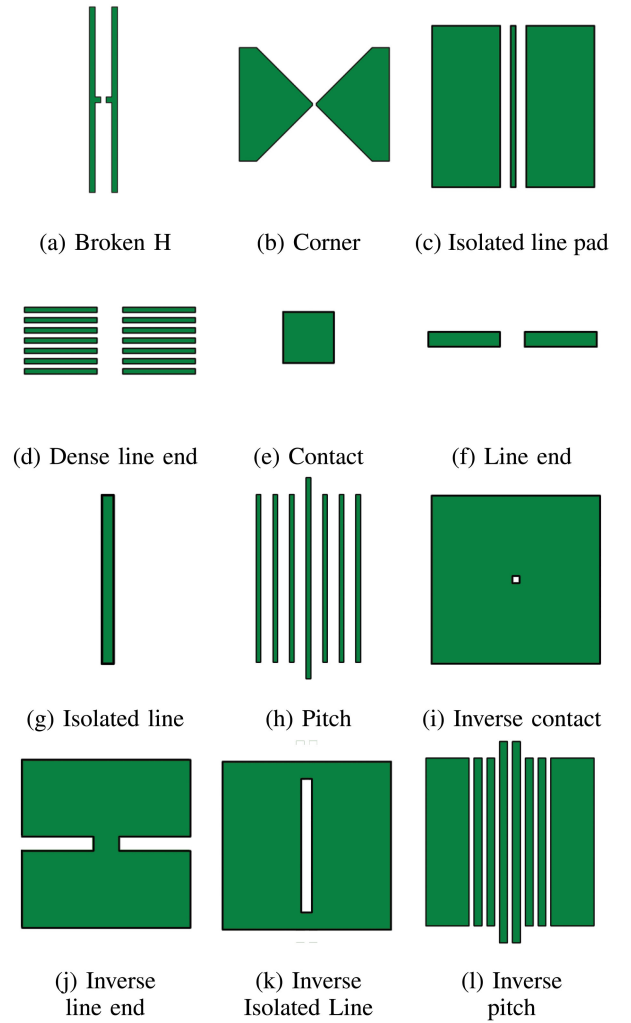


Fig. 1. The types of structure included on the standard test pattern are illustrated. The structures consist of solid structures ([a] to [h]), and inverse structures ([i] to [l]).

B. Lithography Model Optimization

Calibre provides an optimization function which operates by adjusting the lithography model parameters within the aforementioned range. The optimization aims to minimize the error between the predicted CD and the as-fabricated CD. The model's inputs are the optical lithography wavelength and each test pattern's measured CD. The optimized output produces 4 parameters for the lithography model: 1) the NA, which is a dimensionless number that describes the ranges of angles of the projection lens seen from the position of the wafer; 2) the σ , defined as the fraction of the NA of the projection lens filled by the illuminating beam [18]; and 3) the $\delta\sigma$, defined as the transition length from which the intensity of the optical beam rises from 0.5% to 99.5% [18]; and 4) the threshold value, defined as the percentage of the computed illumination which is applied.

The optical wavelength is known for the 193 nm DUV dry-etch process. Unfortunately, the NA, σ , $\delta\sigma$, and the exposure threshold, are not publicly available. Hence, we instead refer to

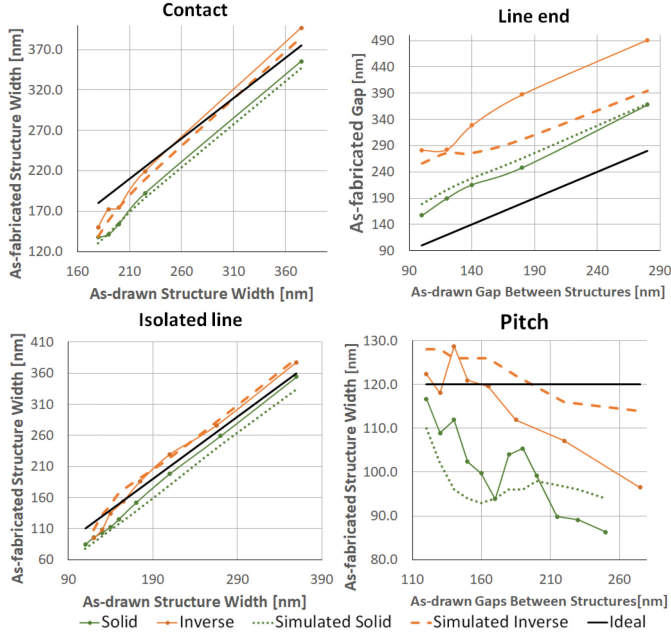


Fig. 2. The as-fabricated CDs are plotted against the as-drawn CDs for the structures shown in Fig. 1(e)–1(l). Each solid structure and their inverse counterpart have shown different CD trends, indicating different process biases are required for each type of structure. The simulated CDs are also included to compare the closeness of the lithography model.

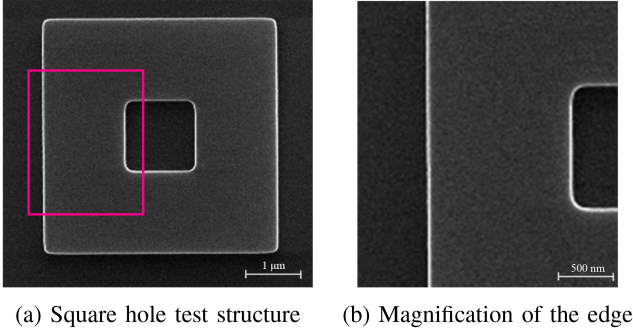


Fig. 3. (a) An SEM of an Inverse Contact structure. (b) A zoom-in illustrating the thick white border can create CD measurement discrepancies. Our convention is to use the average distance between the outer and inner edge of the border.

values given in previous publications for similar processes [20], [21] to determine a range for optimization.

The optimization is performed by sweeping the NA, σ , and $\delta\sigma$ parameters, and generating a lithography prediction of the test patterns. An error value is obtained by comparing the predicted CDs against the as-fabricated CDs. The lithography model parameters prior to optimization are NA = 0.6, σ = 0.6, and $\delta\sigma$ = 0. The NA and σ values are from a previous publication [7], and serve as a starting point. The ranges for the sweeps are chosen from values reported in the literature [20], [21], as well as being based on our own estimations.

During each sweep of the optimization, the optical parameters are used to generate a computed illumination of a structure's mask, as shown in Fig. 4(b). Next, a lithography prediction is generated using a threshold value. The threshold value is the

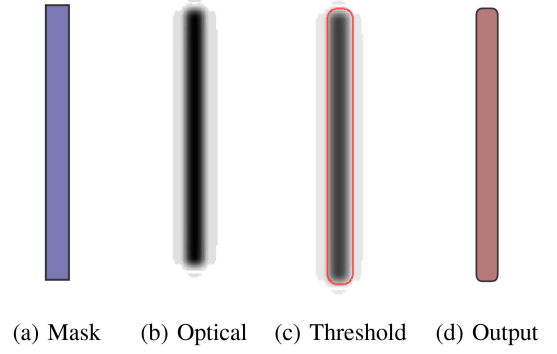


Fig. 4. Steps to optimize the lithography model: (a) the ideal as-drawn mask. (b) the computed illumination generated using the optical wavelength, NA, σ , and $\delta\sigma$. (c) the selection of the threshold value, shown in red. (d) the predicted post-lithography output.

percentage of the predicted illumination that will be applied to the structure. The optimization will select the threshold value producing the best fit (Fig. 4(c)). The error between the CD measurements are then evaluated against errors from previous sweeps. The optimization continues until a combination of parameters with the minimum error is found (Fig. 4(d)). The optimized lithography model has the following parameters: NA = 0.671, σ = 0.884, $\delta\sigma$ = 0.882, and threshold = 0.165.

III. VERIFICATION

In this section we verify the lithography model using two comparison methods. First, we visually evaluate the accuracy of the lithography model. We compare the overall shape and CD measurements of predicted structures to those of the as-fabricated structures obtained from SEM images. Second, we compare the optical responses of contra-DC devices. The simulated responses of the as-drawn designs and the predicted designs are compared against experimental responses.

As regards the visual verification, Fig. 5 shows the Broken H structure which has an as-drawn gap of 120 nm. The computational lithography results predict a gap of 182 nm. The predicted gap (182 nm) closely matches with the fabricated gap (181 nm) shown in SEM images. Other features, such as the end roundings, are common to both the predicted and fabricated structures. Fig. 6 shows a Corner structure predicting the effects on close-proximity corners. In this structure, the as-drawn gap between the two tips of the corners is 150 nm. Our computational lithography predicts a gap of 214 nm. This is very similar to the SEM image which shows a gap of 210 nm. Visually, the output of the computational lithography model corresponds very closely to the as-fabricated test patterns.

Fig. 2 shows a plot of the CD of the contact, line end, isolated line, and pitch patterns (note the change in scale for the vertical axis of the pitch pattern). The model is able to produce results comparable to the measured CD. However, the model's predictions are less accurate for the inverse line end pattern; The cause for this requires further investigation.

As regards the optical response, Fig. 7 illustrates the schematic of a contra-DC device. The device consists of two coupled

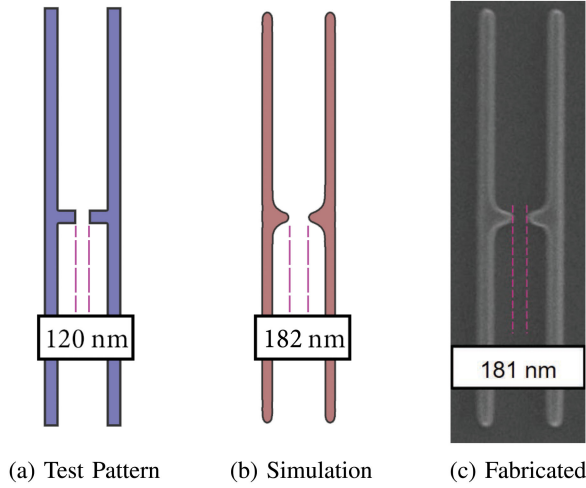


Fig. 5. A Broken H structure is depicted. The CD location is between the two center protrusions and captures how small grating-like structures will be effected by photolithography. The CD predicted by our method (b) is nearly identical to the fabricated one (c).

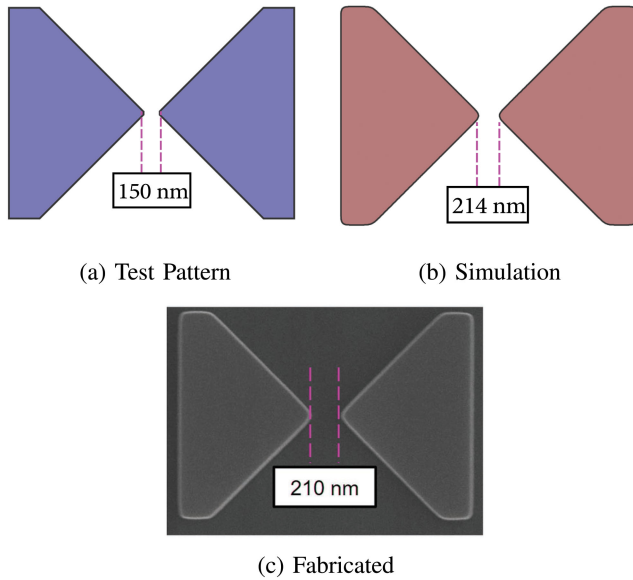


Fig. 6. The Corner structure, which captures how two corners interact when in close proximity, is depicted. The resulting CD from our simulation is highly similar to that of the fabricated one.

Bragg-grating waveguides. The bandwidth of the contra-DC is sensitive to the corrugation widths (ΔW s), e.g., small changes in the ΔW will cause large changes in the bandwidth. The contra-DCs used in our comparison have the anti-reflection configuration described in Ref. [22]. Each contra-DC consists of two waveguides with different widths, and, hence, different propagation constants. The main band of each contra-DC will be centered at an operating wavelength at which the phase-match condition [17], [22] is satisfied.

However, two side-bands, known as the self-reflection (SR) bands, will exist next to the “main band” for the contra-directional coupling on the contra-DC [22]. The SR bands occur

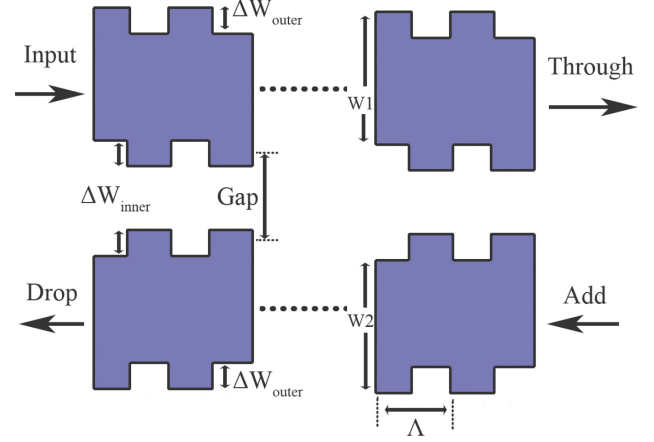


Fig. 7. The schematic of a contra-DC, with the design parameters and the four ports labeled. A single segment block of the Bragg grating with a pitch (Λ) is repeated to obtain a desired length. There are two corrugation widths (ΔW s), which will often be affected differently by the fabrication process.

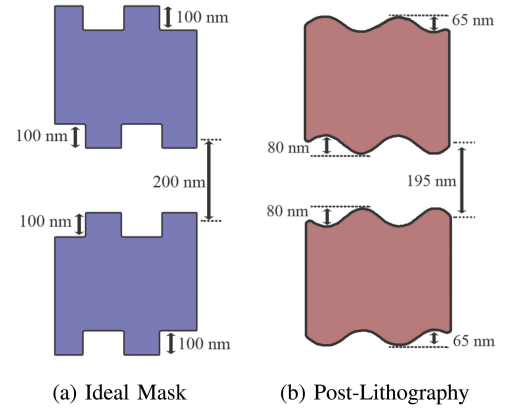
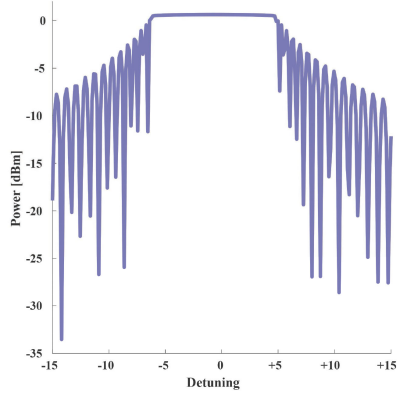


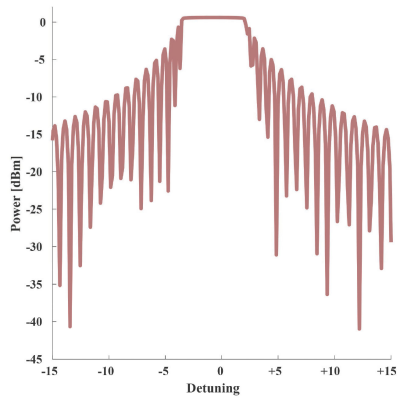
Fig. 8. (a) A simplified contra-DC design, with symmetrical waveguide widths and ΔW s to demonstrate the smoothing and the proximity effects of photolithography. (b) The post-fabrication changes in the gap, ΔW_{inner} , and ΔW_{outer} dimensions are depicted, showing a large asymmetry between the ΔW s. The size reduction of ΔW_{inner} is due to both the smoothing, and proximity effects, whereas the size reduction of ΔW_{outer} is only due to the smoothing effect.

due to each mode of the two waveguides having their own propagation constants leading to the conventional single-waveguide Bragg reflection at a wavelength of $\lambda_{1,2} = 2n_{eff 1,2}\lambda_0$, where $n_{eff 1,2}$ correspond to the effective indices for the waveguide modes located mainly in waveguide 1 and 2, respectively. For broad spectrum applications, there is an appeal to reduce the SR as the SR bands limit the operating spectral ranges.

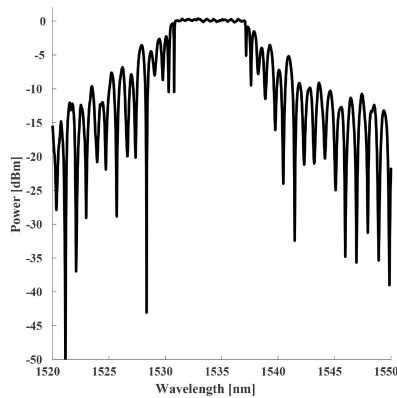
Fig. 8 demonstrates the photolithography effects on the contra-DC. Coupling gaps can increase and ΔW s of the device can become mismatched between the inner and outer portions. As the asymmetry between the ΔW s increases, the SR bands on the drop-port of the contra-DC become increasingly prominent. As the SR bands are related to the individual modes, and by extension the waveguide widths, small variations in the ΔW s, gap, and widths, will significantly change the main bandwidth and the SR bandwidths [22]. In our experimental results, the SR bands are approximately 40 nm away from the main band. Due to



(a) Simulated main band response of the as-drawn contra-DC



(b) Simulated main band response of the as-predicted contra-DC



(c) Measured main band response of the fabricated contra-DC

Fig. 9. The main band bandwidths of CDC3. (a) The as-drawn, (b) the as-predicted, and (c) the as-fabricated, are depicted. The as-drawn simulated bandwidth is 11.5 nm, the as-predicted simulated bandwidth is 5.6 nm, and the as-fabricated measured bandwidth is 6.4 nm.

measurement limitations, we will be comparing SR bandwidth at the shorter wavelength.

The simulated response of the as-drawn device is not accurate enough to match the as-fabricated result, as demonstrated in Fig. 9 for the main band and Fig. 10 for the SR band. Thus, it

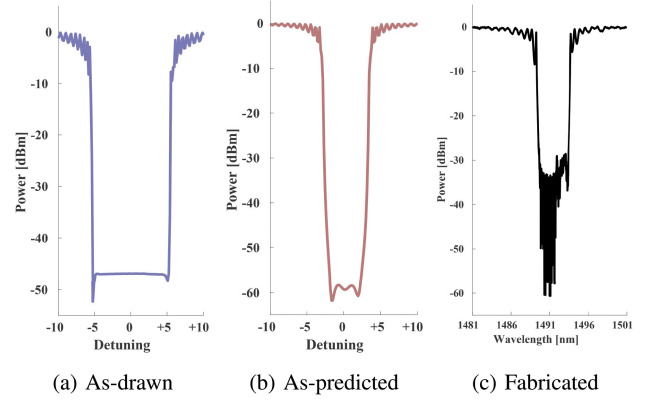


Fig. 10. The SR bandwidths of (a) the as-drawn, (b) the as-predicted, and (c) the as-fabricated, are depicted. The as-drawn simulated bandwidth is 11.1 nm, the as-predicted simulated bandwidth is 6.0 nm, and the as-fabricated measured bandwidth is 5.4 nm.

TABLE I
CONTRA-DC PARAMETERS

Device Name	Λ (nm)	Width 1 (nm)	Width 2 (nm)	Gap (nm)	$\Delta W1$ (nm)	$\Delta W2$ (nm)	Length (μm)
CDC1	270	370	270	175	60	50	270
CDC2	270	370	270	178	60	50	270
CDC3	325	370	270	185	60	50	325
CDC4	325	370	270	182	60	44	325

TABLE II
CONTRA-DC MAIN BAND BANDWIDTHS

Device Name	Ideal As-Drawn (nm)	Lithography As-Predicted (nm)	Experimental (nm)
CDC1	9.9 ± 0.22	3.6	4.3
CDC2	7.6 ± 0.68	3.2	3.9
CDC3	11.5 ± 0.85	5.6	6.4
CDC4	11.4 ± 0.22	5.7	8.0

is apparent that the photolithography effects of the fabrication process have heavily impacted the contra-DC's performance.

Using the lithography model, we predict the resulting shape of the contra-DCs after photolithography effects have been taken into account. The parameters of each of our contra-DCs are listed in Table I. We perform a Finite-Difference-Time-Domain (FDTD) simulation using Lumerical Inc.'s FDTD software and bandstructure method [16]. The coupling coefficient, kappa, and bandwidths are extracted from the bandstructure. The contra-DC response is then simulated using kappa and a Couple-Mode-Theory-Transfer-Matrix-Method based model [23], [24], [25]. We calculate the bandwidths of the experimental results listed in Table II and Table III using the nulls method [26].

Fig. 9 shows the main band response of our CDC3 device. The as-drawn simulation (Fig. 9(a)) shows an ideal bandwidth of 11.5 nm. Our as-predicted simulation (Fig. 9(b)) shows a reduced bandwidth of 5.6 nm. The actual (experimental) bandwidth of 6.4 nm (Fig. 9(c)) closely correlates with the predictions of the lithography model.

TABLE III
CONTRA-DC SR-BAND BANDWIDTHS

Device Name	Ideal As-Drawn (nm)	Lithography As-Predicted (nm)	Experimental (nm)
CDC1	5.6 ± 0.009	1.8	2.2
CDC2	6.4 ± 0.051	1.7	2.6
CDC3	11.1 ± 0.134	6.0	5.4
CDC4	10.4 ± 0.190	4.8	6.1

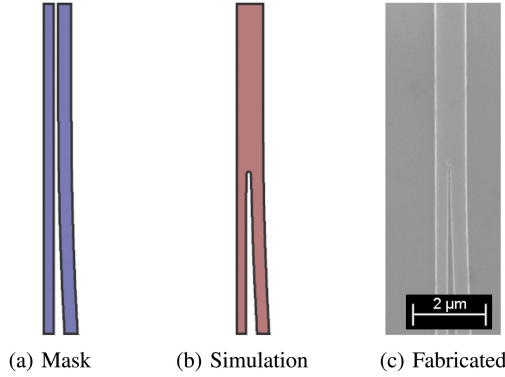


Fig. 11. (a) A coupler design with a gap of 100 nm between the two waveguides. (b) Our simulation indicates that the device will not be fabricated successfully. (c) The SEM of the fabricated device confirms our prediction (the waveguides have merged). The SEM was taken using the Carl Zeiss NTS Ltd. Sigma scanning electron microscope at a magnification of 5000x, using a voltage of 15 kV.

Furthermore, Fig. 10 shows the SR band response of our CDC3 device. The drop-port response is illustrated for readability purposes. In the ideal as-drawn simulation, the SR bandwidth is shown to be 11.1 nm (Fig. 10(a)). Using the lithography model, we predict that the bandwidth will be reduced to 6.0 nm (Fig. 10(b)). The experimental result, shown in Fig. 10(c), has a SR bandwidth of 5.4 nm.

Table II and Table III list the main band bandwidths and the SR band bandwidths respectively, for the experimental, the as-drawn simulation, and the as-predicted simulation. The ideal as-drawn simulations include process width variations from Ref. [27]. Each as-predicted simulation showed a significant improvement in accuracy over the as-drawn simulation for both the main bandwidth and the SR bandwidth.

IV. DESIGNING FOR MANUFACTURABILITY

In this section, we demonstrate a method of designing for manufacturability (DFM) that is akin to OPC practices on the CMOS platform [9], [10], [11], [12], [13]. Using the lithography model, a device's variation tolerance can be evaluated prior to fabrication. In Fig. 11(a), we demonstrate a directional coupler with a gap of 100 nm. the lithography model predicts that the coupler will not be properly fabricated using the 193 nm DUV lithography process, see Fig. 11(b). The result, shown in the SEM image (Fig. 11(c)), confirms that the two waveguides have merged, and is consistent with the lithography model prediction.

Thus, the predictions of the lithography model can be used by designers to make adjustments to their designs via several iterations of redesign. Here, we demonstrate an example the

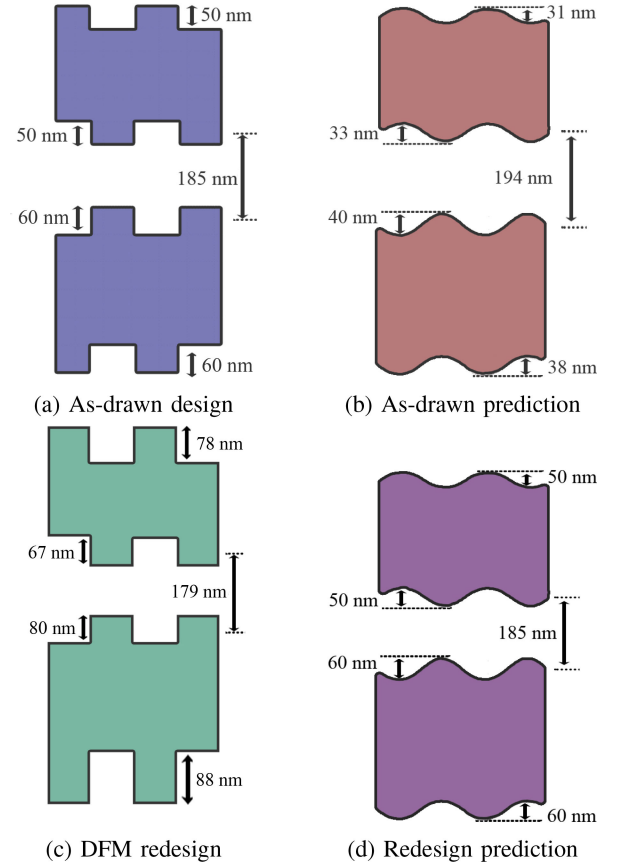


Fig. 12. (a) The as-drawn gap and ΔW parameters of CDC3 is shown. (b) A lithography prediction of the as-drawn parameters. The results show asymmetry for the ΔW s and a larger gap. (c) A redesign of CDC3 using the information obtained from (b). (d) The lithography prediction of the redesigned CDC3. The results indicate that the ΔW s and gap sizes will match the original as-drawn values.

redesign of the CDC3 device listed in Table I. The intended design of CDC3 is shown in Fig. 12(a). The lithography model predicts that the gap will increase and that ΔW_{inner} and ΔW_{outer} will reduce in size by different amounts (Fig. 12(b)).

With the prediction of the changes described above, we perform a redesign of CDC3. Our aim is to produce a predicted result in which the gap and the ΔW s match the intended parameters. First, we decrease the distance between the two waveguides, as we know that the lithography effects will widen gap. Next, we increase ΔW_{inner} while taking note that our changes will also effect the gap. Finally, we increase ΔW_{outer} until the predicted result for ΔW_{outer} is equal in size to the predicted ΔW_{inner} . This process is repeated until the prediction achieves our objective, i.e., the gap = 185 nm and $\Delta W = 50, 60$ nm for the top and bottom waveguides, respectively.

Our redesigned CDC3, shown in Fig. 12(c), has a gap of 179 nm and a ΔW_{inner} of 67 nm and ΔW_{outer} are 78 nm for the top waveguide, and ΔW_{inner} of 80 nm and ΔW_{outer} are 88 nm for the bottom waveguide. The predicted result for this redesign shows that the gap and ΔW s will have the originally intended values, see Fig. 12(d).

As an extension of this work, the DUV lithography model can be used in conjunction with EBL fabrication. Specifically,

designers can fabricate their lithography-sensitive structures using a rapid-prototyping facility, validate their design by measurement, then subsequently submit for low-volume and high-volume DUV foundry fabrication.

V. CONCLUSION

In conclusion, we have built a lithography model using data from fabricated test patterns on a 193 nm DUV lithography process. Our model shows a high degree of similarity to SEM images of fabricated test pattern shapes and demonstrates accuracy improvements in bandwidth predictions for our contra-DC's self-reflection band, the critical test for high performance contra-DCs, and an excellent lithography benchmark. Lastly, we proposed a DFM approach using our computational lithography model. We introduce into our design adjustments to the ΔW and gap parameters of the contra-DC, which the lithography model suggests will resolve the mismatch in the intended ΔW and gap parameters of those measured after fabrication. The lithography model and DFM concept presented in this paper demonstrate the benefits OPC can provide to silicon photonics design. The results greatly encourage further research into adapting CMOS OPC strategies [10], [11], [12] for use in the silicon photonics field.

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