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Experimental realization of subwavelength plasmonic slot waveguides on a silicon platform

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We report the experimental realization of horizontal plasmonic slot waveguides capable of subdiffraction modal confinement at IR wavelengths. These waveguides have a propagation length of $\sim 6\lambda_g$ and are monolithically integrated with conventional silicon photonic waveguides on the same silicon-on-insulator platform. Direct coupling of light from the silicon waveguides to the plasmonic waveguides was achieved with an efficiency of 30% using taper-funnel couplers to obtain mode matching between the two waveguide systems.

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Plasmonic waveguides are attracting much attention owing to their ability to spatially confine light below the diffraction limit [1], thereby potentially enabling photonic device integration on a scale not accessible with conventional dielectric waveguide-based photonic integrated circuits. To date, various plasmonic waveguide structures have been proposed and investigated [2–5] for planar photonic integration. In general, plasmonic waveguides can be classified into three basic types: insulator–metal–insulator (IMI), insulator–metal (IM), and metal–insulator–metal (MIM). As discussed in [6], only waveguides of the MIM type can provide true subdiffraction modal confinement, although the propagation loss is larger than the other two types. For dense photonic integration, the in-plane (or horizontal) plasmonic slot waveguide (PSW) geometry proposed in [3,7] and typically depicted in Fig. 1(a) is especially attractive because of its strong lateral mode confinement, which enables light to propagate through very sharp waveguide bends with a low bending loss.

To date, very few experimental demonstrations of these horizontal PSWs at subwavelength dimensions have been reported owing to the fabrication challenge in realizing nanometer scale waveguides and the lack of an efficient method of coupling light into and out of the nanoscale metal slot. Plasmonic propagation in vertical MIM waveguide structures composed of a 100 nm thick Si_3N_4 layer sandwiched between two Ag thin films was demonstrated [8] with a propagation length of 5λ; however, the coupling method used was inefficient, and the vertical slot waveguide structure may not be the best geometry for realizing very sharp bends necessary for dense planar integration. Chen *et al.* [9] fabricated plasmonic waveguides by coating the top and side walls of a Si waveguide with gold; however, the use of a high-index dielectric such as Si as the waveguide core and the presence of the top Au cladding in theory tend to lead to a high propagation loss. Recently Tian *et al.* [10] reported the fabrication of PSWs using a focused ion beam (FIB). Because of the index mismatch between the substrate (SiO_2) and cladding (air), the structures had an asymmetric vertical mode profile, and the reported propagation length was only 1.7 μm. We also note that the channel plasmon waveguide in [4] also belongs to the MIM type and can potentially have a low loss when the core material is air; however, these reported structures had relatively large dimensions (1.2 μm deep and 500 nm wide V grooves).

In this Letter we report the experimental realization of subwavelength horizontal PSWs with near symmetric mode profile on a silicon-on-insulator (SOI) platform. To efficiently couple light into and out of the plasmonic waveguides, the devices were monolithically integrated with conventional Si photonic waveguides on the same SOI substrate, and direct coupling between the two waveguide systems was achieved via taper-funnel mode transformers. The nanometer-sized plasmonic slot channels were defined using electron beam lithography (EBL) and patterned using argon ion milling, demonstrating the suitability of the latter process as an alternative to the FIB for fabricating nanoplasmonic devices.

Figure 1(a) illustrates the cross-section geometry of the horizontal PSW consisting of a 200 nm wide channel patterned into a 200 nm thick gold layer. The metal layer is assumed to reside directly on the

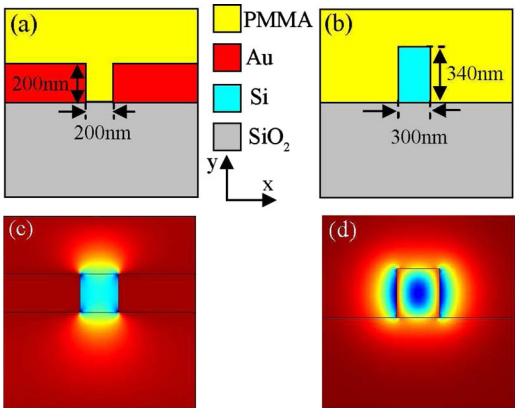

Fig. 1. (Color online) (a) and (b) Schematics of the cross section of the PSW and the Si waveguide, respectively; (c) fundamental quasi-TEM and (d) fundamental TE mode (E_x) at 1550 nm wavelength for waveguide in (a) and (b), respectively.

buffer oxide layer of the SOI chip where the Si layer has been selectively removed. The waveguide is covered with a poly(methyl methacrylate) (PMMA) cladding layer having a refractive index of 1.49, which is closely matched to that of the SiO_2 substrate (1.45) to produce a symmetrical mode profile in the vertical direction for better coupling with the Si waveguide. Figure 1(c) shows the E_x field distribution in the PSW at the 1550 nm wavelength computed using a finite element method (FEM) mode solver with a permittivity value of $\varepsilon = -115.056 + 11.128j$ [11] assumed for gold. As seen from the plot and discussed in detail in [7], the waveguide supports a tightly confined quasi-transverse-electromagnetic (quasi-TEM) plasmonic mode.

Coupling of light into the plasmonic waveguide was achieved via an on-chip Si dielectric waveguide having a nominal width of 300 nm and a thickness of 340 nm (which corresponded to the Si layer thickness of the SOITEC SOI wafer used in the fabrication). The cross section and the fundamental TE mode of the Si waveguide are shown in Figs. 1(b) and 1(d), respectively. To match the mode profiles of the plasmonic and Si waveguides, we employed a taper-funnel structure as shown in Fig. 2(a), where the Si waveguide is tapered from a width of $w1 = 300$ nm down to a width of $w2 = 200$ nm over a length of 1.5 μm, and the plasmonic channel is expanded to a width of $w3 = 800$ nm over a length of $L = 1$ μm, forming a funnel-like structure to collect light radiated from the tip of the Si waveguide. Figure 2(b) shows the E_x field distribution in the horizontal plane through the center of the funnel obtained from a three-dimensional finite-difference time-domain (3D-FDTD) simulation of the structure at $\lambda = 1550$ nm. The plot shows the initial expansion of the mode of the Si waveguide taper to match the plasmonic mode at the open end of the funnel, and the subsequent focusing of light in the funnel down to the mode of the narrow slot waveguide. The coupling efficiency, defined as the ratio of the power transmitted into the PSW to the input power in the Si waveguide, was computed to be 33%. In our initial implementation, no attempt was made to optimize the coupler parameters; however, we note that the coupling efficiency can be further improved by optimizing the taper-funnel geometry, as well as the thickness of the Si waveguide to achieve a better mode matching between the two waveguide systems.

We fabricated a set of PSWs with various lengths on a SOITEC SOI wafer consisting of a 340 nm c-Si layer on a 1 μm thick buried SiO_2 layer. Each plasmonic waveguide was coupled to a Si waveguide at both ends via a taper-funnel coupler. Figure 3 summarizes different stages of the fabrication process flow. Starting with a blank SOI substrate, as shown in Fig. 3(a), we defined the Si waveguides using the EBL with PMMA as the electron beam resist. The pattern was then transferred to the Si layer by inductively coupled plasma reactive ion etching (ICPRIE), resulting in the Si waveguides and tapers as shown in Fig. 3(b). Another PMMA layer was spun onto the chip and a second EBL step was used to open a rectangular window between the two Si taper tips where the plasmonic waveguide was to be defined. A 200 nm thick layer of gold was sputtered onto the chip, followed by metal liftoff in acetone to leave a rectangular gold layer between the Si tapers as shown in Fig. 3(c). A third EBL step was then performed on the gold layer to define the PSW channel and funnels. The PMMA mask (495 PMMA A6, MicroChem) used in this EBL step had a thickness of 415 nm, obtained after spinning at 4000 rpm for 40 s and baked at 180°C for 30 min. After resist development and a post-bake at 120°C for 10 min, the pattern was transferred into the gold layer by Ar ion beam milling to a depth of 200 nm to remove all the gold in the slot channel. The resulting structure is shown in Fig. 3(d). The inset of Fig. 4(a) shows a scanning electron microscope (SEM) image of a typical fabricated structure having a 6 μm long PSW coupled to two Si waveguides via two taper-funnel couplers. The width of the slot channel was measured to be around 170 nm, slightly less than the designed value of 200 nm due to lithography and the etching bias. Also, ion milling caused the sidewalls of the metallic channel to be slightly angled, as can be seen from the SEM image.

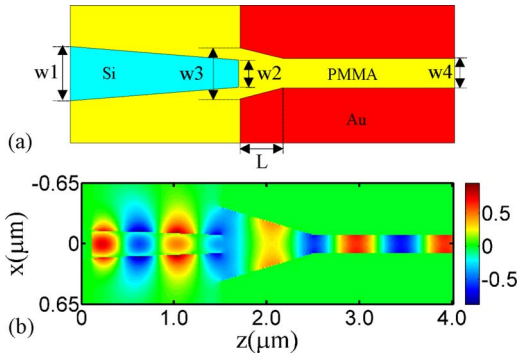

Fig. 2. (Color online) (a) Top-view schematic of the Si-plasmonic taper-funnel coupler with dimensions of $w1 = 300$ nm, $w2 = 200$ nm, $w3 = 800$ nm, $w4 = 200$ nm, $L = 1$ μm. (b) 3D-FDTD result of the E_x field distribution at 1550 nm wavelength taken at the central horizontal plane of the funnel.

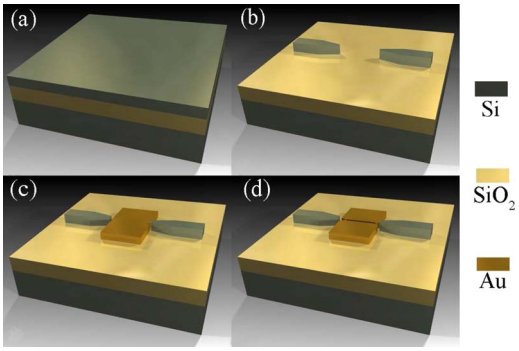

Fig. 3. (Color online) Schematic of the fabrication process flow: (a) the blank SOI substrate, (b) the Si tapers after the first EBL step and ICPRIE etching, (c) deposition of the Au layer for the plasmonic waveguide after the second EBL and liftoff, (d) the PSW and funnels after the third EBL step and Ar ion milling.

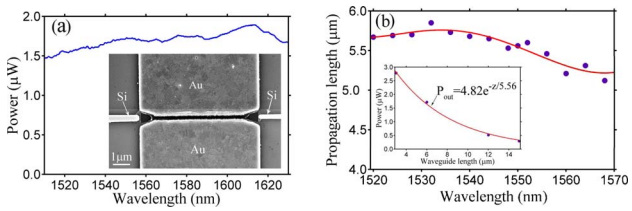

Fig. 4. (Color online) (a) Transmitted power through a 6 μm long PSW as a function of wavelength; inset, SEM image of the fabricated PSW with both ends coupled to Si waveguides via taper-funnel couplers. (b) Propagation length of PSW as a function of wavelength; inset, transmitted power as a function of the plasmonic waveguide length at the 1550 nm wavelength, with the solid curve representing the exponential fit.

The entire chip was next covered with a 1 μm thick PMMA layer as the top cladding and cleaved to expose the Si waveguide facets for light coupling with a fiber. The length of the Si waveguide connected to each end of the PSW was about 1.5 mm. Light from a tunable cw laser with the polarization set to TE using a fiber polarization controller was coupled into the input Si waveguide via a lensed fiber. A second lensed fiber was used to collect the transmitted light at the output Si waveguide for detection by an InGaAs photodetector. Figure 4(a) shows a typical spectral scan of the average transmitted power through a 6 μm long PSW. From the measurements of the transmitted powers through PSWs of different lengths, the attenuation in the PSW can be determined by fitting the transmitted power with an exponential function of the form $P_{\text{out}}=P_{\text{in}}\eta^2\exp(-z/L_p)$, where η is the taper-funnel coupling efficiency, L_p is the propagation length, and P_{in} and P_{out} are the powers in the input and output silicon waveguides, respectively. A typical curve fit is shown in the inset of Fig. 4(b) for measurement data at the 1550 nm wavelength, which yields a propagation length of $L_p=5.56$ μm and $P_{\text{in}}\eta^2=4.82$ μW. By performing the fit at different wavelengths, we obtained a plot of the propagation length versus wavelength over the range 1520–1570 nm as shown in Fig. 4(b). It is seen that the propagation length is relatively constant at about 5.5 ± 0.3 μm, implying that the loss in the PSW is fairly independent of the wavelength over this range. To determine the coupling efficiency of the couplers, we used an independent measurement of a straight Si waveguide having no plasmonic waveguide to determine the input power in the Si waveguide to be $P_{\text{in}}=53$ μW. Using the fitted value of $P_{\text{in}}\eta^2=4.82$ μW in the inset of Fig. 4(b), we obtained a coupling efficiency of $\eta=30\%$ for each coupler. This value is in good agreement with the theoretical value of 33% predicted from our 3D-FDTD simulation.

Using the FEM mode solver, we determined that the theoretical value for the propagation length of a PSW having a width of 170 nm and a height of 200 nm is 10.9 μm. This value is about twice as large as the experimental value obtained from our measurements. The discrepancy between the experimental and theoretical values may be attributed to the quality of the metal film as well as scattering from the rough sidewalls of the metal slot channel. From high-magnification SEM images, we observed our sputtered gold films to have many grain boundaries, which may lead to additional scattering of the surface plasmons. As a result the gold layer might have a larger extinction coefficient than the value from [11] used in the theoretical calculation. Another source of loss in our fabricated PSWs is scattering from the rough sidewalls of the metallic slot channel introduced during the Ar ion milling process. We note that the selectivity and resolution of ion milling are related to the hardness of the resist. Since PMMA is a relatively soft material, we expect that a harder EBL resist such as hydrogen silsesquioxane(HS6) or the use of a hard mask such as Al_2O_3 will allow metal slot channels with smoother and more vertical sidewalls to be fabricated. Compared to the FIB, Ar ion milling is a much faster and more economical process, and our experimental results suggest that Ar ion milling can potentially have broad applications in the fabrication of nanoplasmonic structures.

In summary, we reported the fabrication and experimental performance of subwavelength PSWs on an SOI platform. A propagation length of 5.56 μm (or $\sim 6\lambda_g$, where λ_g is the guided wavelength) was achieved. By integrating plasmonic and Si waveguides on the same SOI chip, efficient coupling of light between the two waveguide systems can be achieved via taper-funnel couplers. Achieving seamless transition between the Si and plasmonic waveguide systems is important, because it allows both plasmonic and Si photonic functionalities to be incorporated on the same substrate, paving the way to the eventual monolithic integration of photonics, plasmonics, and electronics all on the same chip.

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