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Compact all-optical interferometric logic gates based on one-dimensional metal–insulator–metal structures

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ABSTRACT

The whole set of fundamental all-optical logic gates is realized theoretically using a multi-channel configuration based on one-dimensional (1D) metal–insulator–metal (MIM) structures by leveraging the linear interference between surface plasmon polariton modes. The working principle and conditions for different logic functions are analyzed and demonstrated numerically by means of the finite element method. In contrast to most of the previous studies that require more than one type of configuration to achieve different logic functions, a single geometry with fixed physical dimensions can realize all fundamental functions in our case studies. It is shown that by switching the optical signals to different input channels, the presented device can realize simple logic functions such as OR, AND and XOR. By adding signal in the control channel, more functions including NOT, XNOR, NAND and NOR can be implemented. For these considered logic functions, high intensity contrast ratios between Boolean logic states "1" and "0" can be achieved at the telecom wavelength. The presented all-optical logic device is simple, compact and efficient. Moreover, the proposed scheme can be applied to many other nano-photonic logic devices as well, thereby potentially offering useful guidelines for their designs and further applications in on-chip optical computing and optical interconnection networks.

1. Introduction

As one of the most important elements in optical computing networks, all-optical logic gates have recently attracted considerable attention [1–3]. The previously demonstrated all-optical logic gates can be divided into two major classes: one based on linear optical interferences [4–10], and the other enabled by nonlinear optical effects [11–16]. Since the logic operations of linear gates (also known as interferometric logic gates) depend on the relative optical phase of two input signals, the realizations of different Boolean logic states can thus be enabled by the constructive or destructive interference of the signals at the output region of the devices. Due to the fact that it is difficult to precisely control the optical phase difference, these linear type logic gates typically suffer from both inherent instabilities and relatively low intensity contrast ratios between the logic states "1" and "0" [17,18].

One of the most promising solutions to overcome the above challenges in linear all-optical logic gates is by device miniaturization and monolithic integration [3]. However, most of the interferometric logic gates based on conventional photonic structures such as photonic crystals and silicon components [4,8] are fundamentally subject to the diffraction limit, which restricts the further downscaling of their physical dimensions below the wavelength scale. In contrast to these dielectric-based counterparts, photonic components employing surface plasmons hold the promise to confine and transport light at the truly subwavelength scale [19]. Along with many other advantageous such as enabling simultaneous transmission of light and electric signals through the same configuration and allowing easy integrations with other configurations, plasmonic nanostructures have been widely employed to build ultra-compact high-performance opto-electronic components [20]. During recent years, all-optical logic devices based on surface plasmons have attracted increasing research attention and have already been regarded as intriguing alternatives to their photonic crystal based logic counterparts.

To date, several types of plasmonic interferometric logic devices have been intensively studied, which are based on metallic nanowire networks [8,9], metal slot waveguides [10,11] as well as hybrid plasmonic structures [9]. However, in most of these studies, two or even more types of different configurations are required in order to implement all fundamental logic functions, which introduce additional complexity for the designs and applications of these logic devices. To overcome this limitation, here we propose a novel all-optical logic device based on plasmonic waveguides. Through comprehensive numerical investigations on its properties at the telecom wavelength, we demonstrate the realization of the whole set of fundamental logic functions, i.e., OR, AND, NOT, XOR, XNOR, NAND and NOR, without any need of

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modifying or reconfiguring the device. In our design, one-dimensional (1D) metal–insulator–metal (MIM) waveguides are chosen to construct the entire logic device, due to their simple configuration as well as the capabilities of providing nanoscale light confinement, low crosstalk, reasonable propagation distance and nearly 100% transmission through sharp bends [21–26], which make them idea candidates for various ultra-compact devices [27–33] and other applications [34–37]. We show that the MIM-based logic device can effectively realize different logic functions through switching the signals in the input and the control channels. Furthermore, high intensity contrast ratios between logic states "1" and "0" can be achieved. The presented device is simple, compact, efficient and can be easily integrated with other nanophotonic devices as well, which renders it a promising building block for on-chip optical computing and optical interconnection networks.

2. Geometry of the all-optical logic device based on 1D MIM structure

The 2D geometry of the studied logic device is shown schematically in Fig. 1, which comprises four air channels cut into a silver background at the input port, while combining into a single channel at the output region. The input signals are assumed to be launched at port I_1, port I_2 and/or port I_3, whereas port C are the control port for the realizations of more complex functions. Port O is the output port for the Boolean logic states. The input channels, control channel and output channel are denoted by numbers 1–5. All the channels have the same thickness of t. As shown in Fig. 1, the vertical spacing between channels 1 and 2 is S_{12}. S_{14} denotes the separation between channels 1 and 4, while S_{23} represents the vertical distance between channels 2 and 3. In the simulations, all the corners are assumed to be 90° sharp corners. The optical characteristics of the MIM-based logic devices are investigated at $\lambda=1550$ nm by means of the finite-element method (FEM) based software COMSOL 3.5a. The permittivities of Ag and air are $\varepsilon_m=-129+3.3i$ [38] and $\varepsilon_i=1$, respectively. The modal properties of the MIM waveguides are analyzed by the eigenmode solver using the 2D *Perpendicular Wave* package in the *RF module*, whereas the operations of the logic gates are simulated by the *In-plane Harmonic Propagation* package. In order to perform a full-wave 2D numerical simulation of the mode propagation along the channels, the field distribution from the 2D eigenmode solver of a 1D MIM plasmonic waveguide is set as a source boundary condition for the 2D analysis.

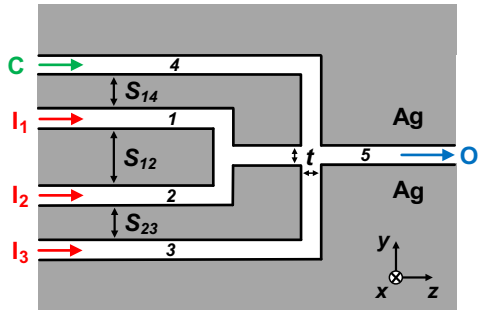

Fig. 1. Schematic of the studied logic device, which consists of four air channels embedded inside a silver background. Port I_1, port I_2 and port I_3 are the input ports where signals are excited. Port C is the control port where control signal is enabled. Port O is the output region for the Boolean logic states. The input channels, control channel and output channel are denoted by numbers 1–5, which share the same thickness of t. S_{12}, S_{14} and S_{23} are the vertical separations between the corresponding channels.

3. Guided mode's properties of 1D MIM structure

Before conducting detailed investigations on the operations of the logic gates, we firstly take a look at the surface plasmon mode traveling along a single air channel cut into a silver background, which is also the fundamental plasmonic mode supported by a one-dimensional (1D) MIM structure. The calculated results for the real part of the modal effective index ($n_{eff}=Re(N_{eff})$) and the propagation length (L) of the considered plasmonic mode are shown in Fig. 2(a) and (b) as the thickness of the air channel varies from 0 nm to 200 nm. Here, the propagation length (L) is obtained by $L=\lambda/[4\pi\mathrm{Im}(N_{eff})]$. It is seen from Fig. 2 that, both the modal effective index and the propagation loss decrease monotonically with the increased size of the air channel. By contrast, the corresponding mode size, although not shown here, gradually increases as t gets larger. To compromise between the physical dimension, modal loss and spatial size of the mode as well as ensuring a single-mode condition, here we chose a 50-nm-thick insulator layer (air channel) to construct the logic device.

Since the proposed logic device contains several parallel air channels, the coupling properties between different channels are also investigated for the MIM structures. The normalized coupling length defined as the ratio of the calculated coupling length (L_c) of the system to the propagation length (L) of the plasmonic mode supported by a single waveguide [39], is shown in Fig. 3 as the separation (S) varies from 10 nm to 100 nm. According to the coupled mode theory [40], the coupling length can be obtained by $L_c=\pi/|k_s-k_a|$, where k_s and k_a are the wavenumbers of the symmetric and anti-symmetric modes of two coupled waveguides, respectively. As seen from Fig. 3, the normalized coupling length can exceed 1 when S is larger than ~70 nm, indicating that low-crosstalk can be enabled under these circumstances. Based on the discussions of coupling characteristics, the separations between adjacent channels should be larger than the critical value to ensure successful operation of the logic device without significant crosstalk between different channels.

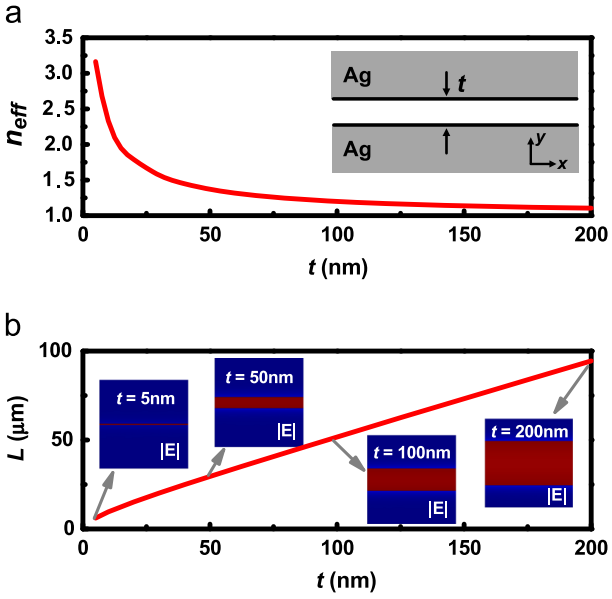

Fig. 2. (a)–(b) Dependence of the real part of the modal effective index (n_{eff}) and the propagation length (L) of the fundamental plasmonic mode on the thickness of the insulator layer (air channel). The insets in (a) shows the cross-sectional view of the MIM waveguide, whereas the insets in (b) depict the electric field for typical configurations (from left to right: $t=5$ nm, $t=50$ nm, $t=100$ nm and $t=200$ nm).

4. Working principle and operation of all-optical logic gates

In this section, comprehensive analysis of the proposed all-optical logic gates will be conducted at the telecom wavelength. The working principle of these linear type interferometric logic gates can be explained based on the wave-optics theory. Constructive interference will occur if the phase difference between two light beams is 2 $k\pi$ (k=0, 1, 2, 3,…), which corresponds to an output signal with a relatively high intensity. On the other hand, if the phase difference is $(2k+1)\pi$ (k=0, 1, 2, 3,…), then destructive interference will take effect, which results in a near-zero intensity at the output region [8]. By properly defining the threshold intensity, the Boolean logic states of "1" and "0" can be enabled based on the two types of interferences. For the studied logic device shown in Fig. 1, the differences in optical paths for various channels are related to S_{12}, S_{23} and S_{14}, respectively, which could lead to constructive or destructive interference between the input signals. In Table 1, we show the detailed settings for these channels of the studied logic device. The effective wavelength of the guided plasmonic mode in a single channel can be obtained by $\lambda_{eff}=\lambda/n_{eff}$. As shown in the table, the optical path difference between signals in channel 2 and channel 1 is 0, which also corresponds to a zero phase difference. While for either channel 3 or channel 4, the difference between its optical path and that of the channel 1 is $\lambda_{eff}/2$, thus corresponding to a phase difference of π. Therefore, constructive interference will occur for the signals at channel 1 and channel 2, whereas the light beams in channel 3 (4) and channel 1 will experience a destructive interference at the output region. Based on the above settings, the detailed geometric parameters for the studied logic device are: t=50 nm, $S_{12}=S_{23}=S_{14}$=566 nm.

In order to realize different logic functions, a combination of two or more channels in the logic device is required. In Table 2, we show the detailed settings for the realizations of the whole set of fundamental logic functions. It is illustrated that, the implementations of OR, AND, XOR functions can be enabled by a combination of two input channels. By leveraging the constructive interference between signals in channel 1 and channel 2 and properly defining the threshold intensity, OR and AND operations can be realized, respectively. While XOR function can be implemented through employing the destructive interference between light beams in channel 2 (or channel 1) and channel 3. On the other hand, for the other four logic functions, i.e. NOT, XNOR, NAND, NOR, the signal in the control channel should be excited in order to enable their operations. The NOT gate requires a combination of signals in channel 1 (or channel 2) and the control channel (channel 4) to realize a destructive interference. While for the operation of a XNOR logic gate, both channel 1 and channel 2, in combination with the control channel, should be utilized. To work as a NAND or NOR gate, the same structure that is used for the XNOR gate can be employed. However, in contrast to the XNOR gate where the input and the control signals are exactly the same, the intensity of the control signal should be two times as large as that of the input signal for the realizations of both NAND and NOR functions. By properly defining the threshold intensity, NAND and NOR functions can then be realized, respectively. Due to the fact that the phase difference can be controlled precisely by the tuning the optical path between different channels, the above gates could have large intensity contrast ratios for the Boolean logic states at the output. In the following, we will show the detailed results for the operations of different logic functions.

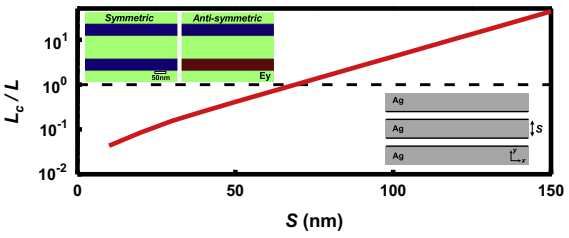

Fig. 3. The dependence of normalized coupling length (L_c/L) on the separation (S) between two MIM waveguides (t=50 nm), where the black dashed line corresponds to the critical condition of L_c/L=1. The lower inset shows the geometry of the coupling system comprising two vertically parallel MIM waveguides, whereas the upper insets depict the E_y field distributions of the symmetric and anti-symmetric modes in a MIM-based coupling system with a separation distance of 100 nm.

Table 1
Settings of different channels in the studied logic device with reference to the first channel (Channel 1).

Channel	2	3	4
Optical path difference	0	$\lambda_{eff}/2$	$\lambda_{eff}/2$
Phase difference	0	π	π
Interference type	Constructive	Destructive	Destructive

4.1. The operation of OR gate

The working principle of the OR gate is shown in Table 3. It is clearly seen that, by activating the input ports I_1 and I_2 without the need of enabling the control port, the output logic states can be varied from 0 to 1 based on the combinations of various input signals. The calculated magnetic field distributions for different logic states are shown in Fig. 4. As seen in Fig. 4(a) and (b), if a single beam is injected into input port I_2 or I_1, the light signal can then transmit through channel 2 or channel 1, and be output at

Table 3
The working principle of OR logic function.

Logic states	Input port I_1	Input port I_2	Input port I_3	Control port C	Output port O
OR	0	0		OFF	0
	0	1		OFF	1
	1	0		OFF	1
	1	1		OFF	1

Table 2
The combination of different channels for the operations of the whole set of fundamental logic functions.

Logic states	Input port I_1	Input port I_2	Input port I_3	Control port C	Special settings
OR	Enabled	Enabled			
AND	Enabled	Enabled			Threshold defined
XOR		Enabled	Enabled		
NOT	Enabled			Enabled	
XNOR	Enabled	Enabled		Enabled	
NAND	Enabled	Enabled		Enabled	Enhanced amplitude required at the control port
NOR	Enabled	Enabled		Enabled	Threshold defined along with enhanced amplitude at the control port

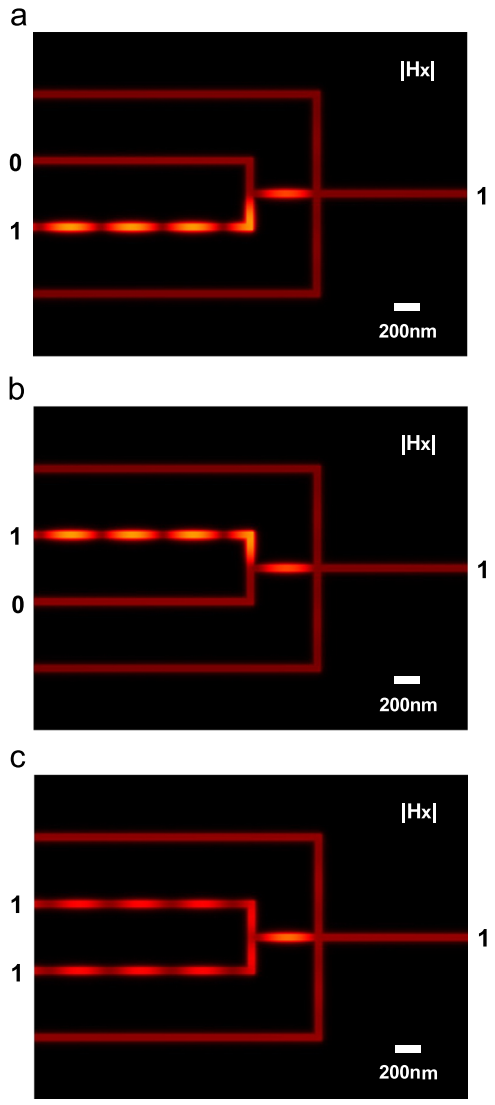

Fig. 4. The simulated field distributions ($|H_x|$) for OR logic gate: (a) logic operation of "0 OR 1=1"; (b) logic operation of "1 OR 0=1"; (c) logic operation of "1 OR 1=1".

port O, which corresponds to the logic operation of "0 OR 1=1" or "1 OR 0=1". On the other hand, if both port I_1 and port I_2 are injected with input beams simultaneously, the light signals can propagate through channel 1 and channel 2, and combine into channel 5. Due to the fact that channel 1 and channel 2 share the same optical path (i.e. no path difference between them), the phase difference between the two signals is zero, which results in a constructive interference between them and consequently leads to the high output intensity at port C. Based on this process, the logic operation of "1 OR 1=1" can be realized, as shown in Fig. 4(c).

4.2. The operation of AND gate

In order to realize AND logic functions, the same configuration that is used for the OR logic gate can be adopted. Based on the previous studies on nanowire network based logic gates [8,11], AND logic operations can be realized by properly defining specific intensity thresholds. In Table 4, the working principle of the AND gate and the related settings are shown in detail. Only when both the input ports are injected with light signals can the logic state of "1" be realized at the output port. The calculated magnetic field distributions of different logic states are depicted in Fig. 5. As seen in Fig. 5(a) and (b), if a single beam is injected into input port I_2 or I_1, the light signal could then transmit through channel 2 or channel 1, and be output at port O. While Fig. 5(c) shows that the light signal can propagate along channel 1 and channel 2 and combine into channel 5 at the output region when both port I_1 and port I_2 are injected with input beams simultaneously. By defining an appropriate intensity threshold between the intensities of the above two cases, the logic gates of "0" and "1" can then be realized, respectively. Based on the definition, the former two processes are related to the logic operations of "0 AND 1=0" and "1 AND 0=0", whereas the latter process corresponds to the logic function of "1

Table 4
The working principle of AND logic function.

Logic states	Input port I_1	Input port I_2	Input port I_3	Control port C	Output port O
AND	0	0		OFF	0
	0	1		OFF	0
	1	0		OFF	0
	1	1		OFF	1

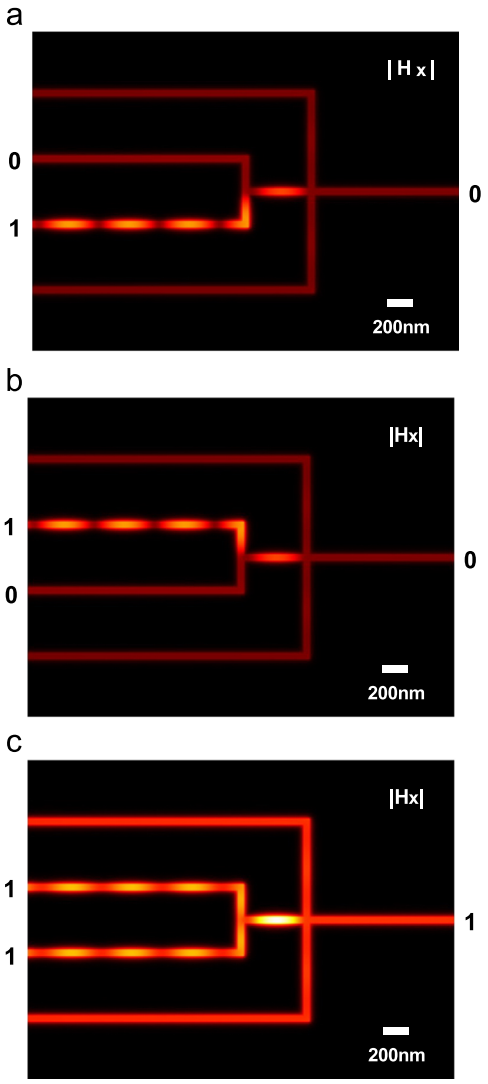

Fig. 5. The simulated field distributions ($|H_x|$) for AND logic gate: (a) logic operation of "0 AND 1=0"; (b) logic operation of "1 AND 0=0"; (c) logic operation of "1 AND 1=1".

Table 5
The working principle of XOR logic function.

Logic states	Input port I_1	Input port I_2	Input port I_3	Control port C	Output port O
XOR		0	0	OFF	0
		0	1	OFF	1
		1	0	OFF	1
		1	1	OFF	0

AND 1=1". Calculations reveal that the intensity contrast ratios between these logic states of "1" and "0" can be as high as ~6 dB for the studied AND logic gate.

4.3. The operation of XOR gate

To implement the XOR logic functions, the destructive interference between light signals in different channels is needed. Here we use channel 2 and channel 3 to realize the XOR operation. The working principle of the gate is shown in Table 5, while the calculated field distributions for different logic states are shown in Fig. 6. As seen in Fig. 6(a) and (b), if a single beam is injected into input port I_3 or I_2, the light signal could then transmit through channel 3 or channel 2, and be output at port O, which corresponds to the logic operation of "0 XOR 1=1" or "1 XOR 0=1". On the other hand, if both port I_2 and port I_3 are injected with input signals, the light beams can propagate through channel 2 and channel 3, and combine into channel 5 at the output region. According to the settings of the channels shown in Table 1, the optical path difference between channel 2 and channel 3 is $\lambda_{eff}/2$, which corresponds to a phase difference of π. Therefore, the destructive interference between the light signals in the two channels results in an output with an approximately zero intensity at port O, which corresponds to the implementation of the logic operation "1 XOR 1=0", as shown in Fig. 6(c). For the studied AND logic gate, the intensity contrast ratios between logic states "1" and "0" can be as high as ~15 dB.

4.4. The operation of NOT gate

The implementation of NOT logic functions can be enabled through adopting a similar configuration to that employed for XOR operations, since both of them are based on the destructive interference between signals in two channels. Here we employ channel 1 and the control channel (channel 4) to realize the NOT operations, with the working principle of the gate and the corresponding field distributions of different logic states shown in Table 6 and Fig. 7, respectively. The intensities for the input and control channels are set the same. It is illustrated in Fig. 7(a) that, if a single beam is injected into input port I_1, the light signal could then transmit through channel 1, and combine with the signal from the control channel, which leads to a near-zero output at port O due to the destructive interference between them. This corresponds to the logic operation of "NOT 1=0". By contrast, if no signal is injected into the input port, the light signal from the control port could travel along channel 4 and channel 5, and be output from port O, which corresponds to the implementation of the logic operation "NOT 0=1", as can be seen from Fig. 7(b). Simulation results indicate that the intensity contrast ratios between logic states "1" and "0" can be as high as ~15 dB for the studied NOT gate.

4.5. The operation of XNOR gate

For the realizations of XNOR logic functions, input channels including channel 1 and channel 2, along with the control channel should be utilized. The intensities for the input and control channels are the same. The working principle of the XNOR gate is shown in Table 7 and the corresponding field plots for different logic states are shown in Fig. 8. As seen in Fig. 8(a), the light beam from the control port can propagate through channel 4 and be output at port O when no signal light is injected into the input ports, which results in the logic operation of "0 XNOR 0=1". If a single beam is injected into input port I_2 or I_1, the light signal could then transmit through channel 2 or channel 1, and combine with the signal from the control port at channel 5. Due to the complete destructive interferences between the input and control signals, the intensities for the two cases at the output port are approximately zero, which lead to the logic operations of "0 XNOR

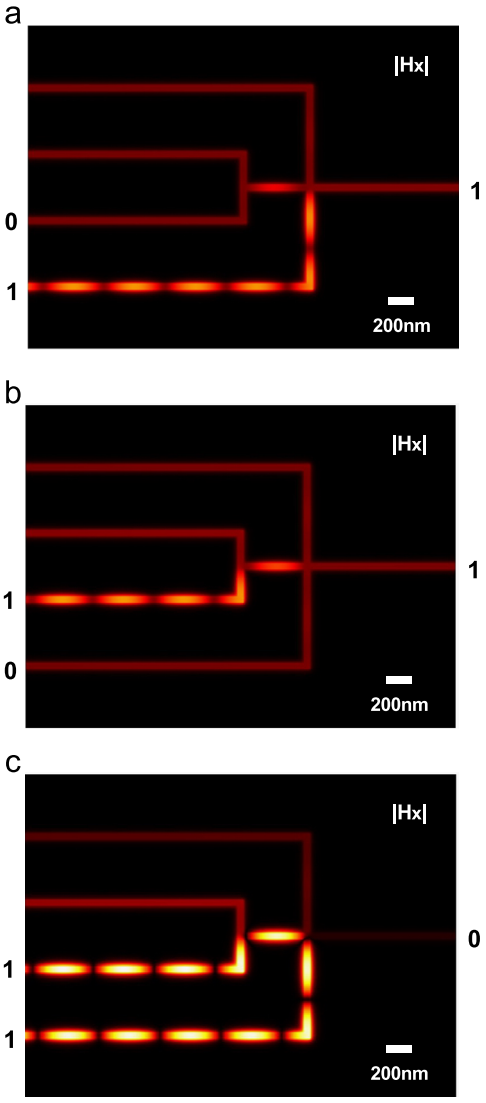

Fig. 6. The simulated field distributions ($|H_x|$) for XOR logic gate (a) logic operation of "0 XOR 1=1"; (b) logic operation of "1 XOR 0=1"; (c) logic operation of "1 XOR 1=0".

Table 6
The working principle of NOT logic function.

Logic states	Input port I_1	Input port I_2	Input port I_3	Control port C	Output port O
NOT	0			ON	1
	1			ON	0

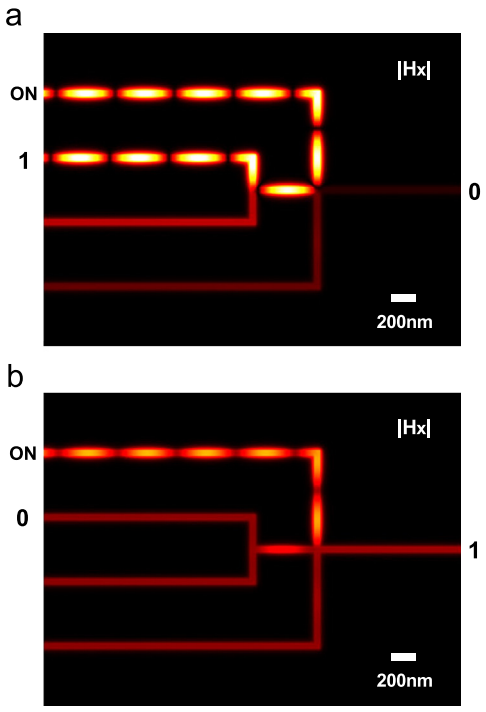

Fig. 7. The simulated field distributions ($|H_x|$) for NOT logic gate: (a) logic operation of "NOT 1=0"; (b) logic operation of "NOT 0=1".

Table 7
The working principle of XNOR logic function.

Logic states	Input port I_1	Input port I_2	Input port I_3	Control port C	Output port O
XNOR	0	0		ON	1
	0	1		ON	0
	1	0		ON	0
	1	1		ON	1

1=0" and "1 XNOR 0=0", respectively. If both port I_1 and port I_2 are injected with input beams simultaneously, the light signal can propagate through channel 1 and channel 2, and finally combine with the control signal at channel 5. Since the intensity of the combined light signals is larger than that of the control signal, an incomplete destructive interference between them occurs, which makes the intensity of the output remain relatively high. Based on this process, the logic operation of "1 XNOR 1=1" can thus be realized. For the currently studied XNOR logic gate, the intensity contrast ratios between logic states "1" and "0" can be as high as ~15 dB.

4.6. The operation of NAND gate

In order to realize NAND logic operations, the same configuration that is used for the XNOR logic gate can be adopted. In contrast to the XNOR gate where the input and the control signals are set exactly the same, the intensity of the control signal should be two times as large as that of the input signal for the realizations of NAND operations. The working principle of the NAND gate and its related settings are shown in Table 8, whereas the calculated magnetic field distributions of different logic states are depicted in Fig. 9. When no light signal is injected into the input ports, the light beam from the control port can propagate through channel 4, and be output at port C. Owing to the high intensity of the control signal, the signal at the output region is strong, as can be seen from Fig. 9(a). This process corresponds to the logic operation of "0

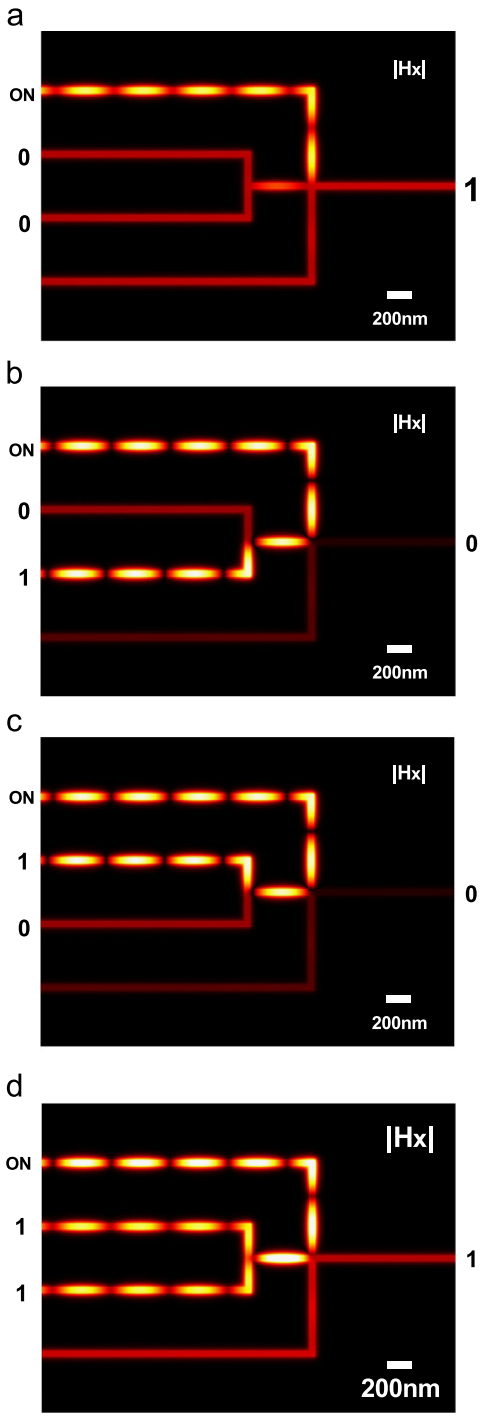

Fig. 8. The simulated field distributions ($|H_x|$) for XNOR logic gate (a) logic operation of "0 XNOR 0=1"; (b) logic operation of "0 XNOR 1=0"; (c) logic operation of "1 XNOR 0=0"; (c) logic operation of "1 XNOR 1=1".

Table 8
The working principle of NAND logic function (with enhanced intensity at the control port).

Logic states	Input port I_1	Input port I_2	Input port I_3	Control port C	Output port O
NAND	0	0		ON	1
	0	1		ON	1
	1	0		ON	1
	1	1		ON	0

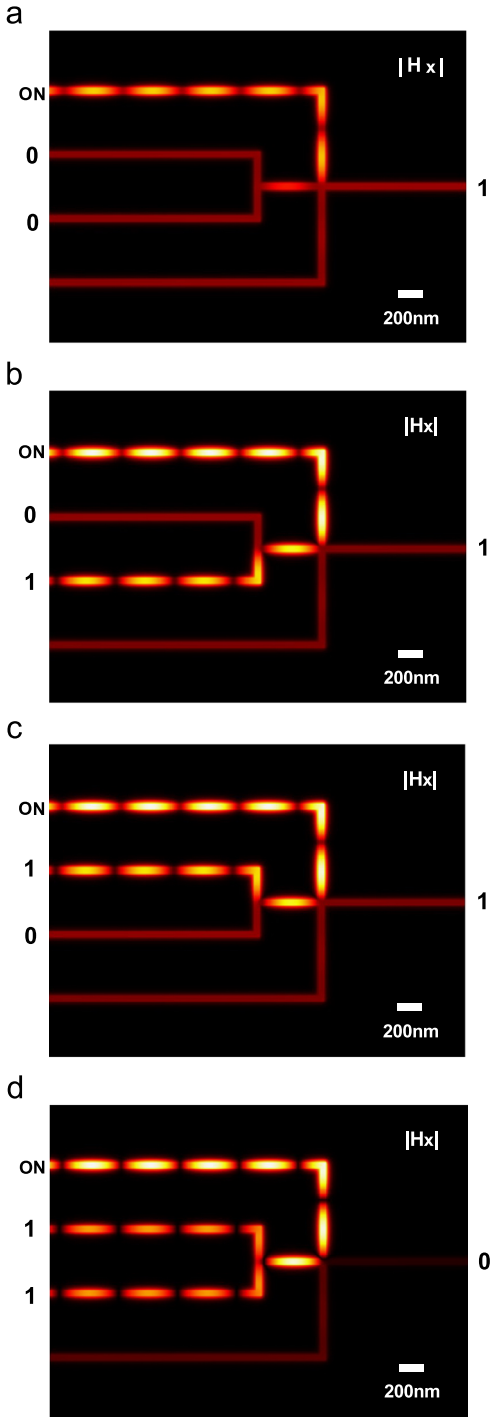

Fig. 9. The simulated field distributions ($|H_x|$) for NAND logic gate (a) logic operation of "0 NAND 0=1"; (b) logic operation of "0 NAND 1=1"; (c) logic operation of "1 NAND 0=1"; (c) logic operation of "1 NAND 1=0".

NAND 0=1". On the other hand, Fig. 9(b) and (c) illustrates that, if a single beam is injected into input port I_2 or I_1, the light signal could then transmit through channel 2 or channel 1, which combines with the control signal at channel 5 and be output at port O. Since the intensity of the control light is two times as large as that of the input light, an incomplete destructive interference between the input and control signals occurs, leading to the relatively high intensity at the output port. The logic operation of "0 NAND 1=1" or "1 NAND 0=1" can thus be enabled based on these processes. When both channel 1 and channel 2 are injected with the input signals, the complete destructive interference between the signals in the input channels and the control channel results in a nearly zero intensity at the output port, which corresponds to the logic function of "1 NAND 1=0". Simulation results reveal that the intensity contrast ratios between logic states "1" and "0" can exceed 15 dB for the studied NAND logic gate.

4.7. The operation of NOR gate

Finally, to work as a NOR gate, the same structure that is used for the NAND gate can be employed. The intensity in the control channel is doubled to ensure successful operations of the gate, which is the same as that adopted for the NAND operation. Similar to the previous studies on nanowire network based logic gates [8,11], NOR logic operations can also be realized by properly defining the intensity thresholds. In Table 9, the working principle of the NOR gate and the related settings are shown in detail. Only when no light signals are injected into the input ports can the logic state of "1" be realized at the output port. The calculated magnetic field distributions of different logic states are demonstrated in Fig. 10(a) illustrates that when no light signal is injected into the input ports, the light beam from the control port can transport through channel 4, and be output at port C. The output signal is strong due to the high intensity of the control signal. On the other hand, if a single beam is injected into input port I_2 or I_1, the light signal could then transmit through channel 2 or channel 1, combine with the control signal at channel 5 and be output at port O, as seen in Fig. 10(b) and (c). Due to the fact that destructive interference occurs between the above signals and the intensity of the control light is two times as large as that of the input light, the intensity at the output port is larger than zero but smaller than that of the control light. While Fig. 10(d) corresponds to the case where the input signals are injected in both channel 1 and channel 2. Owing to the complete destructive interference between the signals in the input channels and the control channel, the intensity at the output port is approximately zero. By defining an appropriate intensity threshold between the intensities of the above three cases, the logic gates of "0" and "1" can then be realized, respectively. Based on the definitions, the first process is related to the logic operation of "0 NOR 0=1", whereas the latter processes corresponds to the logic functions of "0 NOR 1=0", "1 NOR 0=0" and "1 NOR 1=0", respectively. Calculations reveal that for the studied NOR logic gate, the intensity contrast ratios between logic states "1" and "0" can be as high as ~15 dB.

5. Discussions

The above investigations reveal that the whole set of fundamental logic operations with relatively high extinction ratio can be realized through properly combining the signals in the input and control channels. It is worth mentioning that, in the simulations of the proposed logic device, 90° sharp corners are used for all the air

Table 9
The working principle of NOR logic function (with enhanced intensity at the control port).

Logic states	Input port I_1	Input port I_2	Input port I_3	Control port C	Output port O
NOR	0	0		ON	1
	0	1		ON	0
	1	0		ON	0
	1	1		ON	0

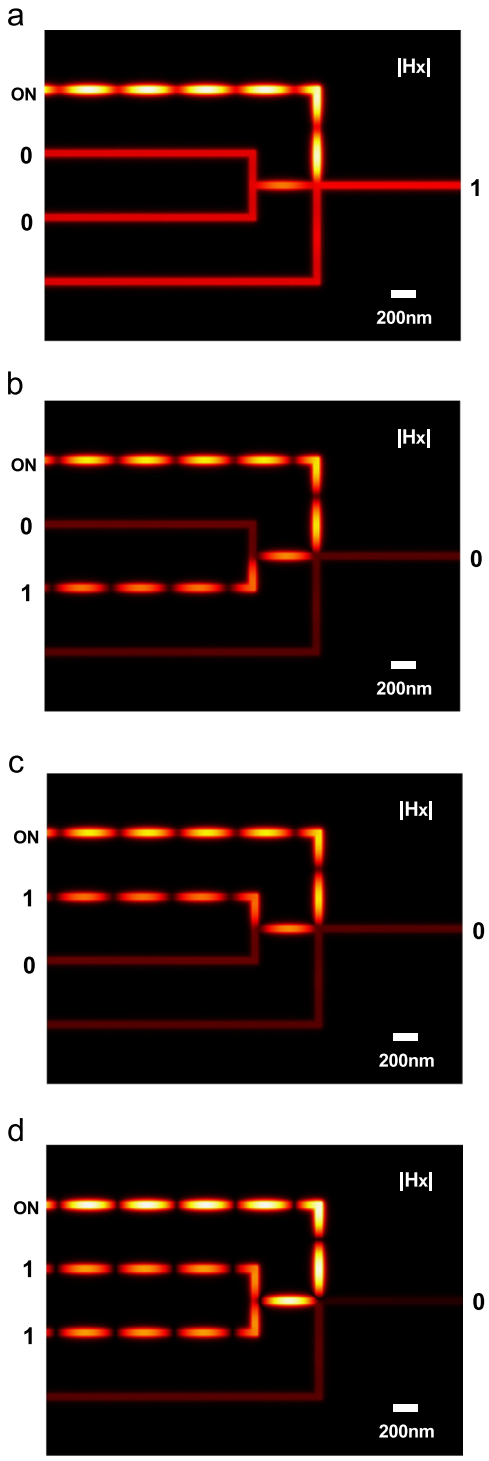

Fig. 10. The simulated field distributions ($|H_x|$) for NOR logic gate (a) logic operation of "0 NOR 0=1"; (b) logic operation of "0 NOR 1=0"; (c) logic operation of "1 NOR 0=0"; (c) logic operation of "1 NOR 1=0".

channels as a proof-of-concept. For further optimization and experimental realizations, obtuse bends with larger angles and rounded corners can be adopted to further miniaturize the propagation losses and enhance the extinction ratios between the output logic states. The efficiency of the device might also be further improved through optimizing other geometric parameters. For practical applications of these logic gates, the realistic devices are 2D configurations rather than the 1D architectures studied here. Therefore, several other important issues also need to be addressed, such as the size of the excitation laser beam [7], additional losses caused by the fabrication imperfections of the device, signal distortion, signal-to-noise ratio, bandwidth etc. Moreover, the overall size of the device could be further miniaturized by switching the operation wavelength to a even shorter range, such as 632.8 nm [5] or 830 nm [7].

6. Conclusions

In conclusion, through comprehensive numerical simulations, we have demonstrated the feasibility of building all-logic gates based on 1D MIM structures. The proposed device is capable of realizing the whole set of fundamental logic functions, i.e., OR, XOR, NOT, AND, XNOR, NAND and NOR. The operation of different functions can be enabled through switching the optical signals at the input ports and the control channels. It is revealed that intensity contrast ratios between logic states "1" and "0" as high as ~15 dB can be achieved for the studied logic functions. The work in this paper could pave the way for the experimental demonstrations and further applications of compact all-optical logic devices based on plasmonic nanostructures.

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