

Subwavelength Graphene-Based Plasmonic THz Switches and Logic Gates

Morteza Yarahmadi, *Graduate Student Member, IEEE*, Mohammad K. Moravvej-Farshi, *Senior Member, IEEE*, and Leila Yousefi, *Member, IEEE*

Abstract—In this paper, we report on the design procedure for developing subwavelength graphene-based plasmonic waveguide, performing as a THz switch or an **AND/OR** logic gate. The propagation length of the surface plasmons (SPs), stimulated by a 6 THz TM polarized incident wave along this waveguide with a top graphene layer whose chemical potential is held at $\mu_C = 300$ meV (ON state) is more than 35 times larger than that in the waveguide with $\mu_C = 0$ eV (OFF state). Numerical results, obtained from full wave simulations using a finite element method, also show that the modulation depth density obtained for the straight plasmonic switching waveguide, whose length is just about 20% of the incident wavelength, is larger than those reported to date. **Moreover, we also designed a logic AND gate composed of a straight waveguide, a Y-branch switch, and a logic OR gate composed of two face Y-branches, whose total lengths are $\sim 37\%$, $\sim 45\%$, and $\sim 53\%$ of the incident wavelength, respectively.** Simulations show that the maximum ON/OFF ratios for these subwavelength plasmonic waveguides that occur between their '1 1' and '0 0' logical states are ~ 41.37 , ~ 39.87 , and ~ 40.76 dB, respectively. These numerical data also show that the modulation depth densities obtained for these devices are also greater than those reported to date. The proposed graphene-based plasmonic switches and gates offer potential building blocks for the future digital plasmonic circuits operating around 6 THz.

Index Terms—Graphene, plasmonic logic gate, plasmonic switch.

I. INTRODUCTION

TERAHERTZ waves can be used in a wide range of applications in communications, sensing, medical imaging, spectroscopy, and ultra-fast computing [1]–[4]. In order to achieve high quality imaging, device integration, or effective nonlinear interaction in the THz frequency range, one needs to confine the electromagnetic field. A promising approach to achieve this goal is the use of plasmonics [5], [6]. In spite of being in photonics regime, metals do not support surface plasmons at THz frequencies. However, it has been recently demonstrated that graphene, as a 2-D metallic material possessing extraordinary electronic and photonic properties, can be

exploited for THz plasmonic applications [7]–[12]. In addition to advantages such as having a 2-D structure, low loss, unique response to THz radiation, graphene illustrates much larger tunability compared to a conventional 2-D electron gas (2DEG) [12]. Therefore, graphene can be utilized to develop ultra-compact, high-performance and actively-tunable devices [7], [8]. Recently, a deep sub-wavelength THz plasmonic waveguide has been proposed, by means of graphene–metal structure [12]. This type of sub-wavelength structure, unlike the conventional or metamaterial waveguides is not bulky, and strongly confines electromagnetic fields as desired. Following this work, we have shown that this type of the waveguide can be used to develop THz plasmonic switches with desired characteristics [13], [14].

Electronic device integration faces two major obstacles- interconnect delays and losses and electron velocity limited data transmission rates [15]. These can be overcome by use of appropriate high frequency devices. Moreover, integration of ordinary diffraction-limited high frequency components into nano-scaled electronic chips faces a new constraint [16]–[18]. On the contrary, surface plasmonic devices with subwavelength dimensions can smoothly be integrated into nano-scaled electronic chips [18]. Yet, a metal-based plasmonic system experiences relatively short propagation length, due to the metal inherent loss. A total promising solution that can overcome this deteriorating obstacle is graphene-based nano-plasmonics [9], [19].

In this paper, we propose a functional, ultra-compact, and low power consumption graphene-based plasmonic waveguides acting as THz switches and logic gates with subwavelength dimensions, suitable for data transmission in modern telecommunication systems. The modulation mechanism is similar to the electro-optical modulation mechanism, except for the optical carrier signal that has been replaced by a plasmonic wave. Here, the modulating signal is the voltage that is applied to the graphene layer. The advantages that these proposed devices offer lie with their subwavelength dimensions, capability for on-chip integration, and low power consumptions.

The rest of this paper is organized as follows. In Section II, after introducing the building blocks of a graphene-based plasmonic switch and giving a brief overview of its basic operating principle, we show how it can be optimized. In Section III, by taking advantage of the optimized parameters, we have designed a logical AND gate with subwavelength dimensions that can operate with very large ON/OFF ratio around the center frequency of 6 THz. In Section IV, we show that using the same principles, a subwavelength Y-branch plasmonic switch with high ON/OFF ratio can also be designed. Section V is dedicated to design of a plasmonic OR gate with subwavelength dimensions.

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M. Yarahmadi and M. K. Moravvej-Farshi are with Faculty of Electrical and Computer Engineering, Advanced Devices Simulation Lab, Tarbiat Modares University, Tehran 1411713116, Iran (e-mail: m.yarahmadi@modares.ac.ir; farshi_k@modares.ac.ir; moravvej@ieee.org).

L. Yousefi is with the School of Electrical and Computer Engineering, University of Tehran, Tehran, 14174, Iran (e-mail: lyousefi@ut.ac.ir).

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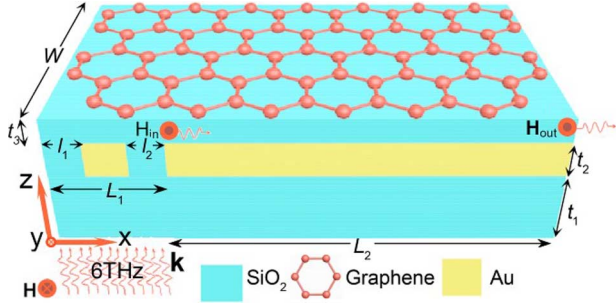


Fig. 1. Schematic of the switch. The dimensions scales are not in proportion. $L_1 = 915$ nm, $L_2 = 10 L_1$, $W = 4.5$ μ m, $l_1 = l_2 = 0.01 L_1$, $t_1 = 100$ nm, $t_2 = 30$ nm, and $t_3 = 20$ nm.

II. SUBWAVELENGTH PLASMONIC SWITCH

A. Building Blocks

A 3-D schematic of the building blocks of the proposed subwavelength graphene-based plasmonic switch structure is shown in Fig. 1 (the dimensions scales are not shown in proportion). The proposed switch structure consists of two 4.5 μ m wide blocks, made of Au/SiO₂/Graphene nano-layers stacked on top of a 100-nm layer of SiO₂. The input block, in which the surface plasmons (SPs) can be excited is similar to the one recently presented by Gu *et al.* [12], with $L_1 = 915$ nm. As shown in Fig. 1, in this block there are two grating elements (SiO₂) with the same lengths $l_1 = l_2 = 0.01 L_1$ on both sides of a 30 nm thick gold layer. Thickness of the top SiO₂ layer (the spacer) that is covered by a sheet of graphene is $t_3 = 20$ nm. When a $+z$ -directed 6 THz TM-polarized beam is used to illuminate the back surface of the input block, SPs can be excited at the graphene/SiO₂ interface. The output (control) block is a straight waveguide of length L_2 that can control and guide the propagation of the plasmonic wave in the input block. By modifying the optical conductivity of the top graphene layer, the propagation of the plasmonic waves can be modulated within the output block.

B. Basic Operation Principles

Distribution of the electric fields (\mathbf{E}) for the SP waves, stimulated by a TM-polarized incident wave, across the proposed structures can be calculated by solving the Maxwell's equation in 3-D

$$\nabla \times \mu_r^{-1}(\nabla \times \mathbf{E} - k_0^2 \frac{\varepsilon_r - j\sigma}{\omega \varepsilon_0}) \mathbf{E} = 0 \quad (1)$$

wherein ε_0 , μ_0 , and k_0 , are free-space permittivity, permeability, and wave number, and ε_r , σ , and ω represent relative permittivity, optical conductivity, and angular frequency. The graphene conductivity is obtained from Kubo formula [9]

$$\sigma \approx -j \frac{e^2 k_B T}{\pi \hbar^2 (\omega - j\tau^{-1})} \left\{ \frac{\mu_c}{k_B T} + 2 \ln \left[1 + \exp \left(-\frac{\mu_c}{k_B T} \right) \right] \right\} \quad (2)$$

where j , e , \hbar , k_B , T , and τ are the imaginary unit, the electric charge of an electron, the reduced Planck's constant, the Boltzmann's constant, temperature and the intraband relaxation time.

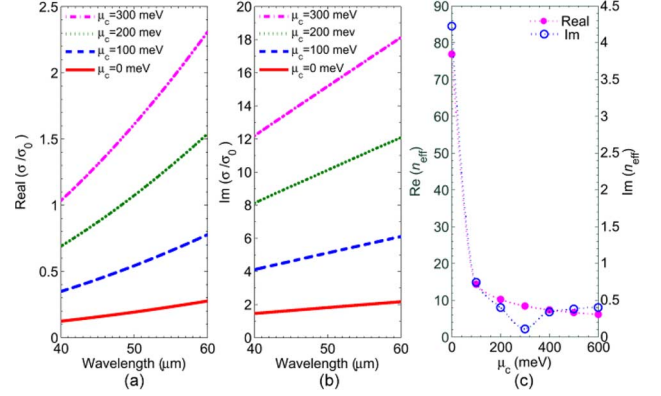


Fig. 2. (a) Real and (b) imaginary parts of the graphene optical conductivity for various chemical potentials, versus wavelength; and (c) the real (●) and imaginary (○) parts of the waveguide effective mode index for the SPs versus graphene chemical potential.

Furthermore, μ_c is the graphene chemical potential that can be controlled by an applied bias voltage, V through [20], [21]

$$|\mu_c| \approx |E_F(V)| = \hbar v_F \{ \pi a_0 |V - V_{\text{Dirac}}| \}^{1/2} \quad (3)$$

where $V_{\text{Dirac}} = 0.8$ V is the voltage offset caused by the natural doping, $v_F = 9 \times 10^5$ m/s is the Fermi velocity of Dirac fermions in graphene, and $a_0 \approx 9 \times 10^{16}$ m⁻² V⁻¹ estimated from a single capacitor model [20]. It should be noted that in (2), contribution of the interband transitions into optical conductivity at 6 THz has been ignored, as compared with the intraband contribution. Furthermore, the effective dielectric constant of the graphene layer with an assumed effective thickness of Δ can be modeled as [8]

$$\varepsilon = [\varepsilon_0 - \frac{\text{Im}(\sigma)}{\omega \Delta}] + j \frac{\text{Re}(\sigma)}{\omega \Delta}. \quad (4)$$

By varying the graphene chemical potential, its conductivity and effective dielectric constant are both modified according to (2) and (4), which in turn modify the real and imaginary parts of the effective mode index for the proposed waveguide structure.

Assuming $T = 300$ K and $\tau = 0.5$ ps, we have calculated the optical conductivity of graphene, in response to the input signals of various wavelengths in the range of $40 \mu\text{m} \leq \lambda \leq 60 \mu\text{m}$. Fig. 2(a) and 2(b), respectively, illustrate the wavelength dependence of the real and imaginary parts of the optical conductivity of graphene normalized with respect to $\sigma_0 = \pi e^2 / 2\hbar$, for the chemical potentials of $\mu_c = 0, 100, 200$, and 300 meV. As can be seen in this figure, the real and imaginary parts of the optical conductivity (for $\mu_c > 0$) both have noticeable variations in the given range that is suitable for use as a switching mechanism.

Moreover, the real and imaginary parts of the waveguide effective mode index, in terms of the chemical potential, have been calculated at the center frequency of 6 THz, for the range of $0 \leq |\mu_c| \leq 600$ meV. The corresponding results are shown in Fig. 2(c). As shown by the figure left axis, the real part of the effective mode index (●) decreases as μ_c increases in the given range. This causes the SPs' mode confinement to decrease by an increase in μ_c . As can also be seen from the Fig. 2(c) right axis, the imaginary part of the effective mode index (○) reaches to the minimum value of 0.11 at $\mu_c = 300$ meV, and then begins to

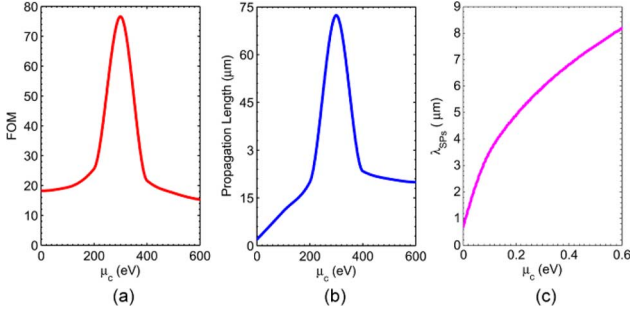


Fig. 3. (a) Figure of merit; (b) propagation decay length; and (c) wavelength of the produced surface plasmons versus the graphene chemical potential.

rise as μ_c increases further. Hence, it is expected that the maximum propagation length for the SPs to occur at $\mu_c = 300$ meV.

To get more in-depth sense about the guiding behavior, a figure-of-merit (FOM) for propagation of SPs can be defined as [22]

$$\text{FOM} = \text{Real}(n)/\text{Im}(n) = 2\pi L_{\text{SP}}/\lambda_{\text{SP}} \quad (5a)$$

that is the propagation decay length,

$$L_{\text{SP}} = [k_0 \text{Im}(n)]^{-1} \quad (5b)$$

normalized with respect to the surface plasmon's wavelength

$$\lambda_{\text{SP}} = 2\pi[k_0 \text{Re}(n)]^{-1}. \quad (5c)$$

Fig. 3 illustrates the profiles of the three parameters, defined in (5a)–(5c), versus the graphene chemical potential. As shown in this figure, the FOM and propagation decay length both maximize at $\mu_c = 300$ meV, while the SP wavelength increases monotonically with μ_c . Therefore, $\mu_c = 300$ meV can be considered as an optimum biasing condition, for the input block to guide highly confined SP waves with longest possible propagation decay length. On the other hand, the high contrast between the low ($L_{\text{SP}} = 2.03 \mu\text{m}$) and high ($L_{\text{SP}} = 72.34 \mu\text{m}$) values of the propagation decay lengths for $\mu_c = 0$ eV and 300 meV, respectively, reveals the promising potential for the proposed structure to act as a plasmonic switch in the THz region.

C. OFF and ON States

To find the field distribution confined within the spacer along the switch structure shown in Fig. 1, we have employed the finite element method for two different biasing conditions to solve (1) numerically. For this numerical simulation, boundaries on the device side-walls (i.e., x - z and y - z planes) are included in the simulation domain and the gold plates are assumed to be a perfect electric conductor—a reasonable assumption for 6 THz [12].

In either biasing condition, the chemical potential of the top graphene layer of the input block is kept fixed at $\mu_c = 300$ meV, while the block back surface is being illuminated by a 6 THz TM signal (see Fig. 1). In this condition, SP waves can be stimulated along the graphene/SiO₂ interface on top of the block, as pointed out in Section II-A. Nonetheless, from the discussion in Section II-B, the chemical potential of the graphene layer on top of the output (control) block is set to be $\mu_c = 0$ eV for OFF state

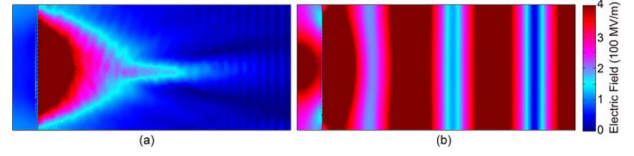


Fig. 4. Top (x - y plane) view of the electric field distribution confined within the SiO₂ layer across the optimized switch of Fig. 1, in the (a) OFF and (b) ON states.

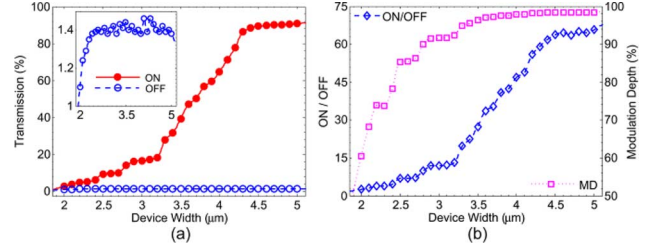


Fig. 5. (a) Transmission in ON and OFF (inset) states and (b) ON/OFF ratio (\diamond) and Modulation depth density (\square) reading on the left and right axes, respectively, all versus the waveguide width.

and 300 meV for ON state. The top (x - y plane) view of electric field profiles confined within the top SiO₂ layer across the structure of length $L = 11 L_1$, are illustrated for both biasing conditions in Fig. 4(a) and 4(b), respectively. In this simulation, we have used the optimum switch dimensions that will be introduced in Section II-D. As seen in this figure, the total electric field of the SP wave coupled into the output block, in the OFF state, propagates with $\lambda_{\text{SP}} = 628$ nm, while decaying rapidly with loss factor of $\sim 0.493 \mu\text{m}^{-1}$. In the ON state, however, the SP wave propagates along the output block with $\lambda_{\text{SP}} = 5.93 \mu\text{m}$ and insignificant loss factor of $\sim 0.014 \mu\text{m}^{-1}$.

D. Switch Optimization

To achieve optimized device dimensions, we performed a parametric study, to see the effects of variations in the device width, length, and the spacer thickness on the switch transmittance in the OFF or ON state, the ON/OFF ratio, and the modulation depth density [23]

$$\text{MD} = \frac{(T_{\text{ON}} - T_{\text{OFF}})}{T_{\text{ON}}} \quad (6)$$

wherein T_{ON} and T_{OFF} are the transmissions for the switch in the ON and OFF states, respectively.

Varying the device width in the range of $2 \mu\text{m} \leq W \leq 5 \mu\text{m}$, we have calculated the switching parameters. The numerical results are illustrated in Fig. 5. Fig. 5(a) illustrates the transmissions in the ON and OFF (inset) states, versus the switch width. As seen from Fig. 5(a), the ON state transmission increases with the waveguide width, until it starts to saturate around 90% for $W > 4.5 \mu\text{m}$. Moreover, the OFF state transmission fluctuates around the average value of $\sim 1.4\%$. The left and right axes of Fig. 5(b) show the corresponding ON/OFF ratio (\diamond) and the modulation depth density (\square), versus the device width, respectively. The data presented in this figure show that the maximum values of ~ 63.92 and $\sim 98.44\%$ for the ON/OFF ratio and the modulation depth density can be achieved for the switching

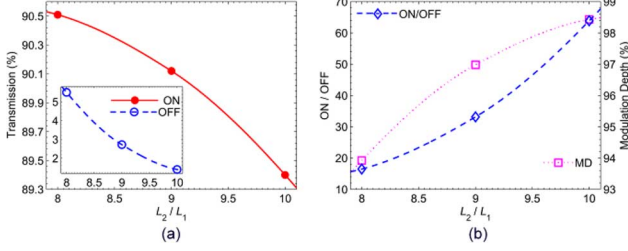


Fig. 6. (a) Transmission in ON and OFF (inset) state and (b) ON/OFF ratio (\diamond) and Modulation depth density (\square) reading on left and right axis, respectively, all versus the normalized length.

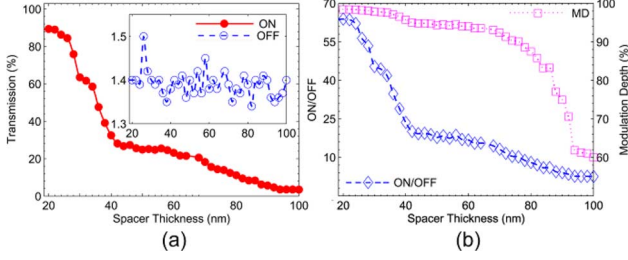


Fig. 7. (a) Transmission in ON and OFF (inset) state and (b) ON/OFF ratio (\diamond) and Modulation depth density (\square) reading on left and right axis, respectively, all versus the spacer thickness.

waveguides of widths $W \geq 4.5 \mu\text{m}$. Hence, $W = 4.5 \mu\text{m}$ can be an optimum choice for the device width.

Next, we vary the switch length ($L = L_1 + L_2$) by merely varying L_2 and keeping L_1 fixed, and calculate the ON and OFF transmissions, ON/OFF ratio, and the modulation depth density versus the normalized length of the output block (L_2/L_1), while W is fixed at $W = 4.5 \mu\text{m}$. The numerical results for various lengths in the range of ($8 \leq L_2/L_1 \leq 10$) are illustrated in Fig. 6. As can be seen variation of length in the given range has little effect ($< 1.5\%$) on the ON state transmission. However, the OFF state transmission increases by $\sim 74.45\%$, as the length L_2 decreases by 20%. As a consequence and as can be read from the left and right axes of Fig. 6(b), the switch ON/OFF ratio (\diamond) and the modulation depth density (\square) decrease by $\sim 47.49\%$ and $\sim 4.6\%$, respectively, as the length L_2 decreases by 20%. Since for $L_2 > 10 L_1$ the change in the ON state transmission and modulation depth density are insignificant, we take the device length to be $L = 11 L_1$.

Finally, keeping the switch width and length fixed at $W = 4.5 \mu\text{m}$ and $L = 11 L_1$, and varying the spacer thickness in the range of $20 \text{ nm} \leq t_3 \leq 100 \text{ nm}$, we have calculated the switch transmissions in OFF and ON states, ON/OFF ratio, and the modulation depth density. The numerical results are illustrated in Fig. 7. As can be observed from Fig. 7(a), as the spacer thicknesses increases beyond $t_3 = 57 \text{ nm}$, the ON state transmission drops to values below 25%. This huge fall is attributed to the significant decrease in the coupling efficiency of the SPs within the input block at 6 THz. As can be seen from the left and right axes of Fig. 7(b), the ON/OFF ratio (\diamond) drops to 17, while the modulation depth (\square) remains above 90%, for thicknesses up to 76 nm. In fact as the spacer thickness approaches 100 nm no desirable SP waves can be stimulated in the input block to be coupled into the output block. From data presented

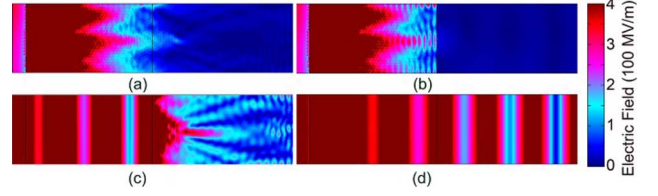


Fig. 8. Top (x - y plane) view of the electric field distribution confined within the SiO_2 layer across the logic AND gate, with the total length of $L = 20 L_1$ in the logical state (a) '0 0' (b) '0 1' (c) '1 0', and (d) '1 1'.

in Fig. 7, one can conclude that $t_3 = 20 \text{ nm}$ can be an optimum choice for the spacer thickness, resulting in a switch with an ON/OFF ratio of ~ 63 and the modulation depth density of $\sim 98\%$. This modulation depth density is 18% larger than that found by Padilla *et al.* [24] obtained from a GaAs-based metamaterial modulator structure. It is also 39% larger than that achieved for a graphene-based metamaterial structure, reported by [25], 57% greater than the modulation depth density obtained for a phase shifter with two graphene layers [22], and 8% greater than the highest value reported so far by [26] for a thermal modulator. It is also larger than those reported in [27]–[29] for graphene-based absorptive metamaterial structures by 8%, 14%, 48%, respectively, and also 80% greater than that obtained for a meta-surface based device as reported in [30]. This makes our proposed structure a superior candidate for future digital plasmonic switches and modulators operating in the THz region.

III. PLASMONIC LOGIC AND GATE

Considering a structure similar to that shown in Fig. 1, consisting an exactly same input block of length L_1 for the output block, except for the length that is changed to $L_2 = 19 L_1$, and the biasing scheme, everything else is kept the same as those of the output block in Fig. 1. The SP wave is stimulated at the graphene/ SiO_2 interface the same way as described in Section II-A. Dividing the output block into two sub-blocks of lengths $L'_2 = 9 L_1$ and $L''_2 = 10 L_1$ with separate contact terminals that can facilitate each sub-block to be biased independently.

We have calculated the electric field distribution across the new structure for four different biasing conditions. The top (x - y plane) views of the electric field distributions confined within the SiO_2 spacer in all four cases are depicted in Fig. 8. In all four cases, the graphene on top of the input block is biased to sustain its chemical potential at $\mu_c = 300 \text{ meV}$, required for stimulating the SP wave. Nonetheless, the first and the second sub-blocks of the output are biased separately to maintain their chemical potentials: (a) both at 0 eV; (b) at 0 and 300 meV; (c) at 300 meV and 0 eV; and (d) both at 300 meV, as shown in Fig. 8(a)–8(d), respectively. In other words, these four figures are, respectively, representing the '0 0', '0 1', '1 0', and '1 1' states of a logic AND gate. Among these for logic states, '1 1' is the only state in which the output port becomes '1' or ON. Nonetheless, the output port in each of the other three states is '0' or OFF. The SP waves transmission at the outputs of the four logic states '0 0', '0 1', '1 0', and '1 1' are also calculated using the finite element method. The numerical results are presented

TABLE I
OUTPUT TRANSMISSION (dB) AND CORRESPONDING LOGIC LEVELS OF THE GRAPHENE-BASED PLASMONIC LOGICAL AND GATE

Logic State	Output transmission level	
	AND	dB
'0 0'	0	-42.44
'0 1'	0	-31.37
'1 0'	0	-13.67
'1 1'	1	-1.07

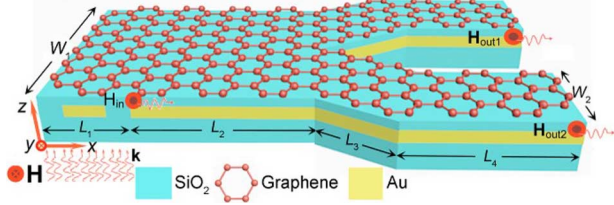


Fig. 9. Schematic of the Y-branch switch structure. The dimensions scales are not in proportion. $L_1 = 915$ nm, $L_2 = 4 L_1$, $L_3 = 11.5 L_1$, $L_4 = 8 L_1$, $W_1 = 8.5 \mu\text{m}$ and $W_2 = 4.25 \mu\text{m}$.

in Table I. As can be seen from the table, the ON/OFF ratios of 41.37, 30.3, and 12.6 dB are, respectively, achieved for '1 1'/'0 0', '1 1'/'0 1', and '1 1'/'1 0' cases. The corresponding modulation depth densities are 99.99%, 99.9%, and 94.5% that are larger than those reported by [23]–[30].

IV. Y-BRANCH PLASMONIC SWITCH

Based on the plasmonic switching blocks presented in Section II, we have designed a Y-branch plasmonic switch, whose 3D schematic representation is shown in Fig. 9. This switch, similar to that introduced in Fig. 1, also consists of an input block and an output block. In the input block except its width that is now $W_1 = 8.5 \mu\text{m}$ everything else is kept the same as those of the input block of Fig. 1. The constituents of the output block and their vertical dimensions are also the same as those shown in Fig. 1. The output block consists of an $8.5 \mu\text{m}$ wide straight waveguide of length $L_2 = 4 L_1$, as an extension to the input block. It is extended on the right by a 10° Y-branch of equal arms of widths $W_2 = 4.25 \mu\text{m}$ and $L_3 = 11.5 L_1$. Each arm is extended by another $4.25 \mu\text{m}$ wide straight waveguide of the same lengths $L_4 = 8 L_1$, providing the switch two output ports, as shown in Fig. 9.

The same technique used to stimulate the SP wave in the input block of the switch in Fig. 1 is also used here. The stimulated SP wave can be coupled into the output block. The Y-branch arms biasing conditions determine whether they are in OFF or ON states. Using the finite element method, we have simulated the total electric field distributions confined within the SiO_2 spacer layer along the switching blocks, under different biasing conditions. Fig. 10 illustrates the top (x - y plane) views of the total electric field across the Y-branch plasmonic switch.

Fig. 10(a) shows the field distribution when the graphene layers on both arms are equally biased to sustain the same chemical potential of $\mu_c = 0$ eV. In this condition (0 0), as shown in this figure, both arms of the Y-branch are in OFF or "0" level. As a consequence the SP waves coupled into both arms are attenuated rapidly such that no signal emerges from either output port. The scale bar on the right measures the field

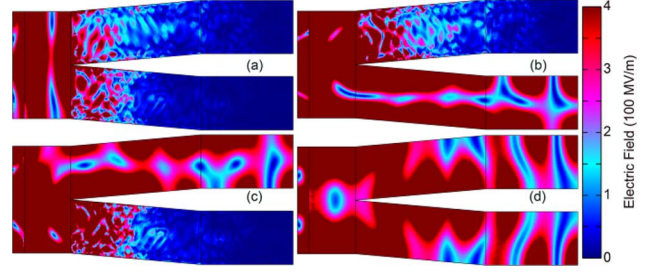


Fig. 10. Top (x - y plane) view of the electric field distribution confined within the SiO_2 layer across the Y-branch switch of Fig. 9, in the logical state (a) '0 0' (b) '0 1' (c) '1 0', and (d) '1 1'.

TABLE II
OUTPUT TRANSMISSION (dB) AND CORRESPONDING LOGIC LEVELS OF THE GRAPHENE-BASED PLASMONIC Y-BRANCH SWITCH

Switching State	Output transmission			
	Out 1		Out 2	
	logic	dB	logic	dB
'0 0'	0	-43.98	0	-45.23
'0 1'	0	-43.98	1	-4.56
'1 0'	1	-4.62	0	-45.23
'1 1'	1	-4.69	1	-4.69

intensity. Fig. 10(b) and 10(c) illustrates the field distributions in biasing conditions, representing the '0 1' and '1 0' logic states, respectively. In either of these two cases, one Y-branch arm is set to the OFF state ($\mu_c = 0$ eV) while the other arm is biased in the ON state ($\mu_c = 300$ meV). Nevertheless, when both arms are in their ON states, experiencing insignificant loss and represent the '1 1' logic state, as depicted in Fig. 10(d).

Transmissions at both output ports of the Y-branch in each of the four logic states '0 0', '0 1', '1 0', and '1 1' are also calculated using the finite element method, and presented in Table II. Note that among the four levels, the maximum total transmission emerges from both outputs of the logic '1 1' state and the minimum total transmission passes through both outputs of the logic '0 0' state, yielding the maximum ON/OFF ratio of ~ 39.87 dB. Nevertheless, similar ratios obtained for the other two logic states ('0 1' and '1 0') with respect to '0 0' are ~ 36.99 dB and ~ 36.93 dB, respectively. The corresponding modulation depth densities are all greater than 99.9% that are also larger than those reported by [23]–[30]. These data also shows that this graphene-based subwavelength plasmonic Y-branch switch is superior to the Y-junction plasmonic switch with millimeter dimensions operating at 1.6 THz, reported in [31].

V. PLASMONIC LOGIC OR GATE

Consider a structure that is schematically shown in Fig. 11. The input block in which the SP waves are stimulated is exactly the same as that of the Y-branch structure. Its width and length are $W_1 = 8 \mu\text{m}$ and $L_1 = 915$ nm. The constituents of the output block and their vertical dimensions are the same as those of the output blocks of the other three devices. It consists of two $8 \mu\text{m}$ wide straight waveguides of lengths $L_2 = 3 L_1$ and $L_6 = 2 L_1$ acting as the input and output ports, respectively, connected by two face-to-face 20° Y-branches, each made of

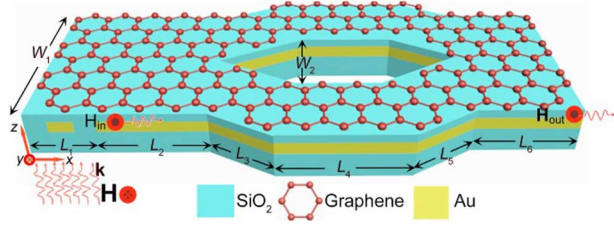


Fig. 11. Schematic of the plasmonic OR logical gate structure. The dimensions scales are not in proportion. $L_1 = 915$ nm, $L_2 = 3 L_1$, $L_3 = L_5 = 8.5 L_1$, $L_4 = 6 L_1$, $L_6 = 2 L_1$, and $W_1 = 8 \mu\text{m}$.

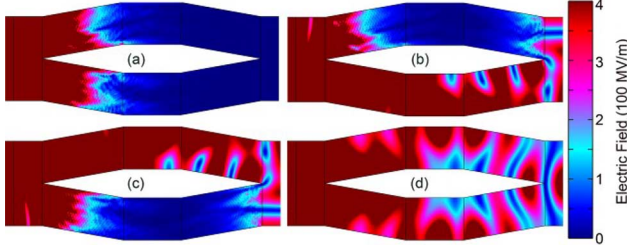


Fig. 12. Top (x - y plane) view of the electric field distribution across the logic OR gate at the middle of a SiO_2 layer in (a) '0 0' (b) '0 1' (c) '1 0' and (d) '1 1' logical states.

$4 \mu\text{m}$ wide arms of equal lengths of $L_3 + L_4 + L_5$, with $L_3 = L_5 = 8.5 L_1$ and $L_4 = 6 L_1$.

Fig. 12 illustrates the top (x - y plane) views of the electric field distributions confined within the spacer layer across the proposed structure of Fig. 11, calculated for four biasing conditions. The logic state '0 0' shown in Fig. 12(a) represents the biasing condition, in which the chemical potential of the graphene that covers straight waveguide of length $L_1 + L_2$ is biased to maintain its chemical potential at $\mu_c = 300$ meV (ON state) while the graphene covering the remaining part of the device is maintained at zero (OFF state). As can be observed from this figure, the output in this logic state is '0' or OFF. Fig. 12(b) and 12(c) represent two symmetric logic states of '0 1' and '1 0'. In either of these two symmetric cases, except for the graphene layer covering one of the two arms ($L_3 + L_4 + L_5$) that is in OFF state, the graphene covering the remaining part of the device is in ON or '1' state, making the output '1' or ON. Moreover, the logic state '1 1' whose output port is also in '1' or ON state is depicted in Fig. 12(d), representing the biasing condition in which the graphene covering the entire device is biased to maintain its chemical potential at $\mu_c = 300$ meV. These four logic states altogether show that the structure of Fig. 11 can act as a plasmonic OR logic gate, with subwavelength dimensions in the THz region. The numerical results are presented in Table III, indicating the minimum and maximum ON/OFF ratios of ~ 37.66 dB for '0 1'/'0 0' or '1 0'/'0 0' and 40.76 dB for '1 1'/'0 0', respectively. The corresponding modulation depth densities are all greater than 99.9% that are also larger than those reported in [23]–[30]. These extremely large ON/OFF ratios have been obtained from the device whose length is $\sim 53\%$ of the incident wavelength. We have realized that if the output port of this logic OR gate is increased to $L_6 = 11 L_1$, its minimum and maximum ON/OFF ratios increase by ~ 3.41 and ~ 3.53 dB, respectively.

TABLE III
OUTPUT TRANSMISSION (dB) AND CORRESPONDING LOGIC LEVELS OF THE GRAPHENE-BASED PLASMONIC LOGICAL OR GATE

Logic State	Output transmission	
	OR	dB
'0 0'	0	-43.01
'0 1'	1	-5.35
'1 0'	1	-5.35
'1 1'	1	-2.25

VI. CONCLUSION

We have designed an optimized graphene-based subwavelength plasmonic switch operating at 6 THz, with ON/OFF ratio of ~ 63 , and modulation depth of $\sim 98\%$. This modulation depth is larger than those recently reported for a GaAs-based metamaterial modulator (80%), a graphene-based metamaterial structure (59%), phase shifter with similar structure (41%), in which the gold layer is substituted by another layer of graphene and thermal modulator (90%). In the ON state, the chemical potential of the graphene layer covering the output block is fixed to 300 meV, while in the OFF condition, it is held at zero. The propagation decay lengths for the output element of the optimized switch in the OFF and ON states are ~ 2.03 and $\sim 72.34 \mu\text{m}$, respectively. Using the optimized dimensions and biasing conditions, we have designed a logic AND gate, a Y-branch switch and a logic OR gate with maximum ON/OFF ratios of ~ 41.37 , ~ 39.87 , and 40.76 dB, respectively. Every one of these ON/OFF ratios can be increased in expense of an increment in the length of the corresponding output port(s). These graphene-based plasmonic switches and logic gates are potential building blocks for future digital plasmonic circuits. The only drawback of these electro-optical devices are their switching speeds that depend on the speeds of their electronic circuits. Nevertheless, optical control of the plasmonic waves has been planned for future works. Moreover, due to the absorptive switching mechanisms in the Y-branch and the OR logic gate in '0 1' or '1 0' logic, about half of the input power is lost within the branch that is in the OFF state.

The present THz plasmonic logic gates that are CMOS compatible have potential to be employed for developing the fundamental unit of an optoelectronic microprocessor, with clock speeds faster than their electronic counterparts.

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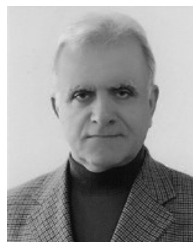
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Morteza Yarahmadi (GSM'15) was born in Lorestan, Iran, in 1988. He received the B.Sc. degree in electronic from Lorestan University, Lorestan, Iran, in 2012, and the M.Sc. degree in optoelectronics from Tarbiat Modares University, Tehran, Iran, in 2014.

His research interests include graphene plasmonics, plasmonic waveguides, THz switch and modulators.



Mohammad K. Moravvej-Farshi (S'86–M'87–SM'05) was born in Yazd, Iran, in 1952. He received the B.Sc. degree in physics from Sharif University of Technology, Tehran, Iran, in 1976, the M.A. degree in physics from the University of Southern California (USC), Los Angeles, CA, USA, in 1978, the M.Sc. degree in electronics from the University of California at Santa Barbara, CA, USA, in 1980, and the Ph.D. degree in electronics from the University of New South Wales, Sydney, Australia, in 1987.

From 1980 to 1984, he was a member of research staff with the Division of Microwave, Iran Telecommunication Research Center. He joined Tarbiat Modares University (TMU), Tehran, Iran, in 1987, where he is currently a Professor of Electronics and Head of the Advanced Device Simulation Lab (ADSL). His current fields of interests include graphene photonics, graphene plasmonics, optical metamaterials, semiconductors optoelectronics and nanoelectronics, all-optical devices based on non-linear phenomena and parity time symmetry, as well as phononic crystal based acoustic devices.

Prof. Moravvej Farshi is currently a senior member of the Optical Society of America (OSA). He is also one of the founders of the Optics and Photonics Society of Iran.



Leila Yousefi (GSM'06–M'09) was born in Isfahan, Iran, in 1978. She received the B.Sc. and M.Sc. degrees in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2000 and 2003, respectively, and the Ph.D. degree in electrical engineering from the University of Waterloo, Waterloo, ON, Canada, in 2009.

From 2009 to 2011, she worked as a Postdoctoral Fellow at the University of Waterloo, performing research on metamaterials, miniaturized antennas, electromagnetic bandgap structures, and MIMO systems.

In 2011, she joined the Integrated Optics Lab in The Johns Hopkins University, Baltimore, MD, USA, as a Post-Doctoral researcher, where she worked in the field of nano-photonics, and plasmonics till 2013. In 2013, she joined University of Tehran, Tehran, Iran, as an Assistant Professor. Currently, she is an assistant professor and director of the Nano-Photonics and Metamaterial Research Lab, in University of Tehran. Her research interests include nano-photonics, plasmonics and metamaterials.