Optics Communications 372 (2016) 85–90

Contents lists available at ScienceDirect

Optics Communications

journal homepage: www.elsevier.com/locate/optcom

Electro-optical logic gates based on graphene–silicon waveguides

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ARTICLE INFO

Article history:
Received 11 January 2016
Received in revised form
3 April 2016
Accepted 4 April 2016

Keywords:
Integrated optics
Optical devices
Waveguide

ABSTRACT

In this paper, designs of electro-optical AND/NAND, OR/ NOR, XOR/XNOR logic gates based on cascaded silicon graphene switches and regular 2×1 multimode interference combiners are presented. Each switch consists of a Mach–Zehnder interferometer in which silicon slot waveguides embedded with graphene flakes are designed for phase shifters. High-speed switching function is achieved by applying an electrical signal to tune the Fermi levels of graphene flakes causing the variation of modal effective index. Calculation results show the crosstalk in the proposed optical switch is lower than -22.9 dB within a bandwidth from 1510 nm to 1600 nm. The designed six electro-optical logic gates with the operation speed of 10 Gbit/s have a minimum extinction ratio of 35.6 dB and a maximum insertion loss of 0.21 dB for transverse electric modes at 1.55 μm.

1. Introduction

With the rapid growth of Internet traffic, it is challenging for bandwidth-limited silicon electronics to meet the demand on data processing [1,2]. Silicon photonics with the advantage of massive parallelism, high bandwidth, and high speed provides a promising approach for computing and processing a tremendous amount of information [3,4]. As a basic unit, silicon-based optical logics have gained increased attention in recent years.

All-optical logic gates using the plasma dispersion effect [5], two-photon absorption (TPA) [6], and four-wave mixing (FWM) [7] have been demonstrated in silicon waveguides. Although they can perform ultrafast speed operations, it is not easy to achieve large-scale integration because strong pumps are needed to induce the nonlinear effects to realize logic functions. Logic gates based on the thermo-optic effect in silicon waveguides suffer from low operation speeds [8,9]. A better alternative would be electro-optically tuned devices. Due to the compact footprint and low power consumption, microring resonator (MRR) is considered as an ideal element to construct electro-optical logic gates. A range of electro-optical logic gates based on silicon MRRs have been demonstrated [10,11]. Nevertheless, they have a limited bandwidth and are sensitive to temperature variations. In contrast, the devices based on Mach–Zehnder interferometers (MZIs) show relatively large optical extinction ratio and broadband operation, but require large footprints [12,13].

Graphene, a two-dimensional material, has the unique and extraordinary electronic and optical properties which make it an attractive option for realizing novel devices, such as gate-variable optical conductivity [14], ultrahigh electron mobility [15], and wideband optical absorption [16]. Plasmonic modes can be supported by the doped graphene. Electro-optical graphene plasmonic logic gates have been designed with a minimum extinction ratio of 15 dB at an operating wavelength of 10 μm [17]. When graphene is combined with the silicon waveguide, the modal effective index of the graphene–silicon waveguide (GSW) varies according to the carrier density in graphene. Previously, Bragg gratings [18], TE-pass polarizers [19], photodetectors [20–22], switches [23], and modulators [16,24] based on GSWs have been reported.

In this paper, 10 Gbit/s electro-optical logic gates for AND/NAND, OR/NOR, and XOR/NXOR operations using cascaded silicon graphene switches based on MZIs (SGMZIs) and 2×1 multimode interference (MMI) combiners are proposed and numerically studied. The variations of the effective indices of guided modes in the phase shifters of SGMZIs are investigated by using finite-difference time-domain (FDTD) simulations. The functionalities and properties of electro-optical logic gates are evaluated and analyzed. These electro-optical logic gates offer the performance merits including large extinction ratio, low insertion loss, high operation speed, and broad bandwidth. Moreover, the dependence of the performance of SGMZI on the dielectric is also discussed.

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http://dx.doi.org/10.1016/j.optcom.2016.04.008
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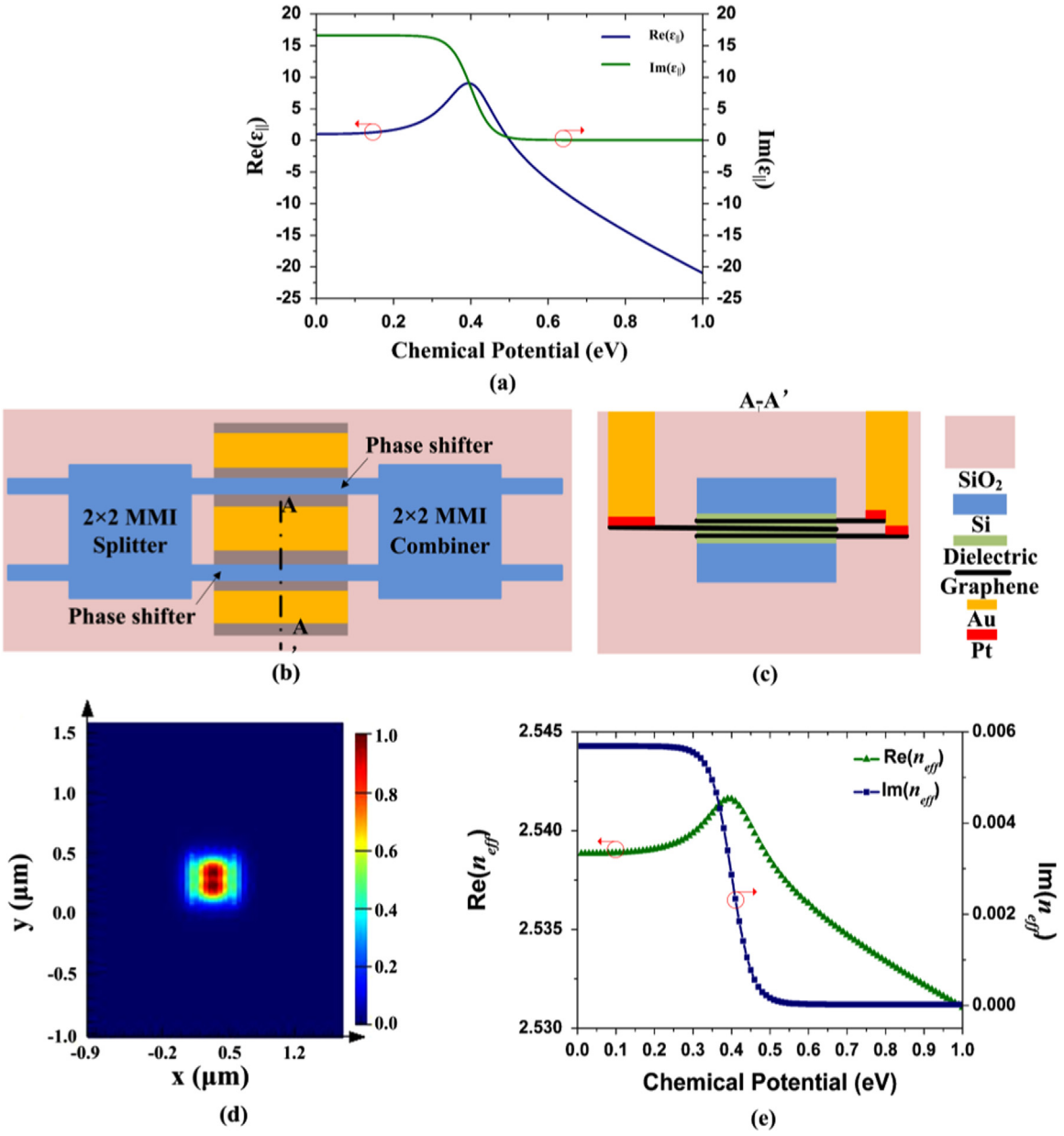

Fig. 1. (a) The in-plane permittivity of graphene as a function of the chemical potential (b) Structure of the 2 × 2 SGMZI (c) Cross-section of the phase shifter (d) Optical mode profile in the silicon slot waveguide embedded with graphene flakes for the TE mode (e) Effective index in the phase shifter of the SGMZI as a function of the chemical potential.

2. MZI-based silicon graphene switch

2.1. Graphene's conductivity and permittivity

The monolayer graphene is treated as an anisotropic material. The in-plane optical conductivity σ of the monolayer graphene obtained from the Kubo formulas is given by the following equations [25]

$$\sigma = \sigma_{\text{intra}} + \sigma_{\text{inter}} \tag{1}$$

$$\sigma_{\text{intra}} = \frac{-ie^2}{\pi\hbar(\omega + i2\Gamma)}\left[\int_0^{\infty} \varepsilon\left(\frac{\partial f_d(-\varepsilon)}{\partial\varepsilon} - \frac{\partial f_d(-\varepsilon)}{\partial\varepsilon}\right)d\varepsilon\right] \tag{2}$$

$$\sigma_{\text{inter}} = \frac{-ie^2(\omega + i2\Gamma)}{\pi\hbar^2}\left[\int_0^{\infty} \frac{f_d(-\varepsilon) - f_d(\varepsilon)}{(\omega + i2\Gamma)^2 - 4(\varepsilon/\hbar)^2}d\varepsilon\right] \tag{3}$$

where e represents the charge of the electron, $\hbar$ is the reduced Planck's constant, ω is angular frequency, $f_d(\varepsilon)$ is the Fermi-Dirac distribution, and $\Gamma = (ev_F^2)/(\mu\mu_c)$ is the scattering rate which is a function of the graphene's carrier mobility μ, the Fermi velocity v_F, and the chemical potential μ_c. The Fermi-Dirac distribution $f_d(\varepsilon)$ is defined as $f_d(\varepsilon) = (e^{(\varepsilon-\mu_c)/k_BT} + 1)^{-1}$, where k_B is the Boltzmann constant and T is temperature.

When the monolayer graphene is treated as an ultra-thin film, the relationship between the in-plane permittivity of the graphene $\varepsilon_{\|}$ and the in-plane optical conductivity σ is as follows [26].

$$\varepsilon_{\|} = 1 + i\frac{\sigma}{\omega\varepsilon_0\Delta} \tag{4}$$

where ε_0 and Δ are the vacuum permittivity and the thickness of the monolayer graphene, respectively.

In the simulation, $T = 300$ K, $\Delta = 0.34$ nm, and $v_F = 9.5 \times 10^5$ m/s are considered. Fig. 1(a) shows the dependence of the in-plane permittivity of graphene on the chemical potential at an operating

wavelength of 1550 nm. The in-plane permittivity of the graphene varies from $\varepsilon_{\parallel}(0.001eV) = 0.994+i16.6$ to $\varepsilon_{\parallel}(1eV) = -21.0+i0.047$.

2.2. Structure and analysis

The structure of the designed SGMZI is shown in Fig. 1(b). A pair of silicon MMI couplers are respectively used as the 3 dB power splitter and combiner in the 2×2 SGMZI and silicon slot waveguides embedded with graphene flakes are designed for phase shifters at the two arms to achieve the switching function. As shown in Fig. 1(c), a 40 nm dielectric are sandwiched in a silicon waveguide with a width of 450 nm and a height of 340 nm to form the silicon slot waveguide. Three layers of evenly spaced graphene flakes are medially inserted into the dielectric. The possible fabrication process can be as follows. The first silicon layer will be fabricated in an SOI process. The dielectric layers will be deposited by plasma-enhanced chemical vapor deposition (PECVD). The graphene layer between adjacent dielectric layers will be deposited by chemical vapor deposition (CVD) or growth epitaxially. The second silicon layer will be formed by an orientated growth or bonding technique. The gold electrode will be connected to a platinum film which is deposited onto the graphene. Oxygen plasma will be used to remove the undesired graphene.

The refractive indices of SiO_2, Si, and dielectric are chosen to be 1.44, 3.47, and 1.98. The calculated mode profile in the silicon slot waveguide embedded with graphene flakes for the transverse electric (TE) mode is shown in Fig. 1(d). Fig. 1(e) shows the dependence of real and imaginary parts of the effective index on the chemical potential at the wavelength of 1550 nm. Because any electric current cannot be generated by the electric field in the perpendicular direction, the value of the perpendicular permittivity of the graphene $\varepsilon_{\perp}$ has little effect on the variation of the effective index. The perpendicular permittivity of the graphene $\varepsilon_{\perp}$ is set to be $\varepsilon_{\perp}=1$ in this work. As illustrated in Fig. 1(e), if the chemical potential μ_c is set to be 0.39 eV, the real part of the effective index $\mathrm{Re}(n_{\mathrm{eff}})$ reaches a maximum. In addition, when the chemical potential μ_c is greater than 0.5 eV, the imaginary part of the effective index $\mathrm{Im}(n_{\mathrm{eff}})$ is on the order of 10^{-4}. In order to improve extinction ratio and reduce power consumption, $\mu_c=0.50$ eV and $\mu_c=0.60$ eV are chosen to be the initial and final states, respectively. The real part of the effective index $\mathrm{Re}(n_{\mathrm{eff}})$ experiences a change of 0.00219, leading to a phase shift of π with the arms' length of 353.72 μm, when the chemical potential μ_c is tuned from 0.50 eV to 0.60 eV. Tunability of the chemical potential μ_c is achieved by applying a driving voltage V_g to a graphene flake. The equation can be written as [16]:

$$\mu_c = \hbar v_F \sqrt{\pi\left|\eta(V_g + V_0)\right|} \tag{5}$$

where V_0 is the voltage offset caused by natural doping and $\eta = 2.17\times10^{16}\ \mathrm{m^{-2}\ V^{-1}}$ is a constant which can be calculated from the parallel plate capacitor model [23]. Thus, $V_g=4.13$ V is needed to shift the chemical potential μ_c from 0.5 eV to 0.6 eV.

When graphene flakes are doped to 0.5 eV, the SGMZI is assumed to be in the cross state and the light comes out from the cross port. When graphene flakes are doped to 0.6 eV, the phase difference between the two arms is almost π, the SGMZI is in the bar state and the light exits from the through port. The response spectra of the SGMZI are shown in Fig. 2. It can be found the crosstalk in the SGMZI is lower than −22.9 dB within a bandwidth from 1510 nm to 1600 nm and less than −25 dB from 1531 nm to 1600 nm. The insertion loss of the device is less than 0.14 dB. The operation speed of the SGMZI is limited by the *RC* delay time of the waveguide structure. For the proposed device, the equivalent capacitance *C* and resistance *R* are respectively estimated as 0.55 pF and 39 mΩ. If additional resistance is not taken into account, the 3 dB bandwidth $f_{3\mathrm{dB}}$ calculated by $f_{3\mathrm{dB}} = \frac{1}{2\pi(2RC)}$ will be estimated to be ~3.7 THz. Fig. 3 shows the optical time response of the SGMZI. It can be seen that when a 10-Gbit/s electrical signal is applied to graphene flakes, the extinction ratios are respectively 38.5 dB and 53.6 dB at the cross and through ports.

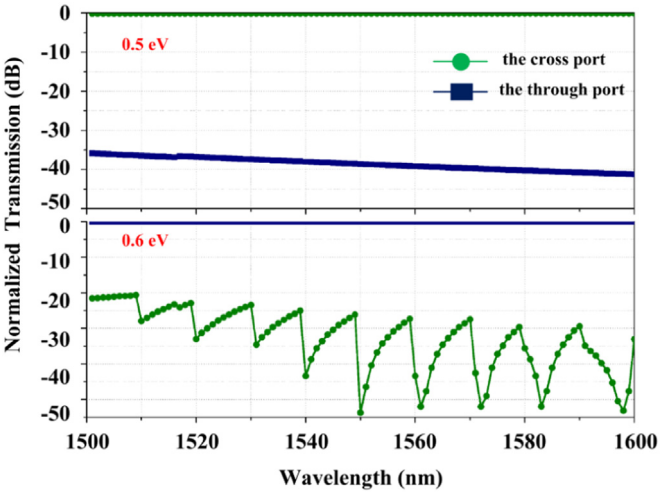

Fig. 2. Transmission spectra of the SGMZI. The circle and rectangle traces represent the transmission to the cross and through ports, respectively.

3. Electro-optical logic gates

3.1. AND/NAND logic operations

Fig. 4(a) shows the schematic of the proposed electro-optical AND/NAND logic device, which is composed of two SGMZIs and a 2×1 MMI combiner. $\mu_c=0.5$ eV achieved by applying a low-level driving voltage and $\mu_c=0.6$ eV attained by application of a high-level driving voltage are assumed to be logic 0 and logic 1. The high and low levels of the optical power arrived at the two output ports are respectively considered as logic 0 and logic 1. When the low-level driving voltage is applied to SGMZI1 ($A=0$, $B=0/1$), the optical signal passes through SGMZI1 and the 2×1 MMI combiner, then exits from the port Output_2 ($X=0$, $Y=1$). When the high- and low-level driving voltages are respectively applied to SGMZI1 and SGMZI2 ($A=1$, $B=0$), the optical signal transits SGMZI1, SGMZI2, and the 2×1 MMI combiner, then comes out from the port Output_2 ($X=0$, $Y=1$). When the two high-level driving voltages are applied to SGMZI1 and SGMZI2 ($A=1$, $B=1$), the optical signal

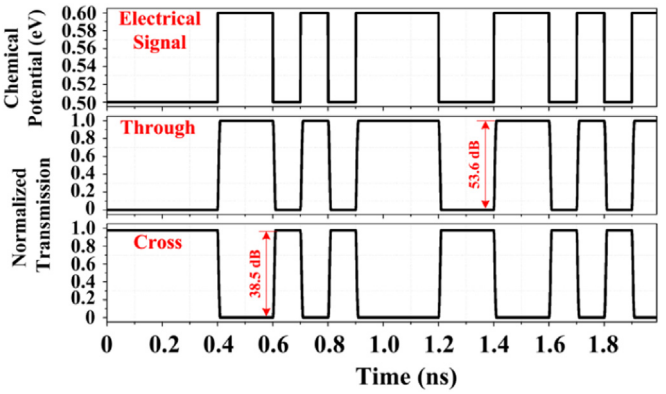

Fig. 3. Optical time response of the SGMZI.

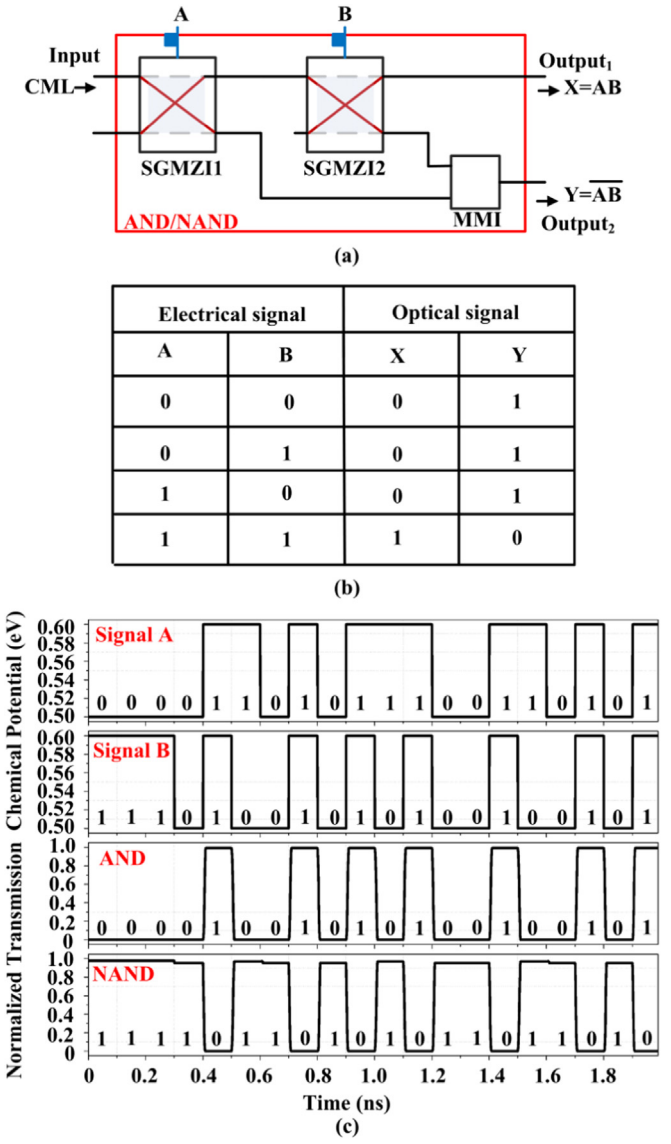

Fig. 4. (a) Schematic of the proposed electro-optical AND/NAND logic device (b) Truth table (c) Dynamic results of the electro-optical AND/NAND logic device with an operation speed of 10 Gbit/s.

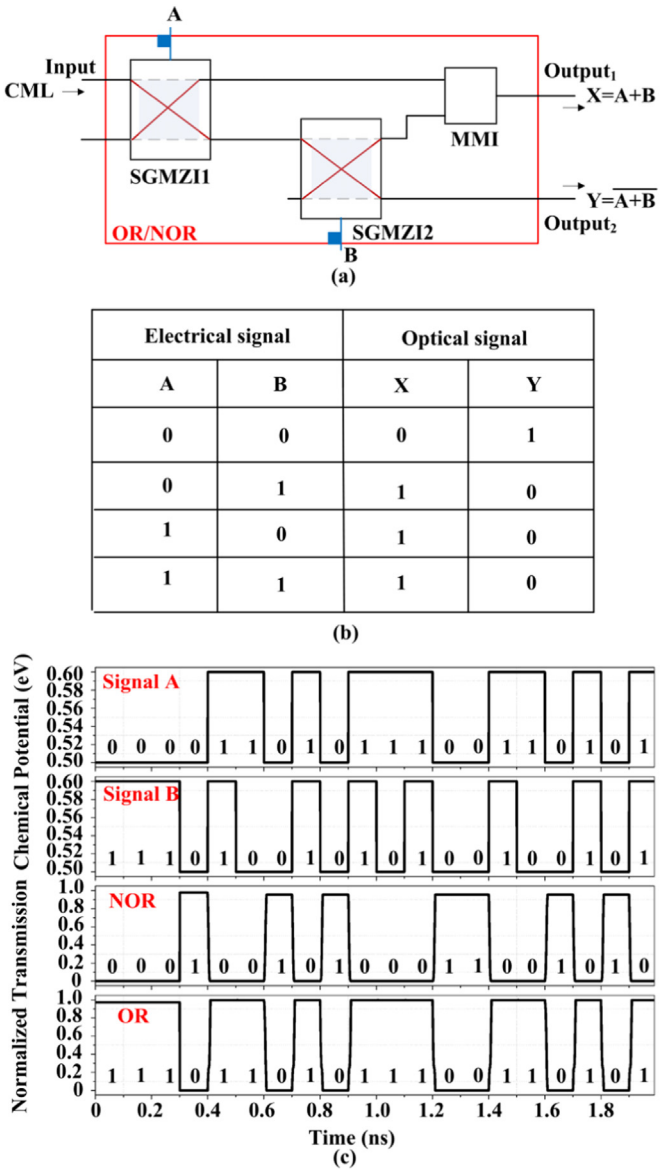

Fig. 5. (a) Schematic diagram of the proposed electro-optical OR/NOR logic device (b) Truth table (c) Dynamic responses of the electro-optical OR/NOR logic device.

propagates through SGMZI1 and SGMZI2, then emerges from the port Output$_1$ ($X=1$, $Y=0$). The truth table of the proposed electro-optical AND/NAND logic device is shown in Fig. 4(b). The dynamic results with the operation speed of 10 Gbit/s are shown in Fig. 4(c). The patterns of the two electrical signals are '00001101011-100110101' (Signal A) and '11101001010100100101' (Signal B), respectively. Their AND and NAND operation results are '00001001010100100101' and '11110110101011011010'. As described in Fig. 4(c), it can be found that the AND/NAND logic operations are carried out correctly at the ports Output$_1$ and Output$_2$ simultaneously. The minimum extinction ratio for the electro-optical AND/NAND logic device is 38.5 dB with the maximum insertion loss of 0.21 dB at an operating wavelength of 1550 nm.

3.2. OR/NOR logic operations

The configuration of the proposed electro-optical OR/NOR logic device using two SGMZIs and a 2×1 MMI combiner is shown in Fig. 5(a). When the high-level driving voltage is applied to SGMZI1 ($A=1$, $B=0/1$), the optical signal passes through SGMZI1 and the 2×1 MMI combiner, then emerges from the port Output$_1$ ($X=1$, $Y=0$). When the two low-level driving voltages are applied to SGMZI1 and SGMZI2 ($A=0$, $B=0$), the optical signal transits SGMZI1 and SGMZI2, then comes out from the port Output$_2$ ($X=0$, $Y=1$). When the low- and high-level driving voltages are respectively applied to SGMZI1 and SGMZI2 (A=0, B=1), the optical signal propagates through SGMZI1, SGMZI2, and the 2×1 MMI combiner, then exits from the port Output$_1$ ($X=1$, $Y=0$). Fig. 5 (b) summarizes the truth table of the proposed electro-optical OR/NOR logic device. The dynamic responses of the electro-optical OR/NOR logic device are shown in Fig. 5(c). The NOR and OR operation results of Signal A and Signal B are '00010010100011-001010' and '11101101011100110101', respectively. As shown in Fig. 5(c), it can be seen that the OR/NOR logic operations are simultaneously achieved at the ports Output$_1$ and Output$_2$. The minimum extinction ratio for the electro-optical OR/NOR logic device is 35.6 dB. The maximum insertion loss is 0.21 dB at an operating wavelength of 1550 nm.

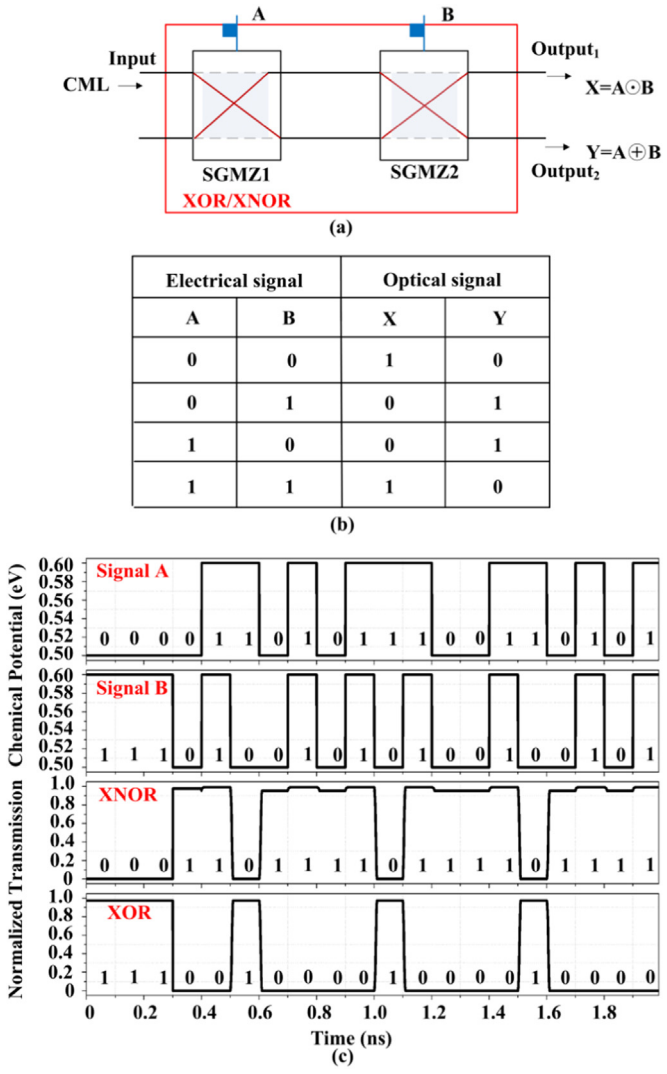

Fig. 6. (a) Schematic illustration of the proposed electro-optical XOR/XNOR logic device (b) Truth table (c) Dynamic operation results of the electro-optical XOR/XNOR logic device.

3.3. XOR/XNOR logic operations

As shown in Fig. 6(a), the proposed electro-optical XOR/XNOR logic device consists of two cascaded SGMZIs. When the same driving voltages are applied to SGMZI1 and SGMZI2 ($A=0$, $B=0$ or $A=1$, $B=1$), the optical signal passes through two cascaded SGMZIs and comes out from the port Output$_1$ ($X=1$, $Y=0$). When the driving voltages applied to SGMZI1 and SGMZI2 are different ($A=1$, $B=0$ or $A=0$, $B=1$), the optical signal propagates through SGMZI1 and SGMZI2, then exits from the port Output$_2$ ($X=0$, $Y=1$). Fig. 6(b) shows the truth table achieved by the proposed device. The dynamic operation results of the proposed electro-optical XOR/XNOR logic device are shown in Fig. 6(c). Signal A and Signal B at 10 Gbit/s are applied to two cascaded SGMZIs. Their XNOR and XOR operation results are respectively '00011011110111101111' and '11100100001000010000'. From Fig. 6(c), it can be found that the XNOR/XOR logic operations are performed correctly at the ports Output$_1$ and Output$_2$. The minimum extinction ratio of 38.4 dB and the maximum insertion loss of 0.21 dB for the electro-optical XNOR/XOR logic device can be obtained at an operating wavelength of 1550 nm.

4. Discussion

The proposed SGMZI is an important element of the electro-optical logic gates described above. In order to reduce the area and power consumption further, the effects of the dielectric on the performance of the SGMZI are studied. The refractive indices of dielectrics in Table 1 are set to be 1.98 and the heights of dielectrics in Table 2 are chosen to be 40 nm. V_π is a voltage that causes the chemical potential μ_c to vary from 0.5 eV to 0.6 eV and leads to a phase shift of π with the arms' length L. As described in Table 1, when the height of the dielectric is set to be 20 nm, the variation of the real part of the effective index Re(n_{eff}) is 0.0025 and $V_\pi \cdot L$=0.641 V·mm. As the height of the dielectric increases from 20 nm to 80 nm, the variation of the real part of the effective index Re(n_{eff}) becomes smaller and the ($V_\pi \cdot L$) product gets larger. Similarly, the impact of the refractive index of dielectric on the performance of the SGMZI is shown in Table 2. When the refractive index of the dielectric is increased, the variation of the real part of the effective index Re(n_{eff}) becomes larger and the ($V_\pi \cdot L$) product is reduced.

According to the foregoing analysis, a 20 nm-thick HfO_2 is preferred as a dielectric to achieve the SGMZI which has low power consumption and relatively compact footprint. Simulation results show the ($V_\pi \cdot L$) product for the SGMZI using the 20 nm-thick HfO_2 is 0.567 V mm with V_π =1.84 V. The minimum extinction ratio and the maximum insertion loss are 38.5 dB and 0.10 dB at the wavelength of 1550 nm, respectively. The performance of the SGMZI can be further improved by increasing the number of embedded graphene layers [27,28].

5. Conclusion

In conclusion, electro-optical logic gates for AND/NAND, OR/NOR, and XOR/XNOR operations based on cascaded SGMZIs and 2×1 MMI combiners have been proposed and numerically analyzed. The variation of modal effective index of silicon slot waveguide can be controlled by electrically tuning the Fermi levels of the embedded graphene flakes, providing an attractive method for realizing high-speed switching function. The designed SGMZI provides an operation speed of 10 Gbit/s and crosstalk lower than −22.9 dB within a bandwidth from 1510 nm to 1600 nm. The minimum extinction ratio of the proposed six electro-optical logic gates is 35.6 dB with a maximum insertion loss of 0.21 dB for the TE mode at a wavelength of 1550 nm. Calculation results have shown that a thin and high-refractive-index dielectric can be used to reduce the area and power consumption further. With the

Table 1
The dependence of the performance of SGMZI on the height of the dielectric.

The height of the dielectric	The variation of the real part of the effective index Re(n_{eff})	$V_\pi \cdot L$ (V mm)
20	0.00250	0.641
40	0.00219	1.461
60	0.00194	2.477
80	0.00173	3.703

Table 2
The dependence of the performance of SGMZI on the refractive index of the dielectric.

The refractive index of the dielectric	The variation of the real part of the effective index Re(n_{eff})	$V_\pi \cdot L$ (V mm)
1.44 (SiO_2)	0.00209	2.898
1.746 (Al_2O_3)	0.00215	1.916
1.98 (Si_3N_4)	0.00219	1.461
2.098 (HfO_2)	0.00221	1.291

advantages of high operation speed, large extinction ratio, low power consumption, and broad bandwidth, these electro-optical logic gates offer competitive options for applications in future optical computing and signal processing.

Acknowledgments

This work is supported by the National Natural Science Foundation of China (61475137, 61274132, 61307071), the 863 Program (2015AA017001), the Specialized Research Fund for the Doctoral Program of Higher Education (20120101110054, 20133305120004), the Science and Technology fund of Zhejiang Province (2013C31083), the Opened Fund of the State Key Laboratory on Integrated Optoelectronics (IOSKL2015KF03), the Natural Science Foundation of Ningbo (2013A610005), and the K.C. Wong Magna Fund in Ningbo University.

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