Optics Letters

Inverse-designed single-step-etched colorless 3 dB couplers based on RIE-lag-insensitive PhC-like subwavelength structures

Luluzi Lu,[1,†] Deming Liu,[1,†] Feiya Zhou,[1] Dongyu Li,[1] Mengfan Cheng,[1] Lei Deng,[1] Songnian Fu,[1] Jinsong Xia,[2] and Minming Zhang[1,*]

[1]School of Optical and Electrical Information, Huazhong University of Science and Technology, Wuhan 430074, China
[2]Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan 430074, China
*Corresponding author: mmz@hust.edu.cn

Received 7 September 2016; revised 30 September 2016; accepted 4 October 2016; posted 5 October 2016 (Doc. ID 275485); published 28 October 2016

Inverse-designed free-form nanophotonic structures have shown great potential in designing ultra-compact integrated photonic devices, but strict fabrication requirements may hinder further applications. We propose here a photonic-crystal-like (PhC-like) subwavelength structure, which is insensitive to the lag effect that is the most common fabrication error. A colorless 3 dB coupler employing such a structure is designed, fabricated, and characterized. With only one-step etching, the coupling region of our final device occupies a compact footprint of 2.72 × 2.72 μm. The simulated insertion loss of each output port is about 3.2 dB over 100 nm bandwidth around 1550 nm, and the measured insertion losses of both ports are 3.35 dB, on average, over the observable 60 nm bandwidth with a near zero loss imbalance.

OCIS codes: (230.1360) Beam splitters; (230.3120) Integrated optics devices; (160.3918) Metamaterials; (230.1150) All-optical devices.

http://dx.doi.org/10.1364/OL.41.005051

The complementary metal oxide semiconductor (CMOS) compatible subwavelength (SW) structures have drawn more and more attention recently, as silicon photonics and corresponding fabrication technologies have experienced remarkable progress. By tuning structure parameters, such as widths, heights and periodicity at subwavelength dimensions, much success has been gained on performance-enhanced or footprint-reduced silicon SW structure-based photonic components, including colorless directional couplers [1], low loss optical crossings [2], low loss grating couplers [3], mode converters [4], and wavelength demultiplexing grating couplers [5], among others. Different methods, such as particle swarm optimization [2], topology optimization [4–6], and nonlinear direct-binary-search (DBS) algorithms [7], were employed to inversely design SW components. Recently, two independent research groups experimentally demonstrated ultra-compact, all-dielectric on-chip devices, a wavelength demultiplexer [6], and a polarization beam splitter [7], based on SW structures consisting of patterns of specially shaped air holes etched into silicon. By engineering the dielectric permittivity profile at the full design space with the aid of the inverse design algorithms, these SW structures may offer a powerful capability of developing photonic components with previously unattainable functionality or higher performance and smaller footprints than traditional ones for a variety of applications.

However, it still remains a huge challenge to fabricate these complex SW structure-based devices to precisely match predesigned specifications. Both sets of SW structures in [6,7] were meant to be fabricated using single step lithography and plasma etching process on silicon-on-insulator (SOI) platforms to prevent alignment errors on the nanoscale. The authors of [6] theoretically demonstrated that the SW structures were robust to sustain 8 nm over- or under-etching. Meanwhile, the authors of [7] claimed a tolerance to fabrication errors of up to ±20 nm in the top silicon thickness by simulation. However, both of them neglected the non-uniform etch depth in the single step plasma etching process because the inverse design algorithms employed generated device patterns in a binary manner and could only handle uniform etch depth. Therefore, the etch depths of all air holes were simply assumed to be the same in both cases, while it may be quite different from the real scenario.

The reactive ion etching (RIE) lag effect, the most common and typical fabrication error in the plasma etching process, accounts for the dependence of the etching rate on the feature size (such as groove width, circle radius, etc.) [8]. Studies show that the smaller feature size leads to the shallower etch depth during a single etch process [9,10]. An etch depth decrease of up to 40 nm or 60 nm was observed for etched grooves with widths from 450 to 50 nm or for etched circular holes with radii from 95 to 50 nm on SOI wafers, respectively. As to the SW structures in [6,7], the non-uniformity of etch depths would become significant because the feature sizes of etch regions may change several or even dozens of times, leading to probably serious distortions to the pre-designed permittivity

profiles and the consequent specification errors or performance degradations.

In this work, a RIE-lag-insensitive PhC-like SW structure for inverse design of single-step-etched on-chip components is proposed. We design and experimentally demonstrate a compact wideband 3 dB coupler based on the PhC-like SW structure using an improved inverse design algorithm. The simulation and experiment results show that 3 dB couplers based on PhC-like SW structures are not only insensitive to the lag effect, but also strongly robust to fabrication errors, which implies that the proposed PhC-like SW structure can be an excellent candidate for precise inverse design of all-dielectric, on-chip photonic components.

Generally, a component is divided into M×N unit shapes, called "pixels," logically in a full-space inverse design process. Each pixel may be fully filled by silicon or air, corresponding to the logical "1" or "0" state, respectively, of the binary pattern that comes from the algorithm to perform finite-difference time domain (FDTD) simulations. Due to the randomness of algorithm, local patterns of an isolate "0" pixel, several or dozens of adjacent "0" pixels will occur randomly, as shown in Figs. 1(a)–1(b). The "fusion" of different numbers of adjacent "0" pixels forms etch regions with different feature sizes, which will cause RIE lag in fabrications. We use a novel partial-air-filling, instead of full-air-filling, feature shape to represent the "0" pixel in a SW structure pattern. For the feasibility of fabrication, a silicon square with a central circular air hole is chosen as the partial-air-filling unit shape. For logical patterns having adjacent "0" pixels, there are silicon walls between the neighboring air holes to prevent "fusions" of "0" pixels, as shown in Fig. 1(c). Compared with SW structures in [6,7], there is an essential evolution for the proposed PhC-like one that all the etch regions will maintain the same feature size for any logical patterns, which is critical to suppress the etch depth fluctuations caused by the RIE lag.

In order to verify the RIE-lag-insensitive feature and precise inverse design capability of the proposed PhC-like SW structure, we designed, fabricated, and characterized a wideband 3 dB coupler based on such a structure, first. The coupler has a footprint of 2.6 × 2.6 μm and is defined on a regular SOI wafer with a 220 nm-thick top silicon ($n \approx 3.45$) layer over a 3 μm-thick buried oxide ($n \approx 1.45$) layer. The device is discretized into 20 × 20 pixels for inverse design. Each pixel is in the shape of a silicon square (130 × 130 nm) with a central circular air hole (radius $r = 45$ nm, etch depth = 140 nm). The layout of input and output waveguides is axisymmetrical. The width of such waveguides is 500 nm and the gap between the two output waveguides is 1 μm wide.

The figure-of-merit (FOM) of the device for inverse design is defined as

$$\mathrm{FOM} = 1 - (1-\alpha)\cdot\frac{1}{N}\cdot\sum(|t_1 - 0.5| + |t_2 - 0.5|) - \alpha\cdot\frac{1}{N}\cdot\sum|t_1 - t_2|, \quad (1)$$

where t_1 and t_2 are the power transmittance of two channels and N is the number of wavelengths; five wavelengths over a 110-nm range are taken into consideration in our simulations. In order to deal with the local optimization property of inverse design algorithms, a weighting coefficient α, with a value from $0 \sim 1$, is used to reach a compromise between the insertion loss (IL) defects (compared to the ideal value) of both channels and the IL imbalance. Therefore, the second item on the right side of equation (1) means a weighted average transmittance defect (equivalent to IL defect), and the third one represents a weighted average transmittance imbalance (equivalent to IL imbalance). For an ideal colorless 3 dB coupler, t_1 and t_2 should be 0.5, and the second and the third items of (1) are both zero, corresponding to FOM = 1.

The 3D FDTD simulations via a commercial software (Lumerical FDTD Solutions) are performed to calculate the FOM, and an improved DBS optimization algorithm is employed to inverse design the device pattern. For a conventional nonlinear DBS optimization algorithm [7,11], a randomly generated 20 × 20 binary matrix is set as the initial pattern and an initial FOM is calculated. Then, one reverses the logical state of each pixel ("0" to "1" or "1" to "0") one by one and evaluates the FOM simultaneously. If the FOM is improved, the new pixel state is maintained. If not, the last state is recalled. One iteration ends when all the pixel states are inspected and the final pattern is set as the initial one of the next iteration. The optimization terminates when FOM exhibits no improvement compared with that of last iteration. For the conventional DBS algorithm, it can be found that the average IL defect increases, while the average IL imbalance decreases, with increasing α. For the case of $\alpha = 0.2$, the best trade-off between the two performance parameters is obtained.

The corresponding optimum SW structure pattern is shown in Fig. 2(a), which seems random and asymmetrical. The simulated ILs of both channels (dotted and dashed lines in Fig. 2(c) are approximately 3.35 dB in average, and the IL imbalance reaches 0.2 dB around 1520 nm. Apparently, the optimized results are still not good enough. This probably results from the local optimization property of DBS algorithm and we think that such situation will get worse when more than one target item in the FOM will have to be optimized at the same time. For an ideal 3 dB coupler with axisymmetrical geometry, the distributions of the electric field and the dielectric permittivity

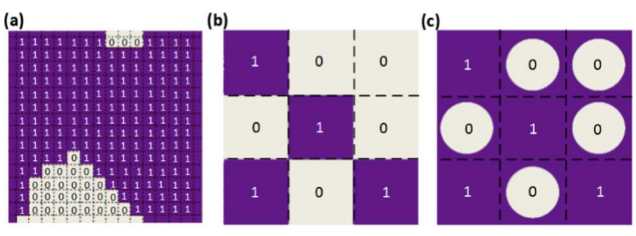

Fig. 1. Local patterns of SW structures in (a) Ref. [6], (b) Ref. [7], and (c) this work. Markers "0" and "1" present the logical states of pixels separated by dashed lines.

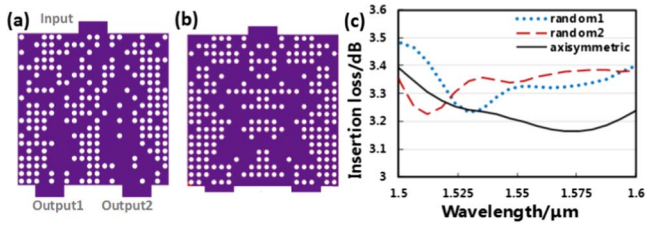

Fig. 2. (a) Optimized pattern of the conventional DBS algorithm; (b) optimized pattern of the improved DBS algorithm; (c) optimum IL profiles of the conventional (dotted and dashed lines) and the improved (solid line) algorithm.

inside the device should also be axisymmetrical, theoretically. In our improved optimization algorithm, the patterns always maintain axisymmetry, and then the IL imbalance will be zero automatically. In this case, only one target item, the average IL defect, need to be optimized in simulations. Specifically, the initial patterns are generated axisymmetrically by mirroring a random 20 × 10 binary matrix along the central axis. All intermediate patterns are also kept axisymmetrical by toggling two axisymmetric pixels at the same time, instead of reversing pixels one by one conventionally, during each iteration. Figure 2(b) shows the optimum pattern using the improved algorithm. Due to the intrinsic balance between two channels, both IL profiles are identical [solid line in Fig. 2(c)]. It can be found that not only a perfect output balance, but also a remarkable IL reduction (up to 0.2 dB) at long wavelengths, is achieved in the simulation based on the improved algorithm.

We fabricated the devices using an electron-beam lithography (EBL) system (Vistec EBPG 5000 Plus) to pattern a 330 nm ZEP-520A electron-beam resist layer spun on the samples, and an inductively coupled plasma (ICP) etcher (Plasmalab System100) to transfer the mask to the silicon device layer. During the single step etching process, we controlled the etching time (called "full-etching time") to fully etch the strip waveguides (220 nm). Due to the RIE lag effect, the circular holes were unable to be fully etched, unlike the waveguides. After etching test chips with circular holes with different radii in the same full-etching time, we measured the profile of the etch depths versus the radii, given in Fig. 3(b). It can be found that the holes deepened about 43 nm along with radius increase of 30 nm. Specifically, Fig. 3(a) shows the cross section SEM picture of the circular holes with different radii from 30 to 60 nm with a step of 5 nm. The etch depth for the 45 nm radius is about 140 nm (the etch depth we used in the simulations).

The SEM picture of the fabricated SW structure 3 dB DC is illustrated in Fig. 3(c). A broadband amplifier spontaneous emission (ASE) light source was vertically coupled into the input port by a chirped 1D grating coupler [12]. The same grating couplers were used at the two output ports and an optical spectrum analyzer (Yokogawa AQ6370C-20) was employed to measure the light coupled out. We measured ILs of a reference component consisting of two same coupling gratings and a waveguide as long as the coupler. By subtracting such ILs from those of the coupler, one can obtain the exact ILs of the SW structure. The measured IL profiles of both channels (solid lines) are shown in Fig. 3(d), which are less than 4 dB over about 60 nm bandwidth (1520–1580 nm). Usually, there are many air holes distributed along the device edges, which are very close (about 20 nm) to the border. However, the quite thin silicon walls between such holes and the device border would be etched through, as shown in Fig. 3(c). This may be the main reason to degrade the device performance at longer wavelengths.

In order to prevent such damage of device borders, we redefine the general PhC-like SW structure by adding an additional 60-nm wide silicon wall (the light gray area) outside the pixelated area, as illustrated in Fig. 4(a). The 60-nm width of the outside wall can assure borders in good condition, according to our experimental results. The footprint of the coupler becomes 2.72 × 2.72 μm. The improved DBS optimization procedure is then repeated. The new optimum pattern is shown in Fig. 4(b), and it resembles a fine-tuned Y-branch structure. The SEM picture, Fig. 4(c), reveals that the edge damage is avoided successfully. Figure 4(d) shows that the measured IL profiles match the simulated profiles much better. Not only low IL profiles (less than 3.5 dB and an average of 3.35 dB over 60 nm bandwidth), but also a near zero (0.1 dB in average) IL imbalance is realized at the same time using the improved structure.

In order to reveal the advantages of the PhC-like SW structure, we demonstrated another type of 3 dB couplers, based on the SW structure with a square feature shape proposed in [7] for comparison. The same inverse design algorithm, SOI wafer, fabrication process, and measurement setup, as described previously, have been employed. The device is also divided into 22 × 22 pixels and each pixel is in the shape of a 120 × 120 nm square. The optimum pattern and SEM picture are shown in Figs. 5(a) and 5(b), respectively. It can be seen that air holes with different patterns occur in the device axisymmetrically but randomly.

We experimentally measured the etch depths of different hole patterns of the device in Fig. 5(a) as we did the circular

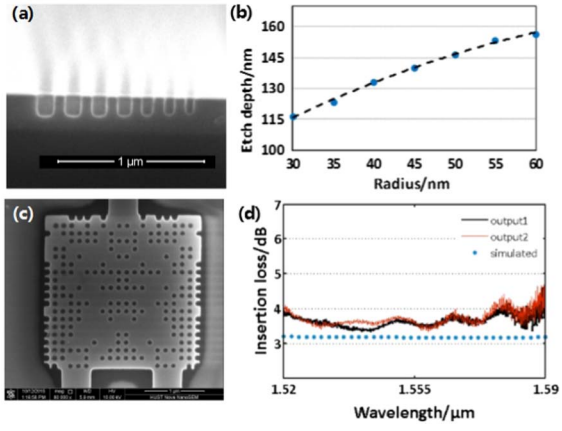

Fig. 3. (a) Cross section SEM picture of the testing holes with different radii from 30 to 60 nm with steps of 5 nm; (b) measured etch depth versus different hole radius (dots) and the fitting curve (dash line); (c) detailed SEM of the 3 dB coupler; (d) simulated (dotted line) and measured (solid lines) IL profiles.

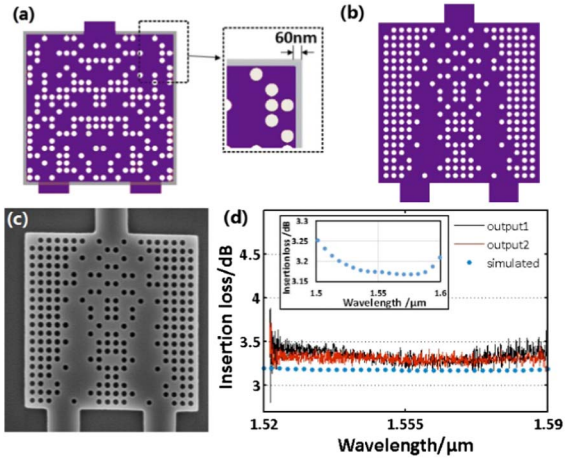

Fig. 4. (a) Modified PhC-like SW structure with an outside silicon wall; (b) new optimum pattern using the modified SW structure; (c) SEM of the fabricated device; (d) simulated (dotted line) and measured (solid lines) IL profiles of the coupler in (c), and the inset shows the simulated IL from 1500 to 1600 nm.

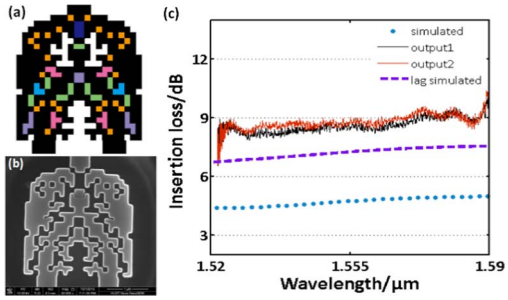

Fig. 5. (a) Optimum pattern and (b) the SEM picture of the 3 dB coupler based on square-feature-shape SW structures. In (a), different colors mark out the regions with different etch depth, see Table 1 for more details. (c) Simulated IL profiles without RIE lag (dotted lines), with RIE lag (dashed lines) and measured profiles (solid lines).

Table 1. Etch Depths of the Seven Types of Air Hole Patterns of the Single-Step-Etched Square-Feature-Shape SW Structure DC

Patterns							White
Etch depth/nm	160	170	177	185	192	200	220

holes using test chips. Generally, the holes with large areas (in white) were etched fully, while those with small sizes (in colors) were under-etched, due to the RIE lag. Specifically, the average etch depth of the isolated square holes (in orange) was 160 nm. We also found that the etch depth was dependent upon not only the length of the shorter edge but also the shape of the air holes. According to the measured results, we simply classify all air holes patterns into seven types based on the average etch depths, as shown in Table 1.

The simulated IL profiles with or without the consideration of lag effect and the measured profiles of the square-feature-shape SW coupler are shown in Fig. 5(c). The simulated IL, without the lag effect (dotted line), averages about 4.75 dB. It is 1.55 dB larger than that of the PhC-like SW coupler, which may result from an air square hole tuning the local permittivity more coarsely than a silicon square with a central air hole. Compared with the simulated and measured IL profiles of the PhC-like SW coupler, the simulated profile of the square-feature-shaped SW coupler, with consideration of the lag effect (dashed line), increased about 2.3 dB at 1550 nm, and the measured profiles (solid lines) increased an average of 3.9 dB. The simulation and experiment results show clearly that notable changes of air hole patterns in SW structures would cause significant etch depth non-uniformity due to RIE lag in single step etching process and may lead to severe performance degradation.

Finally, to further investigate the fabrication accuracy acquisition of the proposed structure, DCs with the same PhC-like SW pattern but different void radii from 37 to 53 nm with a step of 4 nm were designed and fabricated using the same etching process. The measured average IL increased about 0.4 dB and 1 dB for ±4 nm and ±8 nm radii changes, respectively, compared with the device with a void radius of 45 nm, which means that the PhC-like SW structure-based DCs were robust to fabrication errors of void radius.

In conclusion, we designed, fabricated, and characterized an ultra-compact (2.72 × 2.72 μm) colorless 3 dB coupler based on a novel PhC-like SW structure using an asymmetrical DBS algorithm. The asymmetrical DBS algorithm can minimize the IL imbalance to obtain better IL performance during inverse design. The PhC-like SW structure can eliminate the random change of patterns of air holes and offer an outstanding RIE-lag-insensitive feature in single step plasma etching processes. The measured etch depth of all air voids of the proposed coupler maintain uniformity, and the simulated and measured average ILs are 3.2 dB and 3.35 dB over 60 nm bandwidth, respectively, with a nearly zero IL imbalance. Finally, we also experimentally demonstrated that the coupler is robust enough to sustain ±8 nm fabrication errors of the void radius at the cost of 1 dB IL increase. Compared with pioneering work, the PhC-like SW structure is quite robust to fabrication errors and offers the capability of developing integrated photonic components to precisely match inverse-designed functions and specifications on SOI platforms, which may help to promote practical applications of nanostructure components greatly.

Funding. National High Technology Research and Development Program of China (2015AA015504); Major Project of Science and Technology Innovation Program of Hubei Province of China (2014AAA006); National Natural Science Foundation of China (NSFC) (61107051).

†These authors contributed equally to this work and should be considered co-first authors.

REFERENCES

1. R. Halir, A. Maese-Novo, A. Ortega-Moñux, I. Molina-Fernández, J. Wangüemert-Pérez, P. Cheben, D. X. Xu, J. Schmid, and S. Janz, Opt. Express **20**, 13470 (2012).
2. P. Sanchis, P. Villalba, F. Cuesta, A. Håkansson, A. Griol, J. V. Galán, A. Brimont, and J. Martí, Opt. Lett. **34**, 2760 (2009).
3. R. Halir, P. Cheben, S. Janz, D. X. Xu, Í. Molina-Fernández, and J. G. Wangüemert-Pérez, Opt. Lett. **34**, 1408 (2009).
4. J. Lu and J. Vučković, Opt. Express **21**, 13351 (2013).
5. A. Y. Piggott, J. Lu, T. M. Babinec, K. G. Lagoudakis, J. Petykiewicz, and J. Vučković, Sci. Rep. **4**, 7210 (2014).
6. A. Y. Piggott, J. Lu, K. G. Lagoudakis, J. Petykiewicz, T. M. Babinec, and J. Vučković, Nat. Photonics **9**, 374 (2015).
7. B. Shen, P. Wang, R. Polson, and R. Menon, Nat. Photonics **9**, 378 (2015).
8. K. O. Abrokwah, *Characterization and Modeling of Plasma Etch Pattern Dependencies in Integrated Circuits* (Massachusetts Institute of Technology, 2006).
9. Y. Tang, Z. Wang, L. Wosinski, U. Westergren, and S. He, Opt. Lett. **35**, 1290 (2010).
10. J. Zou, Y. Yu, and X. Zhang, Opt. Express **23**, 32490 (2015).
11. B. Shen, R. Polson, and R. Menon, Opt. Express **23**, 20961 (2015).
12. Y. Ding, C. Peucheret, H. Ou, and K. Yvind, Opt. Lett. **39**, 5348 (2014).