Lithography Simulation for the Fabrication of Silicon Photonic Devices with Deep-Ultraviolet Lithography

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***Abstract*—We demonstrate the lithography simulation for the fabrication of silicon photonic devices using deep-ultraviolet lithography. Once the distortions arising from the fabrication process are accounted for, the comparison between predicted and measured results is excellent.**

I. Introduction

In recent years, a wide variety of silicon photonic devices have been demonstrated on the silicon-on-insulator (SOI) platform. Due to the high refractive index contrast, most silicon photonic devices are highly sensitive to dimensional variations and require high-resolution fabrication processes. Electron-beam lithography has been used extensively for fabrication in research, but it is unsuitable for commercial applications. Alternatively, deep-ultraviolet (DUV) lithography, especially at 193 nm [1], has been proven to be capable of making high-quality photonic devices in silicon, and, more importantly, it is CMOS-compatible and can be used for high-volume production. However, with DUV lithography, it is difficult to optimize the illumination settings for various types of patterns simultaneously, e.g., the settings that are optimized for isolated structures such as photonic wires are usually not ideal for dense structures such as photonic crystals [1]. Moreover, researchers are developing devices with feature sizes that are even smaller than the resolution limit, such as integrated waveguide Bragg gratings [2] that suffer from serious lithographic distortions. Therefore, it is important to include the effects of the fabrication process in the design flow so that they are properly accounted for [3]. Image distortions that happen during fabrication of electronic circuits in CMOS advanced processes are routinely corrected, but such corrections may not be compatible with the significantly different and more diverse structures that are encountered in silicon photonics circuits.

In this paper, we use an advanced lithography simulation tool [4] to predict the fabrication imperfections of silicon photonic devices during the lithography process. As mentioned above, integrated Bragg gratings are extremely sensitive to the lithography process, and we will focus on them here. After lithography simulation, we simulate the spectral responses of the virtually fabricated grating devices, and we obtain good matching between the simulation and experimental results.

II. Design and Fabrication

The integrated Bragg gratings are designed in a compact silicon strip waveguide. The waveguide thickness and width are 220 nm and 500 nm, respectively. The thickness of the buried oxide layer is 2 μm. The gratings are achieved by corrugating the waveguide sidewalls. Three types of corrugation shape are used in the mask layout: square, trapezoidal, and triangular, as shown in Fig. 1. For each shape, there are four devices with different corrugation widths (10, 20, 30, and 40 nm). The

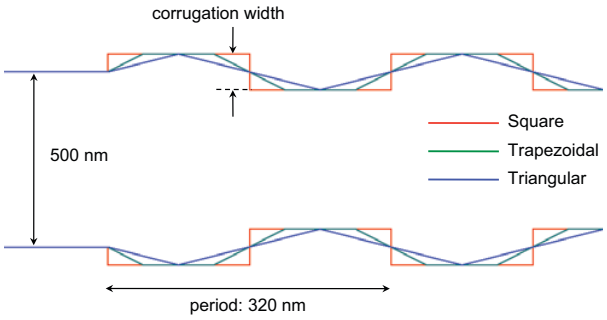

Fig. 1. Schematic illustration of corrugations used in the mask, not to scale.

devices were fabricated via ePIXfab at IMEC using a CMOS-compatible process. The pattern was defined using 193 nm DUV lithography with an ASML PAS5500/1100 step-and-scan system and a dry etching process [1]. Fig. 2 shows the top-view SEM image of a fabricated device designed with 40 nm square corrugations (device A). Unsurprisingly, the fabricated corrugations are severely rounded and resemble sinusoidal shapes. As a result, there will be a significant performance mismatch between the originally designed/modeled device and the device actually fabricated, specifically, the experimentally

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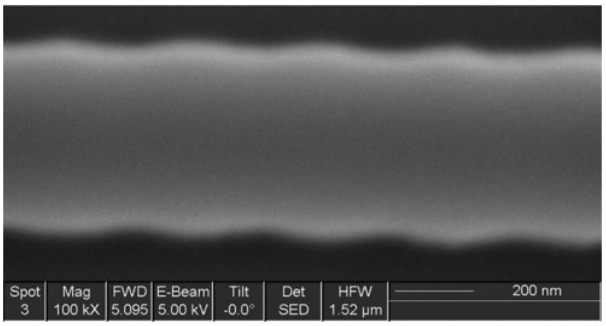

Fig. 2. Top view SEM image of the fabricated device A.

measured bandwidth is usually much narrower than the design value [2].

III. Lithography Simulation

To implement the lithography simulation, we use a commercial tool that has been widely used in the microelectronics industry [4]. For the optical system, we use a conventional circular illumination source. The numerical aperture (NA) and the partial coherence factor (σ) are the key parameters that determine the corrugation distortions; we use NA = 0.6 and σ = 0.6 in our simulation. Note that these parameters were not provided by the foundry, but were estimated so that the post-lithography simulation fit the experimental data for device A and were then fixed for all other devices. Fig. 3 shows the simulation results for device A (the fabricated device is shown in Fig. 2). We can see that the corrugations are greatly smoothed, and their effective amplitudes are also reduced.

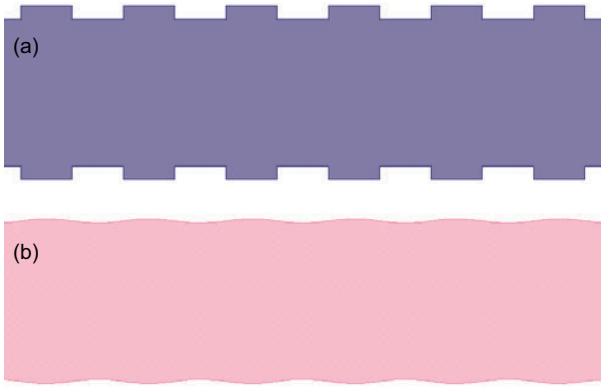

Fig. 3. Lithography simulation for device A. (a) Original design, (b) Simulation result.

IV. Post-Litho Simulation and Measurement

After the lithography simulation, we simulate the spectral responses of the virtually fabricated grating devices using a two-dimensional (2D) finite-difference time-domain (FDTD) method [5], and then compare them with the original design as well as the measurement results of the devices actually fabricated. The measurement method was described in detail in [2]. Fig. 4 shows the transmission spectra for device A. It can be seen that the original design has a bandwidth of about 25 nm, in contrast, the post-litho simulation shows a much narrower bandwidth of about 8 nm. Note that the thickness of the waveguide was slightly reduced to 216 nm in the simulation in order to match the Bragg wavelength [6], which has little effect on the bandwidth. The measured extinction ratio is less than that predicted by the FDTD simulation, which is common for integrated Bragg gratings [2]. This discrepancy may arise from a number of factors, including sidewall roughness [7], fabrication nonuniformity [6], random defects, etc. Fig. 5 shows the results for the device

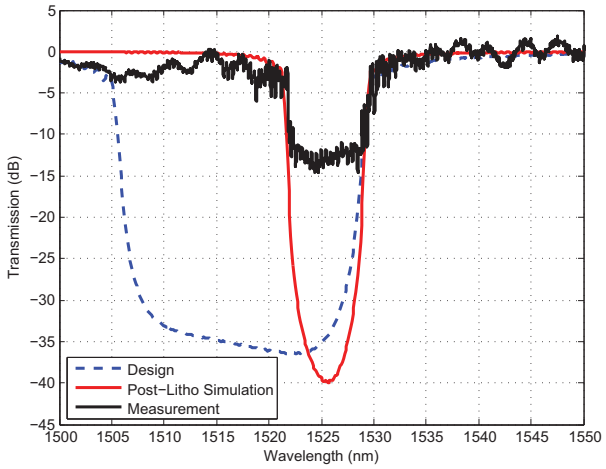

Fig. 4. Comparison for the device designed with 40 nm square corrugations.

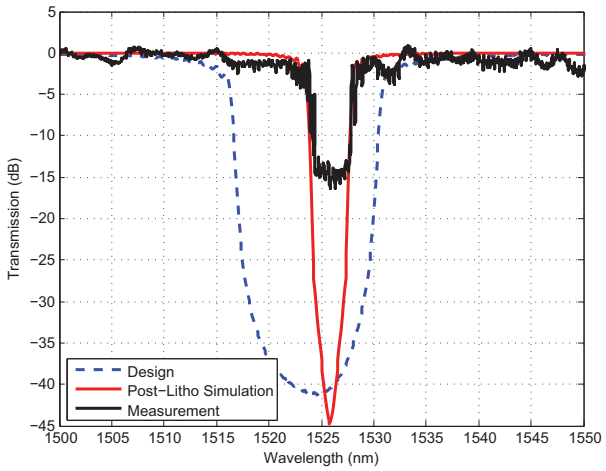

Fig. 5. Comparison for the device designed with 20 nm square corrugations.

designed with 20 nm square corrugations. Similar to Fig. 4, the post-litho simulation shows a bandwidth that is narrower than that of the original design and also agrees well with the measured bandwidth. Fig. 6 plots the simulated and measured bandwidths versus the designed corrugation widths. For all of the three shapes, the post-litho simulation agrees very well

with the measurement, whereas the mismatch between the original design and the measurement is very large.

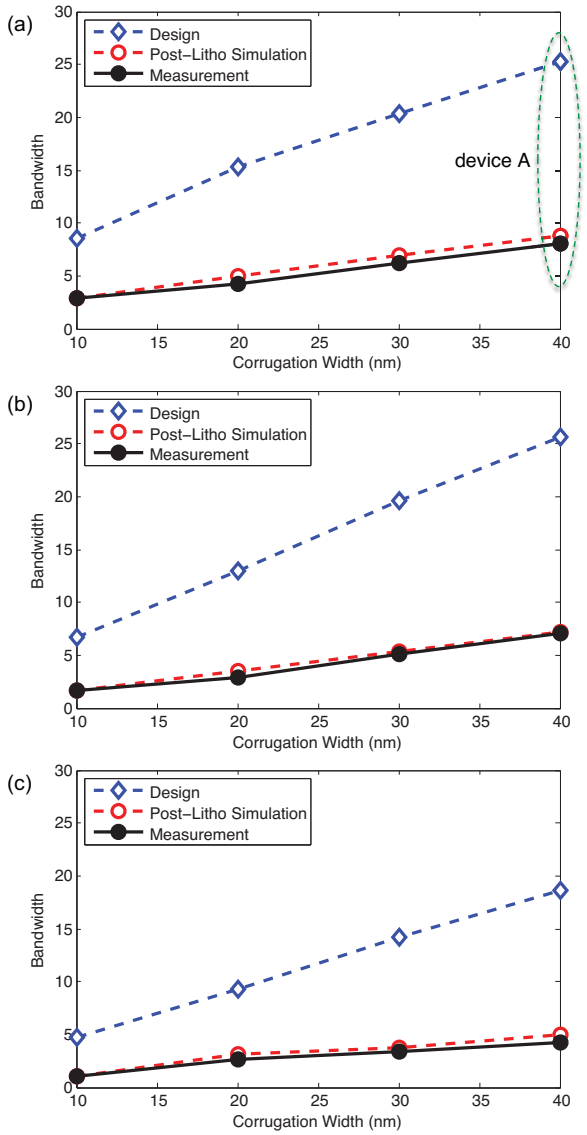

Fig. 6. Bandwidth versus designed corrugation width for (a) square, (b) trapezoidal, and (c) triangular corrugation shapes.

V. Discussion and Conclusion

In summary, we have demonstrated that lithography simulation can effectively predict the fabrication of integrated waveguide Bragg gratings with DUV lithography. This technique can be applied to many other silicon photonic devices, especially ones that are sensitive to lithographic distortions. For example, Fig. 7 shows the simulation result for a photonic crystal cavity. We can see that the simulated bulk holes are smaller than the designed ones, therefore, a bias should be applied to the bulk holes in the mask to obtain the desired hole sizes. Due to the optical proximity effect, the edge holes are smaller than the bulk holes [1], and the displacement of the two cavity side holes introduces extra distortions. Therefore, differential bias needs to be applied to the holes next to the cavity, and this cannot be easily done without lithography simulations.

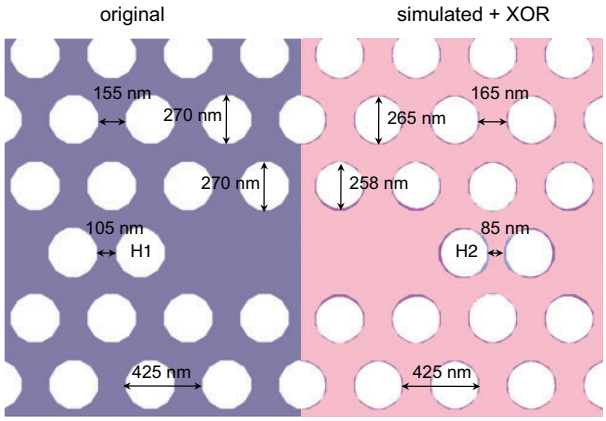

Fig. 7. Lithography simulation for a photonic crystal cavity with three missing holes in the centre. XOR: Boolean operation of XOR (exclusive or) between the original and simulated layouts. The two cavity side holes (H1 and H2) are displaced in order to achieve a high Q-factor.

We believe that this work is an important step in the direction of design-for-manufacturing in the field of silicon photonics. There are, of course, many issues that need to be addressed, e.g., taking account of the etching process and the wafer thickness variations. Fortunately, the development of silicon photonic fabrication can benefit greatly from the vast library of knowledge that already exists in the microelectronics industry, as well as the continued advancements.

Acknowledgment

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