Efficient, compact and low loss thermo-optic phase shifter in silicon

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Abstract: We design a resistive heater optimized for efficient and low-loss optical phase modulation in a silicon-on-insulator (SOI) waveguide and characterize the fabricated devices. Modulation is achieved by flowing current perpendicular to a new ridge waveguide geometry. The resistance profile is engineered using different dopant concentrations to obtain localized heat generation and maximize the overlap between the optical mode and the high temperature regions of the structure, while simultaneously minimizing optical loss due to free-carrier absorption. A 61.6 μm long phase shifter was fabricated in a CMOS process with oxide cladding and two metal layers. The device features a phase-shifting efficiency of 24.77 $\pm$ 0.43 mW/π and a -3 dB modulation bandwidth of 130.0 $\pm$ 5.59 kHz; the insertion loss measured for 21 devices across an 8-inch wafer was only 0.23 $\pm$ 0.13 dB. Considering the prospect of densely integrated photonic circuits, we also quantify the separation necessary to isolate thermo-optic devices in the standard 220 nm SOI platform.

OCIS codes: (250.7360) Waveguide modulators; (250.5300) Photonic integrated circuits.

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1. Introduction

The silicon-on-insulator (SOI) material platform has received much recent attention for its capability to support scalable and inexpensive photonic integrated systems-on-chip. While the field has mainly targeted the telecommunication and data-interconnect industry, new applications such as phased antenna arrays [1, 2] and quantum photonic circuits [3] are attracting increased interest. Two mechanisms are most commonly used for effecting a change of silicon's index of refraction: free-carrier plasma dispersion and the thermo-optic effect [4]. The plasma dispersion effect has been widely leveraged to realize modulation at rates above 10 GHz [5, 6]. However, the intrinsic optical loss due to free-carrier absorption makes this approach unsuitable for a number of emerging applications including integrated quantum optics. First, these modulators exhibit large passive insertion losses that make their use in large scale circuits rapidly prohibitive. Even more deleterious are the intrinsic dynamic losses which prevent pure phase modulation, as is required for tuning inteferometers without degradation of interference visibility or tuning resonators without degradation of their quality factor. Other schemes such as coherent homodyne and heterodyne detection also benefit from lossless phase modulation.

As a result of the relatively large thermo-optic coefficient of silicon near 300 Kelvin and at wavelengths near 1550 nm, $dn/dT = 1.86 \times 10^{-4}$ K^{-1} [7] where n is the refractive index and T is temperature in Kelvin, thermal effects have been successfully used to tune and stabilize

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ring resonators [8, 9] and interferometric switches [10, 11, 12, 13, 14]. Yet, when considering, for example, the development of large-scale quantum photonic circuits based on reconfigurable quantum gates [15], previously demonstrated thermo-optic phase shifters are quite long (preventing dense intregration), have notable insertion loss, or are not implemented with a standard silicon dioxide cladding used in complementary metal-oxide-semiconductor (CMOS) processes for passivation and metal layer fabrication, as shown in Table 1. While phase shifters operating at high rates and with low power requirements are desirable, these characteristics are difficult to achieve simultaneously. This is made clear by expressing power consumption in terms of speed, as $P_\pi = \frac{H}{\tau}\Delta T_\pi$ where H is heat capacity, ΔT_π and P_π are the change in temperature and power dissipation required to achieve π phase shift, and τ is the thermal time constant [10]. This relation expresses the fact that a fast and low-power device, characterized by a small $P\pi \cdot \tau$ product, has to be as small as possible (small H)—but this restricts the length of the modulation region and therefore asks for large ΔT_π, leading to the unavoidable trade-off between speed and power consumption. In many of the designs in Table 1, inneficiency and excess length [16] may be attributed to weak localization of heat to the waveguiding region while extreme efficiency levels [12] are largely due to oxide undercuts and removal of cladding. Here, we demonstrate an ultra-low loss thermo-optic phase shifter in a process with oxide cladding that is 61.6 μm long with a P_π of 24.77 $\pm$ 0.43 mW, where P_π is defined as the power required to achieve π radians phase shift, and a -3 dB bandwidth of 130.0 $\pm$ 5.59 kHz. Our device operates with a V_π of 4.36 V; more than a factor of two lower than the most competitive compact waveguide-integrated thermo-optic phase shifters [10] that benefit from the removal of the top oxide cladding. We also quantify the separation necessary to isolate thermo-optic devices in standard 220 nm SOI.

Table 1. Summary of recent thermo-optic waveguide phase shifter parameters where L is the total heater length, V_π and P_π are the applied voltage and power necessary to reach π radians of phase shift, respectively, and τ is the limiting rise or fall time constant. In results where τ is not reported, the single-pole approximation $\tau = \frac{0.35}{f_{3dB}}$ is used to convert between metrics.

	Material	Cladding	L (μ m)	Loss (dB)	V_π (V)	P_π (mW)	τ (μs)	$P_\pi \cdot \tau$ (mW·μs)
Here	SOI	SiO_2	61.6	0.23 dB	4.36	24.77	2.69	66.9
[10]	Si	Air	>9.42	0.5 dB	11.93	12.7	2.4	30.5
[12]	TiN in SOI	Air	1000	0.3 dB	0.86	0.49	144	70.5
[11]	NiSi in SOI	Air	200	5 dB	1	20	2.8	56
[17]	Cr-Au in SOI	SiO_2	700	32 dB	1.66	46	3.5	160
[14]	Ti in SOI	Air	100	8 dB	13.3	10.6	34.9	370
[16]	Metal in SOI	SiO_2	2500	< 12 dB	-	235	60	14100

2. Device geometry and fabrication

Our optimized thermo-optic phase shifter (Fig. 1 (a) and (b)) was fabricated in the OpSIS process on a SOI wafer with a 220 nm thick top silicon layer [18, 19]. Two levels of boron doping by ion implantation were used, with peak concentrations of $1.7{\cdot}10^{20}$ cm^{-3} for p++ and $7{\cdot}10^{17}$ cm^{-3} for p. Two aluminum routing layers were used; the top layer functioned as an electrical probe pad layer and as a signal routing layer while the bottom layer was used for signal routing. The metal contacting region of the phase shifter was connected to the ridge waveguide using 800 nm wide channels defined in a partially etched 90 nm thick silicon slab with both p and p++ implantation, as shown in Fig. 1(b). The measured sheet resistances were 136 Ω for the p++ -doped 90 nm thick Si layer, 13.6 kΩ for the p-doped 90 nm thick layer and 3.87 kΩ for the p-doped 220 nm thick layer.

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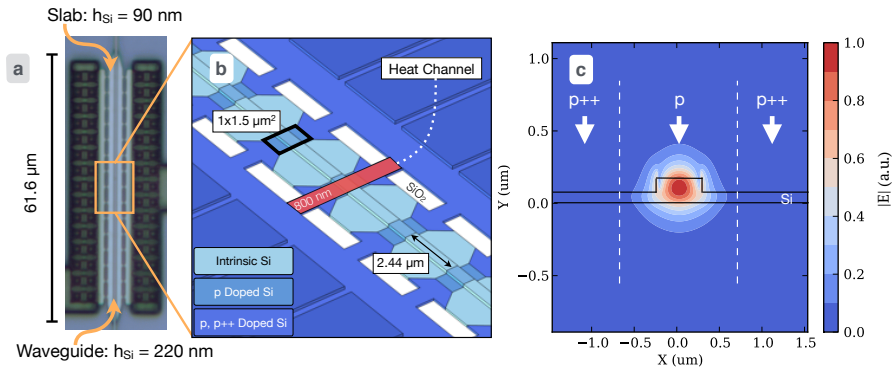

Fig. 1. (a) Optical micrograph of the structure with the vias connecting the lowest metal layer and the doped silicon clearly visible. h_{Si} denotes silicon layer thickness. (b) Perspective view of the phase shifter with annotations for relevant dimensions. (c) Doping profile along the cross section marked red in (b), overlapped with the simulated amplitude of the horizontal component of the electric field.

The design of the device largely proceeds from three principles. Overlap between the silicon-guided optical mode and the thermal profile should be maximized and heat propagation and optical loss should be minimized. By *p*-doping only the 1.0 µm wide transverse waveguide section and *p* and *p*++ doping elsewhere, heat can be generated in a small region with large optical mode overlap. Since the thermal conductivity of SiO_2 is two orders of magnitude smaller than that of silicon, the 800 nm wide channels in Fig. 1(b) connecting the contact region to the ridge waveguide efficiently restrict the outward propagation of heat. Sufficient clearance between the guiding region and the *p*++ -doped region as well as overlapping dopants with the optical mode only every 2.44 µm avoids excess losses to free-carrier absorption, as shown in Fig. 1 (c). Tapered spot size converters allow for an adiabatic transition between the single-mode channel waveguide and ridge waveguide, preventing the excitation of the higher-order modes supported in the latter. This ensures low-loss transition between channel and ridge waveguides at the input and output of the modulator. By adding or removing unit cells corresponding to tiled thermal channel sections, it is possible to achieve a desired device resistance and operating voltage while independently choosing its length.

3. Device simulations

To confirm this localization near the waveguide, we simulated the voltage and temperature fields using the COMSOL Multiphysics finite-element solver. We set room temperature boundary conditions below the buried oxide layer and 10 µm above the top oxide cladding and used previously reported thermal [20, 21, 22] and electrical conductivities for the silicon layers. Since we were interested in the intrinsic device performance, we did not include the metal contacts in the simulation space.

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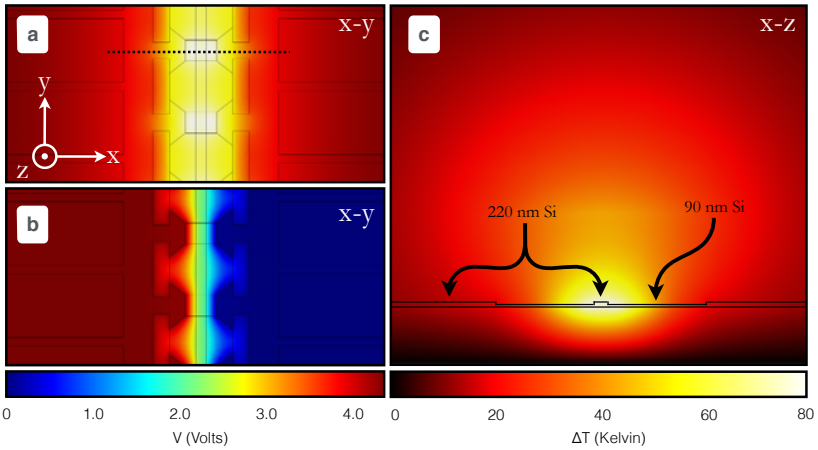

Fig. 2. Planar projections of temperature and voltage distributions from a three-dimensional simulation. (a) and (b) Show the highly localized temperature and voltage distributions, respectively, for an applied voltage corresponding to π phase shift. (c) Temperature distribution with device outline overlay for the dotted-line cross-section in (a). (a) and (c) share the same temperature color bar. The voltage is dropped almost exclusively across the thermal channel.

The device was simulated with the bias voltage set to 4.36 V, corresponding to the measured average value of V_π. Fig. 2(a) and (b) show the strong localization of the temperature and voltage drop near the waveguide as a consequence of the narrow thermal channels and dopant configuration employed here. The change in phase as a function of temperature can be expressed as $\Delta\Phi = \frac{2\pi L}{\lambda_0}\frac{dn}{dT}\Delta T$, where L is the device length, λ_0 is the free-space wavelength, $\frac{dn}{dT}$ is the thermo-optic coefficient and ΔT is the change in temperature. This can be approximated as $\Delta\Phi \simeq 2.4\pi \cdot 10^{-4} \times \Delta T \cdot L$ for the case where λ_0 is 1550 nm and $\frac{dn}{dT}$ is taken as the room temperature thermo-optic coefficient of silicon. Fig. 2(c) shows the temperature distribution in the cladding which is largely surrounding the waveguiding region. We performed the same simulation for the case with air cladding, rather than oxide, revealing that the phase delay could increase by as much as 25% for the same applied potential.

4. Device characterization

4.1. Thermo-optic phase shifter

To characterize the phase shift as a function of power dissipation, the thermo-optic modualtor was fabricated as part of one arm of an unbalanced MZI, with a measured free spectral range of 6.4 nm (Fig. 3), composed of two low-loss multi-mode interferometer (MMI) y-junctions [23]. We coupled light on chip using grating couplers [24] and performed a spectral sweep between 1520 nm and 1570 nm for each applied voltage and power dissipation level. These spectra were then fit to a sinusoid to extract the phase shift with respect to the unbiased spectra. We plot the results in Fig. 3 (e), from which we obtain a P_π of 24.77 $\pm$ 0.43 mW. This corresponds to $V_\pi = 4.36$ V given the device resistance of 769.00 $\pm$ 1.24 Ω.

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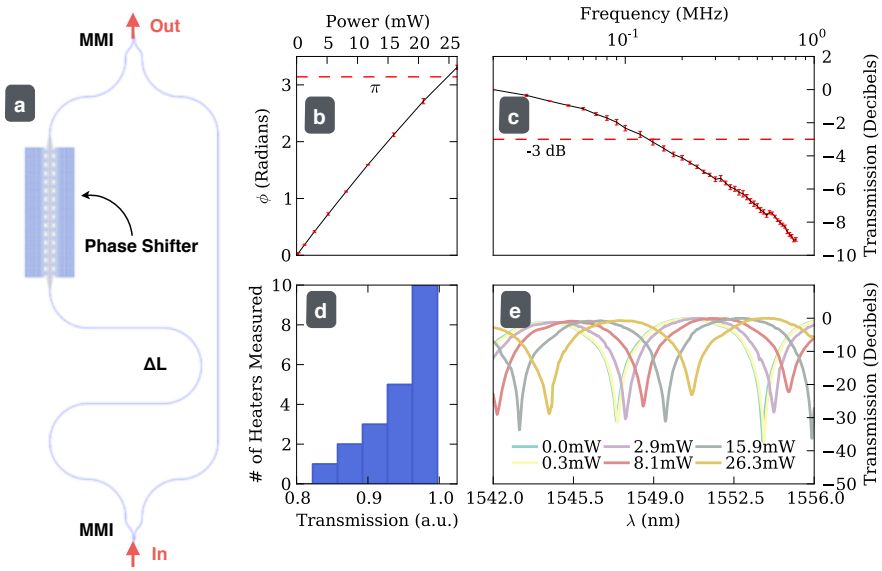

Fig. 3. (a) Annotated test structure layout including MZI with path imbalance and the thermo-optic phase shifter, (b) average phase shift versus dissipated power for three devices, (c) average response of the MZI to pure sinusoids of various frequencies for four devices with a dotted line labeling the -3 dB level, (d) histogram of the transmission through the heater for 21 devices on the same wafer, (e) MZI spectra for various power dissipation levels.

A Stanford Research Systems lock-in amplifier was used to measure the bandwidth of the thermo-optic phase shifter. The frequency of the sinusoidal output signal was swept from 20 kHz to 800 kHz and the amplitude response was recorded at each step. The -3 dB bandwidth of the the phase shifter was measured to be 130.0 $\pm$ 5.59 kHz, as shown in Fig. 3 (e). Adjacent grating couplers were measured on each of the 21 dies and their transmission spectra was recorded. The spectra were then normalized to the grating coupler spectra, MMI insertion loss and waveguide propagation loss yielding a phase shifter insertion loss of 0.23 $\pm$ 0.13 dB. The insertion losses of 21 devices measured across an 8-inch SOI wafer are summarized in the histogram of Fig. 3 (d). The low static loss of our phase shifter enables us to achieve the deep extinction shown under both passive and active operation.

4.2. Thermal decay test structure

Thermal diffusion can adversely affect the performance of adjacent photonic components, which is an important constraint when designing densely integrated large-scale photonic circuits. To manage this thermal cross-talk, it is essential to quantify the necessary separation between thermo-optic devices and other phase-sensitive components.

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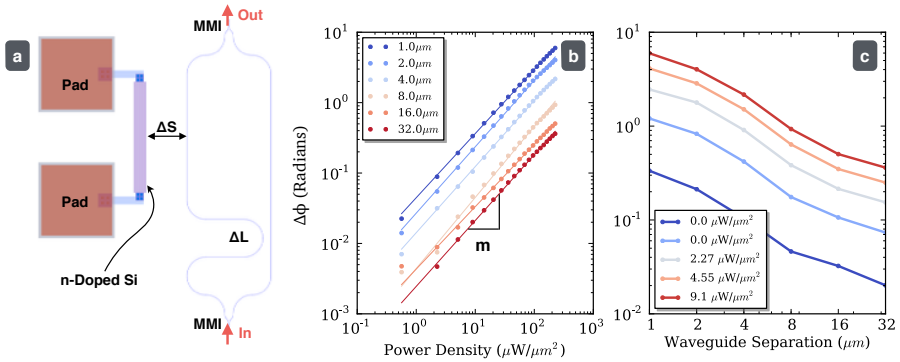

Fig. 4. (a) Annotated layout for the test structure used to probe the temperature distribution within the SOI wafer. The arms of the MZI were designed to have a large separation to avoid a phase shift in both simultaneously. (b) Phase shift imparted on left-most MZI path as a function of the waveguide to heater separation for various power dissipation levels. Power law fit lines are also shown. (c) Phase shift imparted on MZI left-most arm as a function of dissipated power for various waveguide to heater separation levels.

We used a passive unbalanced MZI to probe the decay of heat generated by an *n*-doped (phosphorus $5 \cdot 10^{-3}$ cm^{-3}) resistor, measuring 503.52 $\pm$ 0.09 Ω, running parallel with the MZI at a distance ΔS (Fig. 4a). Six structures with $\Delta S = 1$, 2, 4, 8, 16 and 32 μm were tested. The phase shift was measured for each of the six structures at various bias levels, resuling in the data shown in Fig. 4 (b) and (c). The decay of the induced phase shift $\Delta\Phi$ with power density is linear, as shown in Fig. 4(b), and can be fit to a power law $\Delta\Phi = a_0\rho^m$ where m is 0.937 $\pm$ 0.015. Fig. 4 (c) can be used to provide an indication of how far away waveguiding elements must be placed in order to achieve a desired isolation level.

5. Conclusion

We demonstrate a compact thermo-optic phase shifter that is 61.6 μm long with a P_π of 24.77 $\pm$ 0.43 mW and a -3 dB bandwidth of 130.0 $\pm$ 5.59 kHz. The propagation loss in the device is quite low at 0.23 $\pm$ 0.13 dB and is due to the overlap of the optical mode with the boron-doped silicon and mode conversion between the ridge and rib waveguide geometries. This new thermo-optic phase shifter design enables precise targeting of power dissipation and heat localization, resulting in low thermal crosstalk and high efficiency. We also characterized the thermal decay characteristics of heaters based on resistive, doped silicon in SOI.

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