Electrical Crosstalk Between Memristors in Crossbar Circuits using LAOSS

A dissertation submitted in partial fulfillment of the requirement for the degree of

Master of Technology

By

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Declaration

This is to declare that the thesis entitled**" Electrical Crosstalk Between Memristors in Crossbar Circuits using LAOSS."** submitted to the Indian Institute of Technology, Guwahati for the granting of the Master of Technology degree, is a genuine work completed under Dr. Arun Tej Mallajosyula's supervision.

I declare that this thesis is original work of mine and that this work has not been submitted for any other degree or professional qualification.

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June 2025, Guwahati

Certificate

This is to certify that the work contained in the thesis entitled,**" Electrical Crosstalk Between Memristors in Crossbar Circuits using LAOSS."** is a Bonafide work of **Dalesh Gaurishankar Patle (Roll No: 234102201),** which has been carried out in the Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati under my supervision and this work has not been submitted elsewhere for a degree. The thesis has met all of the institute's standards and is suitable for submission.

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Sincerely

Dalesh Gaurishankar Patle

Abstract

As memristor-based crossbar arrays gain traction for high-density memory applications, addressing the challenge of electrical crosstalk is essential for reliable data storage and retrieval. This study investigates crosstalk between memristors in crossbar circuits, where interference can alter resistance states in adjacent cells, potentially leading to data errors. Using the Large-Area Organic Semiconductor Simulation (LAOSS) platform, this study investigates model crossbar architectures and analyze the current-voltage (I-V) characteristics of single devices as well as full arrays, focusing on configurations with top and bottom electrodes. Through Finite-Element-Analysis (FEA) and FEM-based electrothermal modeling, Crosstalk impacts are assessed under various operating conditions, and techniques for minimizing interference are evaluated. Specific layout optimizations and material choices are also suggested to significantly reduce crosstalk, thereby improving the performance and reliability of memristor-based crossbar circuits. This work contributes practical insights into advancing scalable ReRAM technologies and enhancing data integrity in memory devices.

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1 Introduction

1.1 Introduction to Memristor

A memristor is a two-terminal electronic component that exhibits non-ohmic behaviour, characterized by its unique ability to retain its most recent resistance state even after power is turned off. This non-volatile property makes memristors particularly suitable as memory elements in advanced electronic systems [1].

The concept of the memristor was first introduced by Professor Leon Chua in 1971. In his groundbreaking paper [1], Chua proposed the memristor as a fundamental circuit element that links electric charge and magnetic flux quantities defined as the time integrals of current and voltage, respectively. While theoretically significant, the memristor remained a conceptual device at the time, as it had not yet been physically realized. Today, advancements in nanotechnology and material science have turned the memristor into a practical and transformative component for modern memory and computational technologies.

Two commonly used electronic symbols for a memristor are shown in Figure 1.

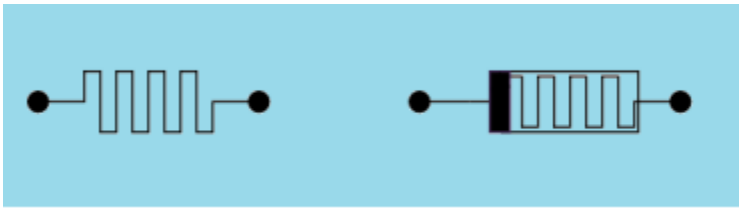

Figure 1: Electronic Symbol of Memristor [1]

1.2 I-V Characteristics of a Memristor

A memristor is a two-terminal, non-linear passive device governed by a state-dependent Ohm's law. Its current-voltage (I-V) behaviour can be described by the equation [1]:

$$V(t)=M(q)I(t) \quad (1)$$

Here, M(q), referred to as "memristance," is a function of charge (q), indicating the device's state-dependent properties. Since charge represents the time integral of current, the memristor inherently possesses a memory effect, retaining information about the history of the current passing through it.

Leon Chua established that devices with such I-V relationships exhibit a characteristic pinched hysteresis loop. As illustrated in Figure 2, this loop intersects the origin (V=0,I=0) and often appears symmetric under both polarities of the applied voltage. However, real-world devices may deviate from this symmetry due to material imperfections or practical design constraints.

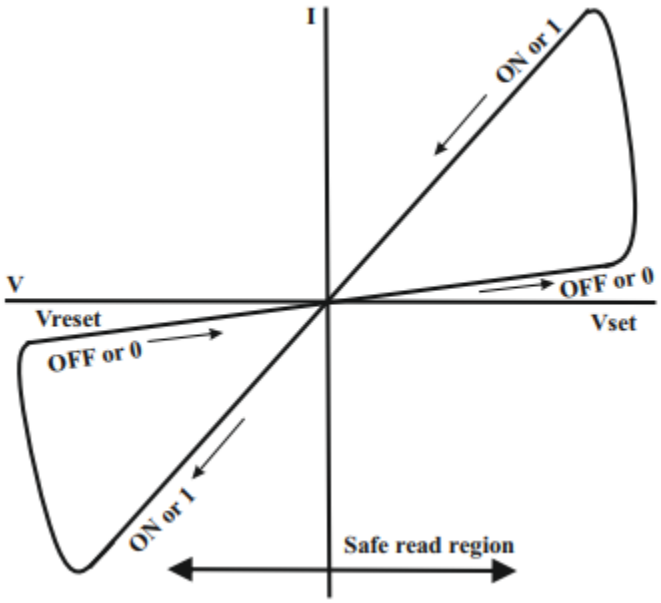

Figure 2: Memristor I-V curve showing switching between one sable state to another stable state [2]

1.3 Crossbar Architecture Using Memristors

A crossbar architecture is a fundamental circuit design used to interconnect arrays of memristors in a compact and efficient manner. As shown in Figure 3, horizontal and vertical lines (word lines and bit lines) form a grid, with memristors placed at each intersection [3]. The simplicity and scalability of this layout make it a promising solution for implementing high-density memory and neuromorphic computing systems.

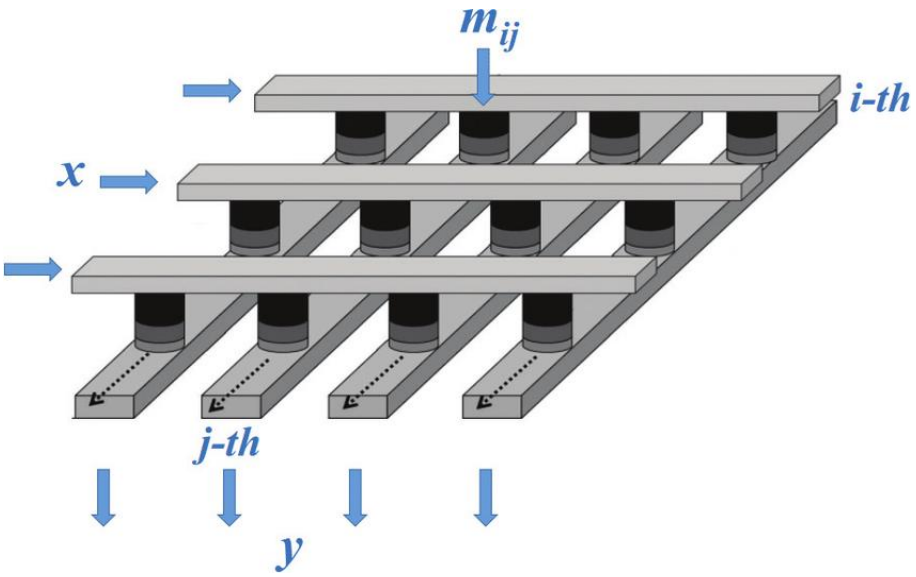

Figure 3: Crossbar architecture [3]

Memristors at each cross-point enable storing data in a minimal footprint, allowing for ultra-dense memory arrays**.** Memristors retain their programmed resistance state even when powered off, making crossbars ideal for non-volatile memory applications. The two-terminal nature of memristors reduces the complexity of interconnections and makes them well-suited for the crossbar layout.

ON/OFF Ratio: The ON/OFF ratio is a fundamental parameter that characterizes the switching performance of memristive devices. It represents the ratio of the current in the ON state (low-resistance state) to the current in the OFF state (high-resistance state).

$$\text{ON/OFF Ratio}=\frac{I(ON)}{I(OFF)} \tag{2}$$

A high ON/OFF ratio is essential for reliable data storage and accurate read operations, as it ensures clear distinction between logic levels. In crossbar architecture, however, the ON/OFF ratio tends to decrease with increasing array size due to the emergence of sneak path currents and leakage effects. This makes maintaining a high ON/OFF ratio a key design challenge when scaling memristors memory arrays.

Read margin: Read margin is a critical metric that defines the reliability of distinguishing between ON and OFF states during a read operation in memory arrays. It is influenced by the difference in current levels of ON and OFF states and is especially important in crossbar structures where sneak path currents may distort read signals. The read margin can be estimated using the formula:

$$\text{Read Margin} = \frac{I(ON) - I(OFF)}{I(ON)} \quad (3)$$

This equation (3) quantifies how much the OFF-state current encroaches upon the ON-state signal, with a higher read margin indicating better separation and more accurate readout. As the size of the crossbar array increases, the read margin typically decreases due to the cumulative effects of leakage and interference from neighbouring cells.

One-Bit line Pull-Up Technique: In this technique, a single word line is selected, and only one bit line is pulled high while all other bit lines are left floating. This configuration, however, introduces a significant number of sneak paths, resulting in higher sneak currents. The total measured current in both ON and OFF states includes contributions from these sneak paths, as shown in the equations (1) and (2).

$$I(ON) = I'(ON) + I(sneak) \quad (4)$$

$$I(OFF) = I'(OFF) + I(sneak) \quad (5)$$

Here, I′(ON) and I′(OFF) represent the intrinsic current of a single memristor cell in the ON and OFF states, respectively. I(sneak) denote the sneak path current contributed by other memristors in the crossbar array. This added current affects the accuracy of read operations, especially in larger arrays, making sneak current suppression an important design consideration.

2 Literature Survey

2.1 Memristors and their Different J-V Characteristics:

The I-V characteristics of memristors play a crucial role in understanding their behaviour in crossbar architectures. This section presents an analysis of the distinct J–V responses of chalcogenide commercial memristors (Ge_2Se_3) in their ON (low-resistance state) and OFF (high-resistance state), as shown in Figure 4. These states highlight the memristor's ability to switch between high and low resistance, a fundamental property for memory and logic applications.

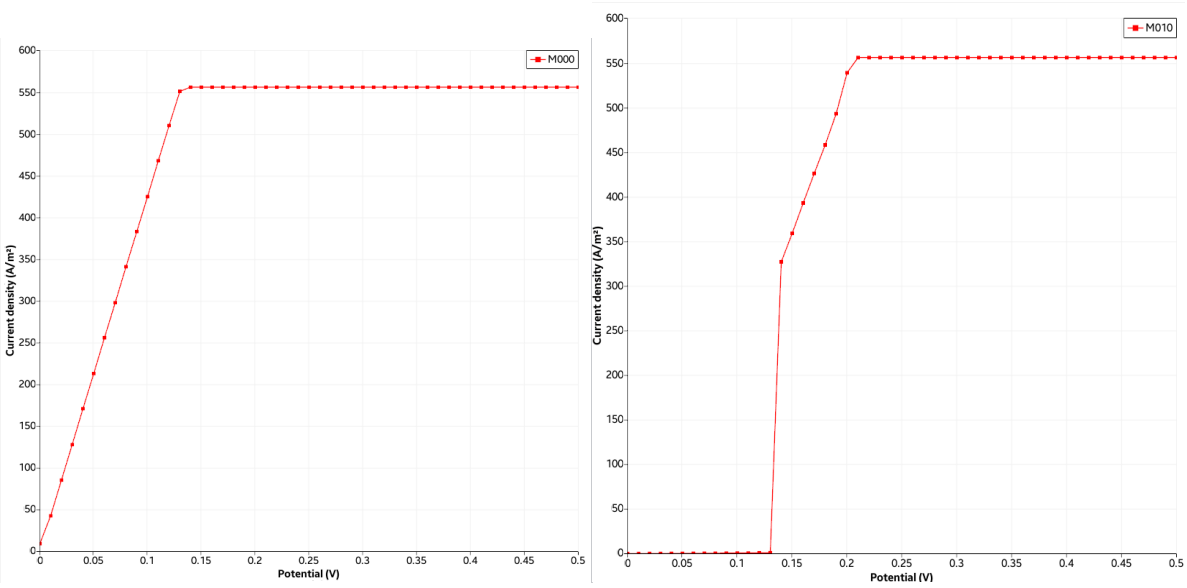

Figure 4: J–V curve of the chalcogenide commercial (Ge_2Se_3) a) ON State b) OFF State

Additionally, the memristor was operated at a reading voltage of 0.1 V to demonstrate its response during read operations in a crossbar array. The **ON** state allows for current conduction, while the **OFF** state restricts it, ensuring data can be reliably read without disturbing the stored state.

The J-V characteristics show, the distinct separation between the ON and OFF states ensures a clear read margin, crucial for data integrity in crossbar configurations. Operating the memristor at a low reading voltage (0.1 V) minimizes the risk of unintended state changes during read operations, enhancing reliability.

2.2 Electric crosstalk and Sneak path

Electrical crosstalk and sneak paths are critical challenges in memristor-based crossbar arrays that significantly impact their performance and reliability

Electrical crosstalk occurs when unintended interactions between adjacent memristors or lines in a crossbar array led to signal interference. This can alter the resistance states of nearby memristors, causing errors during read and write operations. Crosstalk is primarily caused by Capacitive Coupling, Inductive Coupling, Parasitic Effects, Sneak paths.

Sneak paths refer to unwanted current pathways through unselected memristors in the crossbar. These currents flow through unintended routes, affecting the accuracy of read/write operations. They arise due to the inherent nature of the crossbar structure, where multiple memristors share the same word and bit lines.

Sneak paths can reduce the read margin by creating ambiguities in the sensed resistance. Crosstalk can lead to accidental switching of neighbouring memristors, degrading data integrity. Both phenomena become more pronounced in larger arrays and under high-density configurations.

[Figure 5 illustrating the effects of crosstalk and sneak paths] demonstrate how these issues disrupt normal current flow and cause voltage drops across unselected cells.

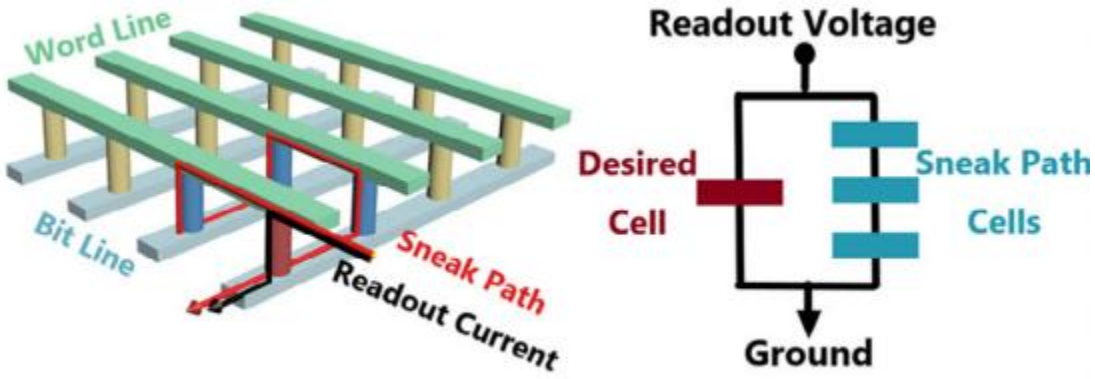

Figure 5: Crossbar architecture and the potential issues on sneak-path current [4]

2.3 Sneak Path Minimization Techniques

Sneak paths significantly limit the performance of memristor-based crossbar arrays. the challenges posed by sneak paths and proposed various minimization strategies. These strategies can be broadly categorized into **read strategies** and **cell gating techniques**, with the latter including methods like **diode gating**, **transistor gating**, and **selector device gating** [4]. Each method offers distinct trade-offs in terms of complexity, area, and performance:

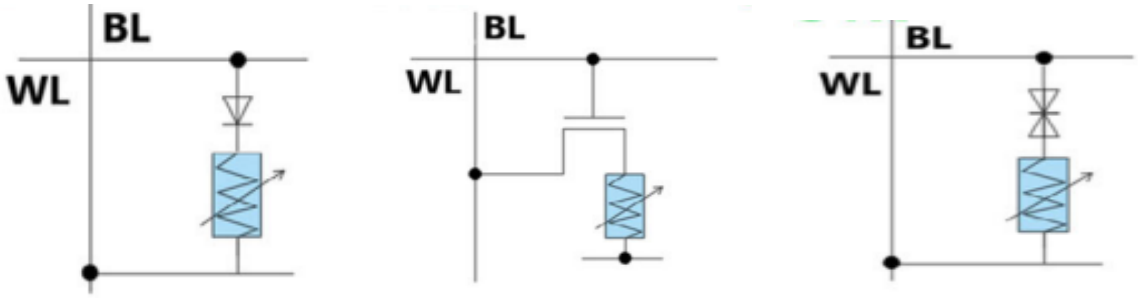

Figure 6:Sneak Path Minimization Techniques, a) diode gating, b) transistor gating, and c) selector device gating. [4]

- **Diode Gating**

This approach is straightforward to implement and introduces minimal fabrication overhead. However, it increases the overall cell footprint and may cause unwanted voltage drops across the diode, potentially affecting the readout accuracy.

- **Transistor Gating (1T1R Architecture)**

The use of a single transistor per resistive switching element enhances selectivity and allows better control over individual cells. Despite its effectiveness, this method significantly increases area consumption and complicates the fabrication process, especially for large-scale integration.

- **Selector Layer Gating (Most Prominent)**

Selector layers are widely adopted due to their advantages in power efficiency, scalability, and suitability for three-dimensional stacking. These layers enable highly dense crossbar architectures

while effectively minimizing leakage and sneak path issues without adding excessive complexity or area.

Selector devices play a pivotal role in memristor-based crossbar arrays, offering significant benefits for device performance and integration. An ideal selector exhibits high non-linearity in its current–voltage (I–V) characteristics, resulting in a high ON/OFF current ratio that enhances read accuracy. Such devices enable compact memory cell designs without increasing the cell footprint, making them suitable for high-density memory applications. Selectors are engineered to switch ON only when the applied voltage exceeds a specific threshold and to automatically revert to the OFF state when the voltage is removed, thereby minimizing standby power consumption. Furthermore, they allow high current flow in the ON state while maintaining extremely low leakage in the OFF state, which is essential for suppressing sneak path currents in crossbar architectures.

To meet these demanding performance requirements, several types of selector devices have been developed. These include tunnel barrier type selectors, field-assisted super-linear threshold (FAST) devices, Threshold switches (TS), diffusive memristors, insulator-metal transition (IMT) selectors, and mixed ionic-electronic conductors (MIECs) [5]. Each type offers distinct advantages depending on the specific application and fabrication compatibility, contributing to the advancement of scalable and energy-efficient memory systems.

- **Threshold-Switch Selector Layer**

A threshold-switch selector layer is a nonlinear device integrated in series with a memristor to suppress sneak path currents in crossbar arrays. It remains in a high-resistance state (HRS) under low voltages and switches to a low-resistance state (LRS) only when the applied voltage exceeds a certain threshold (V_{th}), enabling current flow.

This switching behaviour is typically volatile meaning the device returns to HRS once the voltage is removed. The mechanism relies on field-induced phenomena such as filament formation, charge trapping, or metal ion migration. This selective conduction helps isolate the active cell during reading or writing, thereby improving ON/OFF ratio, read margin, and array scalability.

2.4 LAOSS

The **Large-Area Organic Semiconductor Simulation (LAOSS)** platform is an advanced simulation tool designed for the modeling and optimization of large-area organic and perovskite devices, including solar cells, light-emitting diodes (LEDs), and memristor-based circuits.

LAOSS provides a robust environment for **Finite-Element Analysis (FEA)**, enabling the simulation of complex organic and perovskite semiconductor devices. Features such as **3D ray tracing**, **electro-thermal modelling**, and **visualization of results** make it highly suitable for analysing the interaction of physical and electrical phenomena in advanced devices. Integration with **Setfos** enhances its capability to analyse electrical properties comprehensively, which is critical for optimizing device performance.

LAOSS's ability to simulate electrical crosstalk and sneak paths in memristor-based arrays is particularly valuable. Studies show its effectiveness in predicting current flow, voltage drops, and thermal effects in densely packed crossbars.

To simulate the crossbar structure, electrothermal modelling is used. From a modelling perspective, the device is approximated as a 2D + 1D system. The electrodes are treated as 2D domains, while the coupling between them is represented by a 1D analytical or tabulated law. In this study, electrical coupling features are employed.

The overall system model is derived using the charge conservation continuity equation and Ohm's law, which describes the lateral current densities across the surfaces of the electrodes. This results in the following set of equations [5]:

$$\frac{1}{R^{te}_{\blacksquare,el}}\Delta\psi^{te} = j(\psi^{te},\psi^{be}), \tag{1}$$

$$\frac{1}{R^{be}_{\blacksquare,el}}\Delta\psi^{be} = -j(\psi^{te},\psi^{be}), \tag{2}$$

where the sheet resistance $\frac{1}{R^{te,be}_{\blacksquare,el}} = \frac{1}{\sigma^{te,be}\, d^{te,be}}$, σ being the conductivity [S/m], te and be make reference to the top and bottom electrode respectively, $d^{te,be}$ is the thickness of the top/bottom electrode, $\psi^{te,be} = \psi^{te,be}(x)$ is the electric potential in the top/bottom electrode and j represents the vertical 1D current density law. The left-hand part of Eq. (1) and (2) represents Ohm's law in the electrodes, and the right-hand side represents the transport in the semiconductor layers, which will be referenced as the coupling law, input law or local IV curve hereafter.

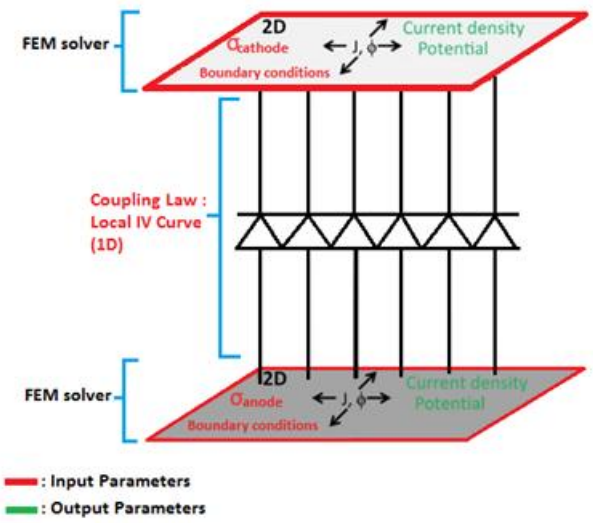

Figure 7: Sketch of the coupled electrodes implementation with boundary conditions [5]

For Coupling Different analytical models for the 1D IV curve are available in LAOSS. Ohm's law is given by: $j(\psi^{te}, \psi^{be}) = \frac{\sigma_s}{d_s}(\psi^{te} - \psi^{be})$ where the subindex s refers to the semiconductor layers.

The method used to solve these equations is the linear Galerkin finite element method (FEM). The FEM breaks a domain into smaller sub-domains or so-called elements and creates a finite set of equations for these new sub-domains. These new sets of equations are approximate locally to the originally more complex equation, and they are later recombined into a global system of equations for the final calculations. These sub-domains are created by creating a mesh for the object concerned.

To implement a crossbar electrode structure in LAOSS, a series of methodical steps must be followed to ensure simulation feasibility. One critical requirement is that the top and bottom electrode geometries must be identical. This is because LAOSS relies on coupling laws that are only valid in well-defined, overlapping domains. Therefore, the shared geometry must be defined as the intersection of the individual top and bottom electrode patterns.

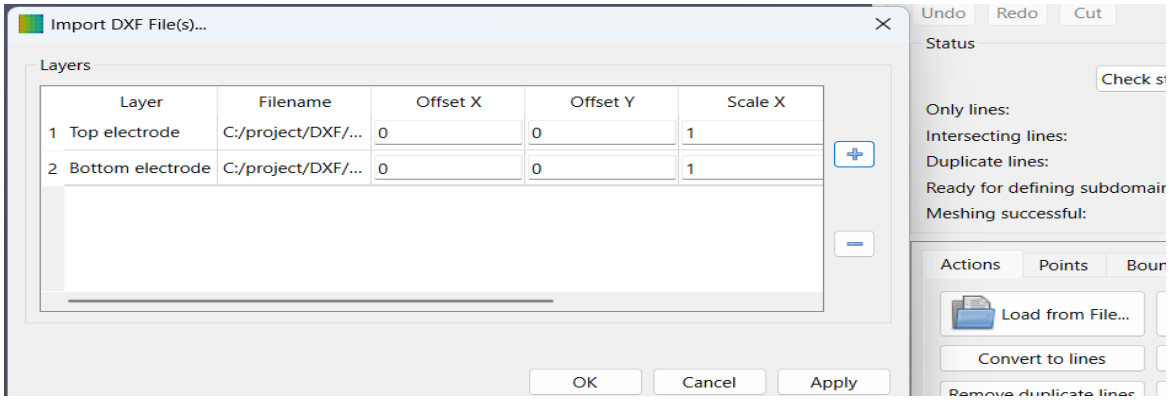

Figure 8: Top and Bottom electrode import menu in LAOSS

The intersection can be constructed using the **Geometry Import** feature available in the LAOSS main menu. Separate geometries for the top and bottom layers can be individually imported and then combined to form the complete set of required domains, as illustrated in Figure 8.

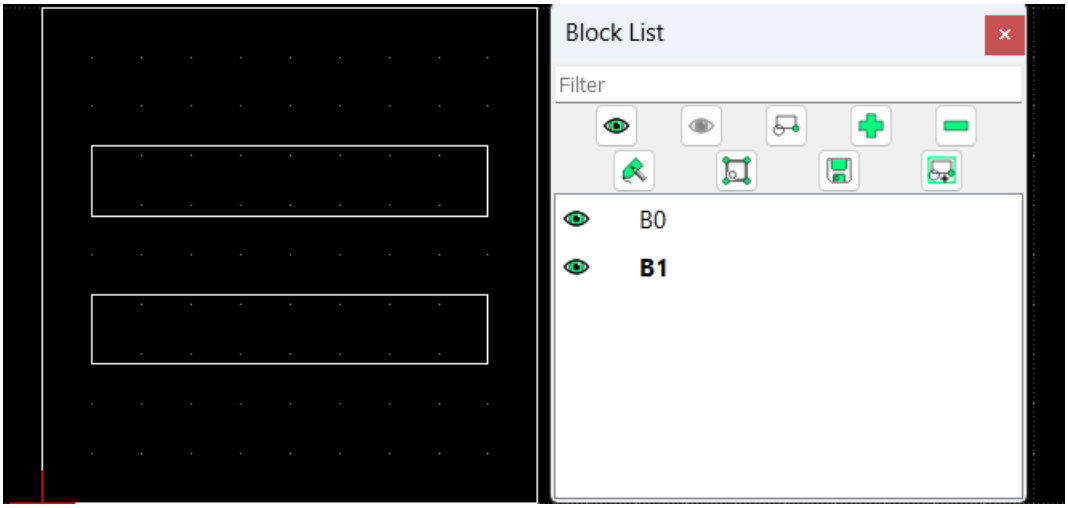

*Figure 9: Bottom electrode for 2*2 in LibraCAD*

The electrode file must be in **DXF format**. To create this DXF file and design the top and bottom electrodes, a CAD software such as **LibreCAD** is required, as shown in Figure 9.

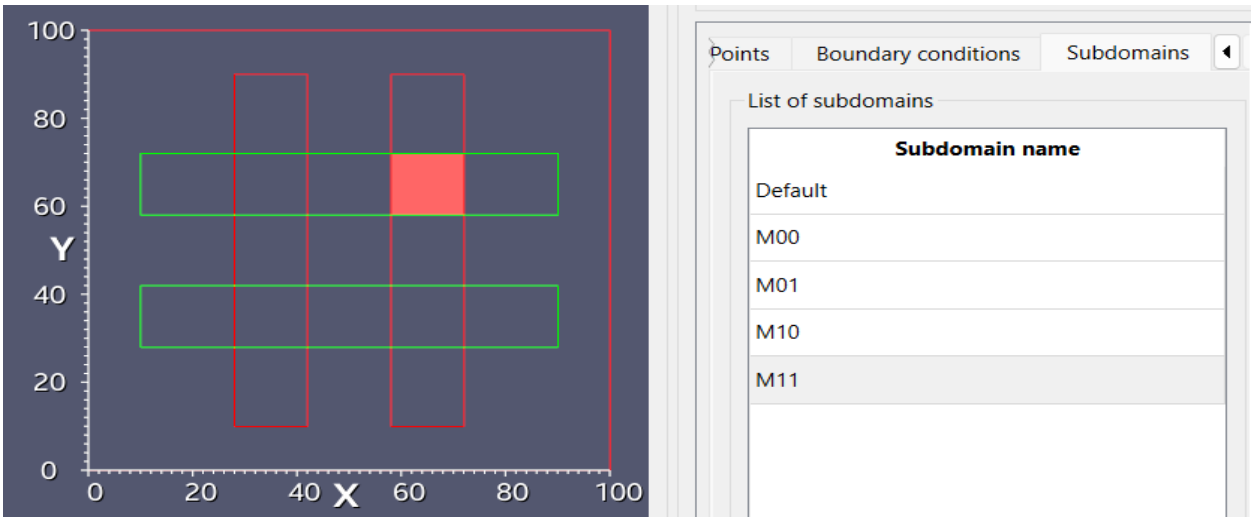

Figure 10: Define subdomain in LAOSS

Only the square regions corresponding to the intersections of the top and bottom electrodes—representing the actual memristor cross-points—will have current-conducting coupling laws applied. It is necessary to define a **subdomain** specifically for the memristor region, as illustrated in Figure 10. All other non-overlapping regions will remain **electrically uncoupled** during the simulation.

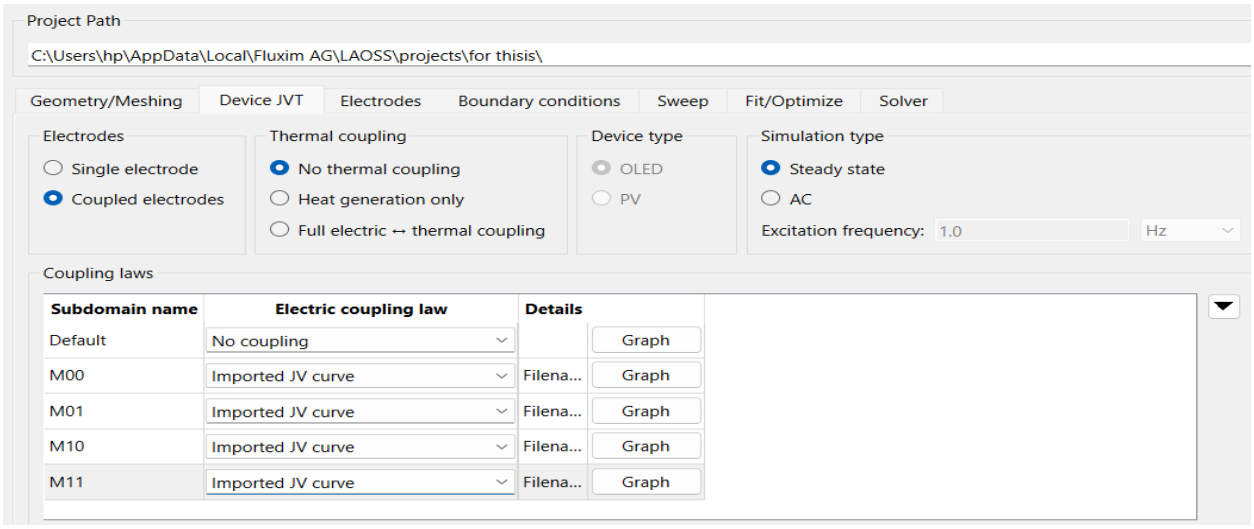

Figure 11: Device JVT Menu in LAOSS

After successfully importing the geometry, it is important to check for any errors and ensure that the geometry is correctly applied to the current project. Once confirmed, the **unit settings and meshing parameters** must be defined.

In the **Device JVT** menu, the following configurations should be applied: **Coupled Electrode**, **No Thermal Coupling**, **Steady-State Simulation Type**, and **Load JV Curve to Each Memristor**, as shown in Figure 11.

Next, in the **Electrode** section, the **sheet resistance** must be specified, and in the **Boundary** section, the appropriate **voltage must be assigned to the electrodes**. Once all these parameters are set, the simulation is ready to run.

LAOSS also provides additional features that can be explored for more detailed analysis, such as **AC Simulation Type**, **Sweep settings**, and other advanced options.

3 Motivation and Problem Formulation

3.1 Motivation

The demand for high-density, low-power memory devices is driving research into emerging technologies that can replace conventional silicon-based memory. Memristors have garnered significant attention due to their non-volatility, scalability, and compatibility with CMOS technology. Their ability to switch between high and low resistance states makes them ideal for applications such as memory storage, neuromorphic computing, and logic circuits.

Crossbar architectures utilizing memristors offer a promising solution for achieving ultra-dense memory arrays. However, as the density of these arrays increases, challenges such as **sneak path currents** arise, adversely affecting the performance and reliability of the devices. Addressing these issues is critical to unlocking the full potential of memristor-based crossbars for real-world applications.

Simulating and analysing these challenges using advanced tools like **LAOSS (Large-Area Organic Semiconductor Simulation)** allows for a deeper understanding of device behaviour and the development of effective mitigation strategies. This motivates the investigation of crosstalk phenomena and its impact on crossbar performance using state-of-the-art simulation techniques.

3.2 Problem Formulation

The primary goal of this study is to investigate and mitigate **sneak path currents** in memristor-based crossbar architectures using the LAOSS simulation platform. The research focuses on:

1. **Understanding Sneak Path Mechanisms:**
    - As the size of the crossbar array scales up, the number of alternative paths for current to flow through unselected memristors also increases, leading to significant leakage and loss of data integrity.
    - Sneak paths cause false current readings during memory operations, which reduces the read margin and can result in incorrect data retrieval or unintentional switching of adjacent cells.
2. **Modelling and Simulation Challenges:**
    - Developing a realistic simulation framework to replicate the behaviour of crossbar arrays, including the effects of crosstalk.
    - Addressing challenges in electrode design, such as achieving accurate current flow through both top and bottom electrodes.
3. **Mitigating Sneak Paths:**
    - Exploring potential solutions, such as optimized electrode configurations, novel read/write schemes.
    - Evaluating the effectiveness of these approaches in improving read margins and overall array reliability.
    - Integrating selector layers with memristors helps to suppress unwanted current paths by allowing current flow only when a specific threshold is reached, effectively isolating the selected cell.
4. **Scalability and Practical Implementation:**
    - Analysing how the proposed solutions scale with larger crossbar arrays.
    - Providing insights into the trade-offs between performance, power consumption, on off ratio, Read Margin and device density.

4 Chalcogenide (Ge_2Se_3) Memristors Crossbar

Chalcogenide memristor crossbars are commercially available, making them a convenient starting point for implementation. The multilayer schematic of a memristor with tungsten (W) electrodes is shown in Figure 12 [6]. Chalcogenide memristors operate based on **electrochemical metallization**, where a voltage causes metal ions (e.g., Ag^+) to migrate through a chalcogenide layer and form a conductive filament, switching the device to a low-resistance state. Reversing the voltage dissolves the filament, returning it to a high-resistance state. This process enables reversible, non-volatile resistive switching suitable for memory applications.

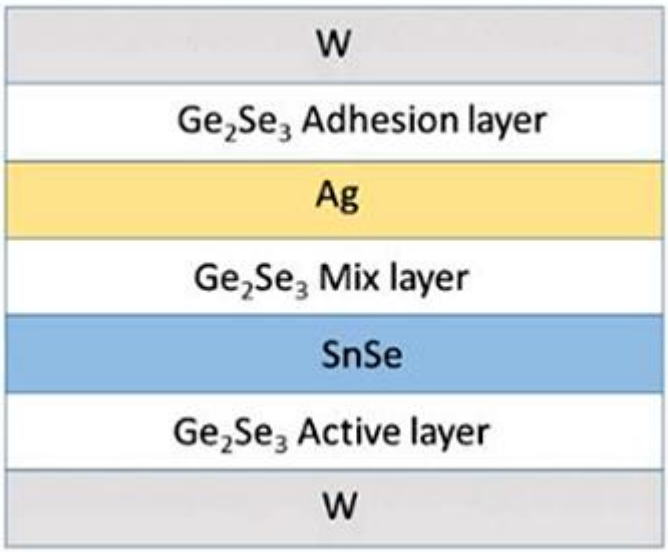

Figure 12:Schematic diagram of a chalcogenide memristor [6]

To characterize the I-V behavior of a single commercial memristor from a 16-pin IC, all other memristors were kept in the OFF state to create a best-case condition. The I-V characteristics of the chalcogenide-based single memristor, as shown in Figure 13, were measured by applying a stepwise voltage increment of 0.01 V with a delay of 0.001 seconds using a Keithley 2450 SourceMeter. From the figure, it is clearly observed that the most **suitable read voltage is approximately 0.1 V,** and crossbar analysis was carried out using the One-Bit Line Pull-Up technique.

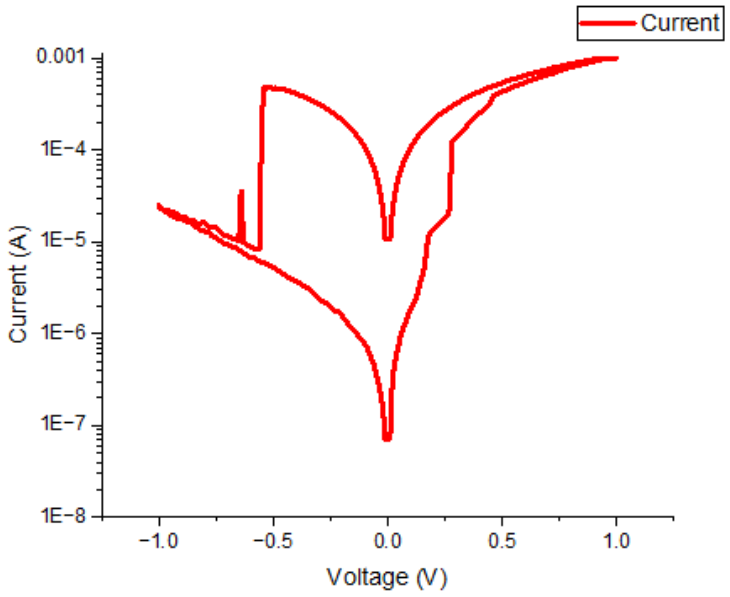

Figure 13: Pacticaly measured IV of chalcogenide memristors using Keithley 2450.

This experimentally obtained I-V curve was then used for further simulation studies in LAOSS, with some simulation results compared against experimental measurements to validate the accuracy of the simulations.

4.1 Single Memristor Design

A single memristor of size **14 um × 14 um** has been designed in LAOSS, as shown in Figure 14. The current-voltage (I-V) characteristics were analysed to differentiate between the **ON state** and **OFF state**, with the corresponding J-V curves displayed in Figure 4(a) and Figure 4(b). This analysis was conducted to verify the memristor's switching behaviour under varying conditions.

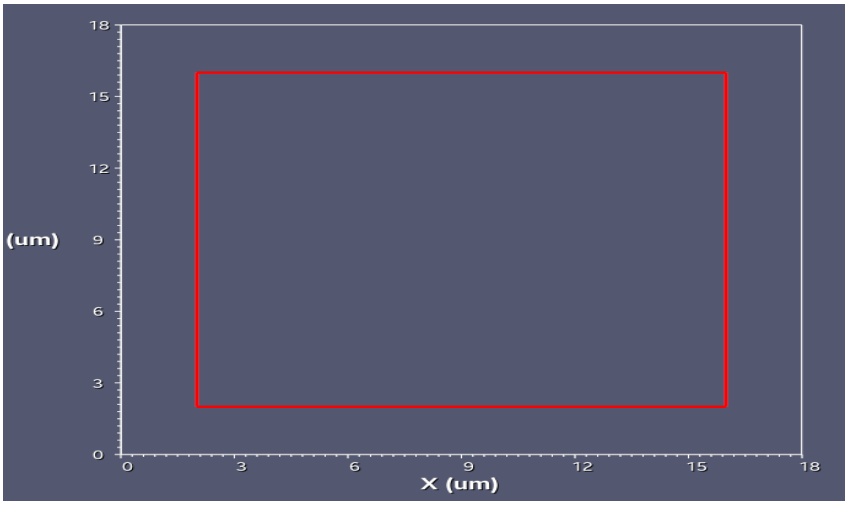

Figure 14: Single Memristor Design (14 um × 14 um)

The practical and simulated I-V characteristics of a single chalcogenide-based commercial memristor (Ge_2Se_3) were evaluated to validate the simulation setup. The results are summarized in Table 1.

Measurement Type	**I(on) (A)**	**I(off) (A)**
Practical	$\sim 1 \times 10^{-4}$	$\sim 1 \times 10^{-7}$
Simulated	2.3×10^{-4}	3.19×10^{-7}

Table 1: Practical and simulated result of Single memristor

4.2 2×2 Crossbar Array

A 2×2 memristor crossbar has been developed, as illustrated in Figure 15. This crossbar includes Two Top Electrodes (Electrode 0 and Electrode 1), Four Memristor and Two Bottom Electrode These electrodes are separated by an insulating layer, ensuring proper isolation.

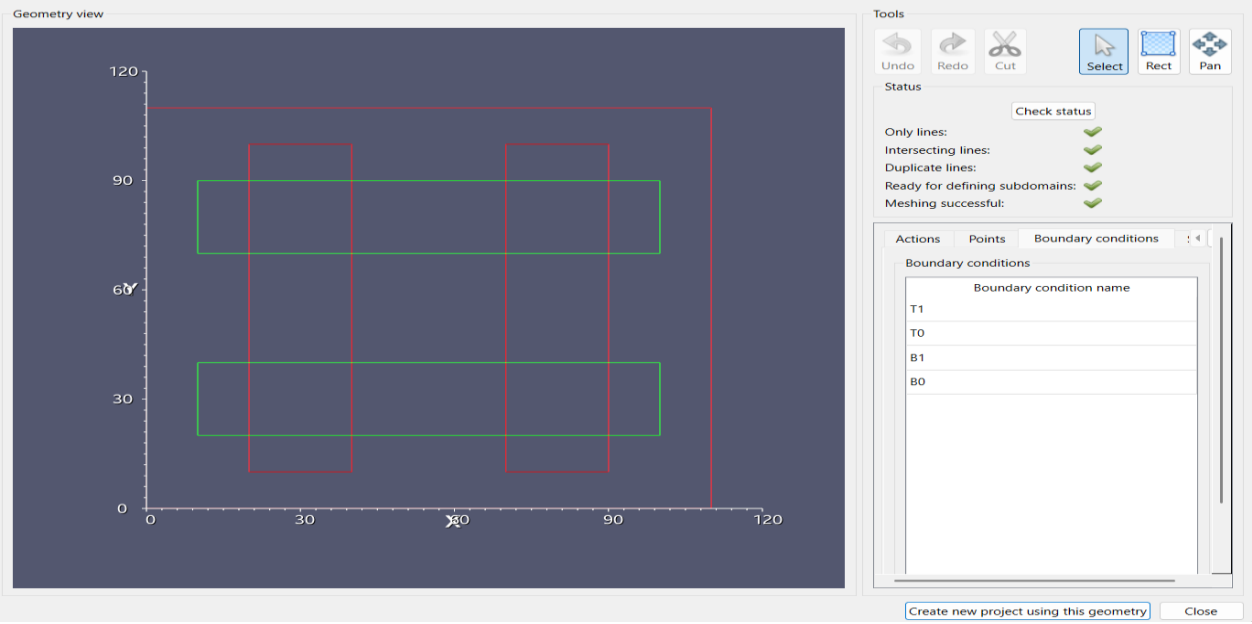

Figure 15: 2×2 Crossbar Design

To evaluate the behavior of a commercial chalcogenide memristor in a 2×2 crossbar array, simulations were conducted under both best-case and worst-case read conditions using LAOSS. The best-case scenario assumes only the target memristor (M_{00}) is in the ON state, while the worst-case scenario assumes all memristors are ON, resulting in the presence of sneak path currents. The

following Table 2 summarizes the key electrical parameters extracted from the simulations, including ON and OFF currents, ON/OFF ratios, and sneak path contributions.

Parameter	Best Case	Worst Case
Configuration	M00 ON; Others OFF	All Memristors ON
Read Voltage (V(read))	0.1 V	0.1 V
I(ON)	2.30×10^{-4} A	3.05×10^{-4} A
I(OFF)	4.19×10^{-7} A	7.75×10^{-5} A
ON/OFF Ratio	549	3.08
Sneak Path Current (I(sneak))	10^{-7}A	7.5×10^{-5} A
Cell Area (F^2)	14 µm × 14 µm	14 µm × 14 µm
Comment	One memristor ON, no sneak paths	One sneak path of 3 series resistors

Table 2: Electrical Performance of 2×2 Chalcogenide Memristor Crossbar Array Under Best and Worst Read Conditions

4.3 3×3 Crossbar Array

A 3×3 memristor crossbar has been developed, as illustrated in Figure 16: 3×3 Crossbar Design. This crossbar includes Three Top Electrodes (Electrode 0, Electrode 1 and Electrode 2), Nine Memristor and Three Bottom Electrode These electrodes are separated by an insulating layer, ensuring proper isolation.

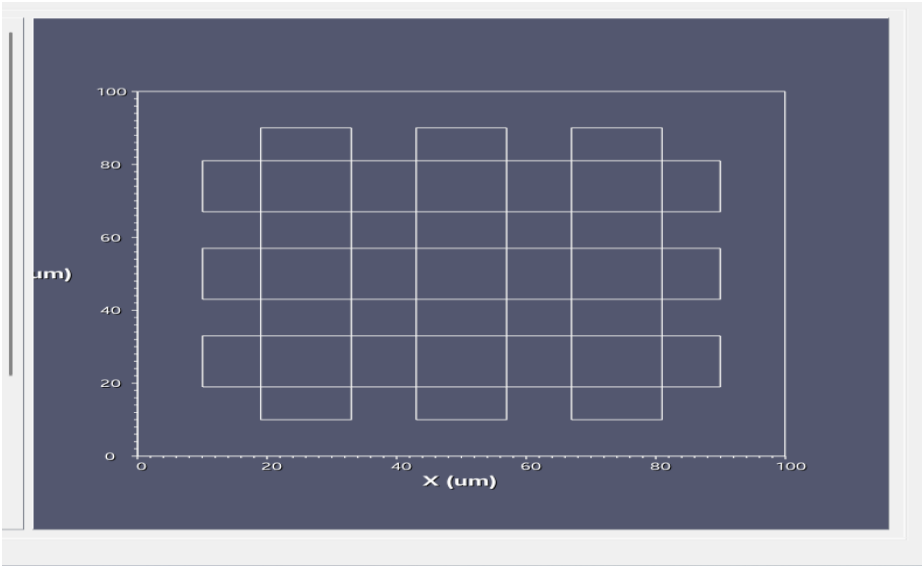

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Figure 16: 3×3 Crossbar Design

Table 3 presents the simulated electrical behaviour of a 3×3 commercial chalcogenide memristor crossbar array using LAOSS. The analysis highlights the performance under ideal and worst-case

scenarios. In the best-case read condition, all memristors except the target (M00) are in the OFF state, yielding a high on-off current ratio. In the worst-case scenario, with all memristors ON, a significant sneak path current dominates the OFF-state current, resulting in a degraded on-off ratio and invalid read conditions due to sneak path interference.

Parameter	**Best Case**	**Worst Case**
Condition	M00 ON; Others OFF	M00 ON; All ON
I(on) (A)	2.30×10^{-4}A	4.1×10^{-4}A
I(off) (A)	4.29×10^{-7}A	1.8×10^{-4}A
On-Off Ratio	536.1	2.28
I(sneak) (A)	1.1×10^{-7}A	1.8×10^{-4} A
Comment	Valid read condition	Sneak current dominates

Table 3 :3×3 Crossbar Array Read Performance

4.4 4×4 Crossbar Array

A 4×4 memristor crossbar has been developed, as illustrated in Figure 17. This crossbar includes Four Top Electrodes), Sixteen Memristor and Four Bottom Electrode These electrodes are separated by an insulating layer, ensuring proper isolation.

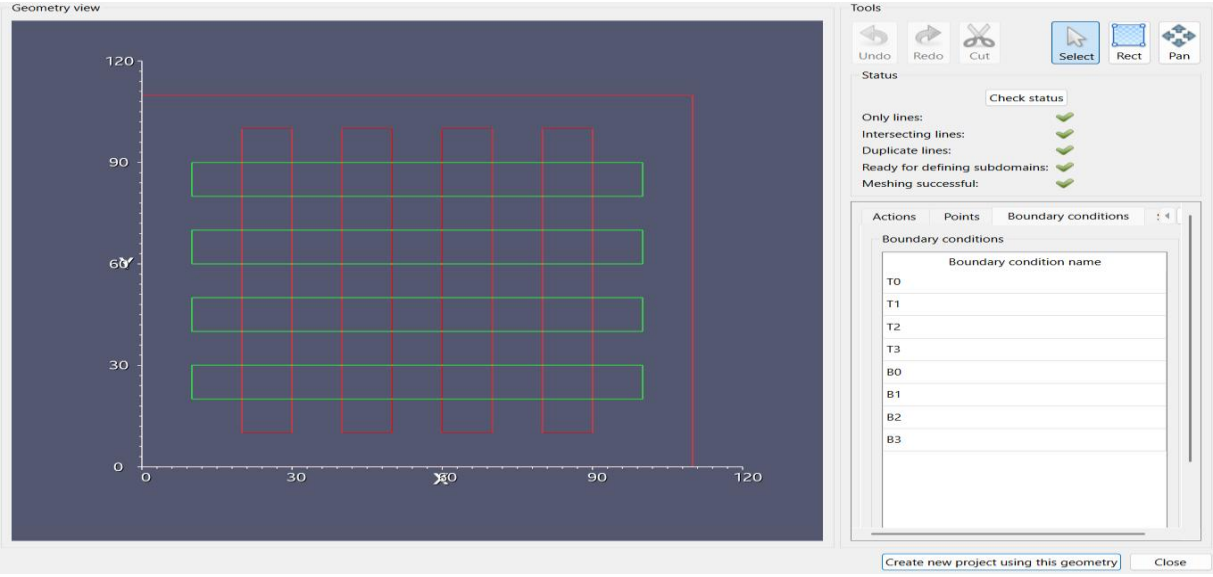

Figure 17: 4×4 Crossbar Design

Table 4 presents the electrical behaviour of a 4×4 crossbar array under best and worst-case conditions. As the array size increases, the sneak path effect becomes more significant. In the worst-case condition, the sneak current surpasses the desired-ON current, leading to unreliable read operations and invalid ON/OFF differentiation.

Parameter	Best Case (M00 ON; Others OFF)	Worst Case (M00 ON; All ON)
I(on) (A)	2.30×10^{-4}A	5.326×10^{-4}A
I(off) (A)	6.07×10^{-7}A	2.929×10^{-4}A
On-Off Ratio	378.9	1.82 *(Not Valid)*
I(sneak) (A)	2.88×10^{-7}A	2.929×10^{-4} A *(> I(on))*
Comment	Stable Read Operation	Sneak Current Dominates

Table 4: Read Performance of 4×4 Crossbar Array

4.5 Conclusion for Chalcogenide Crossbar

From the simulation results, the relationship between sneak path current and crossbar size is illustrated in Figure 18. The number of sneak paths increases exponentially with the size of the array (N×N), particularly in densely packed configurations. These sneak paths are influenced by factors such as input biasing, array dimensions, and the resistive states of individual memristors [8].

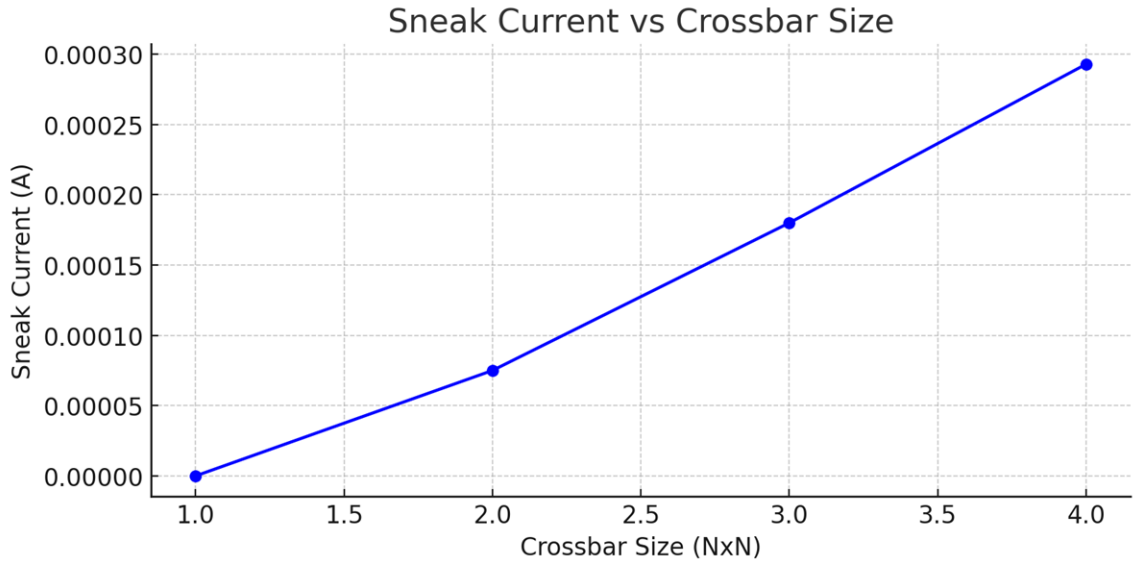

Figure 18: Sneak Current vs Crossbar Size for Chalcogenide Memristor

Experimental observations with commercial chalcogenide memristors revealed that, in some cases, the sneak path current can exceed the ON-state current. This leads to unreliable read operations, significantly degrading the performance of the memory array. Consequently, chalcogenide-based crossbar architectures are unsuitable for high-density memory applications unless additional mitigation techniques are employed.

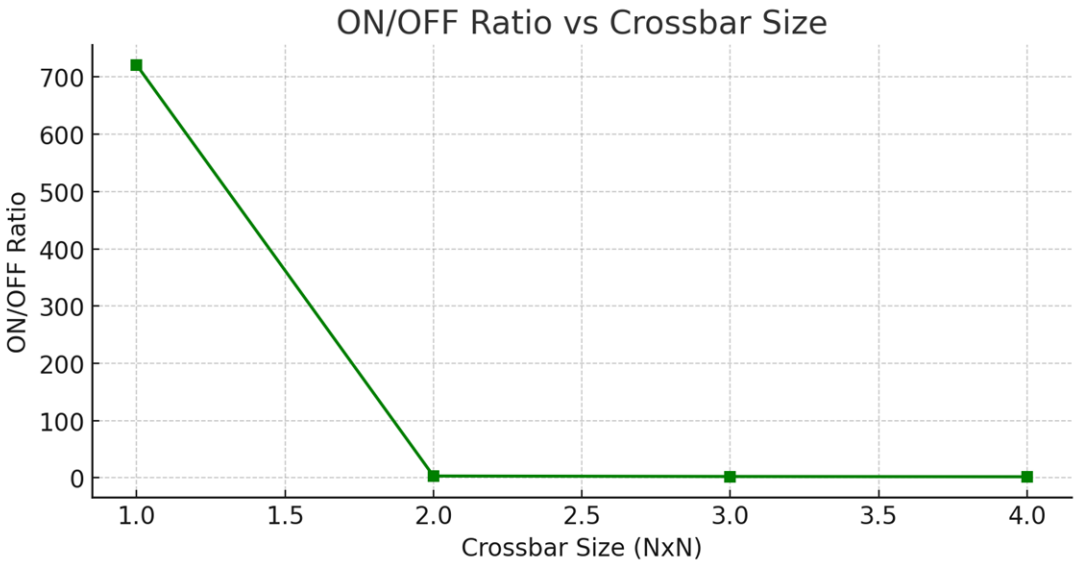

Figure 19: ON/OFF Ratio vs Crossbar Size for Chalcogenide Memristor

Figure 19 demonstrates how the ON/OFF ratio decreases with increasing crossbar array size, while Figure 20 illustrates the corresponding decline in read margin. These trends highlight the critical challenges in scaling chalcogenide memristor crossbars for practical memory systems.

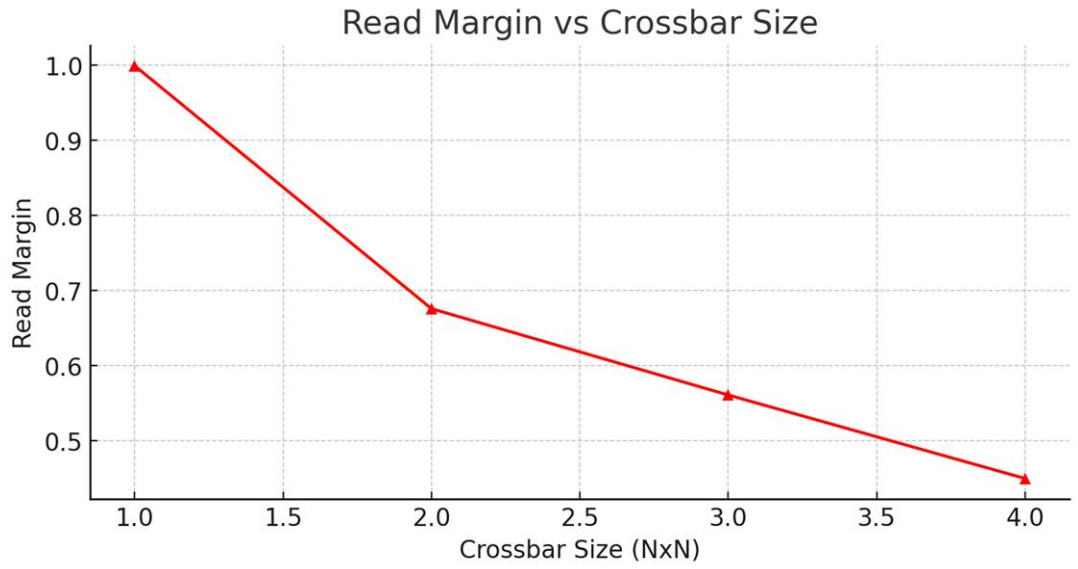

Figure 20: Read Margin Vs Crossbar Size for Chalcogenide Memristor

5 Graphene–SiO_2 Memristor Crossbar

Graphene–SiO_2 memristors offer excellent thermal and chemical stability due to the robust nature of SiO_2 and the high conductivity of graphene. Their compatibility with CMOS processes and potential for reliable switching make them promising candidates for scalable and durable memory applications.

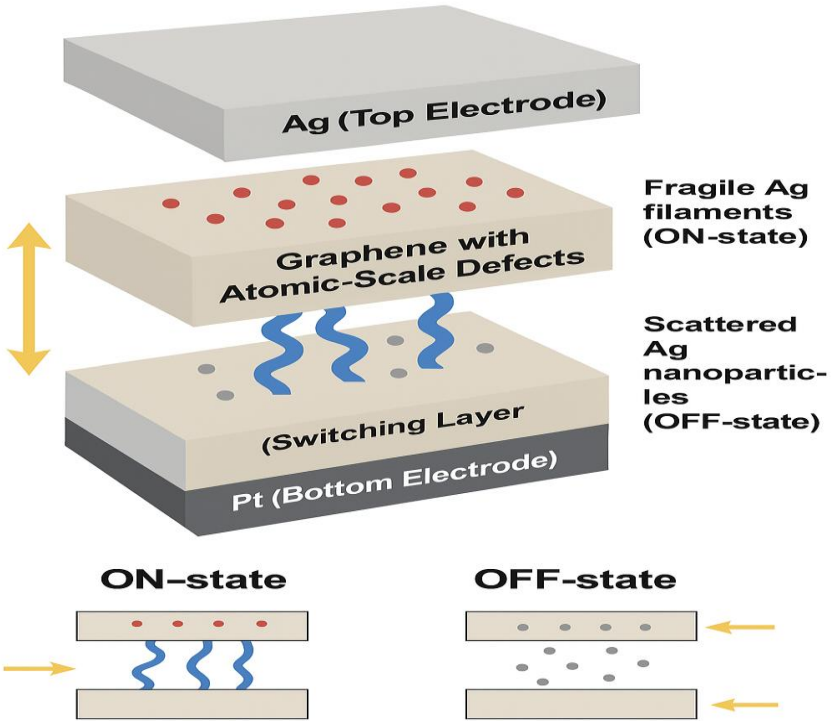

Figure 21: Structure of 1-Selector 1-Resister Scheme Graphene-SiO_2 Memristor

The DDG (Densely Defected Graphene) memristor devices are based on a 1S1R (one-selector, one-resistor) architecture utilizing a Ag/DDG/SiO_2/Pt stack [7]. These devices have been fabricated with a cell area of $4 \times 4\ \mu m^2$ as shown in Figure 21. The structure includes a graphene-based selector integrated with a resistive switching element, enabling efficient suppression of sneak paths through threshold switching behavior. The devices exhibit excellent selectivity, reaching values as high as 5×10^8, which is critical for reliable operation in high-density crossbar arrays [7]. Furthermore, DDG devices demonstrate impressive endurance performance, withstanding over 10^6 switching cycles [9]. These devices utilize threshold switching mechanisms facilitated by defect-engineered graphene layers Improve the I-V as shown in Figure 22, where the defect density—controlled through Si^+ ion irradiation (fluence of $10^{13}\ cm^{-2}$)—directly influences switching behavior and device reliability [7].

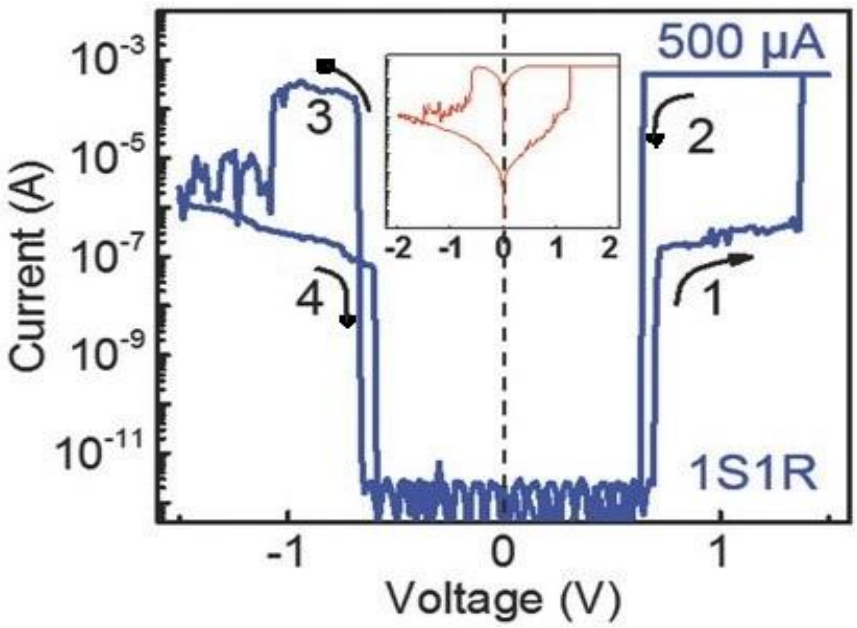

Figure 22: I-V of Graphene–SiO_2 Memristor (Ag/DDG/SiO2/Pt) [7]

When the applied voltage exceeds the threshold (approximately 0.5–1 V), Ag^+ ions migrate through defects in the graphene layer, forming nanoscale conductive filaments within the SiO_2 layer and creating a low-resistance path for high ON-current. Upon voltage removal or drop below the threshold, these filaments rupture due to the Gibbs-Thomson effect, reverting the device to a high-resistance state as the graphene defects inhibit further ion diffusion.

5.1 Crossbar Array

For the Graphene–SiO_2 memristor, simulations were performed using a read voltage of 1 V, and crossbar analysis was carried out using the One-Bit Line Pull-Up technique. Table 5 summarizes the simulation results for various crossbar sizes implemented in LAOSS. The data includes the calculated ON/OFF ratios and corresponding sneak path current levels for 2 × 2, 3 ×3 and 4 × 4 Crossbar array. Based on this analysis, the Graphene–SiO_2 memristor demonstrates improved suppression of sneak currents and maintains a high ON/OFF ratio even as array size increases, highlighting its potential suitability for high-density volatile memory applications.

Configuration	Condition	I(on) (A)	I(off) (A)	I(sneak) (A)	ON/OFF Ratio
Single Memristor	Simulated	4.802×10^{-4}	3.2×10^{-7}	–	1500.6
2×2 Crossbar	Worst (All ON)	4.802×10^{-4}	3.442×10^{-7}	2.42×10^{-8}	1395.4
3×3 Crossbar	Worst (All ON)	4.802×10^{-4}	$3.7. \times 10^{-7}$	5×10^{-8}	1298.4
4×4 Crossbar	Worst (All ON)	4.802×10^{-4}	3.96×10^{-7}	7.6×10^{-8}	1212.6

Table 5: Simulation Result for Graphene-SiO_2 Memristor Crossbar Arrays

5.2 Conclusion For Graphene-SiO_2 Crossbar

Due to DDG Selector layer threshold switching property significant reduction in sneak path current as shown in Figure 23.

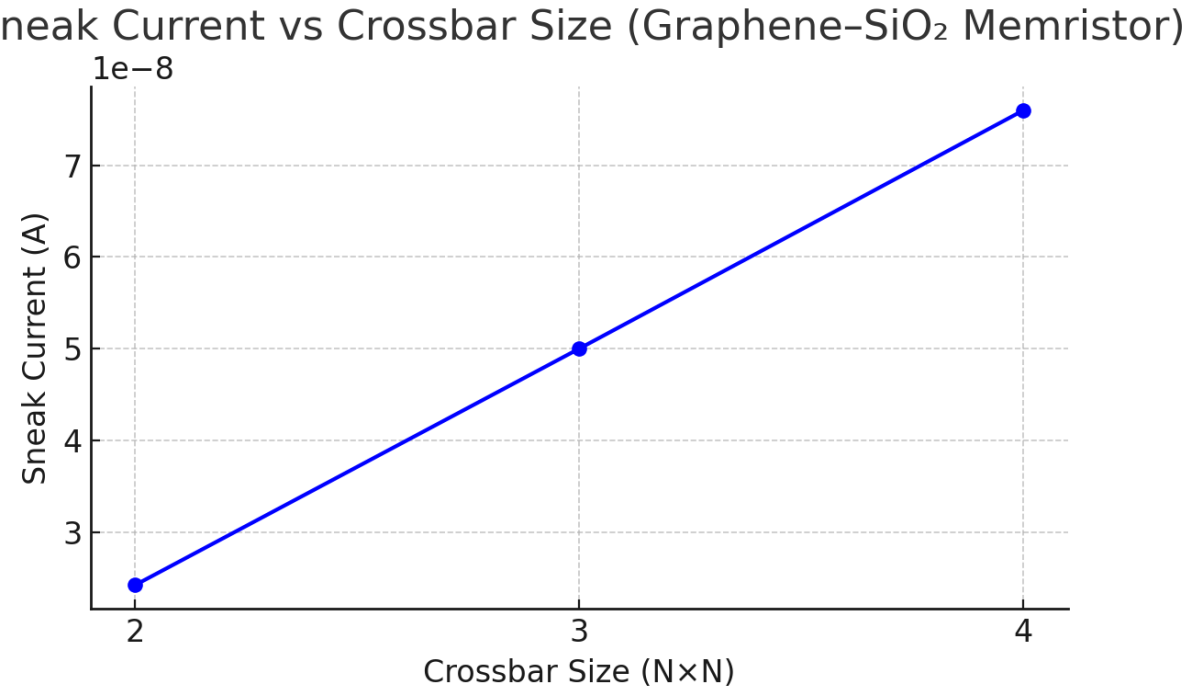

Figure 23: Crossbar Array Size vs Sneak Current for Graphene–SiO_2 Memristor Crossbar Arrays

ON/OFF ratio slightly decreases due to increasing sneak path currents and cumulative leakage, which is typical in memristors crossbar arrays. The log scale emphasizes these subtle but significant shifts in performance as shown in Figure 24.

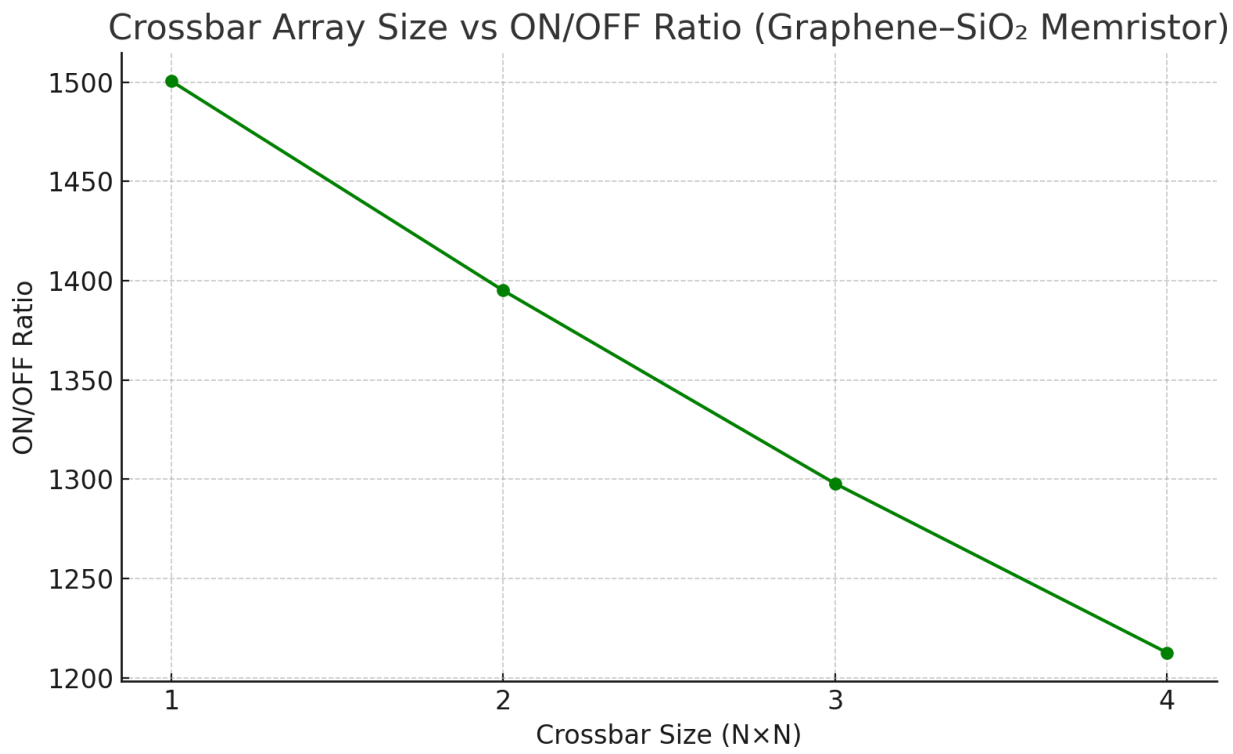

Figure 24: Crossbar Array Size vs ON/Off Ratio for Graphene–SiO_2 Memristor Crossbar Arrays

Read margin slightly decreases due to increasing sneak path currents and cumulative leakage, which is typical in memristors crossbar arrays. The log scale emphasizes these subtle but significant shifts in performance as shown in Figure 25.

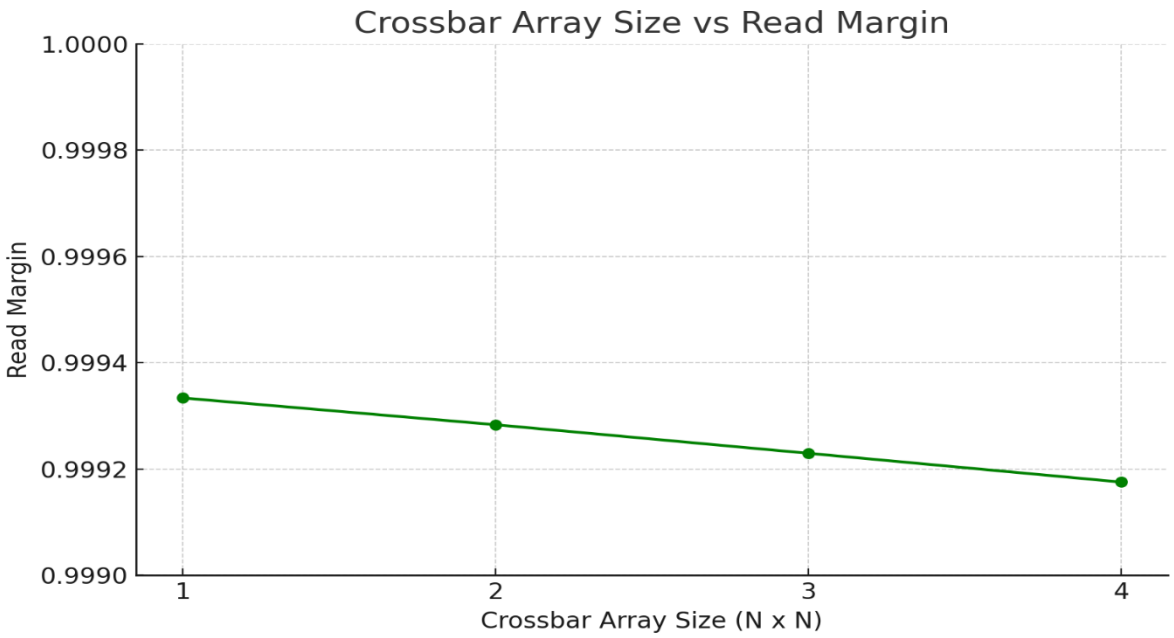

Figure 25: Crossbar Array Size vs Read Margin for Graphene–SiO_2 Memristor Crossbar Arrays

The graphene/SiO_2-based memristor demonstrates a high ON/OFF current ratio and maintains a favourable read margin across varying crossbar sizes, making it a promising candidate for high-density memory applications. Its distinct I–V characteristics, particularly the sharp switching behaviour and well-defined "dead region" between ON and OFF states, effectively suppress sneak path currents—a major challenge in crossbar architectures.

This intrinsic nonlinearity enables improved selectivity during read operations, enhancing overall memory reliability. However, practical implementation faces challenges, particularly in fabricating Densely Defect Growth (DDG) configurations within the SiO_2 layer. Achieving consistent and abrupt filament formation remains difficult, which can impact device reproducibility and yield.

Despite these fabrication complexities, the superior electrical performance of the graphene/SiO_2 memristor justifies its potential for future integration into scalable memory systems.

6 Ag-doped $CH_3NH_3PbI_3$ ($MAPbI_3$: Ag)(HPs) Memristors Crossbar

Ag-doped $MAPbI_3$ memristors offer tunable switching behavior, and a 1S–1R structure effectively suppresses sneak path currents. The proposed design enables reliable, CMOS-compatible memory integration. It also supports cost-effective and scalable fabrication using solution-processed materials.

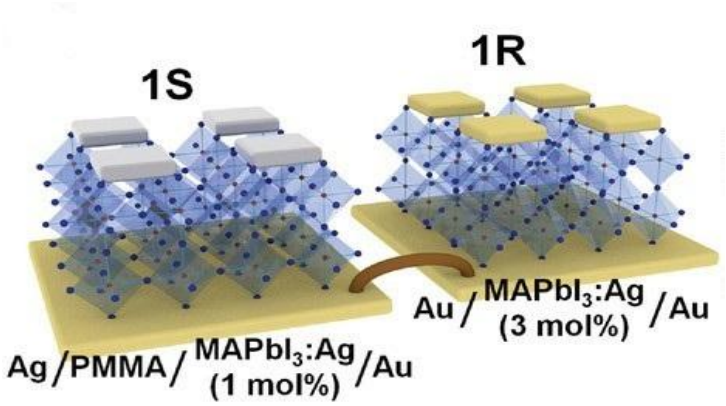

Figure 26: The schematic representation of the $MAPbI_3$: Ag-based 1S-1R structure [8]

The 1S–1R Ag-doped $MAPbI_3$ memristor consists of two vertically stacked layers: a selector (1 mol% Ag-doped $MAPbI_3$ with a PMMA interlayer) and a resistive switching layer (3 mol% Ag-doped $MAPbI_3$) as shown in Figure 26[8]. The selector exhibits nonlinear I–V behavior as shown in Figure 27, blocking sneak path currents at low voltages and allowing current at higher thresholds. The resistor operates via the formation and rupture of Ag conductive filaments, switching between high and low resistance states. This structure enables reliable, scalable memory performance with improved ON/OFF ratios and effective sneak path suppression.

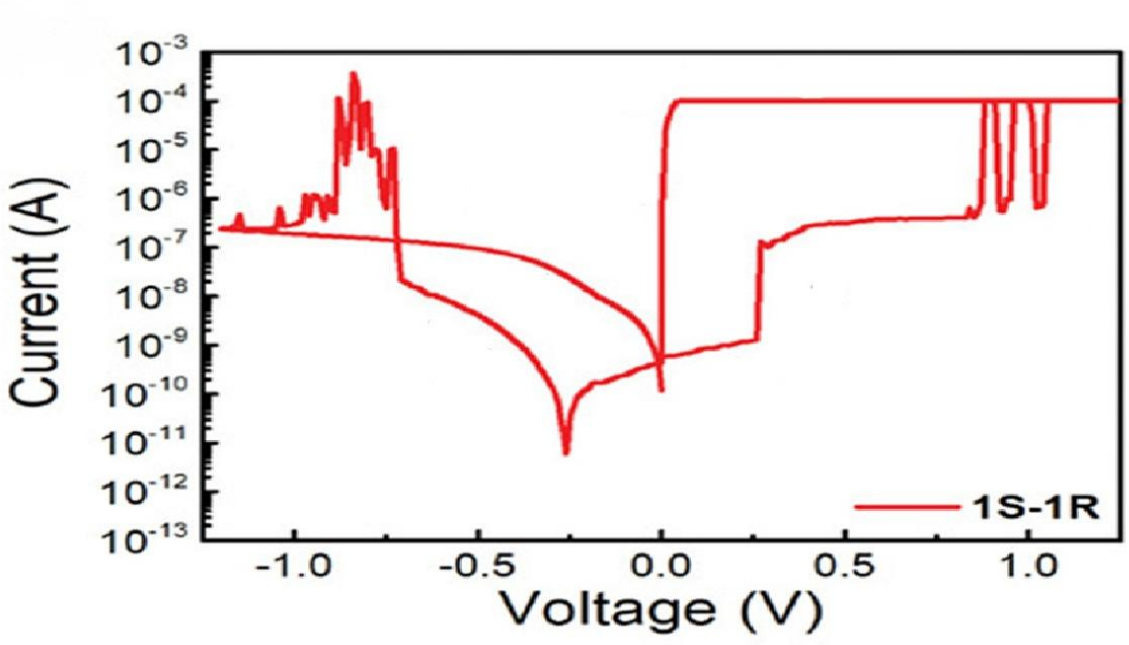

Figure 27: I-V result of the 1S-1R $MAPbI_3$: Ag Memristor device [8]

6.1 Crossbar Array

For the $MAPbI_3$: Ag memristor, simulations were performed using a read voltage of 0.2 V, and crossbar analysis was carried out using the One-Bit Line Pull-Up technique. Table 6 summarizes the simulation results for various crossbar sizes implemented in LAOSS. The data includes the calculated ON/OFF ratios and corresponding sneak path current levels for 2 × 2, 3 ×3 and 4 × 4 Crossbar array.

Configuration	I(ON) (A)	I(OFF) (A)	Sneak Current (A)	ON/OFF Ratio
Single Memristor	9.9959×10^{-5}	3×10^{-7}	N/A	333.20
2×2 Crossbar (Worst)	1.0×10^{-4}	3.5×10^{-7}	5.0×10^{-8}	285.71
3×3 Crossbar (Worst)	1.00109×10^{-4}	4.7×10^{-7}	1.508×10^{-7}	212.98
4×4 Crossbar (Worst)	1.00179×10^{-4}	5.2×10^{-7}	2.2×10^{-7}	192.65

Table 6: Simulation Result for $MAPbI_3$: Ag Memristor Crossbar Arrays

6.2 Conclusion for HPs Crossbar

The $MAPbI_3$: Ag memristor incorporates a threshold-switching selector layer, which significantly reduces sneak path currents, as illustrated in Figure 28. In the crossbar Worst Case configuration, memristors that experience a negative voltage exhibit a high-resistance state, effectively increasing the total resistance of unintended current paths.

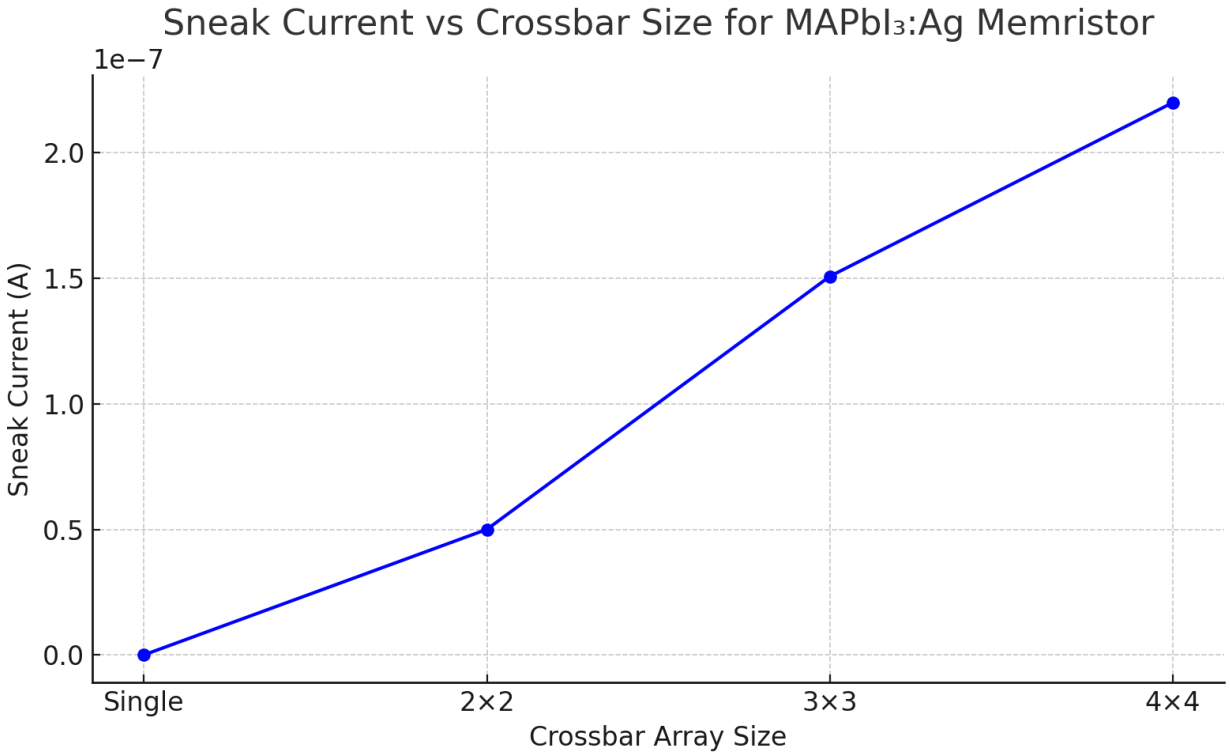

Figure 28: Crossbar Array Size vs Sneak Current for Graph $MAPbI_3$: Ag Memristor Crossbar Arrays

This threshold switching behaviour suppresses sneak currents, thereby enhancing overall device performance. As a result, there is a notable improvement in the ON/OFF current ratio (Equation 2), as depicted in Figure 29, and an increase in read margin (Equation 3), as shown in Figure 30.

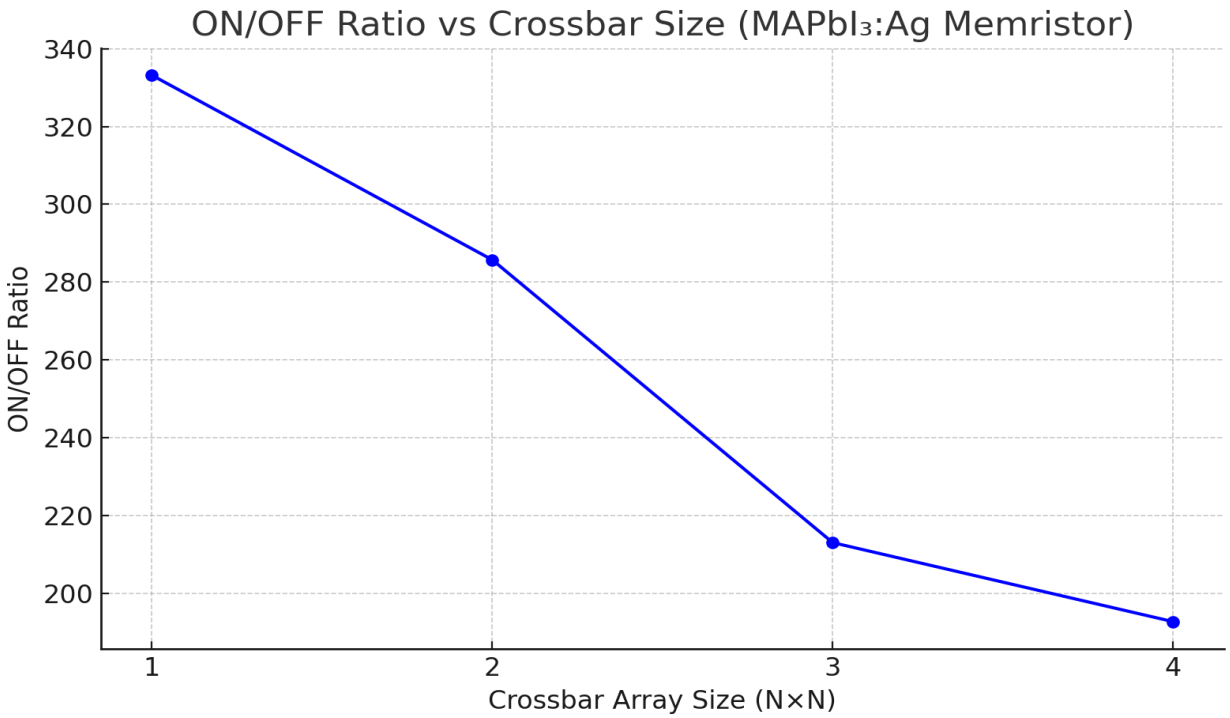

Figure 29: Crossbar Array Size vs ON/OFF for Read MAPbI3: Ag Memristor Crossbar Arrays

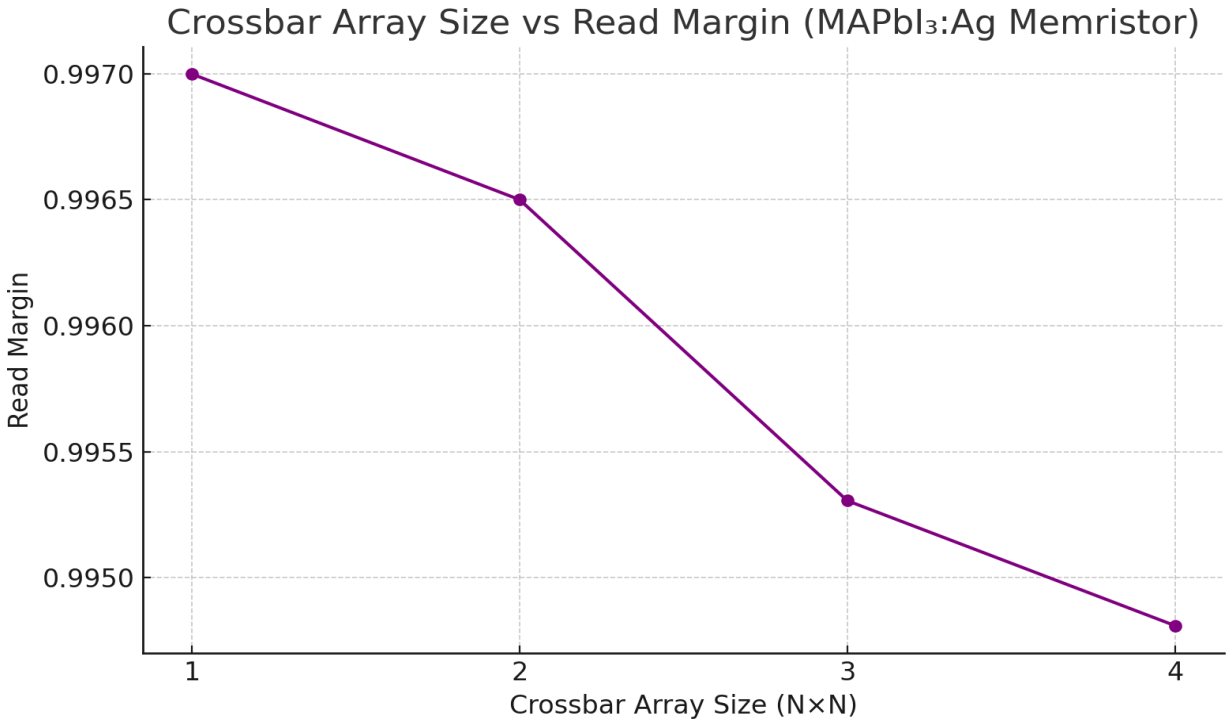

Figure 30: Crossbar Array Size vs Read margin for Graph MAPbI3: Ag Memristor Crossbar Arrays

7 Summary and Future Work

In this research, the successful simulation of memristor crossbar arrays using LAOSS demonstrated that it is a highly effective tool for analysing sneak path currents in N×N memristor architectures. LAOSS makes it considerably easier to visualize and investigate the behaviour of various memristor devices by inputting their respective J–V (current–voltage) characteristics. The initial analysis began with a commercial chalcogenide-based memristor, where the one-bit pull-up technique was employed for read operations. However, the results showed that beyond a 3×3 crossbar size, this device exhibited significantly high sneak path currents, leading to substantial crosstalk during read operations. This behaviour renders it unsuitable for high-density memory applications unless advanced sneak path mitigation strategies are implemented.

To address this, the integration of a threshold-switching selector layer in a 1S1R (one-selector one-resistor) configuration proved highly beneficial. The Graphene–SiO_2 memristor was introduced and simulated up to a 4×4 crossbar array. Due to its threshold switching behavior, this device demonstrated a notable reduction in sneak path currents and substantial improvements in ON/OFF ratio and read margin. These characteristics make the Graphene–SiO_2-based crossbar highly promising for high-density non-volatile memory applications, despite its fabrication complexity.

Subsequently, the $MAPbI_3$: Ag memristor in a 1S1R configuration was also evaluated. This device similarly showed improvements in sneak path suppression, ON/OFF ratio, and read margin. However, its threshold switching was effective only under negative bias conditions in worst-case scenarios. As a result, while $MAPbI_3$: Ag devices offer some potential, their capability to suppress sneak paths is relatively limited compared to the Graphene–SiO_2 memristor.

Overall, this study highlights the critical importance of selector-based architectures in crossbar arrays and reinforces that LAOSS is a valuable simulation platform for modelling, analysing, and optimizing memristor devices for high-density memory applications.

Future work can explore AC simulation in LAOSS to study capacitive and inductive crosstalk in large crossbar arrays (e.g., 8×8, 32×32). Selector layers with better threshold characteristics may be investigated for further sneak-path reduction. evaluating the effect of scaling on parasitic elements and modeling transient behavior under pulsed inputs. LAOSS can be used to simulate material-dependent variations in switching for improved accuracy.

8 References

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