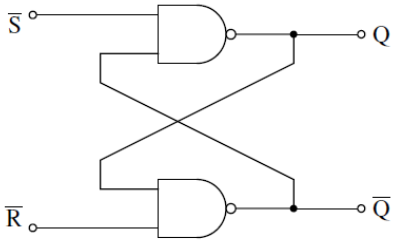
Digital Systems

Assignment – 2

Q-1 Design a combinational circuit with three inputs, x, y, z, and three outputs, A, B, C. When the binary input is 4, 5, 6, or 7, the binary output is 2 less than the binary input. When the binary input is 0, 1, 2, or 3, the output is 4 more than the binary input. **[3 M]**

Q-2 For the S-R latch, assume each NAND gate has a delay of 1 nsec. The inputs to the S-R latch are applied as follows. At every 1 nsec, the value at S is given by 0, 0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1. At every 1 nsec, the value at R is given by 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 1, 1, 1, 1. Find out the waveform at the outputs, Q, Q as functions of time. What is the "hold time" of this latch? (Here "hold time" is the minimum pulse-width at the input for a reasonable output.) **[1M]**

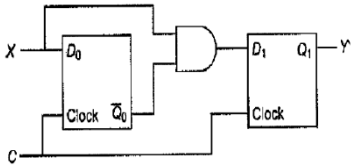


Q-3 Design and draw the optimal logic circuit for the 4-bit synchronous counter to count the prime numbers using JK flipflops with a negative edge trigger clock. **[2.0 M]**

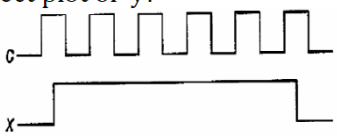
Q-4 Specify the truth table with 4 bits for a Fibonacci number recognizer using Read-Only Memory (ROM). Derive the Boolean function and draw the optimal design circuit for the Fibonacci numbers recognizer using ROM. **[3.0 M]**

Q-5 **[1 M]**

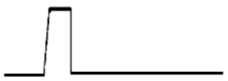
Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D flip-flops are positive edged triggered and have set up times 20 ns and hold times 0.



Consider the following timing diagrams of X and C; the clock period of $C \geq 40$ns. Which one is the correct plot of y?

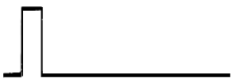


a)

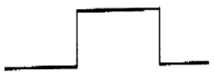


b)

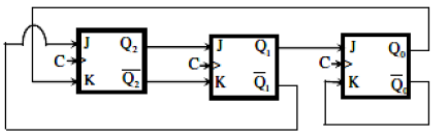
c)



d)



Q-6 **[1M]**



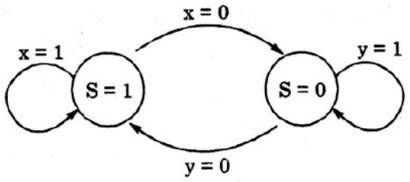
The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0$ = 000. The state sequence for this circuit for the next 3 clock cycles is

a) 001, 010, 011 c) 111, 110, 101

b) 100, 110, 111 d) 100, 011, 001

Q-7 **[1M]**

For a state machine with the following state diagram the expression for the next state S^+ in terms of the current state S and the input variables x and y is



a) $S^+ = S'.y' + S.x$

b) $S^+ = S.x.y' + S'.y.x'$

c) $S^+ = x.y'$

d) $S^+ = S'.y + S.x'$

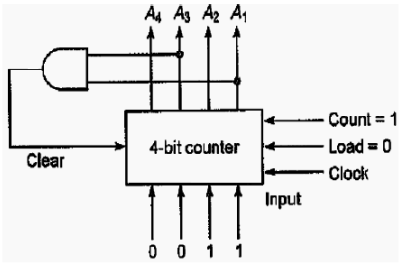
Hint: Explore state machines or state diagrams

Q-8 **[2M]**

The Control signal functions of a 4-bit binary counter are given below (where x is don't care):

Clear	Clock	Load	Count	Function
1	x	x	x	Clear to 0
0	x	0	0	No change
0	↑	1	x	Load input
0	↑	0	1	Cunt next

The counter is connected as follows



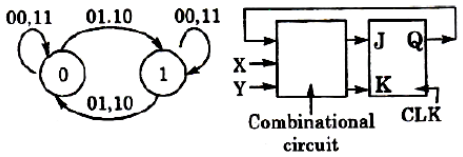
Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence

a) 0, 3, 4 b) 0, 3, 4, 5

c) 0, 1, 2, 3, 4, 5 d) 0, 1, 2, 3, 4

Q-9 **[1M]**

Consider the following state diagram and its realization by a JK flip flop.



The combinational circuit generates J and K in terms of x, y and Q. The Boolean expressions for j and K are:

a) $\overline{x \oplus y}$ and $\overline{x \oplus y}$

b) $\overline{x \oplus y}$ and $x \oplus y$

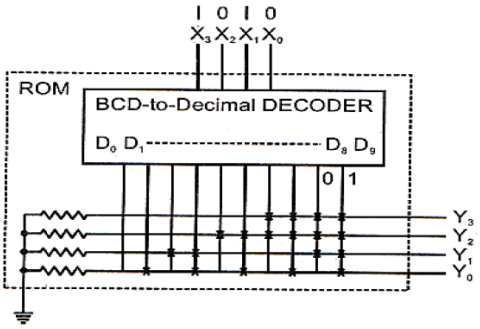
c) $x \oplus y$ and $\overline{x \oplus y}$

d) $x \oplus y$ and $x \oplus y$

Hint: Explore state machines

Q-10

If the input X_3, X_2, X_1, X_0 to the ROM in the figure are 8 4 2 1 BCD numbers, then the outputs Y_3, Y_2, Y_1, Y_0 are



a) gray code numbers

b) 2 4 2 1 BCD numbers

c) excess-3 code numbers

d) none of the above