Digital Systems

Assignment – 1

Q-1 Which of the following is an invalid state in an 8-4-2-1 Binary Coded Decimal counter. **[1 Mark]**

a) 1 0 0 0 b) 1 0 0 1
c) 0 0 1 1 d) 1 1 0 0

Q-2 f (A,B,C,D)= ΠM(0,1,3,4,5,7,9,11,12,13,14,15) is a maxterm representation of a Boolean function f (A,B,C,D) where A is the MSB and D is the LSB. The equivalent minimized representation of this function is **[2 Mark]**

a) $(A+\bar{C}+D)(\bar{A}+B+D)$
b) $A\bar{C}D+\bar{A}BD$
c) $\bar{A}C\bar{D}+A\bar{B}C\bar{D}+A\overline{BC}\bar{D}$
d) $(B+\bar{C}+D)(A+\bar{B}+\bar{C}+D)(\bar{A}+B+C+D)$

Q-3 [1 Mark]

The Boolean expression
$\overline{(\bar{a}+\bar{b}+c+\bar{d})+(b+\bar{c})}$ Simplifies to

a) 1 b) $\overline{a.b}$
c) $a.b$ d) 0

Q-4 [2 Mark]

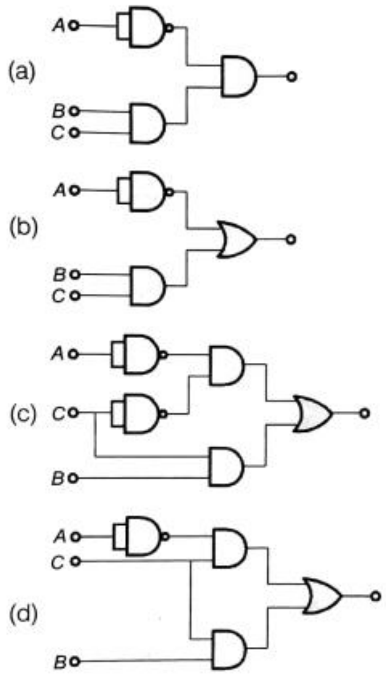
Digital input signals *A, B, C* with A as the MSB and *C* as the LSB are used to realize the Boolean function $F=m_0+m_2+m_3+m_5+m_7$, where m_i denotes the i^{th} minterm. In addition. *F* has a don't care for m_1. The simplified expression for *F* is given by

a) $\bar{A}\bar{C}+\bar{B}C+AC$
b) $\bar{A}+C$
c) $\bar{C}+A$
d) $\bar{A}C+BC+A\bar{C}$

Q-5 [1 Mark]

Which of the following logic circuits is a realization of the function F whose Karnaugh map is shown in figure.

C \ AB	00	01	11	10
0	1	1		
1		1	1	



Q-6 [1 Mark]

The range of signed decimal numbers that can be represented by 6-bit 1's complement number is

a) $-31 \text{to} +31$ b) $-63 \text{to} +63$
c) $-64 \text{to} +63$ d) $-32 \text{to} +31$

Q-7 [2 Mark]

11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?

a) 25, 9 and 57 respectively
b) -6,-6 and -6 respectively
c) -7,-7 and -7 respectively
d) -25,-9 and -57 respectively

Q-8 [2 Mark]

Decimal 43 in Hexadecimal and BCD number system is respectively

a)B2,0100 0011 b)2B,0100 0011
c)2B,0011 0100 d)B2,0100 0100

Q-9 [2 Mark]

A new Binary coded Pentary (BCP) number system is proposed in which every digit of a base -5 number is represented by its corresponding 3-bit binary code. For example, the base -5 number 24 will be represented by its BCP code 010100. In this numbering system, the BCP code 100010011001 corresponds to the following number in base -5 system

a) 423 b) 1324
c) 2201 d) 4231

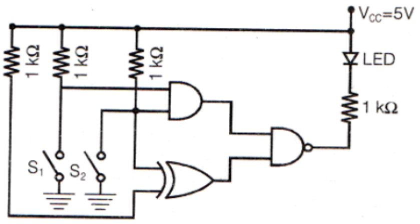
Q-10 [1 Mark]

The Boolean express to $(X+Y)(X+\bar{Y})+\overline{(X+\bar{Y})+\bar{X}}$ simplifies to

a) X b) Y
c) XY d) $X+Y$

Q-11 [2 Mark]

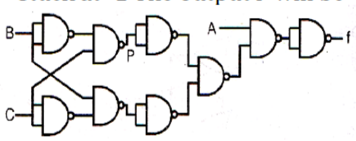
In the figure, the LED



a) emits light when both S_1 and S_2 are closed
b) emits light when both S_1 and S_2 are open.
c) emits light when only of S_1 and S_2 is closed.
d) does not emit light, irrespective of the switch positions.

Q-12 [2 Mark]

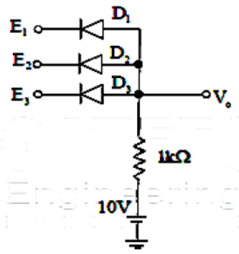
The point P in the following figure is stuck at -1 The output f will be



a) ABC b) A
c) ABC d) $\bar{A}$

Q-13 [1 Mark]

In the circuit shown, diodes D_1, D_2 and D_3 are ideal, and the inputs E_1, E_2 and E_3



a) 3 input OR gate
b) 3 input NOR gate
c) 3 input AND gate
d) 3 input XOR gate

Q-14 [2 Mark]

The product of sum expression of a Boolean function F(A, B, C) of three variables is given by

$$F(A,B,C)=(A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+\bar{B}+\bar{C})$$

The canonical sum of product expression of F(A, B, C) is given by

a) $\overline{AB}C+\bar{A}BC+A\overline{BC}+ABC$

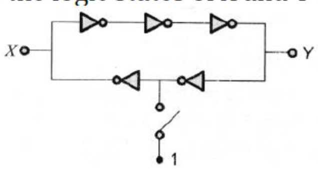
b) $\overline{ABC}+\bar{A}B\bar{C}+A\bar{B}C+AB\bar{C}$

c) $AB\bar{C}+A\overline{BC}+\bar{A}BC+\overline{ABC}$

d) $\overline{ABC}+\bar{A}BC+AB\bar{C}+ABC$

Q-15 [1 Mark]

In the circuit shown, the switch is momentarily closed and then opened. Assuming the logic gates to have equal non-zero delay, at steady state, the logic states of X and Y are



a) X is latched, Y toggles continuously
b) X and Y are both latched
c) Y is latched, X toggles continuously
d) X and Y both toggle continuously

Q-16 [1 Mark]

The range of integers that can be represented by an n bit 2's complement number system is

a) -2^{n-1} to $\left(2^{n-1}-1\right)$

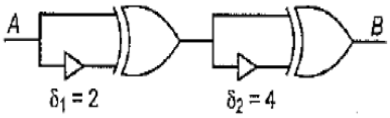
b) $-\left(2^{n-1}-1\right)$ to $\left(2^{n-1}-1\right)$

c) -2^{n-1} to 2^{n-1}

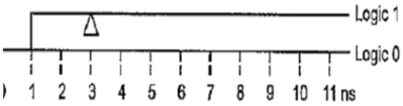
d) $-\left(2^{n-1}+1\right)$ to $\left(2^{n-1}-1\right)$

Q-17 [2 Mark]

Consider the following circuit compose of XOR gates and non-inverting buffers:



The non-inverting buffers have delays $\delta_1 = 2$ns and $\delta_2 = 4$ns as shown in the figure. Both XOR gates and all wires have zero delay. Assume that all wires have zero delay. Assume that all gate inputs, output and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?



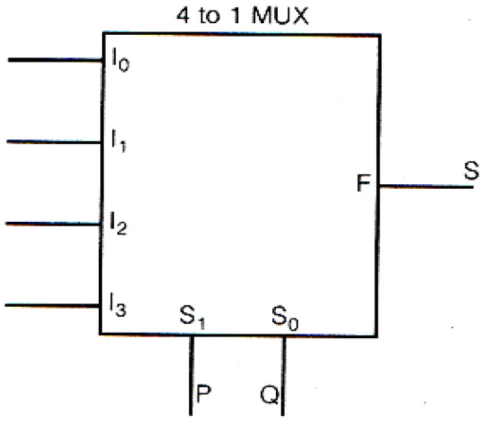
a) 1 b) 2

c) 3 d) 4

Q-18 [2 Mark]

Note: Mux/Demux will be covered soon

Figure shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input C_{in}. Which of the following combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX will realize the sum S?



a) $I_0 = I_1 = C_{in}; I_2 = I_3 = \overline{C}_{in}$

b) $I_0 = I_1 = \overline{C}_{in}; I_2 = I_3 = C_{in}$

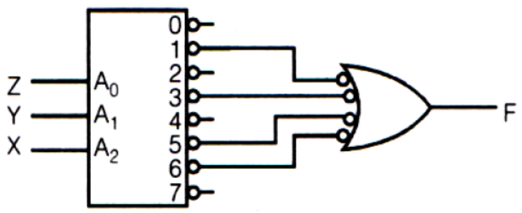
c) $I_0 = I_3 = C_{in}; I_1 = I_2 = \overline{C}_{in}$

d) $I_0 = I_3 = \overline{C}_{in}; I_1 = I_2 = C_{in}$

Q-19 [2 Mark]

Note: Encoder/Decoder will be covered soon

A 3 line to 8 line decoder, with active low outputs is used to implement a 3-variable Boolean function as shown in the figure



The simplified form of Boolean function F(A,B,C) implemented in 'Product of Sum' form will be

a) $(X+Z).(\overline{X}+\overline{Y}+\overline{Z}).(Y+Z)$

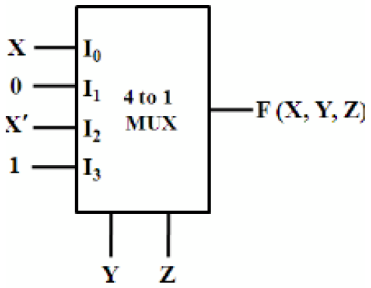
b) $(\overline{X}+\overline{Z}).(X+Y+Z).(\overline{Y}+\overline{Z})$

c) $(\overline{X}+\overline{Y}+Z).(\overline{X}+Y+Z).(X+\overline{Y}+Z).(X+Y+\overline{Z})$

d) $(\overline{X}+\overline{Y}+Z).(\overline{X}+Y+\overline{Z}).(X+\overline{Y}+Z).(X+\overline{Y}+\overline{Z})$

Q-20 [2 Mark]
Note: Mux/Demux will be covered soon

A 4 to 1 multiplexer to realize a Boolean function F (X, Y, Z) is shown in the figure below. The inputs Y and Z are connected to the selectors of the MUX (Y is more significant). The canonical sum-of product expression for F (X, Y, Z) is



a) $\sum m(2,3,4,7)$ b) $\sum m(1,3,5,7)$
c) $\sum m(0,2,4,6$ d) $\sum m(2,3,5,6)$