The Pin connections to the Back Plane

Pin out for the IDC connector from the back-plane to the switch block.

Gnd (4)	1	2	N/C
Clock (5)	3	4	N/C
NMI Switch (6)	5	6	N/C
CPM Switch (7)	7	8	N/C
Aux Clock (8)	9	10	N/C
Ram Disable (9)	11	12	Bank A (65)
Reset Switch (10)	13	14	Bank B (66)

Aux Clock (8) – comes from the latest spec by Gemini

CPM Switch (7) – is for my system only and uses the “spare” line 7.
High is NAS-SYS, Low is CPM
When the CPM Switch is Low, Bank A and Bank B cannot turn on the N2 memory

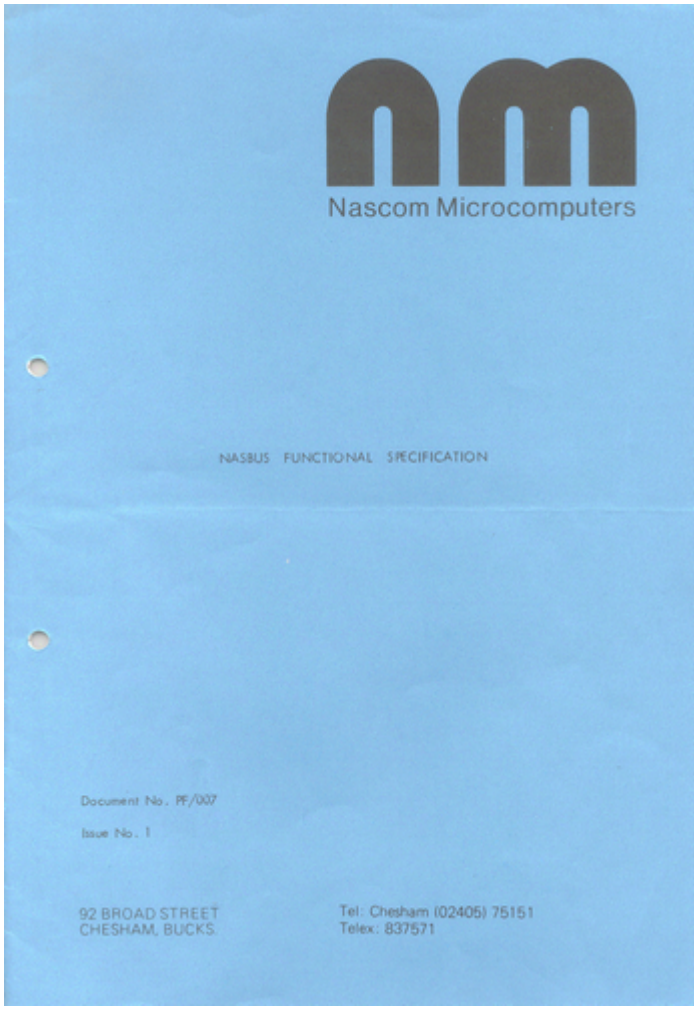
Bank A (65) – is for my system only and uses the line 65
High allows the memory in Bank A on N2
currently static RAM at 1000
Low turns off the N2 memory

Bank B (66) – is for my system only and uses the line 66
High allows the memory in Bank B on N2,
currently PolyDos Rom at D000 and static ram at C000
Low turns off the N2 memory

An extract from https://nascom.wordpress.com/nascom/hardware/nasbus/

I really can't believe that I've got this far with this site without giving more information on the NASBUS itself. It wasn't the most advanced of bus systems, but (at the time) it was quite cheap to implement yourself using stripboard and connectors. The general idea was to design a bus that was cheap and easy for the home computer builder. It was never designed to be an industrial system.

Everything (apart from the NASCOM 1) started with this.



NASBUS Specification

The NASBUS was designed for an 8-bit system, of course. In INMC News issue 1 it is stated that it is expandable up to 16 bits, but that was never done.

The connector was a 78 way single-sided card edge connector with a keyway at position 72. All power, data & control signals were carried by the connector.

These are now, unfortunately, obsolete and even end of line sources have dried up. The one pictured above is my only spare.

A bus was simply made, using suitable stripboard. For a simple bus all that was necessary was to solder the connectors on. If the interrupts were to be used then it was necessary to make breaks in the copper strips and add links to series IEI and IEO, allowing cascading of the signals. Cards not

using interrupts would link IEI to IEO. The system could also allow expansion cards to to take over the bus, control signals BAI and BAO could be connected in series in a similar manner to the above if this function was required.

The NASBUS remained unchanged until Nascom itself was in the hands of the receivers. There was then a legal problem with using the name “NASBUS”! However, a new system was being designed (not by Nascom this time) using 2 cards and called the Multiboard. The idea was that it would replace the Nascom-2 should the receivers fail to find a buyer. (I’m assuming here that the original name was the “Multibus”.) As things happened, the new multi-card design and the rescue of Nascom by Lucas Logic took place at about the same time. The new company, Gemini, now produced a new specification for the bus as a general purpose Z80 system. For the first time it included timing specifications! It now became the Gemini 80-BUS, at which point it was modified to support extended addressing and to add a few more facilities:

- Pin 5 – now the System clock, not specified as 2MHz. All bus timing is relative to this.
- Pin 6 – was spare, now /NMI SW
- Pin 7 – was spare, now reserved
- Pin 8 – was spare, now optional AUX CLK, a 4MHz clock
- Pin 21 – was reserved for /NMI. now /NMI
- Pin 46 – was reserved, now A16
- Pin 47 – was reserved, now A17
- Pin 48 – was reserved, now A18
- Pin 49 – was reserved, now GND
- Pin 59 – was reserved, now INT 0 – interrupt request line
- Pin 60 – was reserved, now INT 1 – interrupt request line
- Pin 61 – was reserved, now INT 2 – interrupt request line
- Pin 62 – was reserved, now INT 3 – interrupt request line
- Pin 63 – was reserved, now /PWRF – power fail warning
- Pin 64 – was reserved, now AUX PWR – auxiliary power (batteries to maintain real time clock and/or CMOS RAM if fitted).
- Pin 65 – was reserved, now NDEF1 – not defined, available for user
- Pin 66 – was unused, now NDEF2 – not defined, available for user
- Pin 67 – was unused, now GND

The addition of A16, A17 & A18 increased the available address space from 64kB to 512kB. However, 8-bit processors could still only use A0-A15 directly connected (for 64kB). In theory Pin 49 could have been used to achieve 1MB, but it was grounded to give separation of the data and address buses. The 80-BUS remained back-compatible with the NASBUS.

True 16-bit compatibility was never added. I suspect that the following might have been the reason: Usually this would require A0-A19 to give a 1MB address range. This was allowed for on pins 30-49. The 16 bit data bus would have been allocated pins 50-65. Unfortunately this puts A19 next to D0 which is simply asking for trouble due to capacitive coupling. It was too late to move the data bus up to pins 51-66 and use pin 50 as a separator as this would have broken back-compatibility with 8-bit systems. I’ve not found any other documented reason, but the GM811 Hardware manual

says this: “The original NASBUS specification made provision for the extra address and data lines of 16 bit processors. Careful consideration reveals that the bus would not be suitable for this, and so a number of new signals have been defined for the lines made free. The importance of good ground signals can not be overemphasized, and so extra ground lines have also been added.”