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EFFICIENT VIRTUAL MEMORY FOR BIG MEMORY SERVERS

In this paper, the authors observe that TLB misses in page-based virtual memory can cause performance issues on memory intensive workloads, up to 51% on execution cycles. Based on this, to avoid missing TLB, they propose a method to directly map the process's virtual addresses within the range of normal memory page size to the physical address on memory-heavy workloads. This is achieved through an abstraction called direct segment. Moreover, normal virtual addresses can use the page-based virtual memory. By applying this approach, the proposed method could eliminate almost all TLB misses.

Paging is a long standing method of memory virtualization which is used in almost every modern operating system. However, the author show that it is not optimal for memory intensive workloads because of TLB misses penalty. Moreover, they introduce a new framework for virtual memory that eliminates almost all TLB performance loss, which is a huge step toward scalability.

This approach is even compatible with conventional page-based virtual memory because it allows paging in other memory regions, which ease integration in to modern systems.

One limitation of the paper is that it may affect performance of applications that depends on sparse virtual memory allocation. Moreover, providing direct access to hardware memory could lead to security issues as well as the risk of misusage of the system.