Template Design Guide

# Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev.** | **Date** | **Author** | **Description** |
| 0.1 | 2/12/2015 | Yalong Xu | First Draft |
|  |  |  |  |

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# Introduction

## 1.1 General Description

Template Design is used to xxx.

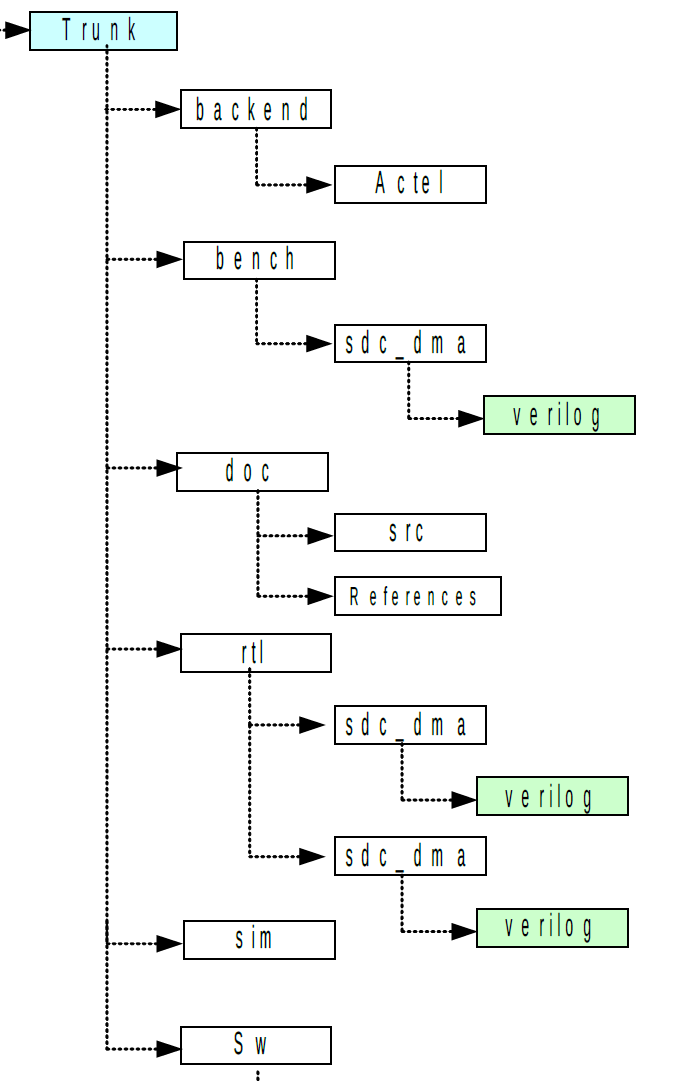
## 1.2 Features

The following lists the main features of Template Design IP core:

* 32-bit Wishbone Interface
* DMA
* Buffer Descriptor
* Compliant with SD Host Controller Spec version 2.0
* Support SD 4-bit mode
* Write/Read FIFO with variable size

## 1.3 Design Directory Structure

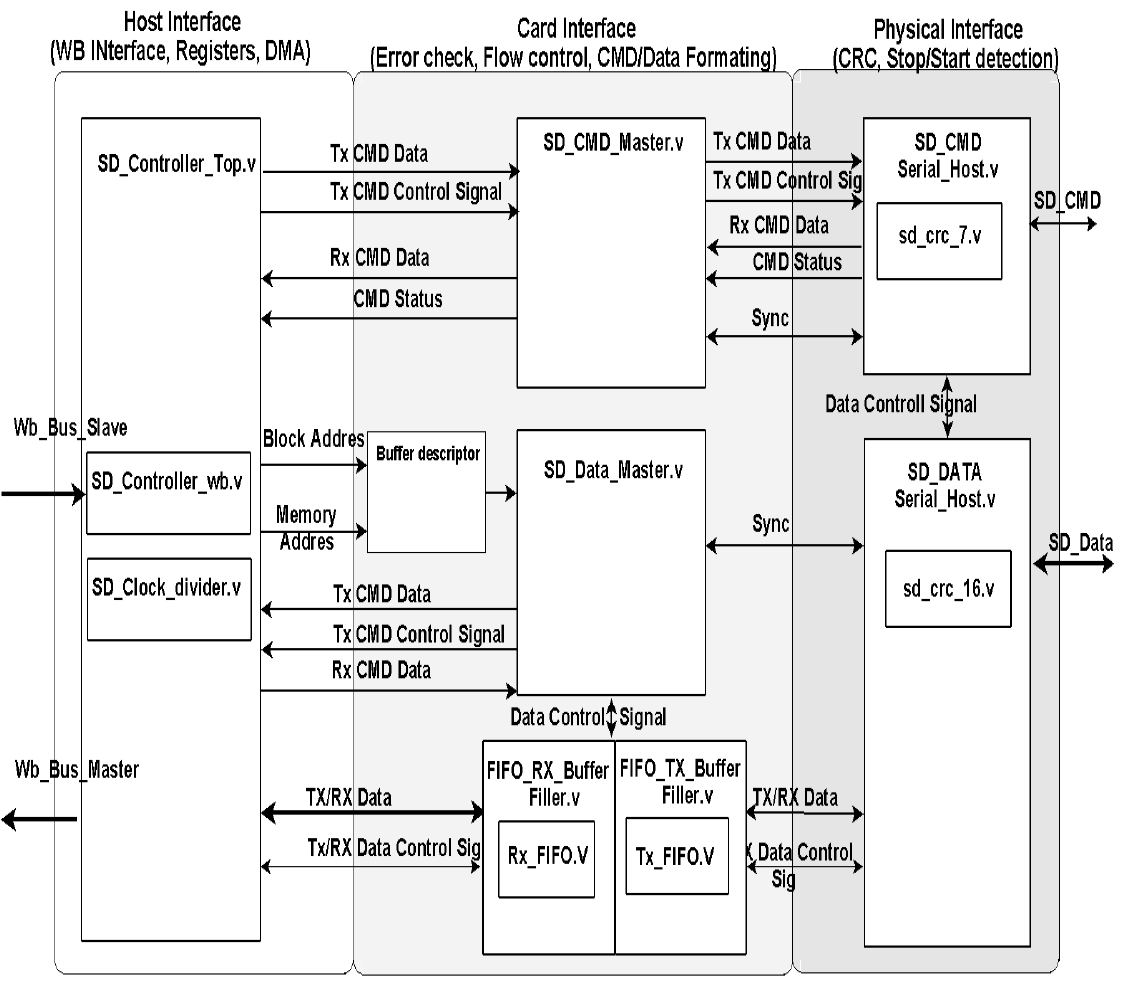
Following picture shows the structure of directories of this design.



# 2. Module Design

## 2.1 Design Architecture

This design **template\_top.v** consists of sub modules **xxx.v**, **yyy.v**, **zzz.v** and some logic for synchronizing, multiplexing and registering outputs. All modules and their sub-modules as well as their relations can be seen in the figure below.



## 2.2 Pinout

### 2.2.1 Port Declaration

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **I/O** | **Width** | **Description** |
| usr\_clk | IN | 1 | Global clock for this module |
| rst\_n | IN | 1 | Sync reset, active low |

## 2.3 Module 1

### 2.3.1 Port Declaration

Pin in/out descripted here

### 2.3.2 Signal Description

Interface signal,

### 2.3.3 Operation

FSM Operation

### 2.3.4 Simulation

Test bench and simulation result report

## 2.4 Module 2

## 2.5 Module 3